TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74HC161AP, TC74HC161AF, TC74HC161AFN
TC74HC163AP, TC74HC163AF, TC74HC163AFN

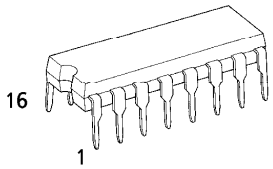
SYNCHRONOUS PRESETTABLE 4 – BIT COUNTER
TC74HC161AP/AF/AFN BINARY, ASYNCHRONOUS CLEAR
TC74HC163AP/AF/AFN BINARY, SYNCHRONOUS CLEAR

(Note) The JEDEC SOP (FN) is not available in Japan.

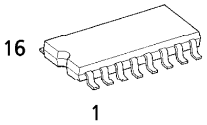
The TC74HC161A and 163A are high speed CMOS BINARY PRESETTABLE COUNTERs fabricated with silicon gate C²MOS technology.
They achieve the high speed operation similar to equivalent STTL while maintaining the CMOS low power dissipation.
The CK input is active on the rising edge. Both $\overline{LOAD}$ and $\overline{CLR}$ inputs are active on low logic level.
Presetting of all four IC's is synchronous to the rising edge of CK.
The clear function of the TC74HC163A is synchronous to CK, while the TC74HC161A is cleared asynchronously.
Two enable inputs (ENP and ENT) and CO are provided to enable easy cascading of counters, which facilitates easy implementation of n-bit counters without using external gates.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

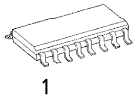
- High Speed ····· f_{MAX} = 63MHz(typ.) at V_{CC} = 5V
- Low Power Dissipation ····· I_{CC} = 4μA(Max.)at Ta = 25°C
- High Noise Immunity ····· $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}| = I_{OL}$ = 4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range ···· V_{CC} (opr.) = 2V ~ 6V
- Pin and Function Compatible with 74LS160 ~ 163



P (DIP16-P-300-2.54A)
Weight : 1.00g (Typ.)

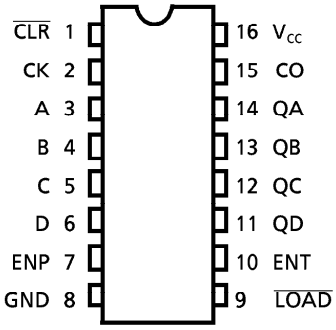


F (SOP16-P-300-1.27)
Weight : 0.18g (Typ.)



FN (SOL16-P-150-1.27)
Weight : 0.13g (Typ.)

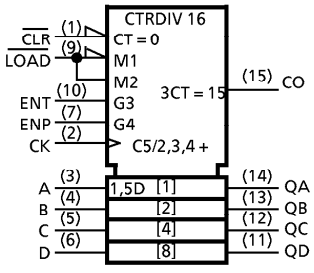
PIN ASSIGNMENT



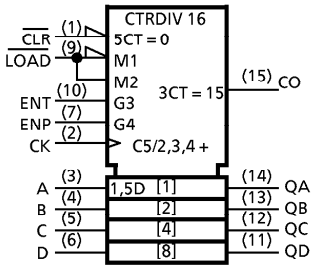
(TOP VIEW)

IEC LOGIC SYMBOL

TC74HC161A



TC74HC163A



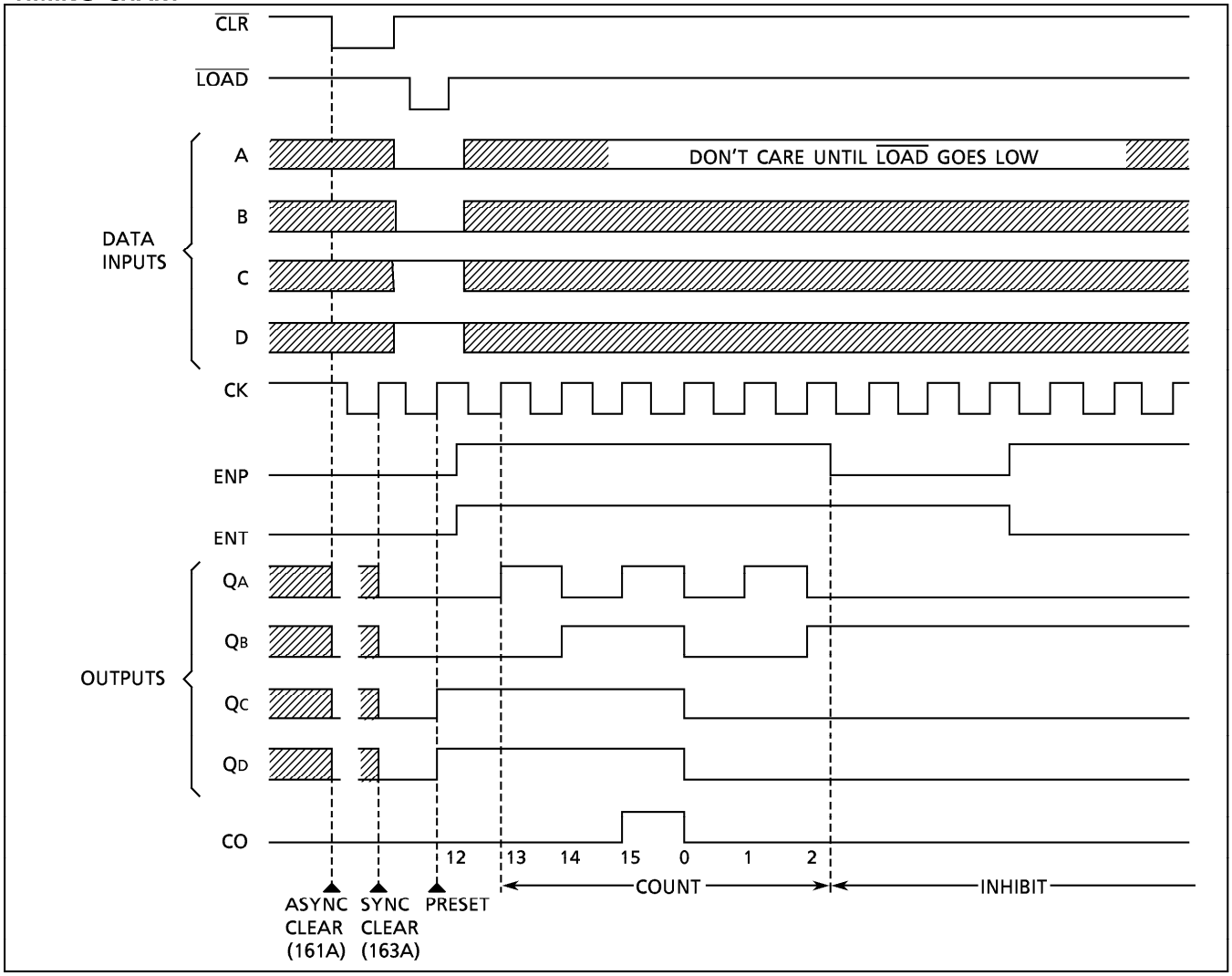
961001EBA2

TRUTH TABLE

TC74HC161A INPUTS					TC74HC163A INPUTS					OUTPUTS				FUNCTION
$\overline{CLR}$	$\overline{LD}$	ENP	ENT	CK	$\overline{CLR}$	$\overline{LD}$	ENP	ENT	CK	QA	QB	QC	QD	
L	X	X	X	X	L	X	X	X	↑	L	L	L	L	RESET TO "0"
H	L	X	X	↑	H	L	X	X	↑	A	B	C	D	PRESET DATA
H	H	X	L	↑	H	H	X	L	↑	NO CHANGE				NO COUNT
H	H	L	X	↑	H	H	L	X	↑	NO CHANGE				NO COUNT
H	H	H	H	↑	H	H	H	H	↑	COUNT UP				COUNT
H	X	X	X	↓	X	X	X	X	↓	NO CHANGE				NO COUNT

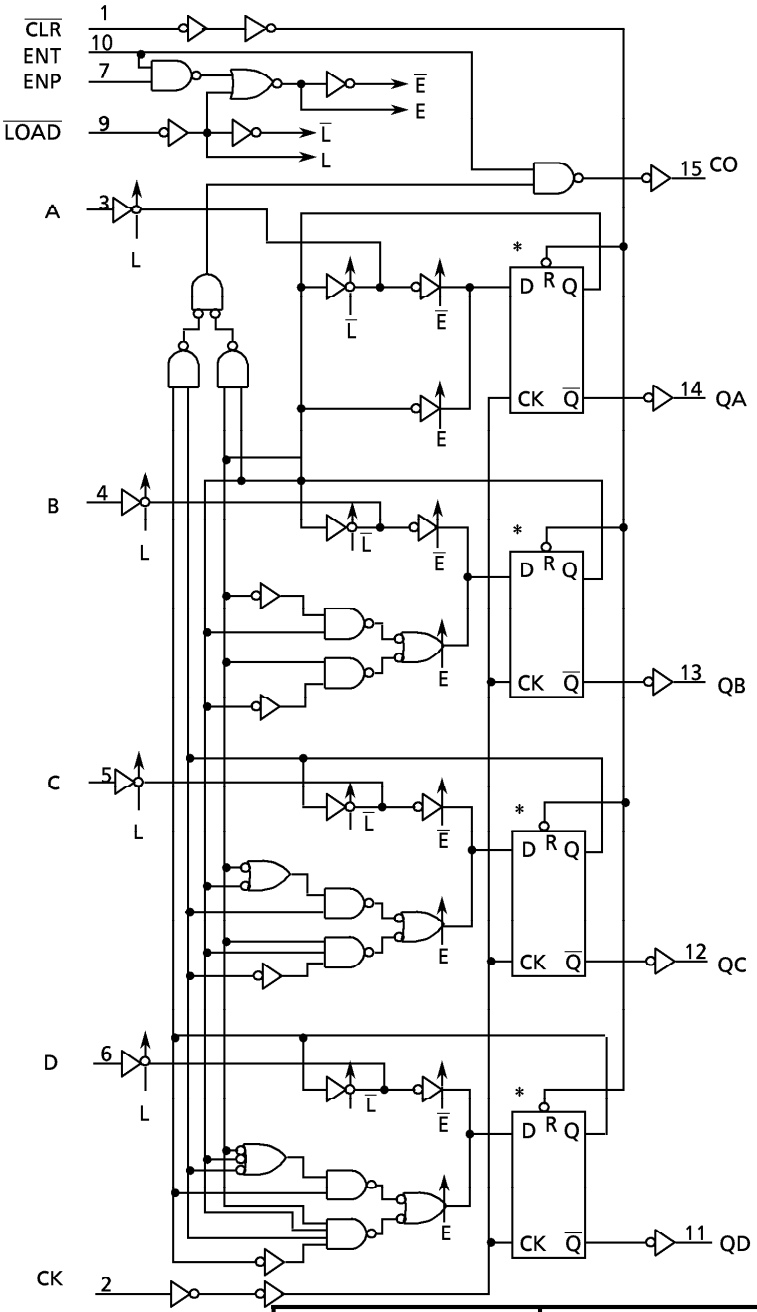
Note X : Don't Care
A, B, C, D : Logic Level of Data Inputs
Carry : CARRY = ENT·QA·QB·QC·QD

TIMING CHART



961001EBA2'

SYSTEM DIAGRAM



* TRUTH TABLE OF INTERNAL F/F

TC74HC161A					TC74HC163A				
D	CK	R	Q	$\overline{Q}$	D	CK	R	Q	$\overline{Q}$
X	X	L	L	H	X	↑	L	L	H
L	↑	H	L	H	L	↑	H	L	H
H	↑	H	H	L	H	↑	H	H	L
X	↓	X	NO CHANGE		X	↓	H	NO CHANGE	

X : Don't Care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7	V
DC Input Voltage	V_{IN}	−0.5~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC} / Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	−65~150	°C

*500mW in the range of Ta= −40°C~65°C. From Ta=65°C to 85 °C a derating factor of −10mW/ °C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2~6	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	t_r, t_f	0~ 1000 (V_{CC} = 2.0V) 0~ 500 (V_{CC} = 4.5V) 0~ 400 (V_{CC} = 6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
High - Level Input Voltage	V_{IH}			2.0 4.5 6.0	1.50 3.15 4.20	− − −	− − −	1.50 3.15 4.20	− − −	V
Low - Level Input Voltage	V_{IL}			2.0 4.5 6.0	− − −	− − −	0.50 1.35 1.80	− − −	0.50 1.35 1.80	V
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	− − −	1.9 4.4 5.9	− − −	V
			I_{OH} = −4 mA I_{OH} = −5.2mA	4.5 6.0	4.18 5.68	4.31 5.80	− −	4.13 5.63	− −	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20μA	2.0 4.5 6.0	− − −	0.0 0.0 0.1	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL} = 4 mA I_{OL} = 5.2mA	4.5 6.0	− −	0.17 0.18	0.26 0.26	− −	0.33 0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS (Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C TYP.	Ta = 25°C LIMIT	Ta = −40~85°C LIMIT	UNIT
Minimum Pulse Width (CK)	$t_{W(H)}$ $t_{W(L)}$	Fig. 1	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Pulse Width ($\overline{CLR}$) *	$t_{W(L)}$	Fig. 4	2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Set−up Time ($\overline{LOAD}$, ENP, ENT)	t_s	Fig. 2, 3	2.0	—	100	125	
			4.5	—	20	25	
			6.0	—	17	21	
Minimum Set−up Time (A, B, C, D)	t_s	Fig. 2	2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Set−up Time ($\overline{CLR}$) **	t_s	Fig. 5	2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Hold Time	t_h	Fig. 2, 3, 5	2.0	—	0	0	
			4.5	—	0	0	
			6.0	—	0	0	
Minimum Removal Time ($\overline{CLR}$) *	t_{rem}	Fig. 4	2.0	—	50	65	
			4.5	—	10	13	
			6.0	—	9	11	
Clock Frequency	f		2.0	—	6	5	MHz
			4.5	—	31	25	
			6.0	—	36	29	

AC ELECTRICAL CHARACTERISTICS ($C_L = 15pF$, $V_{CC} = 5V$, Ta = 25°C, Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}	Fig. 1	—	4	8	ns
Propagation Delay Time (CK−Q)	t_{pLH} t_{pHL}	Fig. 1	—	13	21	
Propagation Delay Time (CK−CO) [Count Mode]	t_{pLH} t_{pHL}	Fig. 1	—	16	26	
Propagation Delay Time (CK−CO) [Preset Mode]	t_{pLH}	Fig. 2	—	18	30	
	t_{pHL}		—	20	35	
Propagation Delay Time (ENT−CO)	t_{pLH} t_{pHL}	Fig. 6	—	10	17	
Propagation Delay Time ($\overline{CLR}$−Q) *	t_{pHL}	Fig. 4	—	17	26	
Propagation Delay Time ($\overline{CLR}$−CO) *	t_{pHL}	Fig. 4	—	20	35	
Maximum Clock Frequency	f_{MAX}		36	63	—	MHz

*: for TC74HC161A only

**: for TC74HC163A only

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	—	25	75	—	95	ns
			4.5	—	7	15	—	19	
			6.0	—	6	13	—	16	
Propagation Delay Time (CK−Q)	t_{pLH} t_{pHL}	Fig. 1	2.0	—	48	125	—	155	
			4.5	—	16	25	—	31	
			6.0	—	14	21	—	26	
Propagation Delay Time (CK−CO) [Count Mode]	t_{pLH} t_{pHL}	Fig. 1	2.0	—	57	150	—	190	
			4.5	—	19	30	—	38	
			6.0	—	16	26	—	33	
Propagation Delay Time (CK−CO) [Preset Mode]	t_{pLH}	Fig. 2	2.0	—	66	175	—	220	
			4.5	—	22	35	—	44	
			6.0	—	19	30	—	37	
	t_{pHL}		2.0	—	72	200	—	250	
			4.5	—	24	40	—	50	
			6.0	—	20	34	—	43	
Propagation Delay Time (ENT−CO)	t_{pLH} t_{pHL}	Fig. 6	2.0	—	39	100	—	125	
			4.5	—	13	20	—	25	
			6.0	—	11	17	—	21	
Propagation Delay Time ($\overline{CLR}$−Q)*	t_{pHL}	Fig. 4	2.0	—	60	150	—	190	
			4.5	—	20	30	—	38	
			6.0	—	17	26	—	33	
Propagation Delay Time ($\overline{CLR}$−CO)*	t_{pHL}	Fig. 4	2.0	—	72	200	—	250	
			4.5	—	24	40	—	50	
			6.0	—	20	34	—	43	
Maximum Clock Frequency	f_{MAX}		2.0	6	18	—	5	—	MHz
			4.5	31	53	—	25	—	
			6.0	36	62	—	29	—	
Input Capacitance	C_{IN}			—	5	10	—	10	pF
Power Dissipation Capacitance	C_{PD} (1)	(Note 1)		—	34	—	—	—	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

When the outputs drive a capacitive load, total current consumption is the sum of C_{PD}, and $\triangle I_{CC}$ which is obtained from the following formula:

In case of TC74HC161A / 163A:

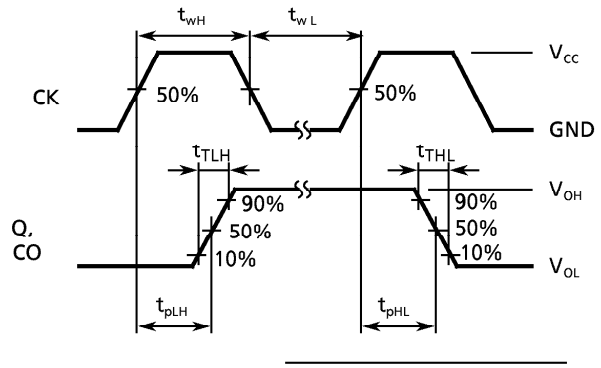
$$\triangle I_{CC} = f_{CK} \cdot V_{CC} \left(\frac{C_{QA}}{2} + \frac{C_{QB}}{4} + \frac{C_{QC}}{8} + \frac{C_{QD}}{16} + \frac{C_{CO}}{16} \right)$$

C_{QA}~C_{QD} and C_{CO} are the capacitances at QA~QD and CO, respectively.
f_{CK} is the input frequency of the CK.

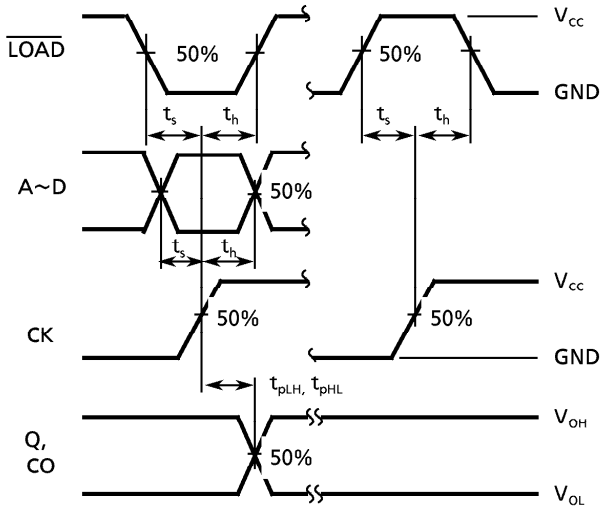
(2) * for TC74HC161A only

SWITCHING CHARACTERISTICS TEST WAVEFORM

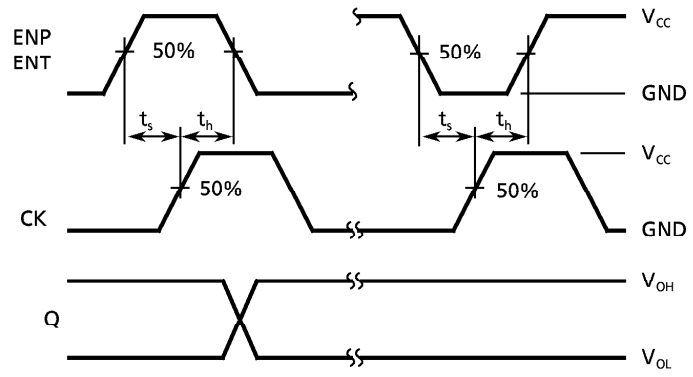
COUNT MODE (Fig. 1)



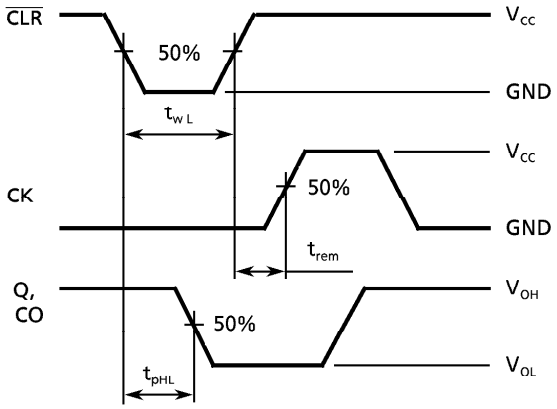
PRESET MODE (Fig. 2)



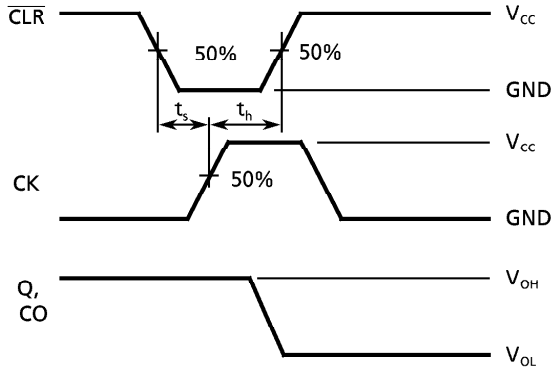
COUNT ENABLE MODE (Fig. 3)



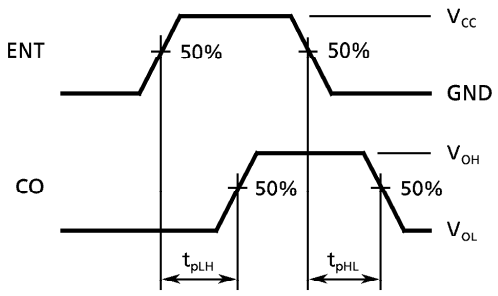
CLEAR MODE (TC74HC161A) (Fig. 4)



CLEAR MODE (TC74HC163A) (Fig. 5)

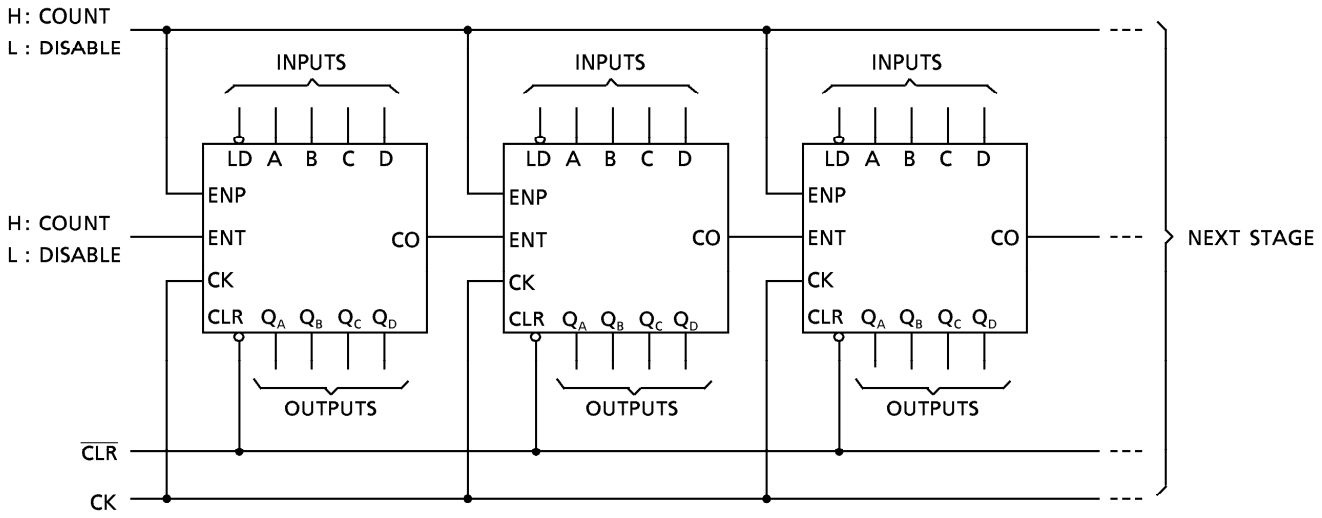


CASCADE MODE (Fix Maximum Count) (Fig. 6)

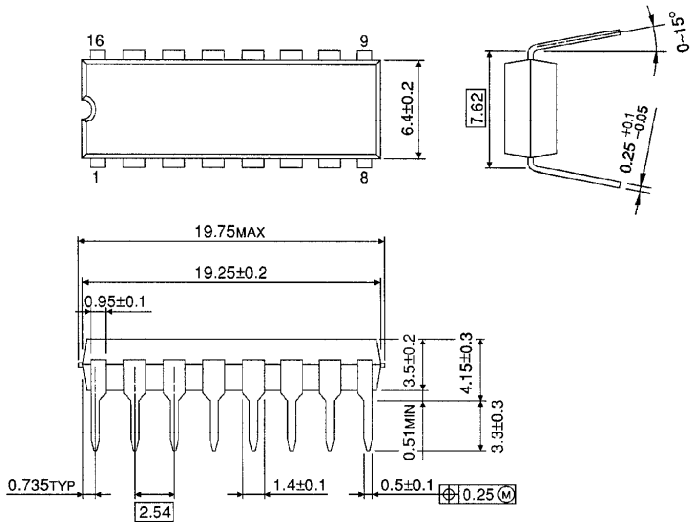


TYPICAL APPLICATION

PARALLEL CARRY N-BIT COUNTER

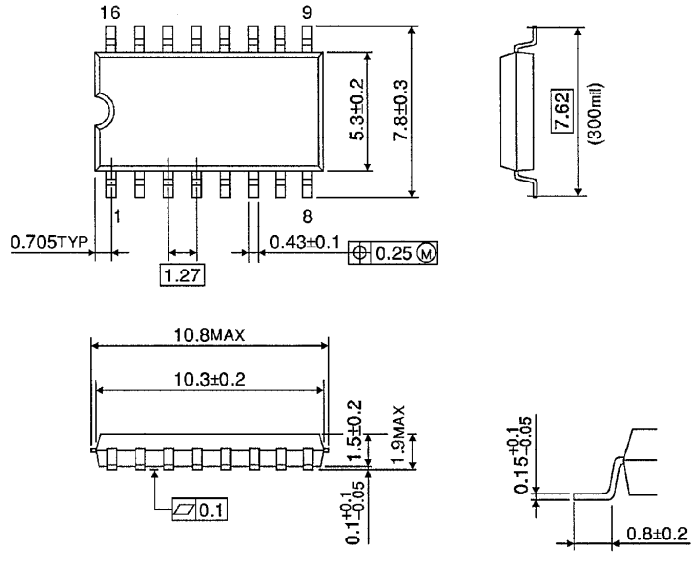


DIP 16PIN OUTLINE DRAWING (DIP16-P-300-2.54A) Unit in mm



Weight : 1.00g (Typ.)

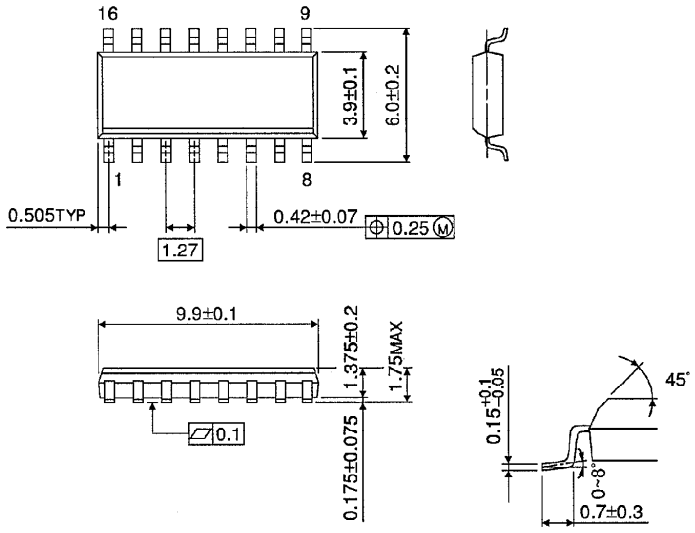
SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27) Unit in mm



Weight : 0.18g (Typ.)

SOP 16PIN (150mil BODY) OUTLINE DRAWING (SOL14-P-150 -1.27) Unit in mm

(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)