

TC74HCT573AP, TC74HCT573AF, TC74HCT573AFW

OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT

The TC74HCT573A is a high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Its inputs are compatible with TTL, NMOS, and CMOS output voltage levels.

Its 8-bit D-type latch is controlled by a latch enable input (LE) and a output enable input (OE).

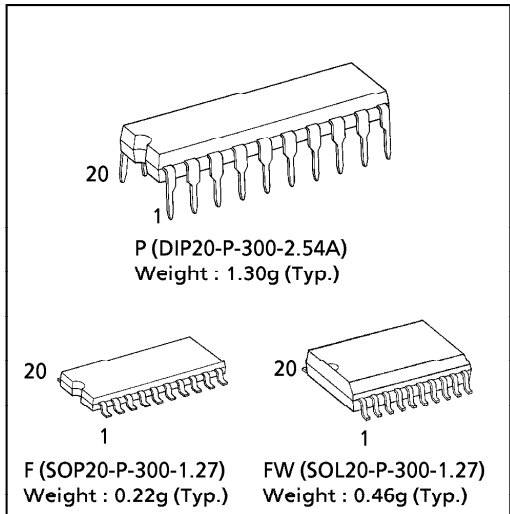
When the OE input is high, the eight outputs are in a high impedance state.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

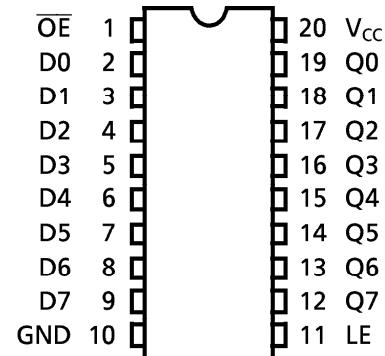
FEATURES:

- High Speed..... $t_{pd} = 18\text{ns}$ (typ.) at $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 4\mu\text{A}$ (Max.) at $T_a = 25^\circ\text{C}$
- Compatible with TTL outputs.... $V_{IL} = 0.8\text{V}$ (Max.)
 $V_{IH} = 2.0\text{V}$ (Min.)
- Output Drive Capability..... 15 LSTTL Loads
- Symmetrical Output Impedance... $|I_{OH}| = I_{OL} = 6\text{mA}$ (Min.)
- Balanced Propagation Delays.... $t_{pLH} \approx t_{pHL}$
- Pin and Function Compatible with 74LS573

(Note) The JEDEC SOP (FW) is not available in Japan.



PIN ASSIGNMENT



(TOP VIEW)

TRUTH TABLE

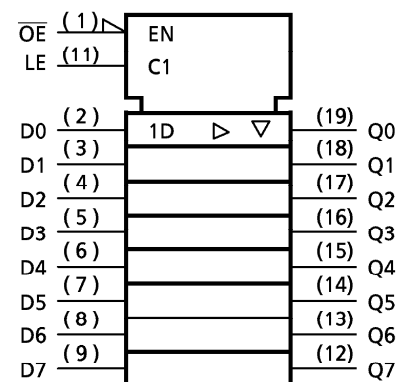
INPUTS			OUTPUT
OE	LE	D	Q
H	X	X	Z
L	L	X	Q _n
L	H	L	L
L	H	H	H

X : Don't Care

Z : High Impedance

Q_n (Q_n) : Q (Q) outputs are latched at the time when the LE input is taken to a low logic level.

IEC LOGIC SYMBOL



961001EBA2

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The diagram illustrates an 8-bit parallel data bus circuit. It consists of eight 74VHC175 D-type flip-flops, each with a clock input (L), a data input (D), and a data output (Q). The clock inputs of all flip-flops are connected to a common clock line, which is the output of a 74VHC04 inverter chain. The data inputs (D) of the flip-flops are connected to eight data inputs (D0 through D7) via 74VHC04 inverters. The data outputs (Q) of the flip-flops are connected to eight data outputs (Q0 through Q7) via 74VHC04 inverters. The circuit is controlled by two inputs: LE (L Enable) and OE (Output Enable). The LE input is connected to the clock input of the first flip-flop (Q0) via a 74VHC04 inverter. The OE input is connected to the clock input of the last flip-flop (Q7) via a 74VHC04 inverter.

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ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 35	mA
DC V_{CC} /Ground Current	I_{CC}	± 75	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	°C

*500mW in the range of $T_a = -40^\circ\text{C} \sim 65^\circ\text{C}$. From $T_a = 65^\circ\text{C}$ to 85°C a derating factor of $-10\text{mW}/^\circ\text{C}$ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	°C
Input Rise and Fall Time	t_r, t_f	0~500	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}		4.5 ┌ 5.5	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V_{IL}		4.5 └ 5.5	—	—	0.8	—	0.8	V
High - Level Output Voltage	V_{OH}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -20 \mu\text{A}$	4.5	4.4	4.5	—	4.4	V
			$I_{OH} = -6 \text{ mA}$	4.5	4.18	4.31	—	4.13	
Low - Level Output Voltage	V_{OL}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 20 \mu\text{A}$	4.5	—	0.0	0.1	—	V
			$I_{OL} = 6 \text{ mA}$	4.5	—	0.17	0.26	—	
3 - State Output Off - State Current	I_{OZ}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{OUT} = V_{CC} \text{ or GND}$	5.5	—	—	± 0.5	—	± 5.0	μA
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC} \text{ or GND}$	5.5	—	—	± 0.1	—	± 1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC} \text{ or GND}$	5.5	—	—	4.0	—	40.0	
	I_C	Per input: $V_{IN} = 0.5\text{V or } 2.4\text{V}$ Other input: $V_{CC} \text{ or GND}$	5.5	—	—	2.0	—	2.9	mA

TIMING REQUIREMENTS (Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C		Ta = -40~85°C	UNIT
				TYP.	LIMIT	LIMIT	
Minimum Pulse Width (LE)	$t_{W(H)}$		4.5 5.5	— —	15 14	19 17	ns
Minimum Set-up Time (Data)	t_s		4.5 5.5	— —	10 9	13 11	
Minimum Hold Time (Data)	t_h		4.5 5.5	— —	5 5	5 5	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	CL (pF)	V_{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		50	4.5 5.5	— —	7 6	12 11	— —	15 14	ns
Propagation Delay Time (LE—Q, $\bar{Q}$)	t_{PLH}		50	4.5 5.5	— —	19 17	29 26	— —	36 33	
	t_{PHL}		150	4.5 5.5	— —	24 22	37 34	— —	46 43	
Propagation Delay Time (D—Q, Q)	t_{PLH}		50	4.5 5.5	— —	17 14	26 23	— —	33 29	
	t_{PHL}		150	4.5 5.5	— —	22 20	34 31	— —	43 39	
Output Enable time	t_{PLH}	$R_L = 1\text{k}\Omega$	50	4.5 5.5	— —	18 15	27 24	— —	34 30	
	t_{PHL}		150	4.5 5.5	— —	23 20	35 32	— —	44 40	
Output Disable time	t_{PLZ} t_{PHZ}	$R_L = 1\text{k}\Omega$	50	4.5 5.5	— —	18 16	24 22	— —	30 28	
Input Capacitance	C_{IN}				—	5	10	—	10	pF
Output Capacitance	C_{OUT}				—	10	—	—	—	
Power Dissipation Capacitance	$C_{PD}(1)$				—	38	—	—	—	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

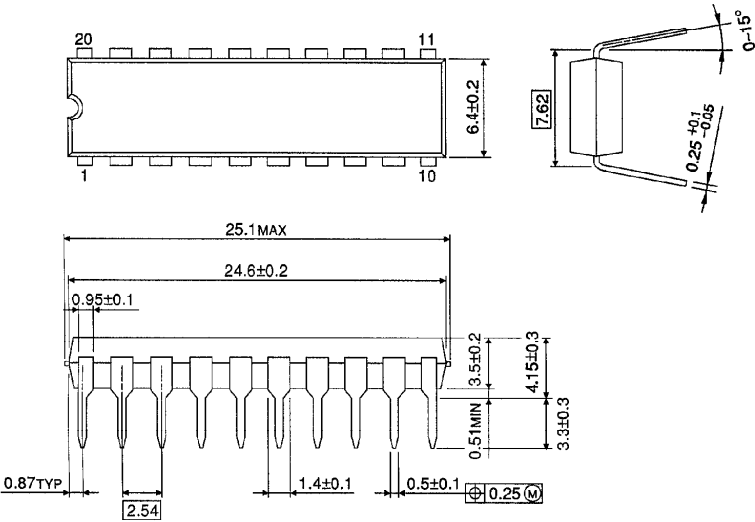
$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

And the total C_{PD} when n pcs. of Latch operate can be gained by the following equation:

$$C_{PD}(\text{total}) = 25 + 13 \cdot n$$

DIP 20PIN OUTLINE DRAWING (DIP20-P-300-2.54A)

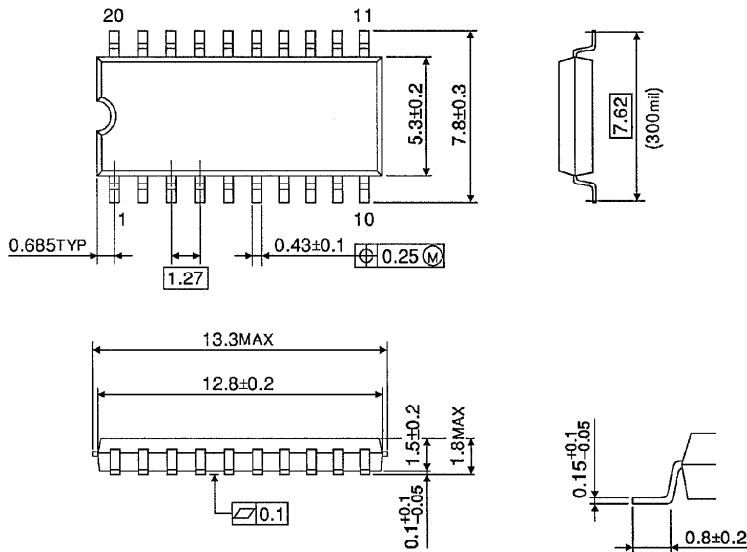
Unit in mm



Weight : 1.30g (Typ.)

SOP 20PIN (200mil BODY) OUTLINE DRAWING (SOP20-P-300-1.27)

Unit in mm

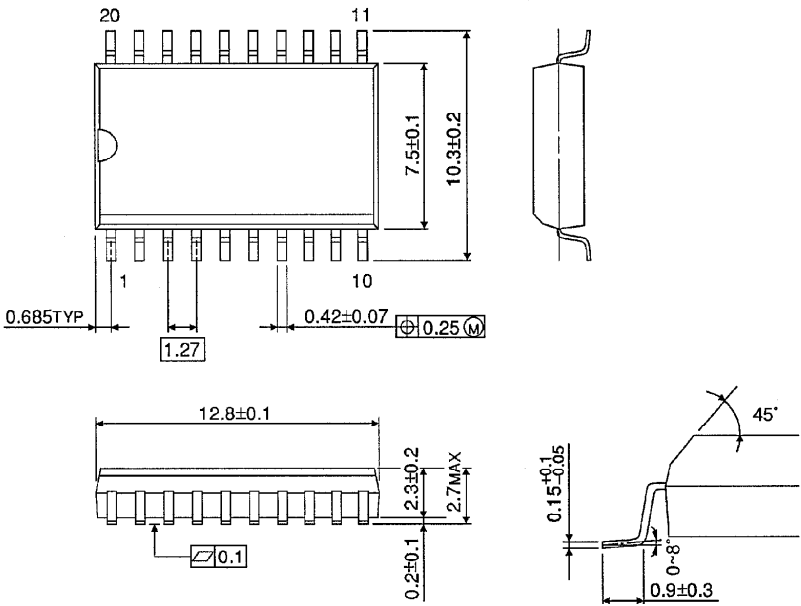


Weight : 0.22g (Typ.)

SOP 20PIN (300mil BODY) OUTLINE DRAWING (SOL20-P-300-1.27)

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.46g (Typ.)