# CMOS 16-Bit Microcontroller
# TMP93PT75F

## 1. Outline and Feature

The TMP93PT75F is a system evaluation LSI having a built in One-Time PROM (72 Kbyte) for TMP93CT75F.

A programming and verification for the internal PROM is achieved by using a general EPROM programmer with an adapter socket.

The function of this device is exactly same as the TMP93CT75F by programming to the internal PROM.

| PARTS NO. | ROM | RAM | PACKAGE | ADAPTER SOCKET NO. |
|---|---|---|---|---|
| TMP93PT75F | OTP 72 Kbyte | 1.8 Kbyte | QFP100-P-1420-0.65A | BM11146 |

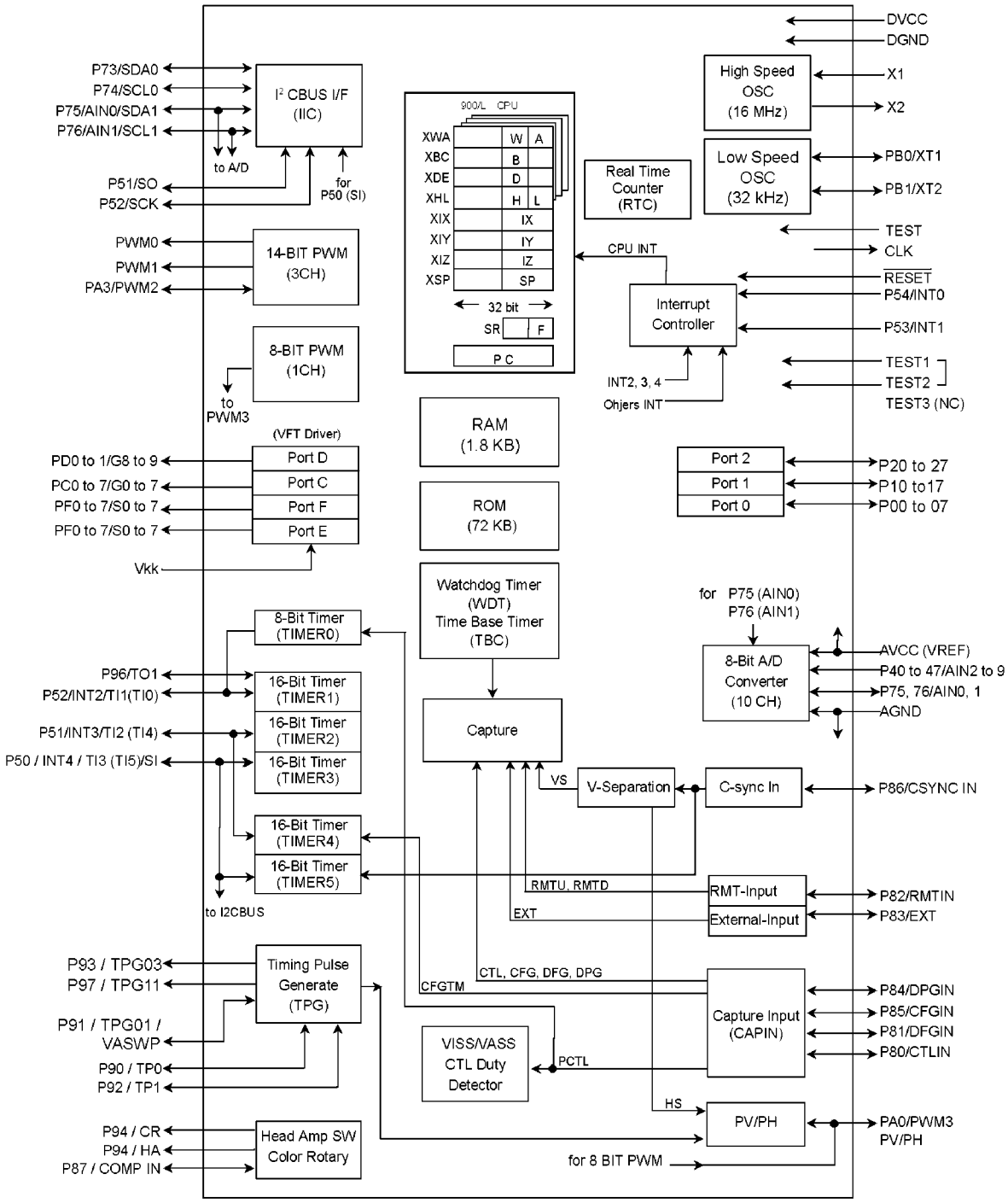



Figure 1.1 TMP93PT75F Block Diagram

## 2. Pin Assignment and Functions

The assignment of input and output pins for the TMP93PT75F, their names and functions are described below.

### 2.1 Pin Assignment

Figure 2.1.1 shows pin assignment of the TMP93PT75F.

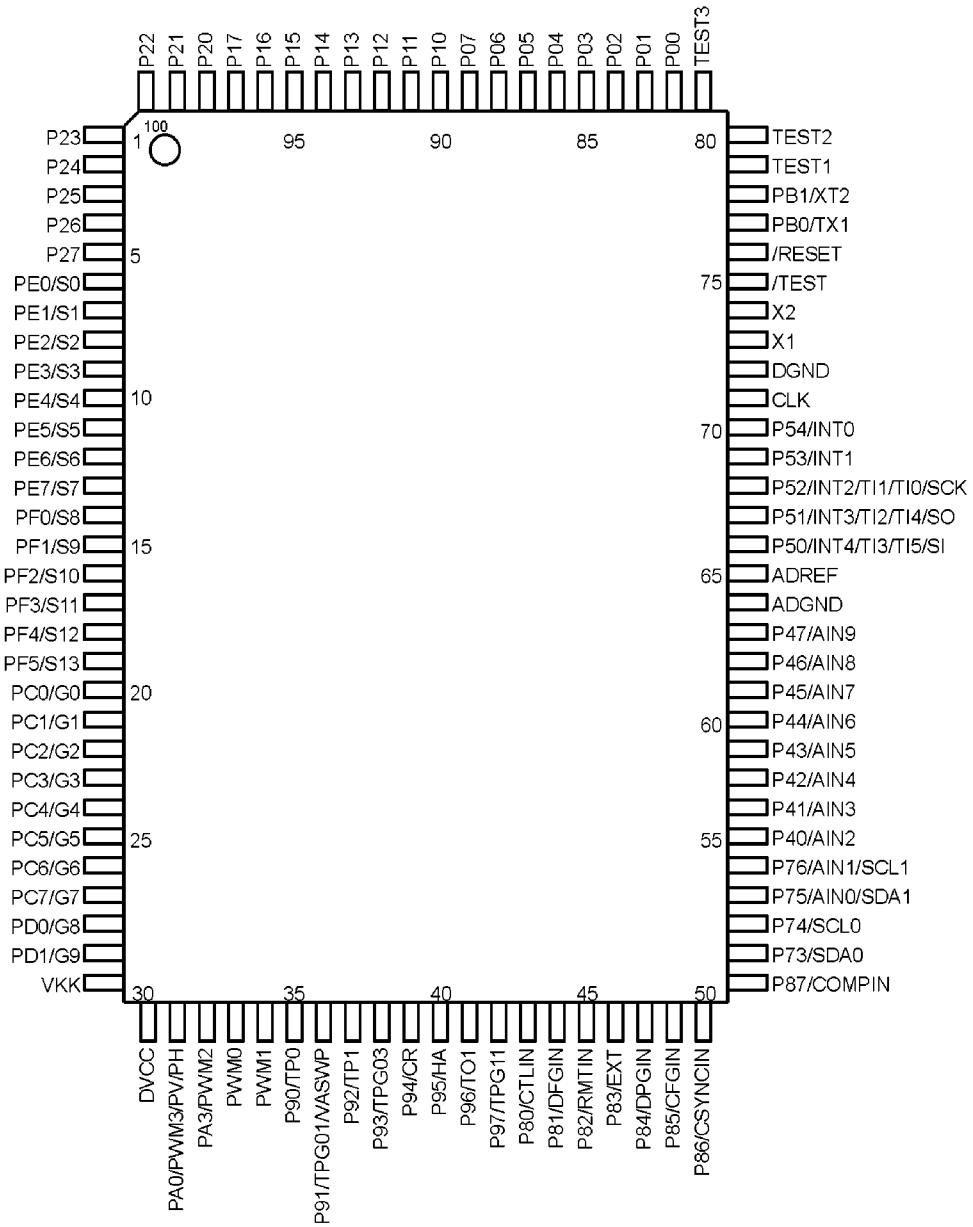



Figure 2.1.1 Pin Assignment (100-pin QFP)

## 2.2 Pin Names and Functions

The names of input/output pins and their functions are described below.

(1) MCU mode

Table 2.2.1 Pin Names and Function (1/3)

| Pin name | Number of pins | I/O | Functions |
|---|---|---|---|
| P00 to P07 | 8 | I/O | port0: I/O ports |
| P10 to P17 | 8 | I/O | port1: I/O ports |
| P20 to P27 | 8 | I/O | port2: I/O ports |
| P40 to P47 | 8 | Input | port4: Input ports |
| /AIN2 to AIN9 | | Input | Analog input: Input to A/D converter |
| P50 | 1 | I/O | Port50: I/O port(schmitt input) |
| /INT4 | | Input | External Interrupt request input 4: Rising edge/Falling edge programable |
| /TI3 | | Input | 16bit timer3(TC3): Timer Input 3 |
| /TI5 | | Input | 16bit timer5(TC5): Timer Input 5 |
| /SI | | Input | SIO received channel |
| P51 | 1 | I/O | Port51: I/O port(schmitt input) |
| /INT3 | | Input | External Interrupt request input 3: Rising edge/Falling edge programable |
| /TI2 | | Input | 16 bit timer2(TC2): Timer Input 2 |
| /TI4 | | Input | 16 bit timer4(TC4): Timer Input 4 |
| /SO | | Input | SIO sending channel |
| P52 | 1 | I/O | Port52: I/O port(schmitt input) |
| /INT2 | | Input | External Interrupt request input 2: Rising edge/Falling edge programable |
| /TI1 | | Input | 16 bit timer1(TC1): Input 1 |
| /TI0 | | Input | 8 bit Timer(TC0): Input 0 |
| /SCK | | Input | SIO clock line |
| P53 | 1 | I/O | Port53: I/O port(schmitt input) |
| /INT1 | | Input | External Interrupt request pin1: Rising edge/Falling edge programable<br>SU/TU-FG(Reel Tacho) |
| P54 | 1 | I/O | Port54: I/O port(schmitt input) |
| /INT0 | | I/O | External Interrupt request pin0: Rising edge/Falling edge programable |
| P73 | 1 | I/O | Port73: I/O port(schmitt input) |
| /SDA0 | | I/O | $I^2$CBUS SDA0 line |
| P74 | 1 | I/O | Port74: I/O port(schmitt input) |
| /SCL0 | | I/O | $I^2$CBUS SCL0 line |
| P75 | 1 | I/O | Port75: I/O port(schmitt input) |
| /SDA1 | | I/O | $I^2$CBUS SDA1 line |
| /AIN0 | | Input | Analog input 0: Analog input signal for A/D converter |
| P76 | 1 | I/O | Port76: I/O ports(schmitt input) |
| /SCL1 | | I/O | $I^2$CBUS SCL1 line |
| AIN1 | | Input | Analog input 1: Analog input signal for A/D converter |
| P80 | 1 | I/O | Port80: I/O port(schmitt input) |
| /CTLIN | | Input | PBCTL Capture input(Capture 0) |
| P81 | 1 | I/O | Port81: I/O port(schmitt input) |
| /DFGIN | | Input | DFG Capture input(Capture 1) |

Table 2.2.1 Pin Names and Function (2/3)

| Pin name | Number of pins | I/O | Functions |
|---|---|---|---|
| P82<br>/RMTIN | 1 | I/O<br>Input | Port82: I/O port(schmitt input)<br>Remote Control Signal Capture input |
| P83<br>/EXT | 1 | I/O<br>Input | Port83: I/O port(schmitt input)<br>External Capture input(Capture 0) |
| P84<br>/DPGIN | 1 | I/O<br>Input | Port84: I/O port(schmitt input)<br>DPG Capture input(Capture 0) |
| P85<br>/CFGIN | 1 | I/O<br>Input | Port85: I/O port(schmitt input)<br>CFG Capture input(Capture 2) |
| P86<br>/CSYNCIN | 1 | I/O<br>I/O | Port86: I/O port(schmitt input)<br>C-sync Capture input |
| P87<br>/COMPIN | 1 | I/O<br>I/O | Port87: I/O port(schmitt input)<br>Envelope Comparate Input(to HA/CR) |
| P90<br>/TP0 | 1 | I/O<br>Output | Port90: I/O port<br>Timing Pulse output 0 |
| P91<br>/VASWP<br>/ TPG01 | 1 | I/O<br>Output<br>Output | Port91: I/O port<br>Video/Audio head switching control signal output<br>TPG01: TPG output 01 |
| P92<br>/TP1 | 1 | I/O<br>Output | Port92: I/O port<br>Timing Pulse output 1 |
| P93<br>/TPG03 | 1 | I/O<br>Output | Port93: I/O port<br>TPG03: TPG output 03 |
| P94<br>/CR | 1 | I/O<br>Output | Port94: I/O port<br>Color Rotary Output |
| P95<br>/HA | 1 | I/O<br>Output | Port95: I/O port<br>Head Amp Switching Control Output |
| P96<br>/TO1 | 1 | I/O<br>Output | Port96: I/O port<br>Timer Out 1 |
| P97<br>/TPG11 | 1 | I/O<br>Output | Port97: I/O port<br>TPG11: TPG output 11 |
| PA0<br>/PV-PH<br>/PWM3 | 1 | I/O<br>Output<br>Output | PortA0: I/O port<br>PV/PH 3-state Output<br>PWM(8bit)output 3: Volume control |
| PA3<br>/PWM2 | 1 | I/O<br>Output | PortA3: I/O port<br>PWM(14bit )output 2: Vol.-syn tuner PWM |
| PWM0 | 1 | Output | PWM(14bit) output0: Capstan PWM |
| PWM1 | 1 | Output | PWM(14bit) output1: Drum PWM |
| PB0<br>/XT1 | 1 | I/O<br>Input | PortB0: I/O port(Open Drain Output)<br>Low Frequency Oscillator connecting pin |
| PB1<br>/XT2 | 1 | I/O<br>Output | PortB1: I/O port(Open Drain Output)<br>Low Frequency Oscillator connecting pin |
| PC0 to PC7<br>/G0 to G7 | 8 | Output<br>Output | PortC: High break down voltage Outputs<br>Grid Outputs |

Table 2.2.1 Pin Names and Function (3/3)

| Pin name | Number of pins | I/O | Functions |
|---|---|---|---|
| PD0,1<br>/G8, 9 | 2 | Output<br>Output | PortD: High break down voltage Outputs<br>Grid Outputs |
| PE0 to PE7<br>/S0 to S7 | 8 | I/O | PortE: I/O ports (with pull-down R)<br>Segment Outputs |
| PF0 to PF5<br>/S8 to S13 | 6 | I/O | PortF: I/O ports (with pull-down R)<br>Segment Outputs |
| TEST1 | 1 | Output | TEST1 should be connected with TEST2 pin. |
| TEST2 | 1 | Input | TEST2 |
| TEST3(NC) | 1 | Output | TEST3(NC) should be open connection. |
| CLK | 1 | Output | Clock output: Output (System Clock ÷ 2) clock.<br>pull-up during reset.<br>can be set to Output disable for reducing noise.(Initial Disable) |
| $\overline{\text{TEST}}$ | 1 | Input | Test pin: Always set to "Vcc"level |
| $\overline{\text{RESET}}$ | 1 | Input | Reset: Initializes LSI. (with pull-up R) |
| X1 | 1 | Input | High Frequency Oscillator connecting pins (16 MHz) |
| /X2 | 1 | Output | High Frequency Oscillator connecting pins (16 MHz) |
| VKK | 1 | | VFT Driver power supply pin |
| DVCC | 1 | | Power supply pin |
| DGND | 1 | | GND pin (0 V) |
| ADREF | 1 | | A/D reference Voltage input |
| ADGND | 1 | | A/D ground input |

(2) PROM mode

Table 2.2.2 shows pin function of the TMP93PT75F in PROM mode.

Table 2.2.2 Pin Name and function of PROM mode

| Pin function | Number of pins | Input / Output | Function | Pin name (MCU mode) |
|---|---|---|---|---|
| A7 to A0 | 8 | Input | Memory address of program | P27 to P20 |
| A15 to A8 | 8 | Input | | P17 to P10 |
| A16 | 1 | Input | | PA0 |
| D7 to D0 | 8 | I/O | Memory data of program | P07 to P00 |
| $\overline{CE}$ | 1 | Input | Chip enable | P93 |
| $\overline{OE}$ | 1 | Input | Output control | P91 |
| $\overline{PGM}$ | 1 | Input | Program control | P92 |
| VPP | 1 | Power supply | 12.75 V / 5 V (Power supply of program) | $\overline{TEST}$ |
| VCC | 1 | Power supply | 6.25 V / 5 V | VCC |
| VSS | 2 | Power supply | 0 V | DGNG, ADGND |
| Pin function | Number of pins | Input / Output | Disposal of pin | |
| P90 | 1 | Input | Fix to low level (security pin) | |
| $\overline{RESET}$ | 1 | Input | Fix to low level (PROM mode) | |
| CLK | 1 | Input | | |
| TEST3 | 1 | Output | Open | |
| X1 | 1 | Input | Self oscillation with resonator | |
| X2 | 1 | Output | | |
| P76, P75,<br>P97 to P94 | 6 | Input | Fix to high level | |
| TEST1 / TEST2 | 2 | Input / Output | Short | |
| P47 to P40<br>P54 to P50<br>P74, P73<br>P87 to P80<br>P97, PA3<br>PB1, PB0<br>PC7 to PC0<br>PD1, PD0<br>PE7 to PE0<br>PF5 to PF0<br>PWM0<br>PWM1<br>ADREF<br>VKK | 40 | I / O | Open | |

# 3. Operation

This section describes the functions and basic operational blocks of the TMP93PT75F.
The TMP93PT75F has PROM in place of the mask ROM which is included in the TMP93CT75F. The other configuration and functions are the same as the TMP93CT75F. Regarding the function of the TMP93PT75 (not described), see the part of TMP93CT75F.
The TMP93PT75F has two operational modes : MCU mode and PROM mode.

## 3.1 MCU mode

### (1) Mode-setting and function

The MCU mode is set by opening the CLK pin (pin open). In the MCU mode, the operation is same as TMP93CT75F.

### (2) Memory-map

The memory map of TMP93PT75F is same as that of TMP93CT75F. Figure 3.1.1 shows the memory map in MCU mode. Figure 3.1.2 show that in PROM mode.

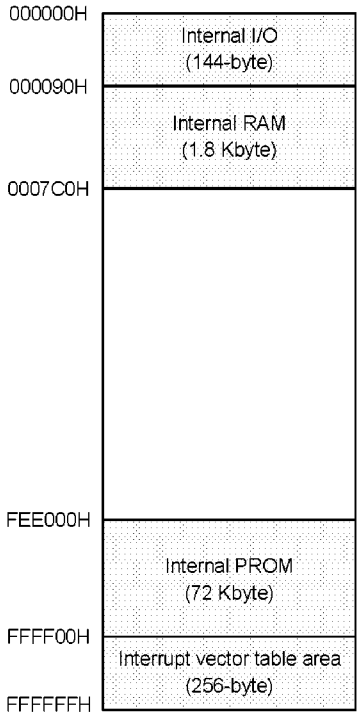



Figure 3.1.1 Memory map in MCU mode

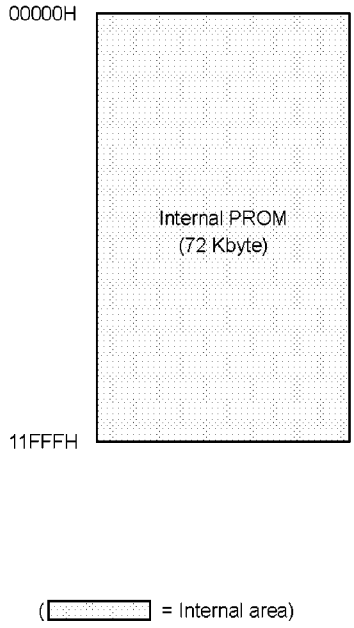



Figure 3.1.2 Memory map in PROM mode

3.2 PROM Mode

(1) Mode setting and Function

PROM mode is set by setting the $\overline{\text{RESET}}$ and CLK pins to the "L" level. The programming and verification for the internal PROM is achieved by using a general EPROM programmer with the adaptor socket.

① Preparation of OTP adaptor

BM11146: for TMP93PT75F

② Setting of OTP adaptor

The switch (SW1) is set to N side.

③ Setting of PROM writer

i) Set PROM type to TC 571000D.

Size: 1 Mbyte

VPP: 12.75 V

tPW: 100 μs

Electric Signature mode: none

ii) Data transmittion

In TMP93PT75F, PROM is placed on addresses 00000 to 11FFFH in PROM mode, and addresses FFE000H to FFFFFFH in MCU mode. Therefore data should be transferred to addresses 00000 to 11FFFH in PROM mode using the object converter (tuconv) or the block transfer mode (see instruction manual of PROM programmer.)

iii) Setting of the program address

Start address: 00000H

End address: 11FFFH

④ Programming

Program and verify according to operating process of PROM programmer.

Figure 3.2.1 shows the setting of the pins in PROM mode.

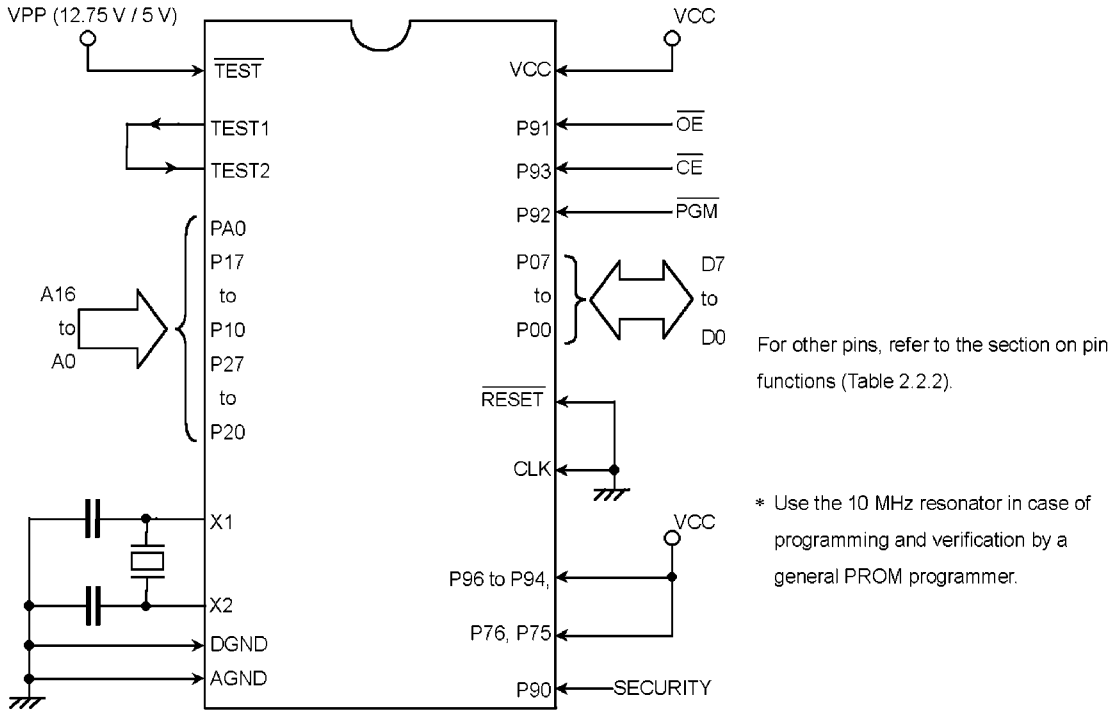



Figure 3.2.1 PROM Mode Pin Setting

(2) Caution for Electric Signature

The TMP93PT75F dose not support the electric signature mode (hereinafter referred to as "signature"). If PROM programmer used the signature, the device would be damaged because of applying voltage of 12 ± 0.5 V to pin 9 (A9) of the address.

Please use without setting the signature.

(3) Program Mode

All bits of the TMP93PT75F are "1" when delivered (the erase state). Data "0" is written in the necessary bit location during program operating.

Writing function can be operated at VPP=12.5 V, $\overline{OE} = V_{IH}$, $\overline{CE} = V_{IL}$. Built-in one time PROM can be written in any sequence. It is possible to write only special address.

(4) Adopter Socket (BM11146 : for TMP93PT75F)

BM11146 is the adapter sockets to write data into the TMP93PT75F. The TMP93PT75F has built-in one time PROM using a general EPROM programmer.

(5) Program Storing Area of PROM Mode

The TMP93PT75F has the program space (FEE000H to FFFFFFH) of 72 Kbytes. The address 00000H to 11FFFH of PROM mode equals to the address FEE000H to FFFFFFH of MCU mode.

(6) Program Write Setting Method Using a general EPROM programmer

PROM to be prepared should equal to TC571000D functions.

1. Set the switch (SW1) of BM11146 (hereinafter referred to as "adapter" ) to the program side (NOR). (Note1)
2. Connect MCU to the adapter. (Note2)
3. Connect the adapter to PROM programmer. (Note2)
4. Set the PROM type of PROM programmer to TC571000D.
5. Set the start address for writing PROM to 00000H, and the end address to 11FFFH. (Note 3)
6. Writing to built-in one time PROM and verifying should be operated according to the operation procedures of PROM programmer.

Note1: If data is written to built-in one time PROM without setting the switch (SW1) to the program side, the device would be damaged.

Note2: Please set with the first pin of the adapter and that of PROM programmer socket matched. If the first pin is conversely set, MCU or programmer would be damaged.

Note3: If data "0" is written to the address which is over 11FFFH, the contents of the original program would be damaged because of writing "0" to the addresses 00000H to 11FFFH.

(7) Programming Flow Chart

The programming mode is set by applying 12.75 V (programming voltage) to the VPP pin when the following pins are set as follows,

(VCC: 6.25 V, $\overline{RESET}$ : "L" level, CLK: "L" level).

While address and data are fixed and $\overline{CE}$ pin is set to "L" level, 0.1 ms of "L" level pulse is applied to PGM pin to program the data.

Then the data in the address is verified.

If the programmed data is incorrect, another 0.1 ms pulse is applied to $\overline{PGM}$ pin.

This programming procedure is repeated until correct data is read from the address. (25 times maximum)

Subsequently, all data are programmed in all addresses.

The verification for all data is done under the condition of Vpp = Vcc = 5 V after all data were written.

Figure 3.2.2 shows the programming flow chart.

Flow chart

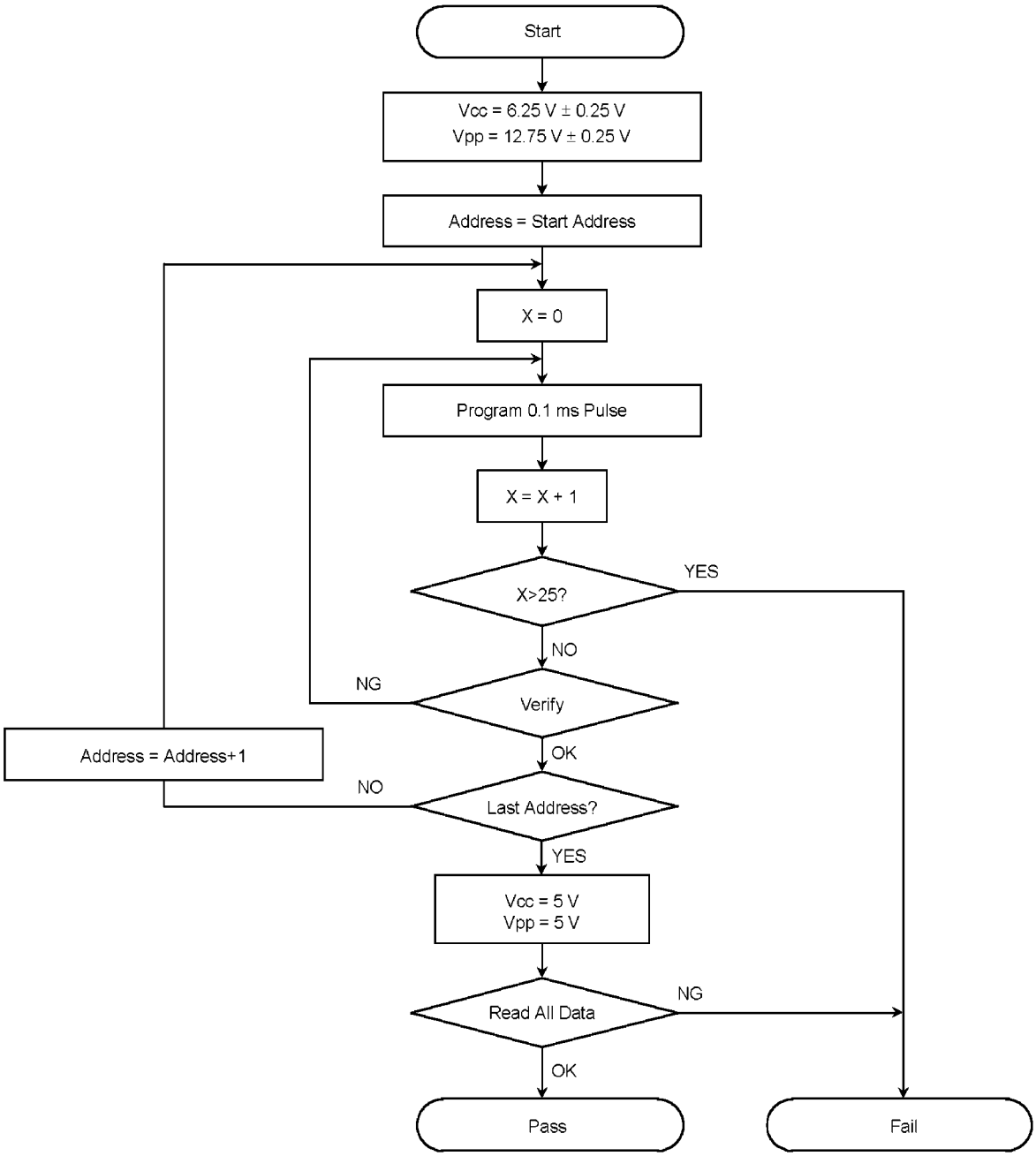



Figure 3.2.2 Flow chart

(8) Security Bit

The TMP93PT75F has a Security Bit in PROM cell.

If the Security Bit is programmed to "0", the content of the PROM is disable to be read (FFH data) in PROM mode.

(How to program the Security Bit.)

The difference from the programming procedures described in section 3.2 (1) are follows.

① Setting OTP adapter

Set the switch (SW1) to S side.

② Setting PROM programmer

i) Transferring the data

ii) Setting of programming address

The security bit is in bit 0 of address 00000H.

Set the start address 00000H and the end address 00000H.

Set the data FEH at the address 00000H.

# 4. Electrical Characteristics

## 4.1 Absolute Maximum Rating

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Power Supply Voltage | Vcc | −0.5 to 6.5 | V |
| Input Voltage | $V_{IN}$ | −0.5 to Vcc+0.5 | |
| Output Voltage (except PC, PD, PE, PF) | $V_{OUT1}$ | −0.5 to Vcc+0.5 | |
| Output Voltage (PC, PD, PE, PF) | $V_{OUT2}$ | Vcc−40 | |
| Output Current (except PC, PD, PE, PF) (per 1 pin) | $I_{OH1}$ | −3.2 | mA |
| Output Current (PC, PD) (per 1 pin) | $I_{OH2}$ | −25 | |
| Output Current (PE, PF) (per 1 pin) | $I_{OH3}$ | −15 | |
| Output Current (per 1 pin) | $I_{OL}$ | 3.2 | |
| Output Current (total except PC, PD, PE, PF) | $\Sigma I_{OH1}$ | −40 | |
| Output Current (total of PC, PD, PE, PF) | $\Sigma I_{OH2}$ | −120 | |
| Output Current (total) | $\Sigma I_{OL}$ | 120 | |
| Power Dissipation (Ta = 70°C) | PD | 600 | mW |
| Soldering Temperature | Tsolder | 260 | °C |
| Storage Temperature | Tstg | −65 to 150 | |
| Operating Temperrature | Topr | −20 to 70 | |

Note) The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

## 4.2 DC Characteristics (1/2)

Ta = −20 to 70°C

| Parameter | | Symbol | Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| Power Supply Voltage | | Vcc | fc = 4 to 16 MHz | 4.5 | | 5.5 | V |
| | | | fs = 30 to 34 kHz | 2.7 | | | |
| Input LowVoltage | P0,P1,P2,P4, P9,PA,PB,PE ,PF | $V_{IL1}$ (CMOS) | Vcc = 2.7 to 5.5 V | −0.3 | | 0.3 Vcc | V |
| | $\overline{RESET}$, P5,P7,P8 | $V_{IL2}$ (Schmit) | | | | 0.25 Vcc | |
| | $\overline{TEST}$ | $V_{IL3}$ (Fixed) | | | | 0.3 | |
| | X1 | $V_{IL4}$ (Xtal) | | | | 0.2 Vcc | |

4.2 DC Characteristics (2/2)

Ta = −20 to 70°C

| Parameter | | Symbol | Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| Input High Voltage | P0,P1,P2,P4, P9,PA,PB,PE ,PF | $V_{IH1}$ (CMOS) | Vcc = 2.7 to 5.5 V | 0.7Vcc | | Vcc + 0.3 | V |
| | $\overline{RESET}$ , P5,P7,P8 | $V_{IH2}$ (Schmit) | | 0.75Vcc | | | |
| | $\overline{TEST}$ | $V_{IH3}$ (Fixed) | | Vcc−0.3 | | | |
| | X1 | $V_{IH4}$ (Xtal) | | 0.8Vcc | | | |
| Output Low Voltage | | $V_{OL}$ | $I_{OL}$ = 1.6 mA (Vcc = 2.7 to 5.5 V) | | | 0.45 | V |
| Output High Voltage | | $V_{OH}$ | $I_{OH}$ = −400 μA (Vcc = 2.7 to 5.5 V) | 2.4 | | | V |
| | | $V_{OH1}$ | $I_{OH}$ = −700 μA (Vcc = 4.5 to 5.5 V) | 4.1 | | | |
| PE, PF | | $I_{OH}$ | Vcc = 4.5 V | −5 | | | mA |
| PC, PD | | | $V_{OH}$ = 2.4 V | −15 | | | |
| Input Leakage Current | | $I_{LI}$ | 0.0 ≦ Vin ≦ Vcc | | 0.02 | ±5 | μA |
| Output Leakage Current | | $I_{LO}$ | 0.0 ≦ Vin ≦ Vcc−0.2 | | 0.05 | ±10 | |
| Power Down Voltage | | $V_{STOP}$ | $V_{IL2}$ = 0.2 Vcc, $V_{IH2}$ = 0.8 Vcc | 2.0 | | 6.0 | V |
| $\overline{RESET}$ Pull Up Resister | | Rrst | Vcc = 5 V ± 10% | 50 | | 150 | kΩ |
| | | | Vcc = 3 V ± 10% | 80 | | 200 | |
| Pin Capacitance | | $C_{IO}$ | OSC = 1 MHz/100 mVP-P | | | 10 | pF |
| Schmitt Width $\overline{RESET}$ , P5,P7,P8, | | $V_{TH}$ | | | 1.0 | | V |
| NORMAL | | Icc | Vcc = 5 V ± 10% fc = 16 MHz | | 30 | 50 | mA |
| RUN | | | | | 17 | 25 | |
| IDLE2 | | | | | 15 | 25 | |
| IDLE1 | | | | | 2.5 | 4 | |
| SLOW | | | Vcc = 3 V ± 10% fs = 32.768 kHz (Typ: Vcc = 3.0V) | | 50 | 80 | μA |
| RUN | | | | | 16 | 30 | |
| IDLE2 | | | | | 25 | 40 | |
| IDLE1 | | | | | 4 | 15 | |
| STOP | | | Vcc = 2.7 to 5.5 V | | 0.2 | 10 | |

Note 1: Typical value are for Ta = 25°C and Vcc = 5 V unless otherwise noted.

Note 2: Icc measurement conditions (NORMAL,SLOW).
Only CPU is operational;output pins are open and input pins are fixed.

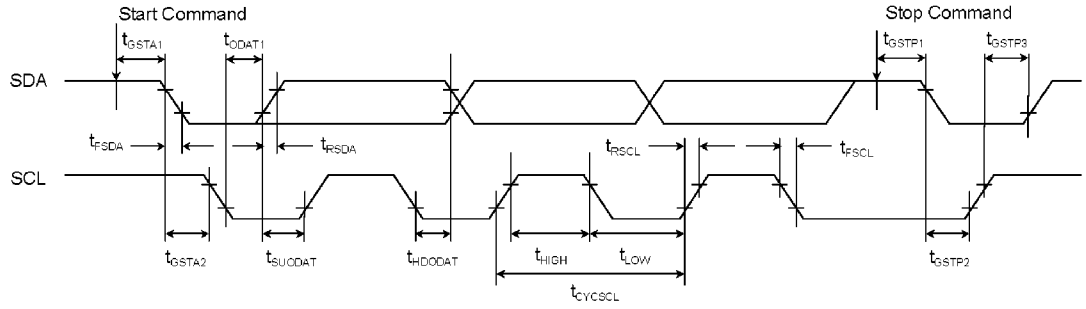
4.3 A/D Conversion Characteristics

Ta = −20 to 70°C, Vcc = 4.5 to 5.5 V

| Parameter | Symbol | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|
| Analog Reference Voltage Supply | ADREF | Vcc−1.5 | Vcc | Vcc | V |
| | ADGND | Vss | Vss | Vss | V |
| Analog Input Voltage Range | VAIN | ADGND | — | ADREF | V |
| Analog Current for ADREF | IREF | — | 1.0 | 1.5 | mA |
| Error | | | | ±3 | LSB |

## 4.4 Serial BUS Interface Timing

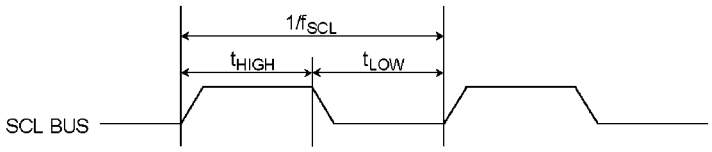
### (1) I²CBUS Logic Timing




| Parameter | Symbol | Min | Standerd | Max | Unit |
|---|---|---|---|---|---|
| SCL cycle | $t_{CYCSCL}$ | 16N+12/f | — | — | s |
| SCL low pulse width | $t_{LOW}$ | — | 8N | — | s |
| SCL High pulse width | $t_{HIGH}$ | 8N+10/f | — | — | s |
| SDA Rising Time (Note 1) | $t_{RSDA}$ | — | — | — | s |
| SDA Falling Time (Note 1) | $t_{FSDA}$ | — | — | — | s |
| SCL Rising Time (Note 1) | $t_{RSCL}$ | — | — | | s |
| SCL Falling Time (Note 1) | $t_{FSCL}$ | — | — | | s |
| The time from start command write to start sheecense | $t_{GSTA1}$ | — | 6/f | | s |
| Start condition hold time, start generation of the first clock after this | $t_{GSTA2}$ | — | 8N+4/f | | s |
| Delay time from SCL rising to data output (Note 2) | $t_{ODAT1}$ | — | — | 10/f | s |
| Set up time of data output for SCL rising (Note 2) | $t_{SUODAT}$ | 8N – (10/f+$t_{FSCL}$) | — | — | s |
| The time of holding data for SCL rising (Note 3) | $t_{HODAT}$ | 3/f | - | — | s |
| The time from stop command write to starting stop sheecense | $t_{GSTP1}$ | — | 6/f | — | s |
| The time from SDA falling to SCL rising (during stop sheecense) | $t_{GSTP2}$ | — | 8N+14/f | — | s |
| Stop condition set up time | $t_{GSTP3}$ | 8N+14/f | — | — | s |

Note1: The time of rising/falling depend on the feature of bus interface.
Note2: The worst case is at the first bit of slave address.
Note3: The worst case is at the acknowledge bit.

(2) Master SCL output timing




@ fc = 16 MHz

$t_{HIGH}$ = 8 N/fc
$t_{LOW}$ = 8 N/fc + 8/fc + 4X/fc
fSCL = 1 / ($t_{LOW}$ + $t_{HIGH}$)

N: Dividing value set by I2CCR1 <SCK2 : 0>
X: Delay constant value between internal SCL and external SCL

ex1: Delay constant value between internal SCL and external SCL is "0".
I2CCR1 <SCK2 : 0> = 011 (60.6 kHz)
1/ (8 × 16/16 + 8 × 16/16 + 8/16 + 4 × 0/16) = 60.6 kHz

ex2: Delay constant value between internal SCL and external SCL is "3".
I2CCR1 <SCK2 : 0> = 011 (60.6 kHz)
1/ (8 × 16/16 + 8 × 16/16 + 8/16 + 4 × 3/16) = 60.6 kHz

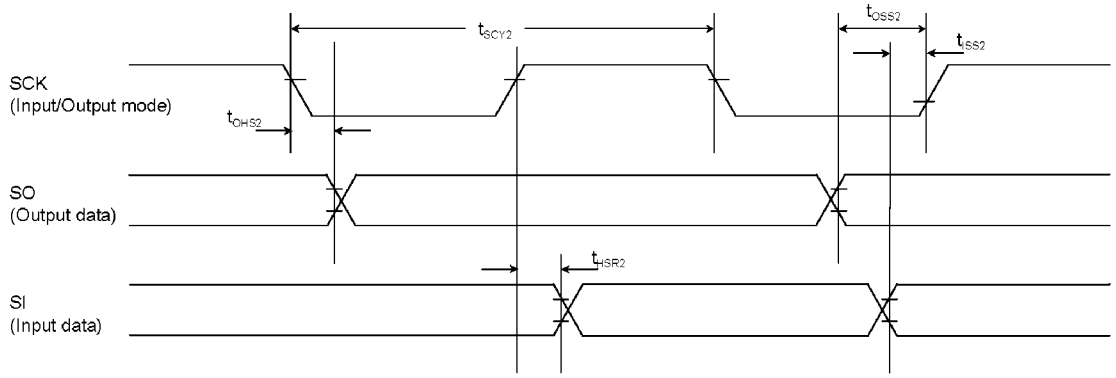
(3) Clock Syncro 8 bit SIO mode

1. SCK Input mode

| Parameter | Symbol | Expression | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| SCK cycle | $t_{SCY2}$ | $2^5X$ | | s |
| SCK falling→Latch output data | $t_{OHS2}$ | 6X | | s |
| Enable output data→SCK raising | $t_{OSS2}$ | $t_{SCY2} - 6X$ | | s |
| SCK raising→Latch input data | $t_{HSR2}$ | 6X | | ns |
| Enable input data→SCK raising | $t_{ISS2}$ | 0 | | ns |

2. SCK Output mode

| Parameter | Symbol | Expression | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| SCK cycle | $t_{SCY2}$ | $2^5X$ | $2^{11}X$ | s |
| SCK falling→Latch output data | $t_{OHS2}$ | 2X | | s |
| Enable output data→SCK raising | $t_{OSS2}$ | $t_{SCY2} - 6X$ | | s |
| SCK raising→Latch input data | $t_{HSR2}$ | 2X | | s |
| Enable input data→SCK raising | $t_{ISS2}$ | 0 | | ns |



## 4.5 Read operation in PROM mode

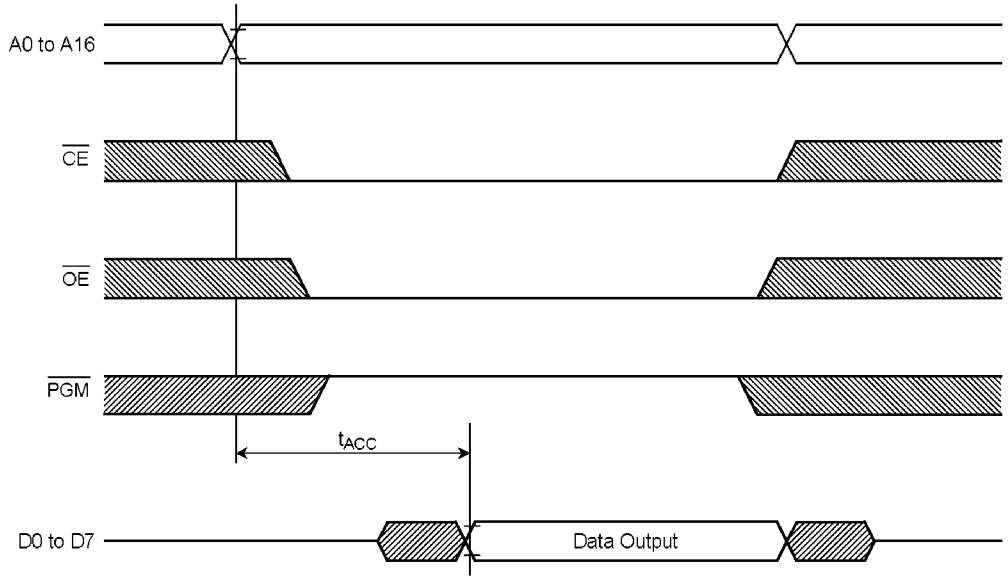
DC/AC characteristics

Ta = 25 + 5°C Vcc = 5 V ± 10 %

| Parameter | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{PP}$ Read Voltage | $V_{PP}$ | — | 4.5 | 5.5 | V |
| Input High Voltage (A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$) | $V_{IH1}$ | — | 2.2 | VCC + 0.3 | V |
| Input low Voltage (A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$) | $V_{IL1}$ | — | −0.3 | 0.8 | V |
| Address to Output Delay | $t_{ACC}$ | $C_L$ = 50 pF | — | 2.25TCYL + $\alpha$ | ns |

TCYC = 400 ns(10 MHz Clock)

$\alpha$ = 20 ns

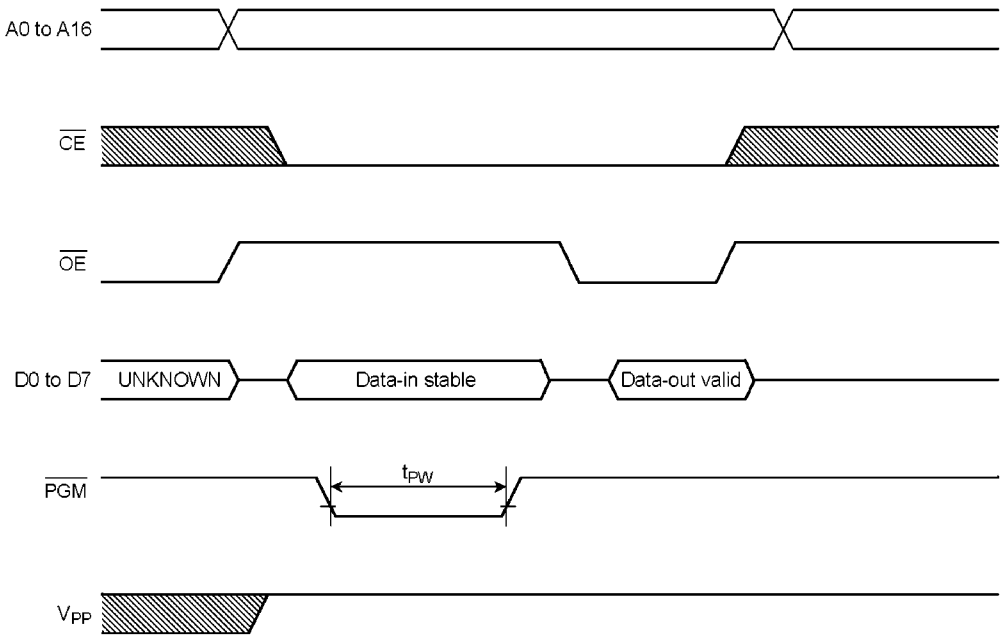


4.6 Program operation in PROM mode

DC/AC characteristics

Ta = 25 + 5°C Vcc = 6.25 V ± 0.25 %

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Programming Supply Voltage | $V_{PP}$ | — | 12.50 | 12.75 | 13.00 | V |
| Input High Voltage (D0 to D7, A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$) | $V_{IH}$ | — | 2.6 | | $V_{CC}$ + 0.3 | V |
| Input low Voltage (D0 to D7, A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$) | $V_{IL}$ | — | −0.3 | | 0.8 | V |
| $V_{CC}$ Supply Current | $I_{CC}$ | fc = 10 MHz | — | | 50 | mA |
| $V_{PP}$ Supply Current | $I_{PP}$ | $V_{PP}$ = 13.00 MHz | — | | 50 | mA |
| $\overline{PGM}$ Program Pulse Width | $T_{PW}$ | $C_L$ = 50 pF | 0.095 | 0.1 | 0.105 | ms |




Note1: The power suppply of VPP (12.75 V) must be set power-on at the same time or the later time for a power supply of VCC and must be cliar power-on at th esame time or early time for a power supply of VCC.

Note2: The pulling up/down device on condition of VPP = 12.75 suffers a damage for the device.

Note3: The maximum spec of VPP pin is 14.0 V. Be carefull a ocershoot at the programming.