

## Low Voltage / Low Power CMOS 16-Bit Microcontrollers

### TMP93CS40F / TMP93CS41F TMP93CS40DF / TMP93CS41DF

## 1. OUTLINE AND DEVICE CHARACTERISTICS

The TMP93CS40/S41 are high-speed advanced 16-bit microcontrollers developed for controlling medium-to large-scale equipment. The TMP93CS41 does not have a ROM; the TMP93CS40 has a built-in ROM. Otherwise, the devices function in the same way.

The TMP93CS40/S41F are housed in a 100-pin flat package.

The device characteristics are as follows:

- (1) Original 16-bit CPU (900/L CPU)
  - TLCS-90 instruction mnemonic upward-compatible
  - 16-Mbyte linear address space
  - General-purpose registers, register bank system
  - 16-bit multiplication / division and bit transfer / arithmetic instructions
  - Micro DMA : 4 channels (1.6  $\mu$ s / 2 bytes at 20 MHz)
- (2) Minimum instruction execution time : 200 ns at 20 MHz
- (3) Internal RAM : 2 Kbyte  
Internal ROM :
 

|           |              |
|-----------|--------------|
| TMP93CS40 | 64-Kbyte ROM |
| TMP93CS41 | None         |
- (4) External memory expansion
  - Can be expanded to up to 16M bytes (for both programs and data).
  - AM8 /  $\overline{16}$  pin (selects the external data bus width)
  - Can mix 8- and 16-bit external data buses.
  - ... Dynamic bus sizing
- (5) 8-bit timer : 2 channels
- (6) 8-bit PWM timer : 2 channels
- (7) 16-bit timer : 2 channels
- (8) Pattern generator : 2 channels
- (9) 4-bit serial interface : 2 channels
- (10) 10-bit A/D converter : 8 channels
- (11) Watchdog timer
- (12) Chip select / wait controller : 3 blocks
- (13) Interrupt functions : 29
  - 9 CPU interrupts... SWI instruction, and Illegal instruction
  - 14 internal interrupts
  - 6 external interrupts

} 7-level priority can be set.
- (14) I/O ports  
79 pins for TMP93CS40 and 61 pins for TMP93CS41
- (15) Standby function : 4 Halt modes (Run, Idle2, Idle1, Stop)
- (16) Clock gear function
  - Dual clock operation
  - Clock gear: High-frequency clock can be varied from  $f_c$  to  $f_c / 16$ .

## (17) Wide Operating Voltage

- $V_{CC} = 2.7$  to  $5.5$  V

## (18) Package

| Type No.                   | Package             |
|----------------------------|---------------------|
| TMP93CS40F<br>TMP93CS41F   | QFP100-P-1414-0.50  |
| TMP93CS40DF<br>TMP93CS41DF | QFP100-P-1414-0.50C |

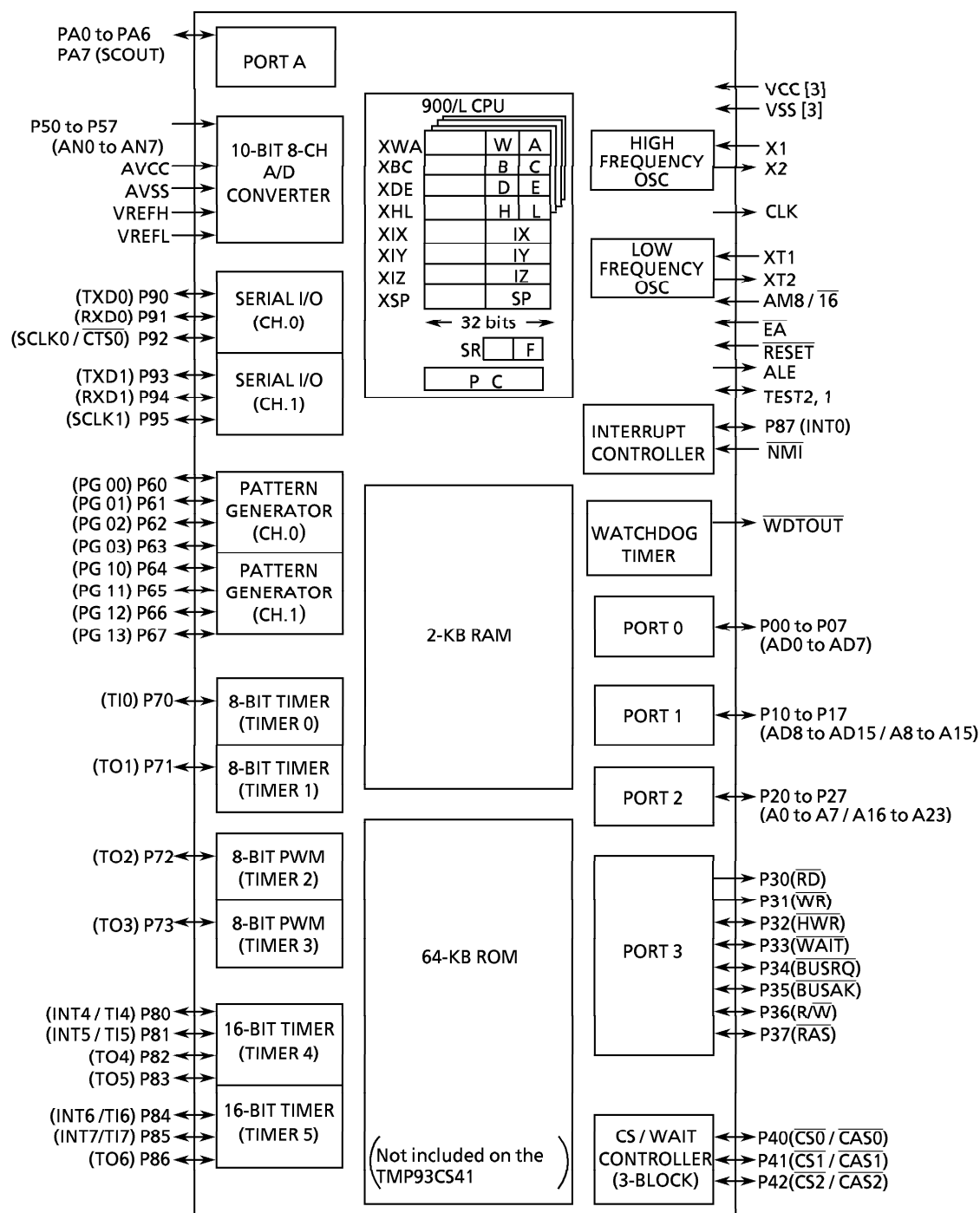


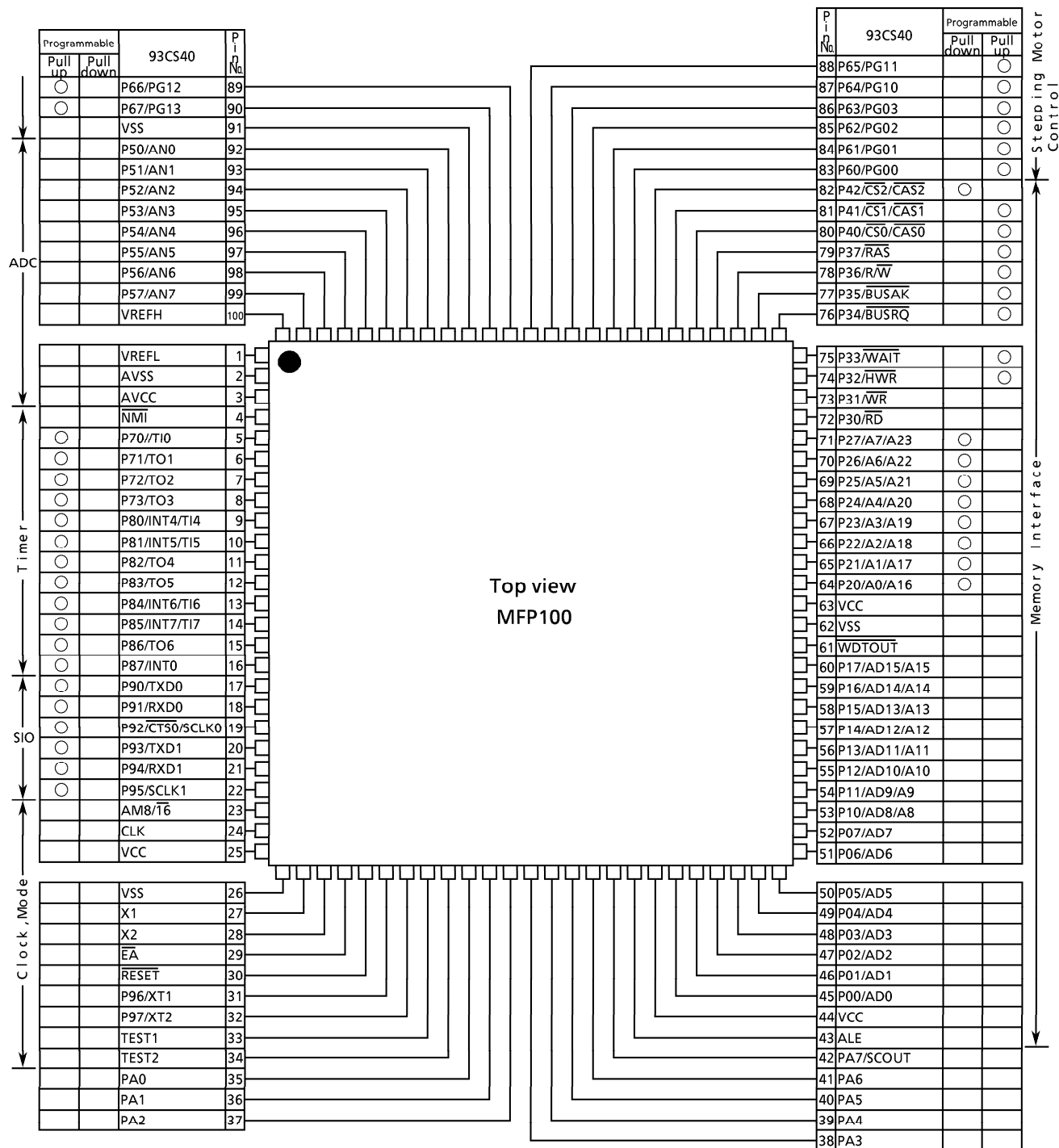
Figure 1 TMP93CS40/TMP93CS41 Block Diagram

## **2. PIN ASSIGNMENT AND FUNCTIONS**

The assignment of input / output pins on the TMP93CS40/TMP93CS41, their names and outline functions are described below.

### **2.1 Pin Assignment**

Figure 2.1 shows the pin assignment for the TMP93CS40F/S41F and TMP93CS40DF/S41DF.



(Note) Because the TMP93CS41 does not have an internal ROM, pins P00 to P17 are tied to AD0 to AD15 (when AM8 /  $\overline{I6}$  = 0), or to AD0 to AD7 and A8 to A15 (when AM8 /  $\overline{I6}$  = 1). P30 is tied to RD, P31 to WR.

Figure 2.1 Pin Assignment (100-pin MFP)

## 2.2 Pin Names and Functions

The names of the input / output pins and their functions are described below.

Table 2.2 Pin Names and Functions

| Pin Name                                         | Number of Pins | I/O                         | Function                                                                                                                                                                                                                                 |
|--------------------------------------------------|----------------|-----------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| P00 to P07<br>AD0 to AD7                         | 8              | I/O<br>Tri-State            | Port 0: I/O port that allows at the bit level<br>Address/data (lower): Bits 0 to 7 of address/data bus                                                                                                                                   |
| P10 to P17<br>AD8 to AD15<br>A8 to A15           | 8              | I/O<br>Tri-State<br>Output  | Port 1: I/O port that allows at the bit level<br>Address data (upper): Bits 8 to 15 of address/data bus<br>Address: Bits 8 to 15 of address bus                                                                                          |
| P20 to P27<br>A0 to A7<br>A16 to A23             | 8              | I/O<br><br>Output<br>Output | Port 2: I/O port that allows selection of I/O at the bit level<br>(with pull-down resistor)<br>Address: bits 0 to 7 of address bus<br>Address: bits 16 to 23 of address bus                                                              |
| P30<br>$\overline{RD}$                           | 1              | Output<br>Output            | Port 30: Output port<br>Read: Strobe signal for reading external memory                                                                                                                                                                  |
| P31<br>$\overline{WR}$                           | 1              | Output<br>Output            | Port 31: Output port<br>Write: Strobe signal for writing data on pins AD0 to AD7                                                                                                                                                         |
| P32<br>$\overline{HWR}$                          | 1              | I/O<br>Output               | Port 32: I/O port (with pull-up resistor)<br>High write: Strobe signal for writing data on pins AD8 to AD15                                                                                                                              |
| P33<br>$\overline{WAIT}$                         | 1              | I/O<br>Input                | Port 33: I/O port (with pull-up resistor)<br>Wait: Pin used to request CPU bus wait                                                                                                                                                      |
| P34<br>$\overline{BUSRQ}$                        | 1              | I/O<br>Input                | Port 34: I/O port (with pull-up resistor)<br>Bus request: Signal used to request bus release                                                                                                                                             |
| P35<br>$\overline{BUSAK}$                        | 1              | I/O<br>Output               | Port 35: I/O port (with pull-up resistor)<br>Bus acknowledge: Signal used to acknowledge bus release                                                                                                                                     |
| P36<br>$R/\overline{W}$                          | 1              | I/O<br>Output               | Port 36: I/O port (with pull-up resistor)<br>Read/write: 1 represents read or dummy cycle; 0 represents write cycle.                                                                                                                     |
| P37<br>$\overline{RAS}$                          | 1              | I/O<br>Output               | Port 37: I/O port (with pull-up resistor)<br>Row address strobe: Outputs $\overline{RAS}$ strobe for DRAM.                                                                                                                               |
| P40<br>$\overline{CS0}$<br><br>$\overline{CAS0}$ | 1              | I/O<br>Output<br><br>Output | Port 40: I/O port (with pull-up resistor)<br>Chip select 0: Outputs 0 when address is within specified address area.<br>Column address strobe 0: Outputs $\overline{CAS}$ strobe for DRAM when address is within specified address area. |

Note : This device's built-in memory or built-in I/O cannot be accessed by an external DMA controller using the  $\overline{BUSRQ}$  and  $\overline{BUSAK}$  signals.

| Pin Name                   | Number of Pins | I/O                     | Function                                                                                                                                                                                                                  |
|----------------------------|----------------|-------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| P41<br>CS1<br>CAS1         | 1              | I/O<br>Output<br>Output | Port 41: I/O port (with pull-up resistor)<br>Chip select 1: Outputs 0 if address is within specified address area.<br>Column address strobe 1: Outputs CAS strobe for DRAM if address is within specified address area.   |
| P42<br>CS2<br>CAS2         | 1              | I/O<br>Output<br>Output | Port 42: I/O port (with pull-down resistor)<br>Chip select 2: Outputs 0 if address is within specified address area.<br>Column address strobe 2: Outputs CAS strobe for DRAM if address is within specified address area. |
| P50 to P57<br>AN0 to AN7   | 8              | Input<br>Input          | Port 5: Input port<br>Analog input: Analog signal input for A/D converter                                                                                                                                                 |
| VREFH                      | 1              | Input                   | Pin for high level reference voltage input to A/D converter                                                                                                                                                               |
| VREFL                      | 1              | Input                   | Pin for low level reference voltage input to A/D converter                                                                                                                                                                |
| P60 to P63<br>PG00 to PG03 | 4              | I/O<br>Output           | Ports 60 - 63: I/O ports that allow selection of I/O at the bit level (with pull-up resistor)<br>Pattern generator ports: 00 to 03                                                                                        |
| P64 to P67<br>PG10 to PG13 | 4              | I/O<br>Output           | Ports 64 - 67: I/O ports that allow selection of I/O on a bit basis (with pull-up resistor)<br>Pattern generator ports: 10 to 13                                                                                          |
| P70<br>TI0                 | 1              | I/O<br>Input            | Port 70: I/O port (with pull-up resistor)<br>Timer input 0: Timer 0 input                                                                                                                                                 |
| P71<br>TO1                 | 1              | I/O<br>Output           | Port 71: I/O port (with pull-up resistor)<br>Timer output 1: Timer 0 or timer 1 output                                                                                                                                    |
| P72<br>TO2                 | 1              | I/O<br>Output           | Port 72: I/O port (with pull-up resistor)<br>PWM output 2: 8-bit PWM timer 2 output                                                                                                                                       |
| P73<br>TO3                 | 1              | I/O<br>Output           | Port 73: I/O port (with pull-up resistor)<br>PWM output 3: 8-bit PWM timer 3 output                                                                                                                                       |
| P80<br>TI4<br>INT4         | 1              | I/O<br>Input<br>Input   | Port 80: I/O port (with pull-up resistor)<br>Timer input 4: Timer 4 count / capture trigger signal input<br>Interrupt request pin 4: Interrupt request pin with programmable rising / falling edge                        |
| P81<br>TI5<br>INT5         | 1              | I/O<br>Input<br>Input   | Port 81: I/O port (with pull-up resistor)<br>Timer input 5: Timer 5 count / capture trigger signal input<br>Interrupt request pin 5: Interrupt request pin with rising edge                                               |
| P82<br>TO4                 | 1              | I/O<br>Output           | Port 82: I/O port (with pull-up resistor)<br>Timer output 4: Timer 4 output pin                                                                                                                                           |
| P83<br>TO5                 | 1              | I/O<br>Output           | Port 83: I/O port (with pull-up resistor)<br>Timer output 5: Timer 4 output pin                                                                                                                                           |

| Pin Name             | Number of Pins | I/O                   | Function                                                                                                                                                                                           |
|----------------------|----------------|-----------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| P84<br>TI6<br>INT6   | 1              | I/O<br>Input<br>Input | Port 84: I/O port (with pull-up resistor)<br>Timer input 6: Timer 5 count / capture trigger signal input<br>Interrupt request pin 6: Interrupt request pin with programmable rising / falling edge |
| P85<br>TI7<br>INT7   | 1              | I/O<br>Input<br>Input | Port 85: I/O port (with pull-up resistor)<br>Timer input 7: Timer 5 count / capture trigger signal input<br>Interrupt request pin 7: Interrupt request pin with rising edge                        |
| P86<br>TO6           | 1              | I/O<br>Output         | Port 86: I/O port (with pull-up resistor)<br>Timer output 6: Timer 5 output pin                                                                                                                    |
| P87<br>INT0          | 1              | I/O<br>Input          | Port 87: I/O port (with pull-up resistor)<br>Interrupt request pin 0: Interrupt request pin with programmable level / rising edge                                                                  |
| P90<br>TXD0          | 1              | I/O<br>Output         | Port 90: I/O port (with pull-up resistor)<br>Serial data send 0                                                                                                                                    |
| P91<br>RXD0          | 1              | I/O<br>Input          | Port 91: I/O port (with pull-up resistor)<br>Serial data receive 0                                                                                                                                 |
| P92<br>CTS0<br>SCLK0 | 1              | I/O<br>Input<br>I/O   | Port 92: I/O port (with pull-up resistor)<br>Serial data send enable 0 (Clear to Send)<br>Serial Clock I/O 0                                                                                       |
| P93<br>TXD1          | 1              | I/O<br>Output         | Port 93: I/O port (with pull-up resistor)<br>Serial data send 1                                                                                                                                    |
| P94<br>RXD1          | 1              | I/O<br>Input          | Port 94: I/O port (with pull-up resistor)<br>Serial data receive 1                                                                                                                                 |
| P95<br>SCLK1         | 1              | I/O<br>I/O            | Port 95: I/O port (with pull-up resistor)<br>Serial clock I/O 1                                                                                                                                    |
| PA0 to PA6           | 7              | I/O                   | Ports A0 to A6: I/O ports                                                                                                                                                                          |
| PA7<br>SCOUT         | 1              | I/O<br>Output         | Port A7: I/O port<br>System Clock Output: Outputs $f_{FPH}$ or $f_{SYS}$ clock.                                                                                                                    |
| WD $\overline{TOUT}$ | 1              | Output                | Watchdog timer output pin                                                                                                                                                                          |
| NMI                  | 1              | Input                 | Non-maskable interrupt request pin: Interrupt request pin with programmable falling edge or with both edges programmable.                                                                          |
| CLK                  | 1              | Output                | Clock output: Outputs $\lceil f_{SYS} \div 2 \rceil$ clock.<br>Pulled-up during reset.<br>Can be disabled to reduce noise.                                                                         |
| $\overline{EA}$      | 1              | Input                 | External access: On the TMP93CS41, the $V_{SS}$ pin should be connected.<br>On the TMP93CS40, the $V_{CC}$ pin should be connected.                                                                |

| Pin Name                  | Number of Pins | I/O               | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|---------------------------|----------------|-------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| AM8 / $\overline{16}$     | 1              | Input             | <p>Address Mode: Selects external Data Bus width.<br/>(On the TMP93CS40)<br/>The Vcc pin should be connected. The Data Bus Width for external access is set by the Chip Select / WAIT Control register, Port 1 Control register.</p> <p>(On the TMP93CS41)<br/>The Vss pin should be connected to access either fixed 16-bit Bus width, or 16-bit Bus interchangeable with 8-bit Bus.<br/>The Vcc pin should be connected to access a fixed 8-bit Bus Width.</p> |
| ALE                       | 1              | Output            | Address Latch Enable<br>(Can be disabled to reduce noise.)                                                                                                                                                                                                                                                                                                                                                                                                       |
| $\overline{\text{RESET}}$ | 1              | Input             | Reset: Initializes TMP93CS40/TMP93CS41. (with pull-up resistor)                                                                                                                                                                                                                                                                                                                                                                                                  |
| X1/X2                     | 2              | I/O               | High Frequency Oscillator connecting pin                                                                                                                                                                                                                                                                                                                                                                                                                         |
| P96<br>XT1                | 1              | I/O<br>Input      | Port 96: I/O port (open drain output)<br>Low Frequency Oscillator connecting pin                                                                                                                                                                                                                                                                                                                                                                                 |
| P97<br>XT2                | 1              | I/O<br>Output     | Port 97: I/O port (open drain output)<br>Low Frequency Oscillator connecting pin                                                                                                                                                                                                                                                                                                                                                                                 |
| TEST1 / TEST2             | 2              | Output<br>/ Input | TEST1: should be connected to TEST2 pin.                                                                                                                                                                                                                                                                                                                                                                                                                         |
| VCC                       | 3              |                   | Power supply pin (All VCC pins should be connected to the power supply pin.)                                                                                                                                                                                                                                                                                                                                                                                     |
| VSS                       | 3              |                   | GND pin (0 V) (All VSS pins should be connected to GND (0V).)                                                                                                                                                                                                                                                                                                                                                                                                    |
| AVCC                      | 1              |                   | Power supply pin for A/D converter                                                                                                                                                                                                                                                                                                                                                                                                                               |
| AVSS                      | 1              |                   | GND pin for A/D converter (0 V)                                                                                                                                                                                                                                                                                                                                                                                                                                  |

Note : All pins that have built-in pull-up/down resistors (other than the  $\overline{\text{RESET}}$  pin) can be disconnected from the built-in pull-up/down resistor by software.

### **3. Operation**

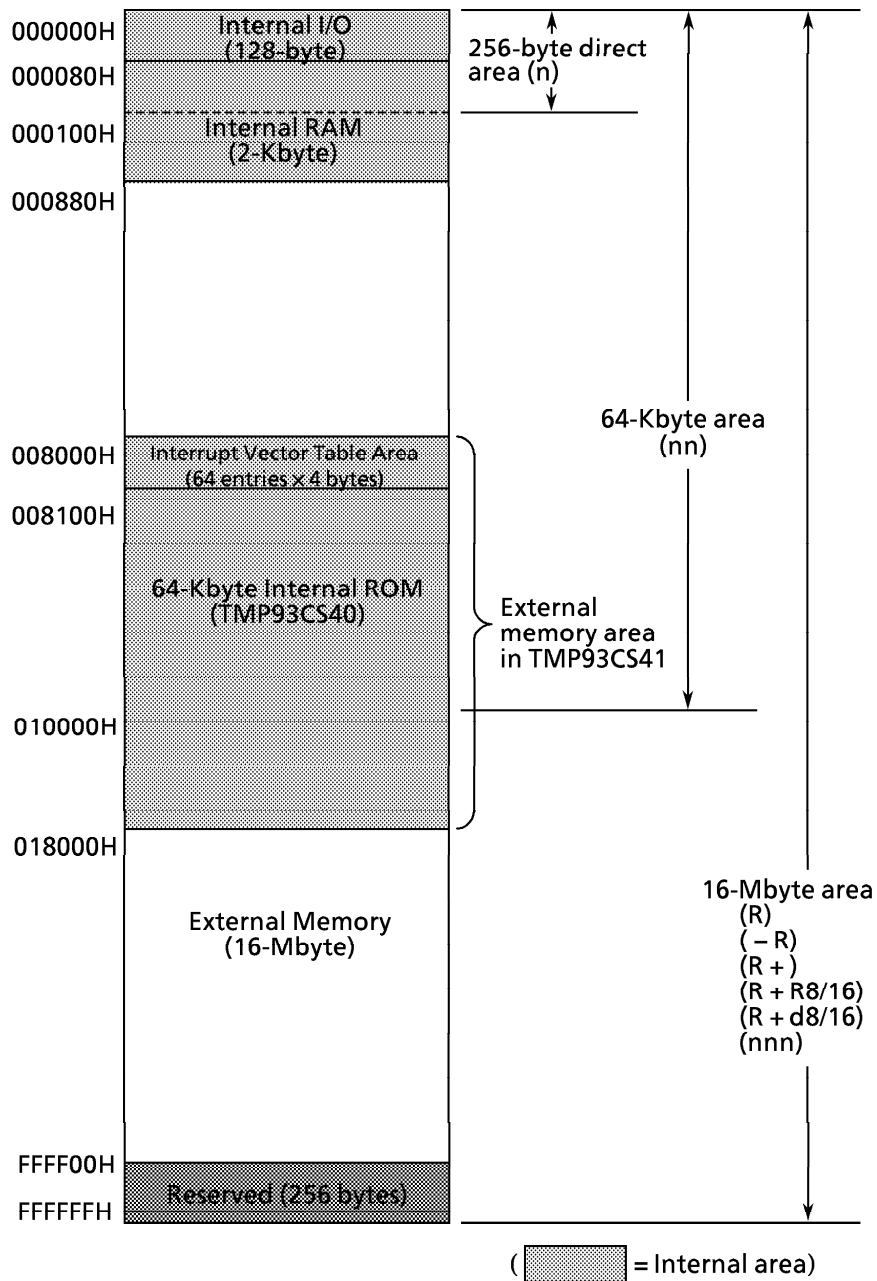
This section describes the functions and basic operation of all blocks of the TMP93CS40/S41 devices.

#### **3.1 CPU**

The TMP93CS40/S41 devices have a built-in high-performance 16-bit CPU (900/L CPU). (For a description of this CPU's operation, see the sub-section TLCS-900/L CPU in the previous section.

### 3.2 Memory Map

Figure 3.2 is a memory map of the TMP93CS40 / S41.



Note: The 256-byte area from FFFF00H to FFFFFFFH cannot be used.

Figure 3.2 Memory Map

## 4. ELECTRICAL CHARACTERISTICS

### 4.1 Absolute Maximum Ratings

(TMP93CS40F, TMP93CS41F)  
(TMP93CS40DF, TMP93CS41DF)

"X" used in an expression shows a frequency for the clock  $f_{PPI}$  selected by  $SYSCR1 < SYSCK >$ . The value of X changes according to whether a clock gear or a low speed oscillator is selected. An example value is calculated for  $f_c$ , with gear = 1/ $f_c$  ( $SYSCR1 < SYSCK$ , GEAR 2 to 0) = 0000).

| Symbol              | Parameter                      | Rating                         | Unit |
|---------------------|--------------------------------|--------------------------------|------|
| V <sub>CC</sub>     | Power Supply Voltage           | − 0.5 to 6.5                   | V    |
| V <sub>IN</sub>     | Input Voltage                  | − 0.5 to V <sub>CC</sub> + 0.5 | V    |
| Σ I <sub>OL</sub>   | Output Current (total)         | 120                            | mA   |
| Σ I <sub>OH</sub>   | Output Current (total)         | − 80                           | mA   |
| P <sub>D</sub>      | Power Dissipation (Ta = 85 °C) | 600                            | mW   |
| T <sub>SOLDER</sub> | Soldering Temperature (10 s)   | 260                            | °C   |
| T <sub>STG</sub>    | Storage Temperature            | − 65 to 150                    | °C   |
| T <sub>OPR</sub>    | Operating Temperature          | − 40 to 85                     | °C   |

### 4.2 DC Characteristics (1/2)

Ta = − 40 to 85 °C

| Symbol           | Parameter                                                                                               |                              | Min.                  | Typ (Note 1) | Max.                                                        | Unit | Condition                                                   |                                                              |
|------------------|---------------------------------------------------------------------------------------------------------|------------------------------|-----------------------|--------------|-------------------------------------------------------------|------|-------------------------------------------------------------|--------------------------------------------------------------|
| V <sub>CC</sub>  | Power Supply Voltage<br>(AV <sub>CC</sub> = V <sub>CC</sub><br>AV <sub>CC</sub> = V <sub>SS</sub> = 0V) |                              | 4.5<br>2.7            |              | 5.5                                                         | V    | fc = 4 to 20 MHz<br>fs = 30 to 34 kHz<br>fc = 4 to 12.5 MHz |                                                              |
| V <sub>IL</sub>  | Input Low Voltage                                                                                       | AD0 to 15                    | −0.3                  |              | 0.8<br>0.6                                                  | V    | V <sub>CC</sub> ≥ 4.5 V<br>V <sub>CC</sub> < 4.5 V          |                                                              |
| V <sub>IL1</sub> |                                                                                                         | Port 2 to A (except P87, P5) |                       |              | 0.3 V <sub>CC</sub>                                         |      | V <sub>CC</sub> = 2.7 to 5.5 V                              |                                                              |
| V <sub>IL2</sub> |                                                                                                         | RESET, NMI, INT0             |                       |              | 0.25 V <sub>CC</sub>                                        |      |                                                             |                                                              |
| V <sub>IL3</sub> |                                                                                                         | EA, AM8/16                   |                       |              | 0.3                                                         |      |                                                             |                                                              |
| V <sub>IL4</sub> |                                                                                                         | X1, P5                       |                       |              | 0.2 V <sub>CC</sub>                                         |      |                                                             |                                                              |
| V <sub>IH</sub>  | Input High Voltage                                                                                      | AD0 to 15                    | 2.2<br>2.0            |              | V <sub>CC</sub> + 0.3                                       |      | V                                                           | V <sub>CC</sub> ≥ 4.5 V<br>V <sub>CC</sub> < 4.5 V           |
| V <sub>IH1</sub> |                                                                                                         | Port 2 to A (except P87)     | 0.7V <sub>CC</sub>    |              |                                                             |      |                                                             | V <sub>CC</sub> = 2.7 to 5.5 V                               |
| V <sub>IH2</sub> |                                                                                                         | RESET, NMI, INT0             | 0.75V <sub>CC</sub>   |              |                                                             |      |                                                             |                                                              |
| V <sub>IH3</sub> |                                                                                                         | EA, AM8/16                   | V <sub>CC</sub> − 0.3 |              |                                                             |      |                                                             |                                                              |
| V <sub>IH4</sub> |                                                                                                         | X1                           | 0.8V <sub>CC</sub>    |              |                                                             |      |                                                             |                                                              |
| V <sub>OL</sub>  | Output Low Voltage                                                                                      |                              |                       |              | 0.45                                                        | V    |                                                             | I <sub>OL</sub> = 1.6 mA<br>(V <sub>CC</sub> = 2.7 to 5.5 V) |
| V <sub>OH1</sub> | Output High Voltage                                                                                     | 2.4                          |                       |              | I <sub>OH</sub> = −400 μA<br>(V <sub>CC</sub> = 3 V ± 10 %) |      |                                                             |                                                              |
| V <sub>OH2</sub> |                                                                                                         | 4.2                          |                       |              | I <sub>OH</sub> = −400 μA<br>(V <sub>CC</sub> = 5 V ± 10 %) |      |                                                             |                                                              |

(Note 1) Typical values are for Ta = 25 °C and V<sub>CC</sub> = 5 V unless otherwise noted.

## 4.2 DC Characteristics (2/2)

| Symbol            | Parameter                                       | Min.      | Typ. (Note 1) | Max.       | Unit       | Condition                                                               |
|-------------------|-------------------------------------------------|-----------|---------------|------------|------------|-------------------------------------------------------------------------|
| I DAR<br>(Note 2) | Darlington Drive Current<br>(8 Output Pins Max) | - 1.0     |               | - 3.5      | mA         | V EXT = 1.5 V<br>R EXT = 1.1 k $\Omega$<br>(when V CC = 5 V $\pm$ 10 %) |
| I LI              | Input Leakage Current                           |           | 0.02          | $\pm$ 5    | $\mu$ A    | 0.0 $\leq$ V IN $\leq$ V CC                                             |
| I LO              | Output Leakage Current                          |           | 0.05          | $\pm$ 10   |            | 0.2 $\leq$ V IN $\leq$ V CC - 0.2                                       |
| V STOP            | Powerdown Voltage<br>(at Stop, RAM Back-up)     | 2.0       |               | 6.0        | V          | V IL2 = 0.2V CC,<br>V IH2 = 0.8V CC                                     |
| R RST             | RESET Pull-up Resistor                          | 50<br>80  |               | 150<br>200 | k $\Omega$ | V CC = 5 V $\pm$ 10 %<br>V CC = 3 V $\pm$ 10 %                          |
| C IO              | Pin Capacitance                                 |           |               | 10         | pF         | f c = 1 MHz                                                             |
| V TH              | Schmitt Width<br>RESET, NMI, INTO               | 0.4       | 1.0           |            | V          |                                                                         |
| RKL               | Programmable<br>Pull-down Resistor              | 10<br>30  |               | 80<br>150  | k $\Omega$ | V CC = 5 V $\pm$ 10 %<br>V CC = 3 V $\pm$ 10 %                          |
| RKH               | Programmable<br>Pull-up Resistor                | 50<br>100 |               | 150<br>300 |            | V CC = 5 V $\pm$ 10 %<br>V CC = 3 V $\pm$ 10 %                          |
| I CC              | Normal (Note 3)                                 |           | 19            | 25         | mA         | V CC = 5 V $\pm$ 10 %<br>f c = 20 MHz                                   |
|                   | Normal2 (Note 4)                                |           | 24            | 30         |            |                                                                         |
|                   | Run                                             |           | 17            | 25         |            |                                                                         |
|                   | Idle2                                           |           | 10            | 15         |            |                                                                         |
|                   | Idle1                                           |           | 3.5           | 5          |            |                                                                         |
|                   | Normal (Note 3)                                 |           | 6.5           | 10         | mA         | V CC = 3 V $\pm$ 10 %<br>f c = 10 MHz<br>(Typ: V CC = 3.0 V)            |
|                   | Normal2 (Note 4)                                |           | 9.5           | 13         |            |                                                                         |
|                   | Run                                             |           | 5.0           | 9          |            |                                                                         |
|                   | Idle2                                           |           | 3.0           | 5          |            |                                                                         |
|                   | Idle1                                           |           | 0.8           | 1.5        |            |                                                                         |
|                   | Slow (Note 3)                                   |           | 20            | 35         | $\mu$ A    | V CC = 3 V $\pm$ 10 %<br>f s = 32.768 kHz<br>(Typ: V CC = 3.0 V)        |
|                   | Run                                             |           | 16            | 30         |            |                                                                         |
|                   | Idle2                                           |           | 10            | 20         |            |                                                                         |
|                   | Idle1                                           |           | 5             | 15         |            |                                                                         |
|                   | Stop                                            |           | 0.2           | 10         |            |                                                                         |

Note 1: Typical values are for Ta = 25 °C and V CC = 5 V unless otherwise noted.

Note 2: I-DAR is guaranteed for up to eight ports.

Note 3: I CC measurement conditions (Normal, Slow):

Only CPU is operational; output pins are open and input pins are fixed.

Note 4: I CC measurement conditions (Normal2):

All functions are operational; output pins are open and input pins are fixed.

## 4.3 AC Characteristics

(1)  $V_{CC} = 5\text{ V} \pm 10\%$ 

| No. | Symbol     | Parameter                                                             | Variable    |              | 16 MHz |     | 20 MHz |     | Unit |
|-----|------------|-----------------------------------------------------------------------|-------------|--------------|--------|-----|--------|-----|------|
|     |            |                                                                       | Min         | Max          | Min    | Max | Min    | Max |      |
| 1   | $t_{OSC}$  | Osc. Period (= x)                                                     | 50          | 31250        | 62.5   |     | 50     |     | ns   |
| 2   | $t_{CLK}$  | CLK Width                                                             | $2x - 40$   |              | 85     |     | 60     |     | ns   |
| 3   | $t_{AK}$   | A0 to A23 Valid $\rightarrow$ CLK Hold                                | $0.5x - 20$ |              | 11     |     | 5      |     | ns   |
| 4   | $t_{KA}$   | CLK Valid $\rightarrow$ A0 to A23 Hold                                | $1.5x - 70$ |              | 24     |     | 5      |     | ns   |
| 5   | $t_{AL}$   | A0 to A15 Valid $\rightarrow$ ALE Fall                                | $0.5x - 15$ |              | 16     |     | 10     |     | ns   |
| 6   | $t_{LA}$   | ALE Fall $\rightarrow$ A0 to A15 Hold                                 | $0.5x - 20$ |              | 11     |     | 5      |     | ns   |
| 7   | $t_{LL}$   | ALE High Width                                                        | $x - 40$    |              | 23     |     | 10     |     | ns   |
| 8   | $t_{LC}$   | ALE Fall $\rightarrow$ RD/WR Fall                                     | $0.5x - 25$ |              | 6      |     | 0      |     | ns   |
| 9   | $t_{CL}$   | RD/WR Rise $\rightarrow$ ALE Rise                                     | $0.5x - 20$ |              | 11     |     | 5      |     | ns   |
| 10  | $t_{ACL}$  | A0 to A15 Valid $\rightarrow$ RD/WR Fall                              | $x - 25$    |              | 38     |     | 25     |     | ns   |
| 11  | $t_{ACH}$  | A0 to A23 Valid $\rightarrow$ RD/WR Fall                              | $1.5x - 50$ |              | 44     |     | 25     |     | ns   |
| 12  | $t_{CA}$   | RD/WR Rise $\rightarrow$ A0 to A23 Hold                               | $0.5x - 25$ |              | 6      |     | 0      |     | ns   |
| 13  | $t_{ADL}$  | A0 to A15 Valid $\rightarrow$ D0 to D15 Input                         |             | $3.0x - 55$  |        | 133 |        | 95  | ns   |
| 14  | $t_{ADH}$  | A0 to A23 Valid $\rightarrow$ D0 to D15 Input                         |             | $3.5x - 65$  |        | 154 |        | 110 | ns   |
| 15  | $t_{RD}$   | RD Fall $\rightarrow$ D0 to D15 Input                                 |             | $2.0x - 60$  |        | 65  |        | 40  | ns   |
| 16  | $t_{RR}$   | RD Low Pulse Width                                                    | $2.0x - 40$ |              | 85     |     | 60     |     | ns   |
| 17  | $t_{HR}$   | RDRise $\rightarrow$ D0 to D15 Hold                                   | 0           |              | 0      |     | 0      |     | ns   |
| 18  | $t_{RAE}$  | RDRise $\rightarrow$ A0 to A15 Output                                 | $x - 15$    |              | 48     |     | 35     |     | ns   |
| 19  | $t_{WW}$   | WR Low Pulse Width                                                    | $2.0x - 40$ |              | 85     |     | 60     |     | ns   |
| 20  | $t_{DW}$   | D0 to D15 Valid $\rightarrow$ WR Rise                                 | $2.0x - 55$ |              | 70     |     | 45     |     | ns   |
| 21  | $t_{WD}$   | WR Rise $\rightarrow$ D0 to D15 Hold                                  | $0.5x - 15$ |              | 16     |     | 10     |     | ns   |
| 22  | $t_{AWH}$  | A0 to A23 Valid $\rightarrow$ WAIT Input <sup>(1 WAIT + n mode)</sup> |             | $3.5x - 90$  |        | 129 |        | 85  | ns   |
| 23  | $t_{AWL}$  | A0 to A15 Valid $\rightarrow$ WAIT Input <sup>(1 WAIT + n mode)</sup> |             | $3.0x - 80$  |        | 108 |        | 70  | ns   |
| 24  | $t_{CW}$   | RD/WR Fall $\rightarrow$ WAIT Hold <sup>(1 WAIT + n mode)</sup>       | $2.0x + 0$  |              | 125    |     | 100    |     | ns   |
| 25  | $t_{APH}$  | A0 to A23 Valid $\rightarrow$ PORT Input                              |             | $2.5x - 120$ |        | 36  |        | 5   | ns   |
| 26  | $t_{APH2}$ | A0 to A23 Valid $\rightarrow$ PORT Hold                               | $2.5x + 50$ |              | 206    |     | 175    |     | ns   |
| 27  | $t_{CP}$   | WR Rise $\rightarrow$ PORT Valid                                      |             | 200          |        | 200 |        | 200 | ns   |
| 28  | $t_{ASRH}$ | A0 to A23 Valid $\rightarrow$ RAS Fall                                | $1.0x - 40$ |              | 23     |     | 10     |     | ns   |
| 29  | $t_{ASRL}$ | A0 to A15 Valid $\rightarrow$ RAS Fall                                | $0.5x - 15$ |              | 16     |     | 10     |     | ns   |
| 30  | $t_{RAC}$  | RAS Fall $\rightarrow$ D0 to D15 Input                                |             | $2.5x - 70$  |        | 86  |        | 55  | ns   |
| 31  | $t_{RAH}$  | RAS Fall $\rightarrow$ A0 to A15 Hold                                 | $0.5x - 15$ |              | 16     |     | 10     |     | ns   |
| 32  | $t_{RAS}$  | RAS Low Pulse Width                                                   | $2.0x - 40$ |              | 85     |     | 60     |     | ns   |
| 33  | $t_{RP}$   | RAS High Pulse Width                                                  | $2.0x - 40$ |              | 85     |     | 60     |     | ns   |
| 34  | $t_{RSH}$  | CAS Fall $\rightarrow$ RAS Rise                                       | $1.0x - 40$ |              | 23     |     | 10     |     | ns   |
| 35  | $t_{RSC}$  | RAS Rise $\rightarrow$ CAS Rise                                       | $0.5x - 25$ |              | 6      |     | 0      |     | ns   |
| 36  | $t_{RCD}$  | RAS Fall $\rightarrow$ CAS Fall                                       | $1.0x - 40$ |              | 23     |     | 10     |     | ns   |
| 37  | $t_{CAC}$  | CAS Fall $\rightarrow$ D0 to D15 Input                                |             | $1.5x - 65$  |        | 29  |        | 10  | ns   |
| 38  | $t_{CAS}$  | CAS Low Pulse Width                                                   | $1.5x - 30$ |              | 64     |     | 40     |     | ns   |
|     |            |                                                                       |             |              |        |     |        |     |      |
|     |            |                                                                       |             |              |        |     |        |     |      |

## AC Measuring Conditions

- Output Level : High 2.2 V / Low 0.8 V , CL = 50 pF  
(However, CL = 100 pF for AD0 to AD15, A0 to A23, ALE, RD, WR, HWR, R/W, CLK, RAS, CAS0 to CAS2)
- Input Level : High 2.4 V / Low 0.45 V (AD0 to AD15)  
High 0.8 V<sub>CC</sub> / Low 0.2 V<sub>CC</sub> (except for AD0 to AD15)

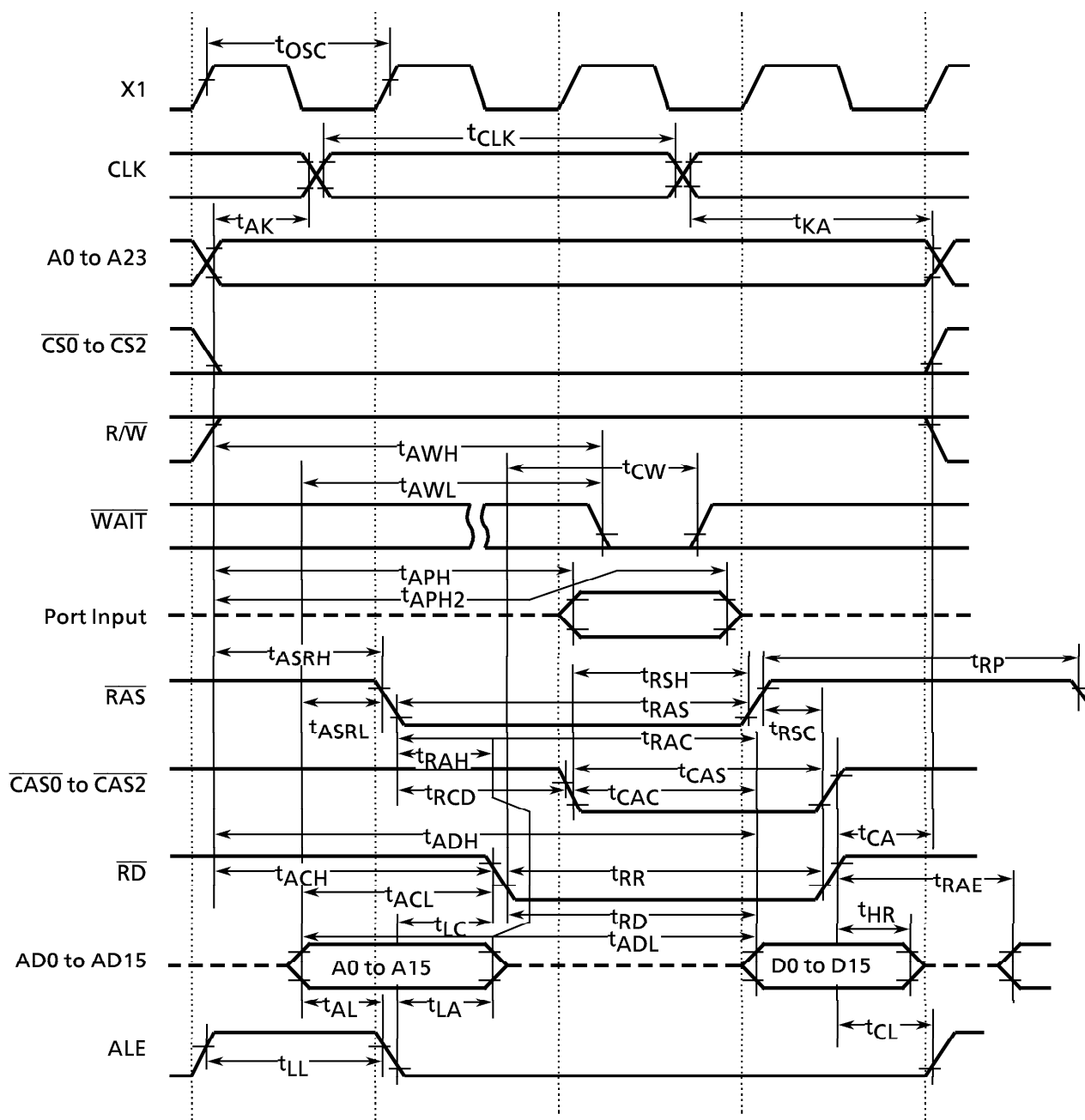
(2)  $V_{CC} = 3\text{ V} \pm 10\%$ 

| No. | Symbol     | Parameter                                                                                            | Variable     |              | 12.5 MHz |     | Unit |
|-----|------------|------------------------------------------------------------------------------------------------------|--------------|--------------|----------|-----|------|
|     |            |                                                                                                      | Min          | Max          | Min      | Max |      |
| 1   | $t_{OSC}$  | Osc. Period (= x)                                                                                    | 80           | 31250        | 80       |     | ns   |
| 2   | $t_{CLK}$  | CLK Width                                                                                            | $2x - 40$    |              | 120      |     | ns   |
| 3   | $t_{AK}$   | A0 to A23 Valid $\rightarrow$ CLK Hold                                                               | $0.5x - 30$  |              | 10       |     | ns   |
| 4   | $t_{KA}$   | CLK Valid $\rightarrow$ A0 to A23 Hold                                                               | $1.5x - 80$  |              | 40       |     | ns   |
| 5   | $t_{AL}$   | A0 to A15 Valid $\rightarrow$ ALE Fall                                                               | $0.5x - 35$  |              | 5        |     | ns   |
| 6   | $t_{LA}$   | ALE Fall $\rightarrow$ A0 to A15 Hold                                                                | $0.5x - 35$  |              | 5        |     | ns   |
| 7   | $t_{LL}$   | ALE High Width                                                                                       | $x - 60$     |              | 20       |     | ns   |
| 8   | $t_{LC}$   | ALE Fall $\rightarrow$ $\overline{RD}/\overline{WR}$ Fall                                            | $0.5x - 35$  |              | 5        |     | ns   |
| 9   | $t_{CL}$   | $\overline{RD}/\overline{WR}$ Rise $\rightarrow$ ALE Rise                                            | $0.5x - 40$  |              | 0        |     | ns   |
| 10  | $t_{ACL}$  | A0 to A15 Valid $\rightarrow$ $\overline{RD}/\overline{WR}$ Fall                                     | $x - 50$     |              | 30       |     | ns   |
| 11  | $t_{ACH}$  | A0 to A23 Valid $\rightarrow$ $\overline{RD}/\overline{WR}$ Fall                                     | $1.5x - 50$  |              | 70       |     | ns   |
| 12  | $t_{CA}$   | $\overline{RD}/\overline{WR}$ Rise $\rightarrow$ A0 to A23 Hold                                      | $0.5x - 40$  |              | 0        |     | ns   |
| 13  | $t_{ADL}$  | A0 to A15 Valid $\rightarrow$ D0 to D15 Input                                                        |              | $3.0x - 110$ |          | 130 | ns   |
| 14  | $t_{ADH}$  | A0 to A23 Valid $\rightarrow$ D0 to D15 Input                                                        |              | $3.5x - 125$ |          | 155 | ns   |
| 15  | $t_{RD}$   | $\overline{RD}$ Fall $\rightarrow$ D0 to D15 Input                                                   |              | $2.0x - 115$ |          | 45  | ns   |
| 16  | $t_{RR}$   | $\overline{RD}$ Low Pulse Width                                                                      | $2.0x - 40$  |              | 120      |     | ns   |
| 17  | $t_{HR}$   | $\overline{RD}$ Rise $\rightarrow$ D0 to D15 Hold                                                    | 0            |              | 0        |     | ns   |
| 18  | $t_{RAE}$  | $\overline{RD}$ Rise $\rightarrow$ A0 to A15 Output                                                  | $x - 25$     |              | 55       |     | ns   |
| 19  | $t_{WW}$   | $\overline{WR}$ Low Pulse Width                                                                      | $2.0x - 40$  |              | 120      |     | ns   |
| 20  | $t_{DW}$   | D0 to D15 Valid $\rightarrow$ $\overline{WR}$ Rise                                                   | $2.0x - 120$ |              | 40       |     | ns   |
| 21  | $t_{WD}$   | $\overline{WR}$ Rise $\rightarrow$ D0 to D15 Hold                                                    | $0.5x - 40$  |              | 0        |     | ns   |
| 22  | $t_{AWH}$  | A0 to A23 Valid $\rightarrow$ $\overline{WAIT}$ Input <sup>(1 WAIT + n mode)</sup>                   |              | $3.5x - 130$ |          | 150 | ns   |
| 23  | $t_{AWL}$  | A0 to A15 Valid $\rightarrow$ $\overline{WAIT}$ Input <sup>(1 WAIT + n mode)</sup>                   |              | $3.0x - 100$ |          | 140 | ns   |
| 24  | $t_{CW}$   | $\overline{RD}/\overline{WR}$ Fall $\rightarrow$ $\overline{WAIT}$ Hold <sup>(1 WAIT + n mode)</sup> | $2.0x + 0$   |              | 160      |     | ns   |
| 25  | $t_{APH}$  | A0 to A23 Valid $\rightarrow$ PORT Input                                                             |              | $2.5x - 120$ |          | 80  | ns   |
| 26  | $t_{APH2}$ | A0 to A23 Valid $\rightarrow$ PORT Hold                                                              | $2.5x + 50$  |              | 250      |     | ns   |
| 27  | $t_{CP}$   | $\overline{WR}$ Rise $\rightarrow$ PORT Valid                                                        |              | 200          |          | 200 | ns   |
| 28  | $t_{ASRH}$ | A0 to A23 Valid $\rightarrow$ $\overline{RAS}$ Fall                                                  | $1.0x - 60$  |              | 20       |     | ns   |
| 29  | $t_{ASRL}$ | A0 to A15 Valid $\rightarrow$ $\overline{RAS}$ Fall                                                  | $0.5x - 40$  |              | 0        |     | ns   |
| 30  | $t_{RAC}$  | $\overline{RAS}$ Fall $\rightarrow$ D0 to D15 Input                                                  |              | $2.5x - 90$  |          | 110 | ns   |
| 31  | $t_{RAH}$  | $\overline{RAS}$ Fall $\rightarrow$ A0 to A15 Hold                                                   | $0.5x - 25$  |              | 15       |     | ns   |
| 32  | $t_{RAS}$  | $\overline{RAS}$ Low Pulse Width                                                                     | $2.0x - 40$  |              | 120      |     | ns   |
| 33  | $t_{RP}$   | $\overline{RAS}$ High Pulse Width                                                                    | $2.0x - 40$  |              | 120      |     | ns   |
| 34  | $t_{RSH}$  | $\overline{CAS}$ Fall $\rightarrow$ $\overline{RAS}$ Rise                                            | $1.0x - 55$  |              | 25       |     | ns   |
| 35  | $t_{RSC}$  | $\overline{RAS}$ Rise $\rightarrow$ $\overline{CAS}$ Rise                                            | $0.5x - 25$  |              | 15       |     | ns   |
| 36  | $t_{RCD}$  | $\overline{RAS}$ Fall $\rightarrow$ $\overline{CAS}$ Fall                                            | $1.0x - 40$  |              | 40       |     | ns   |
| 37  | $t_{CAC}$  | $\overline{CAS}$ Fall $\rightarrow$ D0 to D15 Input                                                  |              | $1.5x - 120$ |          | 0   | ns   |
| 38  | $t_{CAS}$  | $\overline{CAS}$ Low Pulse Width                                                                     | $1.5x - 30$  |              | 80       |     | ns   |
|     |            |                                                                                                      |              |              |          |     |      |
|     |            |                                                                                                      |              |              |          |     |      |
|     |            |                                                                                                      |              |              |          |     |      |
|     |            |                                                                                                      |              |              |          |     |      |
|     |            |                                                                                                      |              |              |          |     |      |

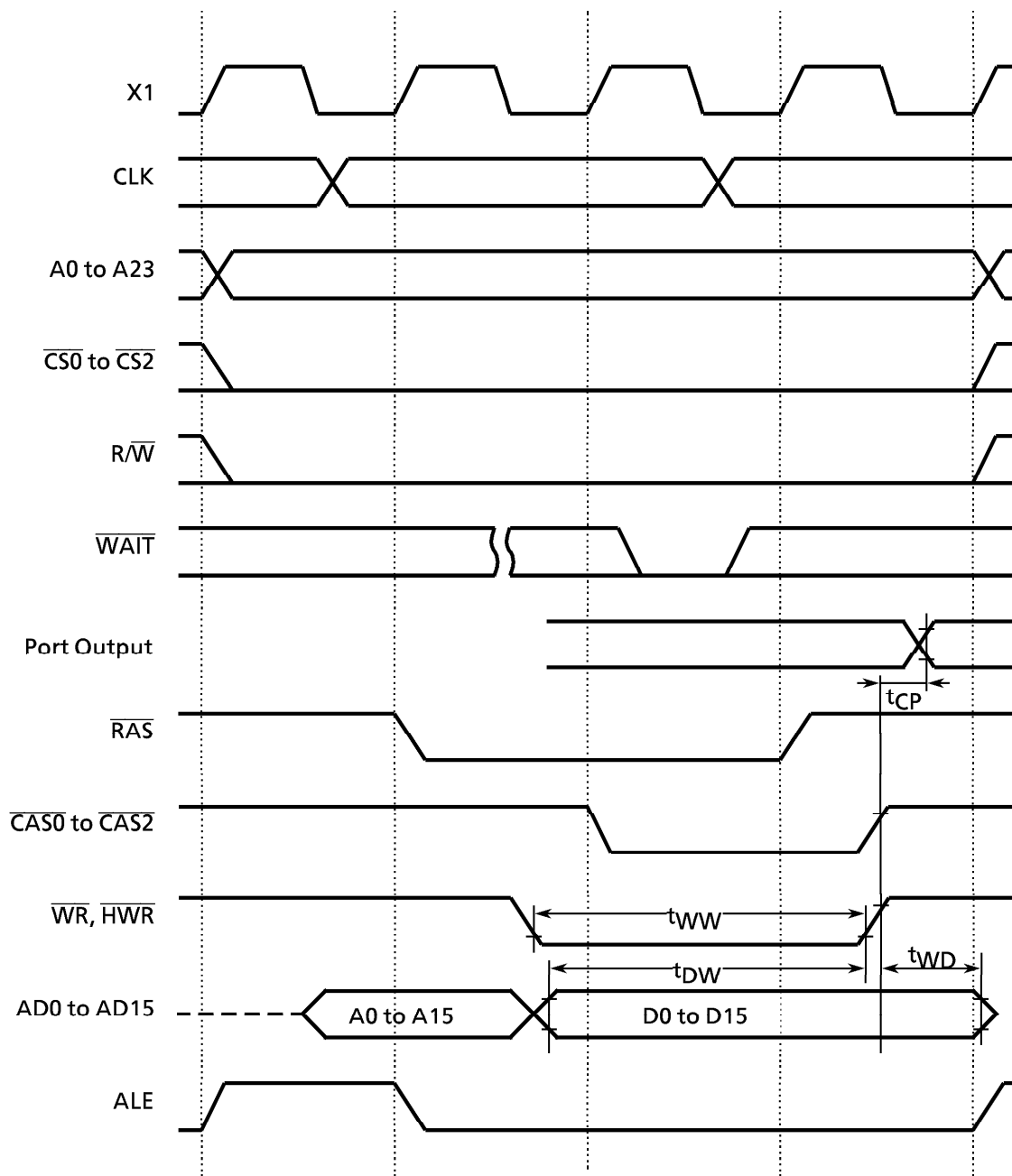
## AC Measuring Conditions

- Output Level: High  $0.7 \times V_{CC}$  / Low  $0.3 \times V_{CC}$ , CL = 50 pF
- Input Level: High  $0.9 \times V_{CC}$  / Low  $0.1 \times V_{CC}$

## (1) Read Cycle



## (2) Write Cycle



## 4.4 A/D Conversion Characteristics

AVCC = VCC, AVSS = VSS

| Symbol                                        | Parameter                                                   | Power Supply                  | Min                    | Typ             | Max                    | Unit |
|-----------------------------------------------|-------------------------------------------------------------|-------------------------------|------------------------|-----------------|------------------------|------|
| V <sub>REFH</sub>                             | Analog Reference Voltage ( + )                              | V <sub>CC</sub> = 5V ± 10 %   | V <sub>CC</sub> – 1.5V | V <sub>CC</sub> | V <sub>CC</sub>        | V    |
|                                               |                                                             | V <sub>CC</sub> = 3V ± 10 %   | V <sub>CC</sub> – 0.2V | V <sub>CC</sub> | V <sub>CC</sub>        |      |
| V <sub>REFL</sub>                             | Analog Reference Voltage ( – )                              | V <sub>CC</sub> = 5V ± 10 %   | V <sub>SS</sub>        | V <sub>SS</sub> | V <sub>SS</sub> + 0.2V |      |
|                                               |                                                             | V <sub>CC</sub> = 3V ± 10 %   | V <sub>SS</sub>        | V <sub>SS</sub> | V <sub>SS</sub> + 0.2V |      |
| V <sub>AIN</sub>                              | Analog Input Voltage Range                                  |                               | V <sub>REFL</sub>      |                 | V <sub>REFH</sub>      |      |
| I <sub>REF</sub><br>(V <sub>REFL</sub> = 0 V) | Analog Current for Analog Reference Voltage<br><VREFON> = 1 | V <sub>CC</sub> = 5V ± 10 %   |                        | 0.5             | 1.5                    | mA   |
|                                               |                                                             | V <sub>CC</sub> = 3V ± 10 %   |                        | 0.3             | 0.9                    |      |
|                                               | <VREFON> = 0                                                | V <sub>CC</sub> = 2.7 to 5.5V |                        | 0.02            | 5.0                    | μA   |
| –                                             | Error (not including quantizing errors)                     | V <sub>CC</sub> = 5V ± 10 %   |                        | ± 1.0           | ± 3.0                  | LSB  |
|                                               |                                                             | V <sub>CC</sub> = 3V ± 10 %   |                        | ± 1.0           | ± 3.0                  |      |

Note 1 : 1LSB = (V<sub>REFH</sub> – V<sub>REFL</sub>) / 2<sup>10</sup> [V]Note 2 : The operation of this A/D converter is guaranteed only using f<sub>c</sub> (the high-frequency oscillator). It is not guaranteed for f<sub>s</sub>.The operation above is guaranteed for f<sub>FPH</sub> ≥ 4 MHz.Note 3 : The value I<sub>CC</sub> includes the current which flows through the AV<sub>CC</sub> pin.

## 4.5 Serial Channel Timing

## (1) I/O Interface Mode

## ① SCLK Input Mode

| Symbol           | Parameter                                                | Variable                       |                             | 32.768 MHz (Note) |        | 12.5 MHz |     | 20 MHz |     | Unit |
|------------------|----------------------------------------------------------|--------------------------------|-----------------------------|-------------------|--------|----------|-----|--------|-----|------|
|                  |                                                          | Min                            | Max                         | Min               | Max    | Min      | Max | Min    | Max |      |
| t <sub>SCY</sub> | SCLK Cycle                                               | 16X                            |                             | 488 μs            |        | 1.28     |     | 0.8    |     | μs   |
| t <sub>OSS</sub> | Output Data → Rising Edge or Falling Edge* of SCLK       | t <sub>SCY</sub> / 2 – 5X – 50 |                             | 91.5 μs           |        | 190      |     | 100    |     | ns   |
| t <sub>OHS</sub> | SCLK Rising Edge or Falling Edge* → Output Data Hold     | 5X – 100                       |                             | 152 μs            |        | 300      |     | 150    |     | ns   |
| t <sub>HSR</sub> | SCLK Rising Edge or Falling Edge* → Input Data Hold      | 0                              |                             | 0                 |        | 0        |     | 0      |     | ns   |
| t <sub>SRD</sub> | SCLK Rising Edge or Falling Edge* → Effective Data Input |                                | t <sub>SCY</sub> – 5X – 100 |                   | 336 μs |          | 780 |        | 450 | ns   |

Note: System clock is f<sub>s</sub>, or input clock to prescaler is divisor clock of f<sub>s</sub>.

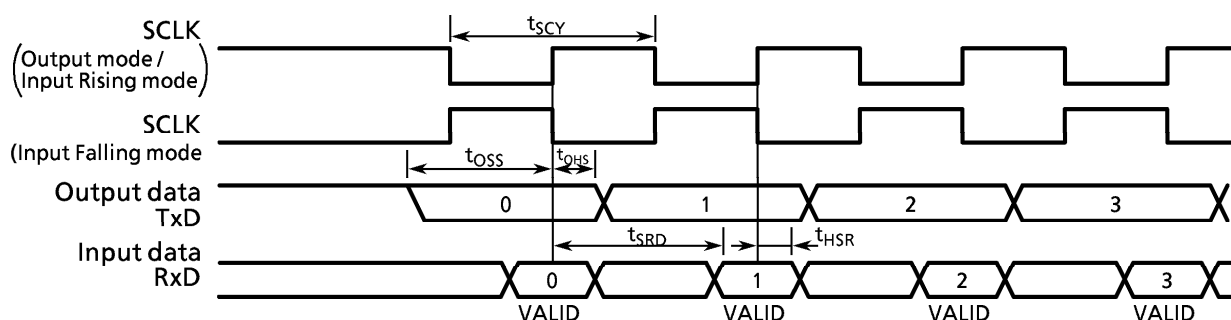
\* The rising edge is used in SCLK Rising mode.

The falling edge is used SCLK Falling mode.

## ② SCLK Output Mode

| Symbol           | Parameter                               | Variable                    |                             | 32.768 MHz (Note) |        | 12.5 MHz |        | 20 MHz |       | Unit |
|------------------|-----------------------------------------|-----------------------------|-----------------------------|-------------------|--------|----------|--------|--------|-------|------|
|                  |                                         | Min                         | Max                         | Min               | Max    | Min      | Max    | Min    | Max   |      |
| t <sub>SCY</sub> | SCLK Cycle (Programmable)               | 16X                         | 8192X                       | 488 μs            | 250 ms | 1.28     | 655.36 | 0.8    | 409.6 | μs   |
| t <sub>OSS</sub> | Output Data → SCLK Rising Edge          | t <sub>SCY</sub> – 2X – 150 |                             | 427 μs            |        | 970      |        | 550    |       | ns   |
| t <sub>OHS</sub> | SCLK Rising Edge → Output Data Hold     | 2X – 80                     |                             | 60 μs             |        | 80       |        | 20     |       | ns   |
| t <sub>HSR</sub> | SCLK Rising Edge → Input Data Hold      | 0                           |                             | 0                 |        | 0        |        | 0      |       | ns   |
| t <sub>SRD</sub> | SCLK Rising Edge → Effective Data Input |                             | t <sub>SCY</sub> – 2X – 150 |                   | 428 μs |          | 970    |        | 550   | ns   |

Note: System clock is f<sub>s</sub>, or input clock to prescaler is divisor clock of f<sub>s</sub>.



#### 4.6 Timer/Counter Input Clock (TI0, TI4, TI5, TI6, TI7)

| Symbol     | Parameter                    | Variable   |     | 12.5 MHz |     | 20 MHz |     | Unit |
|------------|------------------------------|------------|-----|----------|-----|--------|-----|------|
|            |                              | Min        | Max | Min      | Max | Min    | Max |      |
| $t_{VCK}$  | Clock Cycle                  | $8X + 100$ |     | 740      |     | 500    |     | ns   |
| $t_{VCKL}$ | Low Level Clock Pulse Width  | $4X + 40$  |     | 360      |     | 240    |     | ns   |
| $t_{VCKH}$ | High Level Clock Pulse Width | $4X + 40$  |     | 360      |     | 240    |     | ns   |

#### 4.7 Interrupt and Capture

##### (1) $\overline{NMI}$ , INT0 interrupts

| Symbol      | Parameter                                      | Variable |     | 12.5 MHz |     | 20 MHz |     | Unit |
|-------------|------------------------------------------------|----------|-----|----------|-----|--------|-----|------|
|             |                                                | Min      | Max | Min      | Max | Min    | Max |      |
| $t_{INTAL}$ | $\overline{NMI}$ , INT0 Low Level Pulse Width  | $4X$     |     | 320      |     | 200    |     | ns   |
| $t_{INTAH}$ | $\overline{NMI}$ , INT0 High Level Pulse Width | $4X$     |     | 320      |     | 200    |     | ns   |

##### (2) INT4 to 7 interrupts, capture

The INT4 to 7 input pulse width depends on the CPU operation clock and timer (9-bit prescaler). The following shows the pulse width for each clock.

| System clock selected<br><SYSCK> | Prescaler clock selected<br><PRCK1 to 0> | $t_{INTBL}$ (INT4 to 7 low level pulse width) |        | $t_{INTBH}$ (INT4 to 7 high level pulse width) |        | Unit    |
|----------------------------------|------------------------------------------|-----------------------------------------------|--------|------------------------------------------------|--------|---------|
|                                  |                                          | Variable                                      | 20 MHz | Variable                                       | 20 MHz |         |
|                                  |                                          | Min                                           | Min    | Min                                            | Min    |         |
| 0 (fc)                           | 00 ( $f_{FPH}$ )                         | $8X + 100$                                    | 500    | $8X + 100$                                     | 500    | ns      |
|                                  | 01 (fs)                                  | $8XT + 0.1$                                   | 244.3  | $8XT + 0.1$                                    | 244.3  |         |
|                                  | 10 (fc/16)                               | $128X + 0.1$                                  | 6.5    | $128X + 0.1$                                   | 6.5    |         |
| 1 (fs)<br>(Note 2)               | 00 ( $f_{FPH}$ )                         | $8XT + 0.1$                                   | 244.3  | $8XT + 0.1$                                    | 244.3  | $\mu s$ |
|                                  | 01 (fs)                                  |                                               |        |                                                |        |         |

Note 1: XT represents the frequency of the low frequency clock fs. Calculated at fs = 32,768 kHz.

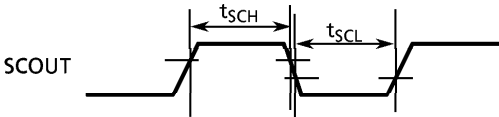
Note 2: When using fs as the system clock, fc/16 cannot be selected as the prescaler clock.

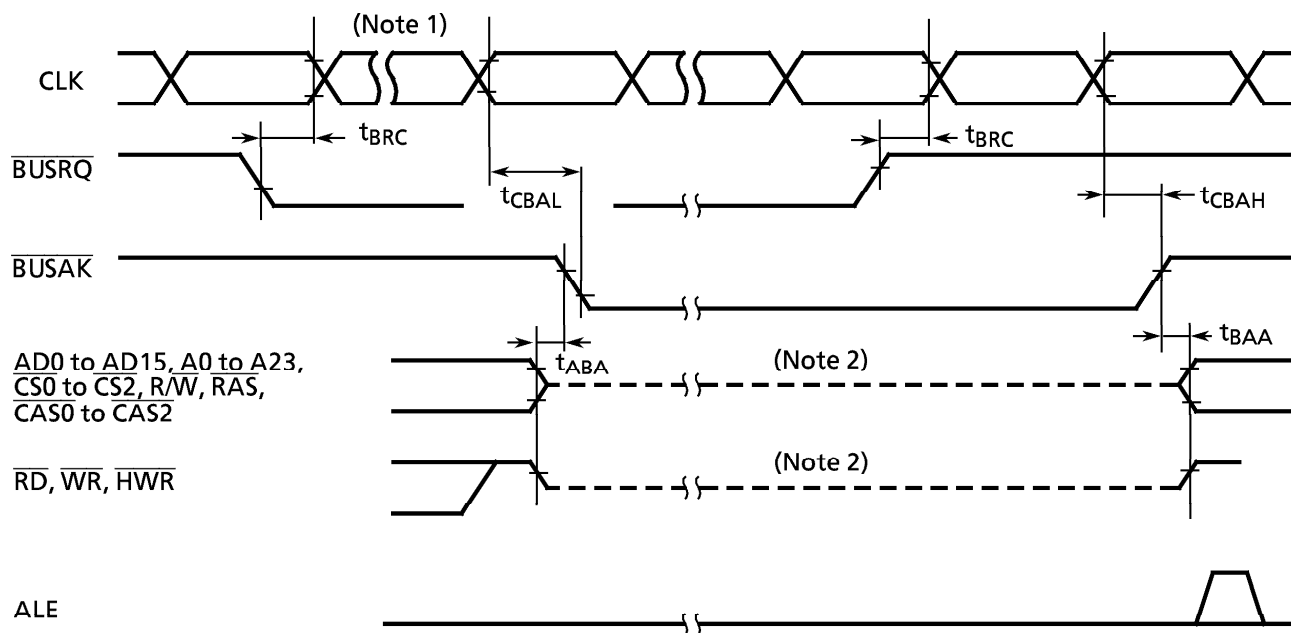
4.8 SCOUT pin AC characteristics

| Symbol           | Parameter                                              | Variable  |     | 10 MHz |     | 20 MHz |     | Unit |
|------------------|--------------------------------------------------------|-----------|-----|--------|-----|--------|-----|------|
|                  |                                                        | Min       | Max | Min    | Max | Min    | Max |      |
| t <sub>SCH</sub> | High-Level Pulse Width<br>V <sub>CC</sub> = 5 V ± 10 % | 0.5X – 10 |     | 30     |     | 15     |     | ns   |
|                  | High-Level Pulse Width<br>V <sub>CC</sub> = 3 V ± 10 % | 0.5X – 20 |     | 20     |     | –      | –   |      |
| t <sub>SCL</sub> | Low-Level Pulse Width<br>V <sub>CC</sub> = 5 V ± 10 %  | 0.5X – 10 |     | 30     |     | 15     |     | ns   |
|                  | Low-Level Pulse Width<br>V <sub>CC</sub> = 3 V ± 10 %  | 0.5X – 20 |     | 20     |     | –      | –   |      |

Measurement condition

- Output level: High 2.2 V / Low 0.8 V, CL = 10 pF



4.9 Timing Chart for Bus Request ( $\overline{\text{BUSRQ}}$ ) / Bus Acknowledge ( $\overline{\text{BUSAK}}$ )

| Symbol            | Parameter                                                | Variable |              | 12.5 MHz |     | 20 MHz |     | Unit |
|-------------------|----------------------------------------------------------|----------|--------------|----------|-----|--------|-----|------|
|                   |                                                          | Min      | Max          | Min      | Max | Min    | Max |      |
| $t_{\text{BRC}}$  | $\overline{\text{BUSRQ}}$ Set-up Time to CLK             | 120      |              | 120      |     | 120    |     | ns   |
| $t_{\text{CBAL}}$ | CLK $\rightarrow$ $\overline{\text{BUSAK}}$ Falling Edge |          | $1.5X + 120$ |          | 240 |        | 195 | ns   |
| $t_{\text{CBAH}}$ | CLK $\rightarrow$ $\overline{\text{BUSAK}}$ Rising Edge  |          | $0.5X + 40$  |          | 80  |        | 65  | ns   |
| $t_{\text{ABA}}$  | Output Buffer off to $\overline{\text{BUSAK}}$           | 0        | 80           | 0        | 80  | 0      | 80  | ns   |
| $t_{\text{BAA}}$  | $\overline{\text{BUSAK}}$ to Output Buffer on            | 0        | 80           | 0        | 80  | 0      | 80  | ns   |

Note 1: Even if the  $\overline{\text{BUSRQ}}$  signal goes low, the bus will not be released while the  $\overline{\text{WAIT}}$  signal is low. The bus will only be released when  $\overline{\text{BUSRQ}}$  goes low while  $\overline{\text{WAIT}}$  is high.

Note 2: This line shows only that the output buffer is in the off state.

It does not indicate that the signal level is fixed.

Just after the bus is released, the signal level set before the bus was released is maintained dynamically by the external capacitance. Therefore, to fix the signal level using an external resistor during bus release, careful design is necessary, as fixing of the level is delayed.

The internal programmable pull-up/pull-down resistor is switched between the active and non-active states by the internal signal.

#### 4.10 Recommended oscillator

The TMP93CM40/M41 are evaluated with various resonators. The evaluation results are displayed below to enable appropriate selection for any given application.

Note : The load capacitance of the resonator consists of the load capacitors C1 and C2 which are to be connected and the floating capacitance of the target board.

Even if the specified values of C1 and C2 are used, there is a possibility that the oscillator will malfunction due to varying load capacitance on the target boards. Hence the oscillator's wiring patterns on the board should be designed to be as short as possible.

It is recommended that evaluation of the resonators be conducted on the target board.

##### (1) Examples of Resonator Connection

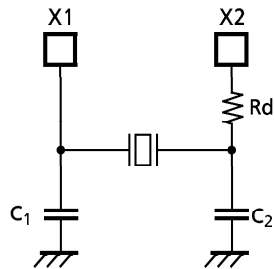


Figure 1: Example of High Frequency Resonator Connection

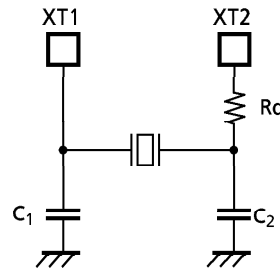


Figure 2: Example of Low Frequency Resonator Connection

## (2) Ceramic resonator: Toyama Murata Mfg. Co., Ltd (Note 1)

Ta = -20 to 80°C

| Parameter                  | Frequency (MHz) | Recommended resonator | Recommended value   |                     |         | Vcc [V]    |
|----------------------------|-----------------|-----------------------|---------------------|---------------------|---------|------------|
|                            |                 |                       | C <sub>1</sub> [pF] | C <sub>2</sub> [pF] | Rd [kΩ] |            |
| High-frequency oscillation | 4.00            | CSA4.00MG             | 30                  | 30                  | 0       | 2.7 to 5.5 |
|                            |                 | CST4.00MGW            | (30) (Note 2)       | (30) (Note 2)       |         |            |
|                            | 10.00           | CSA10.0MTZ093         | 30                  | 30                  |         |            |
|                            |                 | CST10.0MTW093         | (30) (Note 2)       | (30) (Note 2)       |         |            |
|                            | 12.50           | CSA12.5MTZ093         | 30                  | 30                  |         |            |
|                            |                 | CST12.5MTW093         | (30) (Note 2)       | (30) (Note 2)       |         |            |
|                            | 16.00           | CSA16.00MXZ040        | 5                   | 5                   |         | 4.5 to 5.5 |
|                            |                 | CST16.00MXW0C1        | (5) (Note 2)        | (5) (Note 2)        |         |            |
|                            | 20.00           | CSA20.00MXZ040        | 3                   | 3                   |         |            |

Note 1 : TOYAMA MURATA MFG. CO., LTD. (JAPAN)

Product Engineering Service Section

Phone : 0764-29-1221, Fax : 0764-29-4962

Note 2 : For built-in condenser type

## (3) Crystal resonator: Nihon Denpa Kogyo (Note 1)

Ta = -10 to 60 °C

| Parameter                  | Frequency (MHz) | Recommended resonator | Recommended value   |                     |         | Vcc [V]    |
|----------------------------|-----------------|-----------------------|---------------------|---------------------|---------|------------|
|                            |                 |                       | C <sub>1</sub> [pF] | C <sub>2</sub> [pF] | Rd [kΩ] |            |
| High-frequency oscillation | 4.00            | NT040016A             | 12                  | 12                  | 0       | 2.7 to 5.5 |
|                            | 10.00           | NT100016A             | 10                  | 10                  |         |            |
|                            | 12.50           | NT125016A             | 10                  | 10                  |         |            |
|                            | 16.00           | NT160016A             | 10                  | 10                  |         | 4.5 to 5.5 |
|                            | 20.00           | NT200016A             | 7                   | 7                   |         |            |
| Low-frequency oscillation  | 32.768 kHz      | NT0003125A            | 15                  | 15                  | 470     | 2.7 to 5.5 |

Note 1 : NDK AMERICA, INC. : U.S.A

NDK ELECTRONICS SINGAPORE PTE, LTD.

NDK ELECTRONICS (HK) LIMITED: HONG KONG

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Note 2 : High-frequency resonator

NR-18 : Lead mount type

AT-51 : Lead mount type

CP12A : Surface mount type

Note 3 : Low-frequency resonator

MX-38T : Lead mount type