TMPR3904AF
(32 bit TX System RISC)

1. GENERAL DESCRIPTION

The TMPR3904AF (to be called "TX3904A" hereinafter) is a standard micro controller of the 32-bit RISC Microprocessor TX39 family. The TX3904A uses the TX39 Processor Core as the CPU. The TX39 Processor Core is a RISC CPU core Toshiba developed based on the R3000A architecture of MIPS Technologies, Inc. As micro-controllers that can be embedded, besides the TX39 Processor Core, the TX3904A has built-in peripheral circuits such as memory controllers, DMA controllers, serial ports, and timers/counters.

2. FEATURES

- Built-in TX39 Processor Core
  - Toshiba has uniquely developed this on the basis of the R3000A architecture of the MIPS.
  - Instruction cache 4KB/Data cache 1KB
  - Built-in debug support unit
- DRAM Controller
  - Four-bank x two-channel configuration
  - Fast page mode/Hyper page (EDO) mode support
- ROM Controller
  - Two-bank x two-channel configuration
  - Mask ROM, EPROM, E^2PROM, Flash Memory, SRAM support
  - Page mode ROM support
- DMA Controller
  - Independent four channels
  - Single address mode/Dual address mode
- Interrupt Controller
  - Internal nine sources, external eight sources
  - Non-maskable interrupt (NMI)

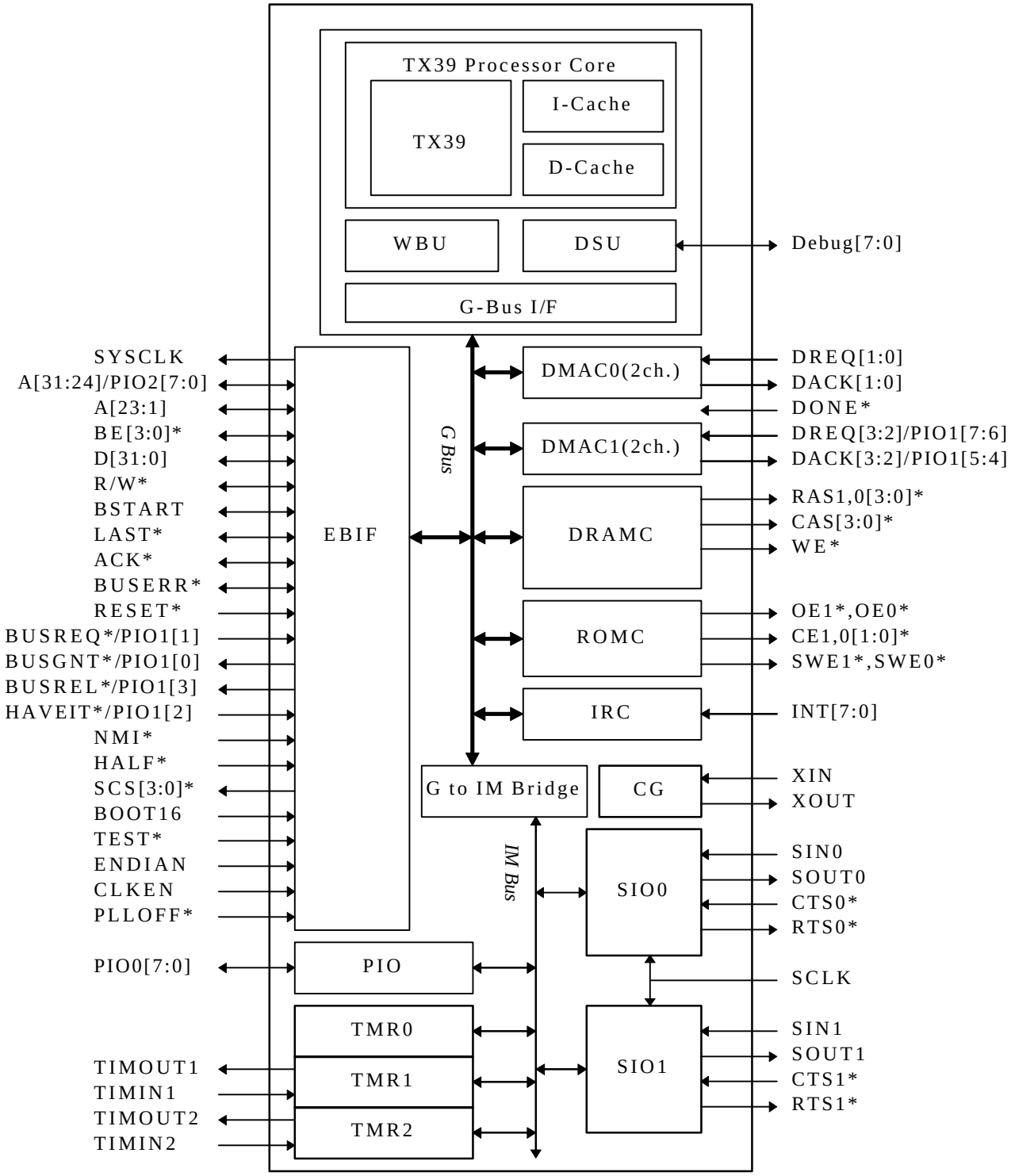
- Timer/Counter
  - 24-bit up counter three channels
  - Watchdog timer mode support
- Serial I/O
  - Two-channel UART
- I/O Ports
  - Exclusive port: one channel; shared port: two channels
  - 16-bit Bus Support

- Power Supply Voltage: 3.3V
- Power Consumption: 900mW (3.3V, at 66 MHz operation, Typ)
- Maximum Operation Frequency: 66 MHz
- Package: 208 pin plastic QFP

R3000A is a trademark of MIPS Group, a division of Silicon Graphics, Inc.

3. SYSTEM CONFIGURATION

3.1 TMPR3904AF BLOCK DIAGRAM



4. PINS

4.1 PIN ASSIGNMENT

Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
1	XIN	29	VSS	57	A[19]	85	TSTO2
2	VDD	30	TOUT[2]	58	A[20]	86	BOOT16
3	LAST*	31	TOUT[3]	59	A[21]	87	HALF*
4	R/W*	32	WE*	60	VSS	88	ENDIAN
5	BE[3]*	33	A[1]	61	VDD	89	BUSGNT*
6	BE[2]*	34	VDD	62	A[22]	90	BUSREL*
7	BE[1]*	35	A[2]	63	A[23]	91	DACK[0]
8	BE[0]*	36	A[3]	64	A[24]	92	DACK[1]
9	VSS	37	A[4]	65	A[25]	93	DACK[2]
10	VDD	38	VSS	66	A[26]	94	DACK[3]
11	RAS0[0]*	39	A[5]	67	A[27]	95	DONE*
12	RAS0[1]*	40	A[6]	68	VSS	96	VSS
13	RAS0[2]*	41	A[7]	69	VDD	97	VDD
14	VDD	42	A[8]	70	A[28]	98	DREQ[0]
15	VSS	43	VDD	71	A[29]	99	DREQ[1]
16	RAS0[3]*	44	VSS	72	A[30]	100	DREQ[2]
17	RAS1[0]*	45	A[9]	73	A[31]	101	DREQ[3]
18	RAS1[1]*	46	A[10]	74	CE0[0]*	102	HAVEIT*
19	VSS	47	A[11]	75	CE0[1]*	103	BUSREQ*
20	RAS1[2]*	48	A[12]	76	CE1[0]*	104	VDD
21	RAS1[3]*	49	A[13]	77	CE1[1]*	105	SCS[3]*
22	CAS[0]*	50	A[14]	78	OE1*	106	SCS[2]*
23	CAS[1]*	51	A[15]	79	VSS	107	SCS[1]*
24	VDD	52	VDD	80	VDD	108	SCS[0]*
25	CAS[2]*	53	VSS	81	OE0*	109	VSS
26	CAS[3]*	54	A[16]	82	SWE0*	110	PIO0[0]
27	TOUT[0]	55	A[17]	83	SWE1*	111	PIO0[1]
28	TOUT[1]	56	A[18]	84	TSTO1	112	PIO0[2]

Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
113	PIO0[3]	137	VDD	161	D[10]	185	INT[7]
114	VDD	138	D[28]	162	D[9]	186	VSS
115	PIO0[4]	139	D[27]	163	D[8]	187	PCST[2]
116	PIO0[5]	140	D[26]	164	VSS	188	PCST[1]
117	PIO0[6]	141	D[25]	165	VDD	189	PCST[0]
118	PIO0[7]	142	VSS	166	D[7]	190	DCLK
119	VSS	143	D[24]	167	D[6]	191	SDAO
120	TIMOUT2	144	D[23]	168	D[5]	192	DBGE*
121	TIMOUT1	145	D[22]	169	D[4]	193	SDI*
122	TIMIN2	146	D[21]	170	D[3]	194	DRESET*
123	TIMIN1	147	VDD	171	D[2]	195	TEST*
124	SCLK	148	VSS	172	VSS	196	RESET*
125	SIN1	149	D[20]	173	VDD	197	ACK*
126	SIN0	150	D[19]	174	D[1]	198	BUSERR*
127	CTS1*	151	D[18]	175	D[0]	199	BSTART*
128	CTS0*	152	D[17]	176	NMI*	200	VSS
129	VDD	153	D[16]	177	INT[0]	201	VDD
130	SOUT1	154	D[15]	178	INT[1]	202	SYSCLK
131	SOUT0	155	D[14]	179	INT[2]	203	PLLOFF*
132	RTS1*	156	VDD	180	VDD	204	CLKEN
133	RTS0*	157	VSS	181	INT[3]	205	VDDP
134	D[31]	158	D[13]	182	INT[4]	206	VSSP
135	D[30]	159	D[12]	183	INT[5]	207	VSS
136	D[29]	160	D[11]	184	INT[6]	208	XOUT

* Active-low signal

4.2 PIN FUNCTIONS

Name	I/O	5V tolerant input	Function
System Interface			
SYSCLK	O	-	System Clock Outputs a clock with frequency either equal to or half of that of the TX39 Processor Core.
A[31:1]	I/O	A	Address bus. It is an output when the TX3904A is a bus master, an input in otherwise. A[31:24] are shared with PIO2.
(PIO2[7:0])	I/O	A	
BE[3:0]*	I/O	A	Byte Enable Indicates valid data positions on the data bus D[31:0]. It is an output when the TX3904A is a bus master, an input in otherwise. BE[3]* : D[31:24] BE[2]* : D[23:16] BE[1]* : D[15:8] BE[0]* : D[7:0]
D[31:0]	I/O	A	Data bus. D[15:0] is used in 16-bit bus mode.
SCS[3:0]*	O	-	System Chip Select Asserts when accessing the address range that is set by the internal register.
R/W*	I/O	A	Read/Write Indicates the bus operation being executed is either read or write. It is an output when the TX3904A is a bus master, an input in otherwise. High: Read Low: Write
BSTART*	I/O	A	Bus Start Asserts during the first clock period of the bus operation. It is an output when the TX3904A is a bus master, an input in otherwise.
LAST*	I/O	A	Last Indicates that it is the last of the bus operation. It is an output when the TX3904A is a bus master, an input in otherwise.
ACK*	I/O	A	Acknowledge Slave devices inform the bus master that the bus operation may be finished. It is an input when the TX3904A is a bus master, an output in otherwise.

5V tolerant input : A = Available, N.A = Not Available

Name	I/O	5V tolerant input	Function
BUSERR*	I/O	A	Bus Error Informs of bus errors. It is an input when the TX3904A is a bus master, an output in otherwise.
RESET*	I	N.A	Reset Initializes the TX3904A by setting this signal low for 12 SYSCLK or more.
Clock			
XIN	I	N.A	Crystal Input Connect a crystal oscillator.
XOUT	O		Crystal Output Connect a crystal oscillator.
PLLOFF*	I	N.A	PLL OFF A signal to halt the PLL oscillation of the TX3904A built-in clock generator.
CLKEN	I	N.A	Clock Enable A signal to enable the TX3904A internal clock.
External Bus Master Interface			
BUSREQ*	I	A	Bus Request Changes to low when the external bus master requests for the bus ownership of the TX39 Processor Core. A pin that is shared with the PIO1.
(PIO1[1])	I/O	A	
BUSGNT*	O	-	Bus Grant Asserted when the TX39 Processor Core informs that it is releasing the bus ownership in response to BUSREQ*. A pin that is shared with the PIO1.
(PIO1[0])	I/O	A	
HAVEIT*	I	A	Have It Indicates to the TX3904A that the external bus master has the bus ownership. A pin that is shared with the PIO1.
(PIO1[2])	I/O	A	
BUSREL*	O	-	Bus Release Asserted when TX39 processor core requests the external bus master to release the bus ownership. A pin that is shared with the PIO1.
(PIO1[3])	I/O	A	
Interrupt Signals			
NMI*	I	A	Non Maskable Interrupt Non-maskable interrupt input.

5V tolerant input : A = Available, N.A = Not Available

Name	I/O	5V tolerant input	Function
INT[7:0]	I	A	Interrupt Request External interrupt request signals. An active level and level sensed/edge triggered are designated by the chip configuration register.
Memory Interface			
RAS0[3:0]* RAS1[3:0]*	O	-	Row Address Strobe RAS signals for a DRAM.
CAS[3:0]*	O	-	Column Address Strobe CAS signals for a DRAM.
WE*	O	-	Write Enable Write enable signal for a DRAM.
OE0* OE1*	O	-	Output Enable Output enable signals of a ROM.
CE0[1:0]* CE1[1:0]*	O	-	Chip Enable Chip select signals of a ROM.
SWE0* SWE1*	O	-	SRAM Write Enable Write enable signals of an SRAM and Flash ROM.
DMA Interface			
DREQ[3:0]	I	A	DMA Request The external I/O device requests a DMA transfer. DREQ[3:2] are shared with the PIO1.
(PIO1[7:6])	I/O	A	
DACK[3:0]	O	-	DMA Acknowledge Acknowledge signals to DMA transfer request through the DREQ. DACK[3:2] are shared with the PIO1.
(PIO1[5:4])	I/O	A	
DONE*	I	A	Done Input: LOW is input to terminate data transfer. Output: Notification that transfer ended. This signal is asserted during one SYSCLK period when DMA transfer ends.

5V tolerant input : A = Available, N.A = Not Available

Name	I/O	5V tolerant input	Function
Timer/Counter			
TIMOUT2 TIMOUT1	O	-	Timer Output Output signals of the timer.
TIMIN2 TIMIN1	I	N.A	Timer Input External signals for the timer.s count.
Serial Port			
SIN1 SIN0	I	A	Serial Input Data input signals of the serial I/O.
SOUT1 SOUT0	O	-	Serial Output Data output signals of the serial I/O.
CTS1* CTS0*	I	A	Clear To Send Control signals of the serial I/O.
RTS1* RTS0*	O	-	Request To Send Control signals of the serial I/O.
SCLK	I	A	Serial Clock Input Clock input of the serial I/O.
IO Port			
PIO0[7:0]	I/O	A	I/O Port0 A signal for I/O Port0. Input/Output can be set in each bit.
Debug Interface			
PCST[2:0] DCLK SDAO	O	-	Debug A signal for the external real time debug system. DBGE*, SDI*, and DRESET* are pulled up internally.
DBGE* SDI* DRESET*	I	N.A	
Others			
BOOT16	I	N.A	Boot 16-bit Sets the memory bus width of the channel-0 of ROM controller. Fix to either high or low according to the bus width of the boot ROM. High: 16 bits Low: 32 bits

5V tolerant input : A = Available, N.A = Not Available

Name	I/O	5V tolerant input	Function
HALF*	I	N.A	Half Speed Bus Mode Designates the half speed bus mode. At low, the TX3904A becomes the half speed bus mode so that the frequency of the bus operation becomes a half of the operation frequency of the TX39 Processor Core. Fix to either high or low.
ENDIAN	I	N.A	Sets the Endian immediately after reset. Fix to either high or low. High: Big Endian Low: Little Endian
TEST*	I	N.A	Test A signal for tests. Fix to high.
TOUT[3:0], TSTO1, TSTO2	O	-	Test output A signal for tests. Leave open.

5V tolerant input : A = Available, N.A = Not Available

5. ELECTRICAL SPECIFICATIONS

5.1 ABSOLUTE MAXMUM RATINGS

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	-0.3 ~ 5.0	V
Input voltage XIN, PLLOFF*, CLKEN, DBGE*, SDI*, DRESET*, TEST*, RESET*, BOOT16, HALF*, ENDIAN, TIMIN	V_{IN1}	-0.3 ~ V_{DD} + 0.3V	V
Other inputs	V_{IN2}	-0.3 ~ 5.3V	V
Storage temperature	T_{STG}	-40 ~ 125	°C
Maximum power dissipation	P_D	1.2	W

Note: Using the LSI at specifications higher than the maximum ratings can cause permanent damage to the LSI device. For normal operation, use under the recommended operating conditions. Exceeding the recommended operating conditions may affect the reliability of the LSI device.

5.2 RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Max.	Unit
Supply voltage	V_{DD}		3.0	3.6	V
Operating temperature	T_a		0	70	°C

5.3 DC CHARACTERISTICS

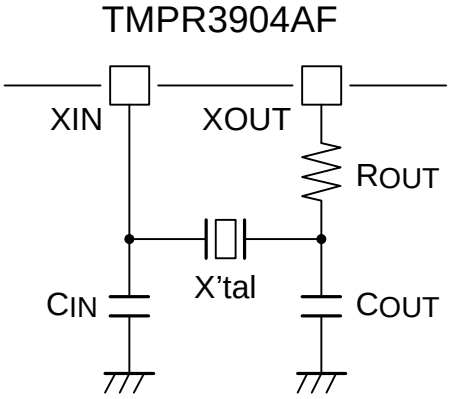
(T_a = 0 ~ 70°C, V_{DD} = 3.3V ± 0.3V, V_{SS} = 0V)

Parameter	Symbol	Condition	Min.	Max.	Unit
Low-level input voltage	V_{IL1}	XIN	-	$V_{DD} \times 0.2$	V
	V_{IL2}	except XIN	-	0.8	
High-level input voltage	V_{IH1}	XIN	$V_{DD} \times 0.8$	-	V
	V_{IH2}	except XIN	2.0	-	
Low-level output current	I_{OL1}	V_{OL} = 0.4V (1)	4.0	-	mA
	I_{OL2}	V_{OL} = 0.4V (2)	8.0	-	mA
	I_{OL3}	V_{OL} = 0.4V (3)	16.0	-	mA
High-level output current	I_{OH1}	V_{OH} = 2.4V (1)	-	-4.0	mA
	I_{OH2}	V_{OH} = 2.4V (2)	-	-8.0	mA
	I_{OH3}	V_{OH} = 2.4V (3)	-	-16.0	mA
Input leakage current	I_{IH1}	(6)	-10	10	μA
	I_{IH2}	(7),(8)	-10	20	μA
	I_{IL1}	(6),(8)	-10	10	μA
	I_{IL2}	(7)	-320	10	μA
Operating current	I_{DD}	V_{DD} = 3.6V, 66MHz	-	330	mA

(1) PCST[2:0], DCLK, SDAO, SYSCLK, SCS[3:0]*, SOUT0, SOUT1, CTS0*, CTS1*,
(2) BE[3:0]*, BSTART*, BUSERR*, ACK*, LAST*, R/W*, BUSGNT*, BUSREL*, BUSREQ*, HAVEIT*, DREQ[3:2], DACK[3:2], PIO0[7:0], DONE*, RTS0*, RTS1*, TIMOUT1, TIMOUT2, RAS0[3:0]*, RAS1[3:0]*, CAS[3:0]*, OE0*, OE1*, CE0[1:0]*, CE1[1:0]*, SWE0*, SWE1*
(3) D[31:0], A[31:1], WE*
(6) Input pins except (7) and (8) below
(7) DBGE*, SDI*, DRESET*, TEST*
(8) XIN

5.4 CRYSTAL OSCILLATOR CHARACTERISTICS

5.4.1 Crystal Oscillator Conditions



Parameter	Symbol	Recommended value	Unit
Crystal Oscillator frequency	f_{IN}	4.125 ~ 8.25	MHz
Output register	R_{OUT}	3.3	kΩ
External condenser	C_{IN},C_{OUT}	10	pF
Clock generator Rising time Falling time	 t_r t_f	 5(1) 5(1)	 ns ns

(1) For a reference. Ask clock generator manufacture.

5.4.2 Electrical Specifications

(T_a = 0 ~ 70°C, V_{DD} = 3.3V ± 0.3V, V_{SS} = 0V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Oscillation start time	t_{STA}	f=4.125~8.25MHz	-	500μs	10ms	-

5.5 AC CHARACTERISTICS

(T_a = 0 ~ 70°C, V_{DD} = 3.3V ± 0.3V, V_{SS} = 0V, C_L = 50pF)

Symbol	Signal	Description	Min.	Max.	Unit
t_{sys}	SYSCLK	Full speed bus mode	15	-	ns
		Half speed bus mode	30	-	ns
t_1	SYSCLK	High Level	5	-	ns
t_2	SYSCLK	Low Level	5	-	ns
t_3	SYSCLK	High Level (Half speed mode)	12	-	ns
t_4	SYSCLK	Low Level (Half speed mode)	12	-	ns
t_5	A[31:1]	Delay	-	22	ns
t_6	BE[3:0]*, R/W*, BSTART*, LAST*	Delay (High to Low)	-	10	ns
t_7	BE[3:0], R/W*, BSTART*, LAST*	Delay (Low to High)	-	10	ns
t_8	D[31:0]	Setup	8	-	ns
t_9	D[31:0]	Hold	0	-	ns
t_{10}	ACK*, BUSERR*	Setup	8	-	ns
t_{11}	ACK*, BUSERR*	Hold	0	-	ns
t_{12}	D[31:0]	Delay	-	12	ns
t_{13}	BUSREQ*	Setup	8	-	ns
t_{14}	BUSREQ*	Hold	0	-	ns
t_{15}	BUSGNT*	Delay	-	10	ns
t_{16}	ACK*	Delay	-	10	ns
t_{17}	HAVEIT*	Setup	8	-	ns
t_{18}	HAVEIT*	Hold	0	-	ns
t_{19}	BUSREL*	Delay	-	10	ns
t_{20}	A[31:1], BE[3:0], R/W*, BSTART*, LAST*	Active to Hi-Z	-	17	ns
t_{21}	A[31:1], BE[3:0], R/W*, BSTART*, LAST*	Hi-Z to active	-	17	ns
t_{22}	A[31:1], BE[3:0], R/W*, BSTART*, LAST*	Setup (Full speed bus mode)	8	-	ns
t_{23}	A[31:1], BE[3:0], R/W*, BSTART*, LAST*	Hold (Full speed bus mode)	0	-	ns
t_{24}	RESET*, INT[7:0]*, NMI*	Setup	8	-	ns

(T_a = 0 ~ 70°C, V_{DD} = 3.3V ± 0.3V, V_{SS} = 0V, C_L = 50pF)

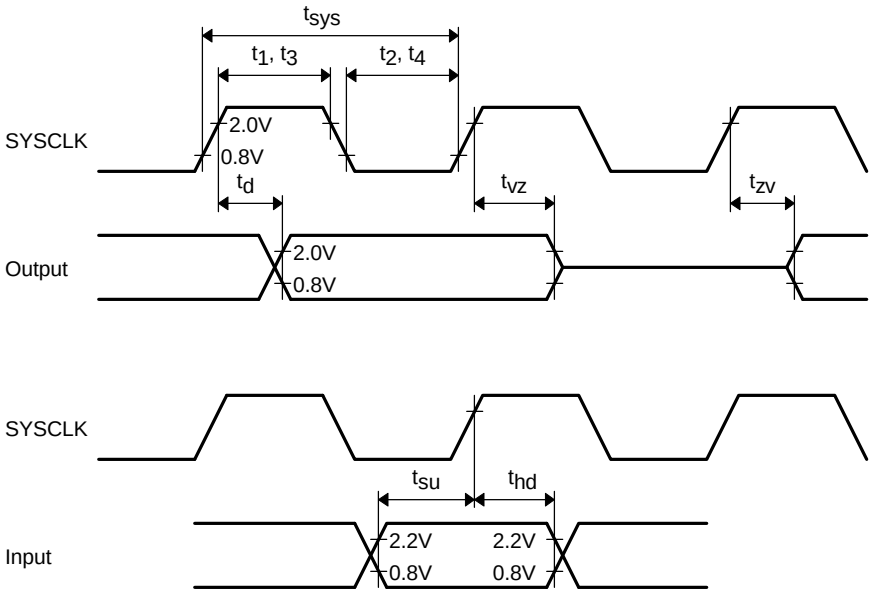
Symbol	Signal	Description	Min.	Max.	Unit
t_{25}	RESET*, INT[7:0]*,NMI*	Hold	0	-	ns
t_{26}	RESET*	Reset time	12	-	t_{sys}
t_{27}	CLKEN	PLL stabilization time upon reset	500(2)	-	μs
t_{28}	SYSCLK		2	-	t_{sys}
t_{29}	PLLOFF*		250	-	μs
t_{30}	RAS1[3:0]*, RAS0[3:0]* CAS[3:0]*	Delay	-	10	ns
t_{31}	WE*	Delay	-	10	ns
t_{32}	CE1[3:0]*, CE0[3:0]* OE1*, OE0*	Delay	-	10	ns
t_{33}	SWE1*, SWE0*	Delay	-	10	ns
t_{34}	DREQ[3:0]	Setup	8	-	ns
t_{35}	DREQ[3:0]	Hold	0	-	ns
t_{36}	DACK[3:0]	Delay	-	10	ns
t_{37}	TIMIN1, TIMIN2	External timer clock	45	-	ns
t_{38}	TIMOUT1,TIMOUT2	Timer output	-	10	ns
t_{39}	SCLK	External baud rate clock	80	-	ns
t_{40}	PIO0[7:0]	Delay	-	10	ns
t_{41}	PIO0[7:0]	Setup	8	-	ns
t_{42}	PIO0[7:0]	Hold	0	-	ns
t_{43}	SCS[3:0]*	Delay	-	10	ns
t_{44}	A[13:1]	Row address output delay	-	15	ns
t_{45}	A[13:1]	Column address output delay	-	15	ns
t_{46}	BSTART*	Low width driven by an external bus master(1)	1	-	t_{sys}
t_{47}	SYSCLK-BSTART*	SYSCLK-BSTART* delay (Half speed bus mode)	0	$t_{sys}/2$ -t_{49}	ns
t_{48}	A[31:1], BE[3:0], R/W*, BSTART*, LAST*	Hold (Half speed bus mode)	0	-	ns
t_{49}	GCLK-SYSCLK	GCLK-SYSCLK delay (Half speed bus mode)	-	8	ns

(1) Both this specification and setup/hold time must be satisfied at the same time when the external bus master drives the BSTART*.

(2) This specification does not include X.tal oscillation start time (t_{STA}).

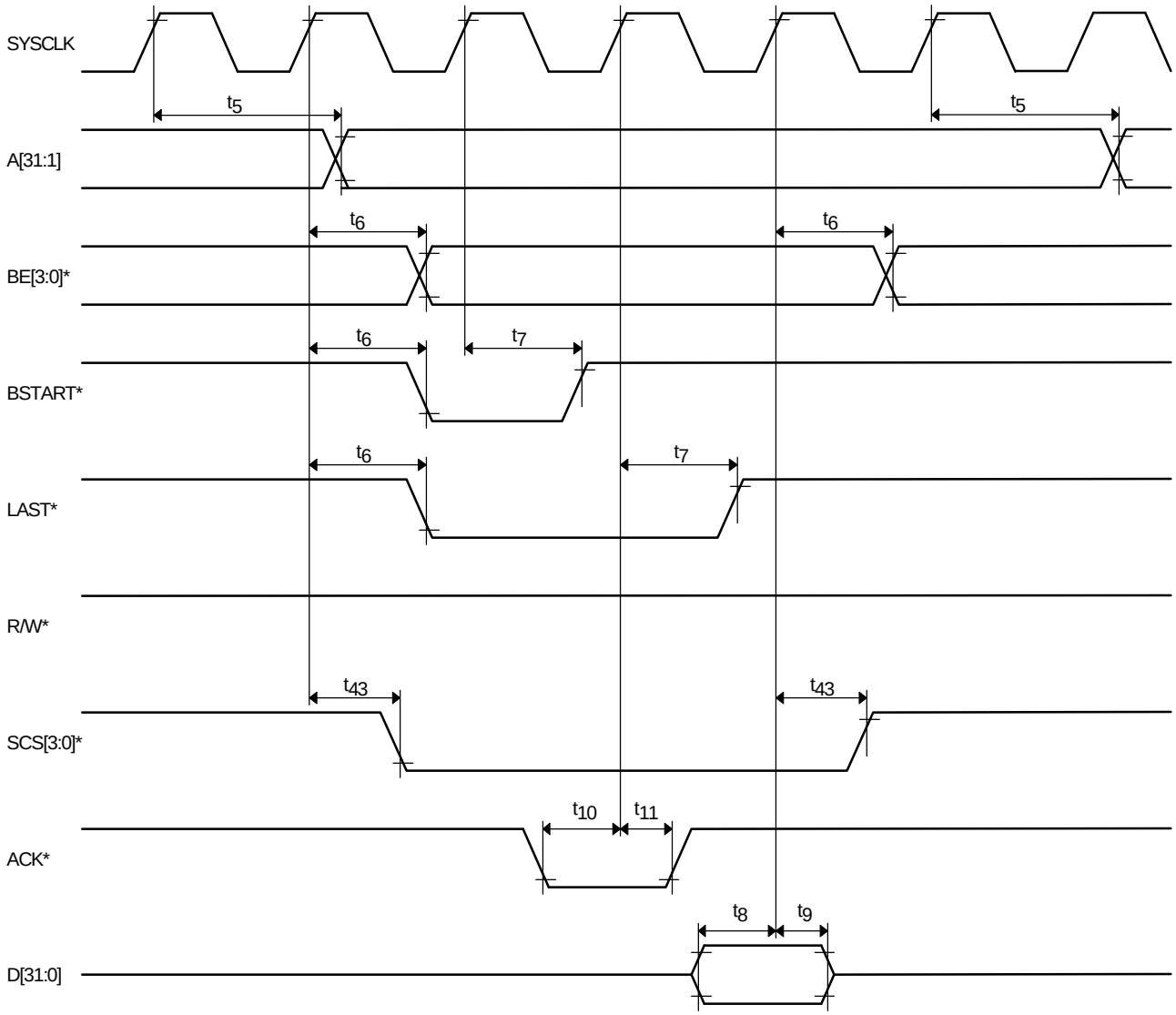
Note: Load capacitance(C_L) for A[31:1], D[31:0] is 100pF.

5.5.1 Definition of AC characteristics



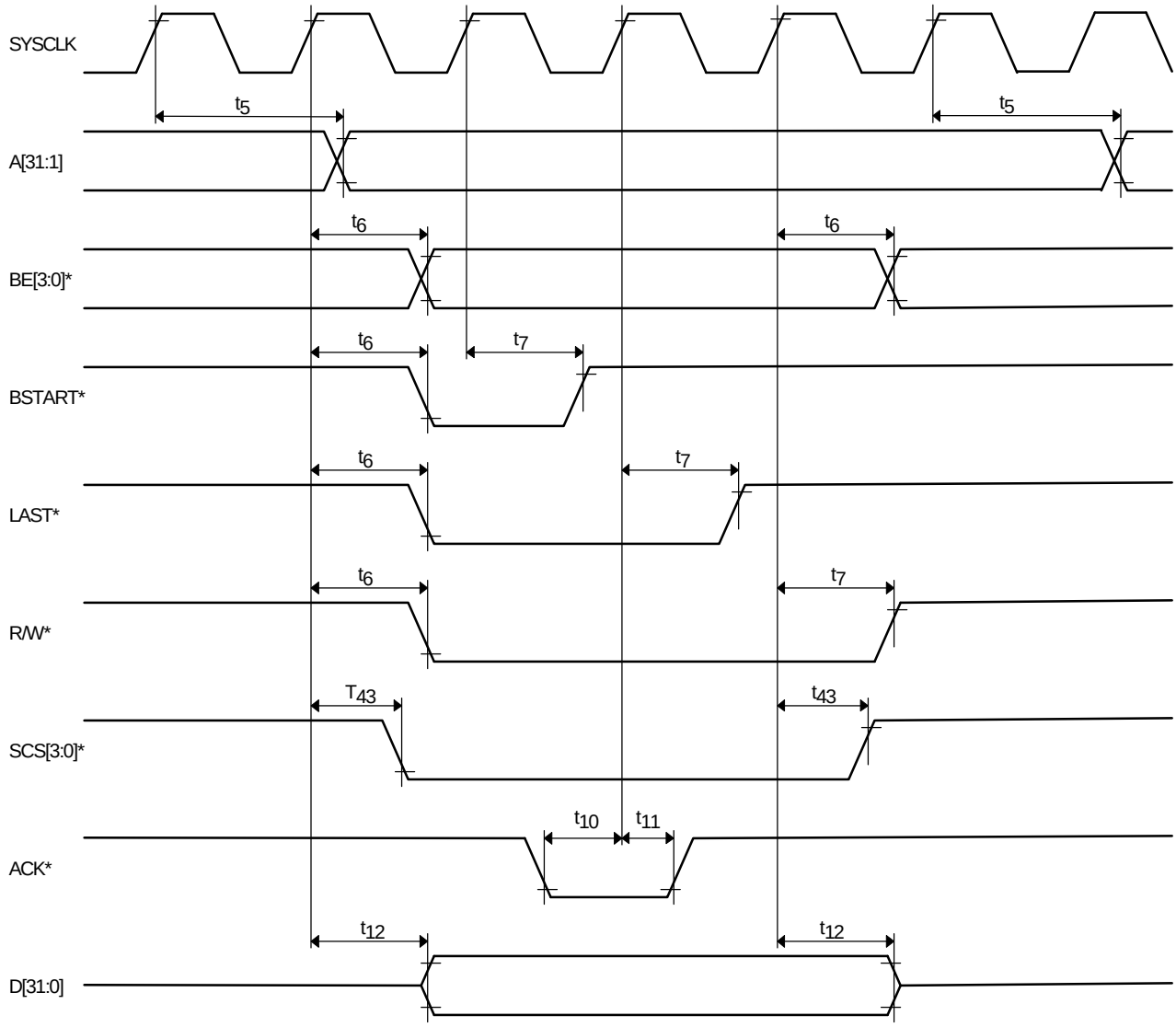
t_d : Output delay
t_{vz} : Output off (active to Hi-Z)
t_{zv} : Output on (Hi-Z to active)
t_{su} : Input setup
t_{hd} : Input hold

5.5.2 Timing diagram



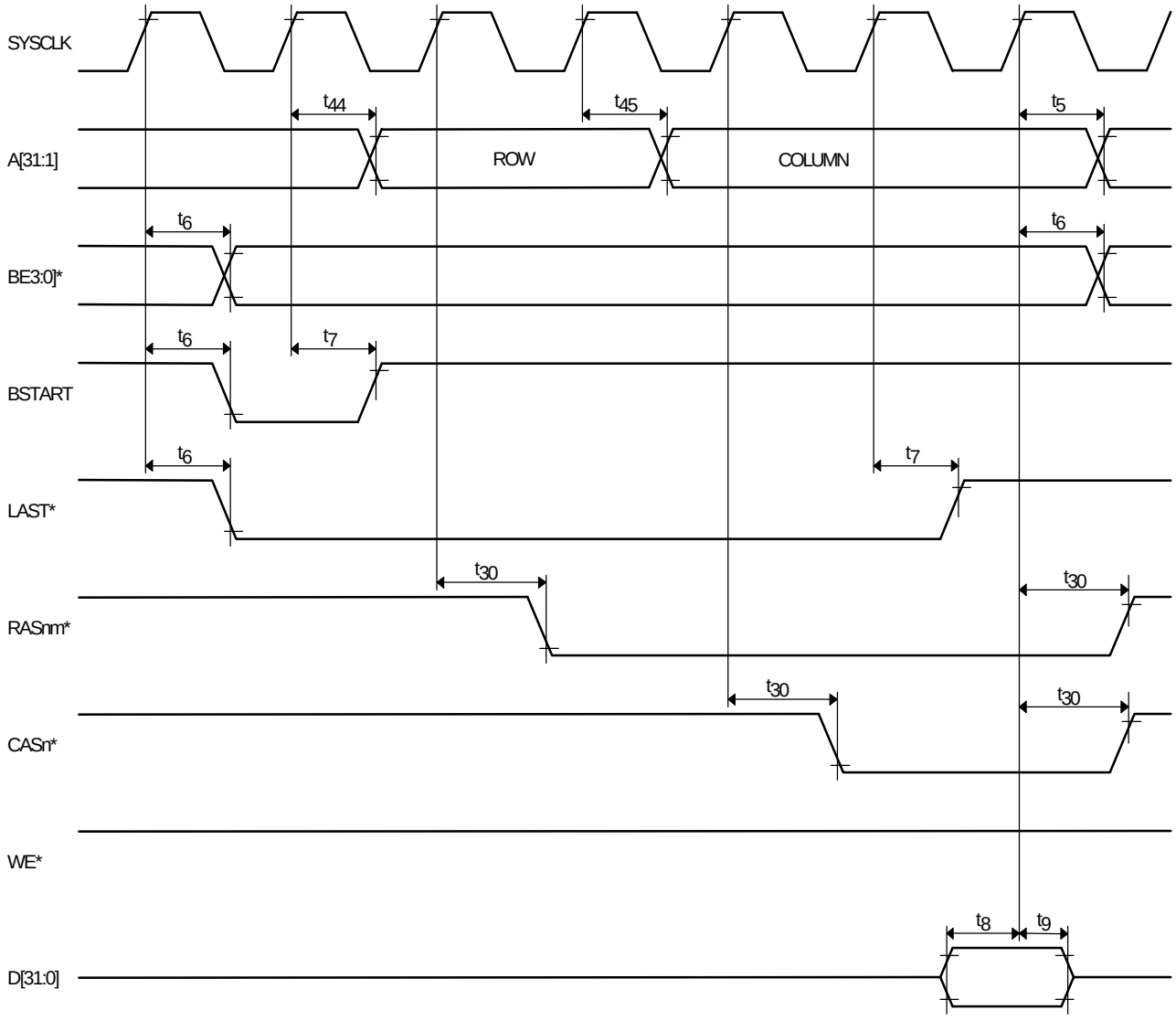
Read operation

Note: SCS[3:0]* are asserted only when a bus master accessed SCS area.

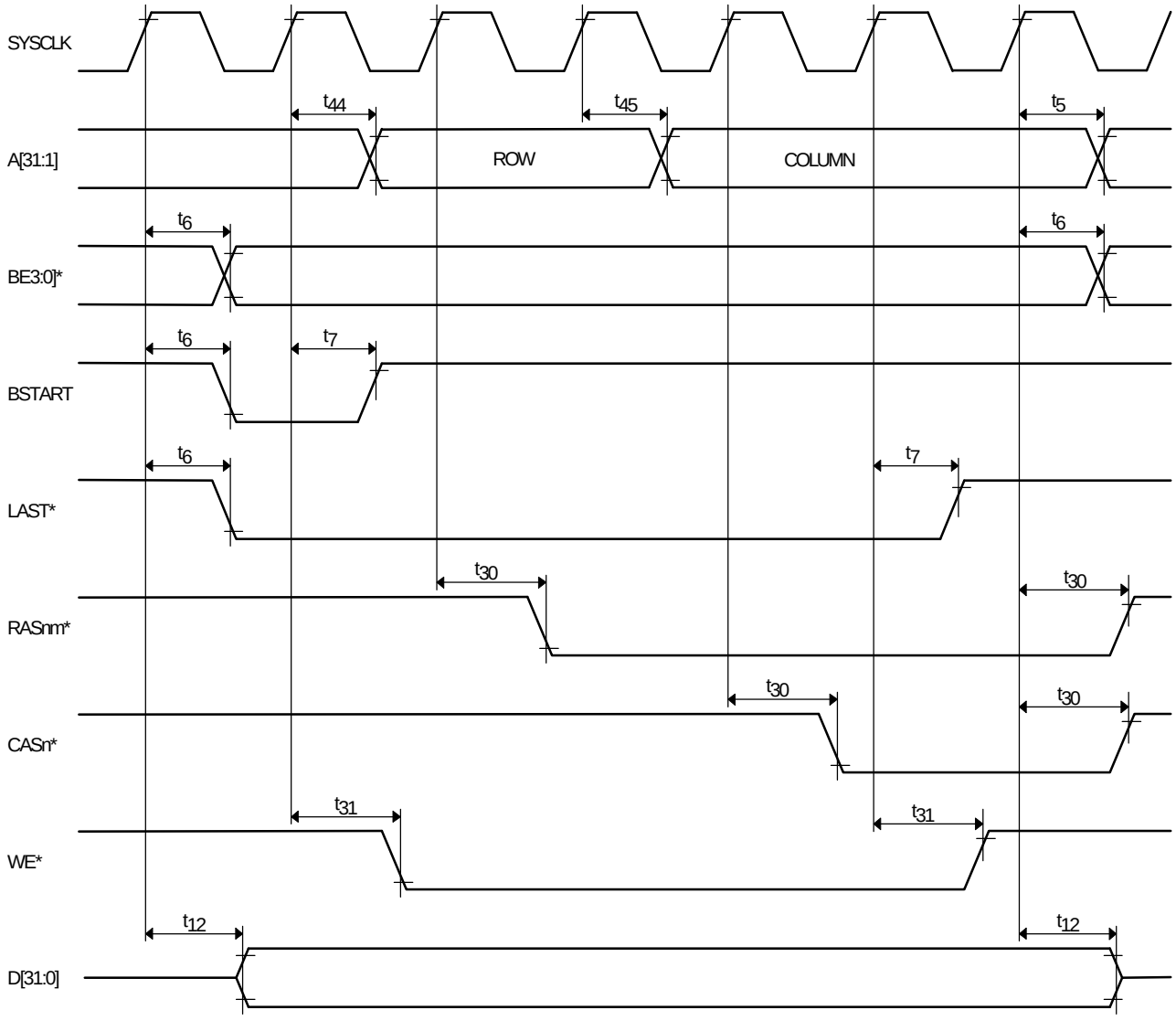


Write operation

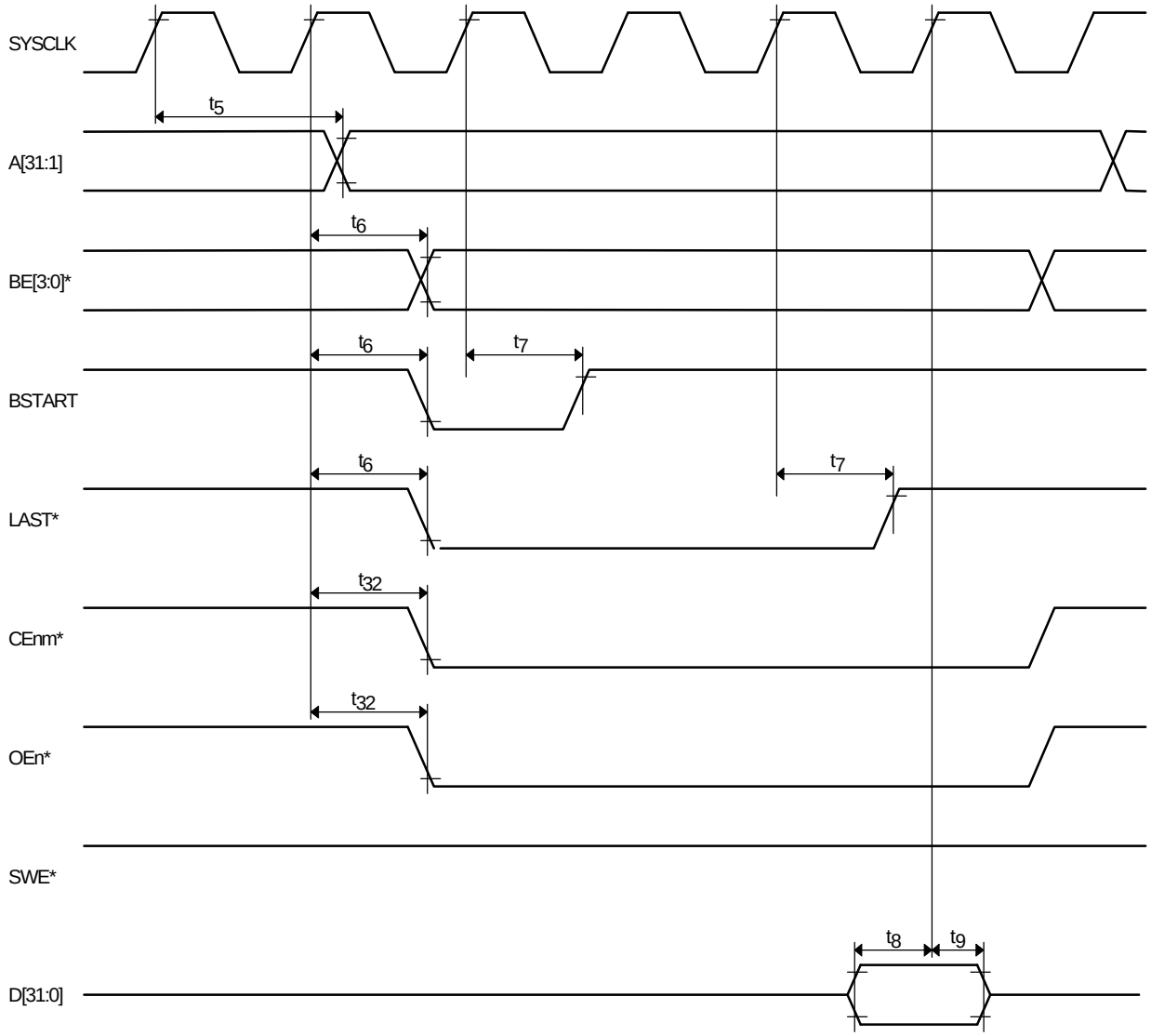
Note: SCS[3:0]* are asserted only when a bus master accessed SCS area.



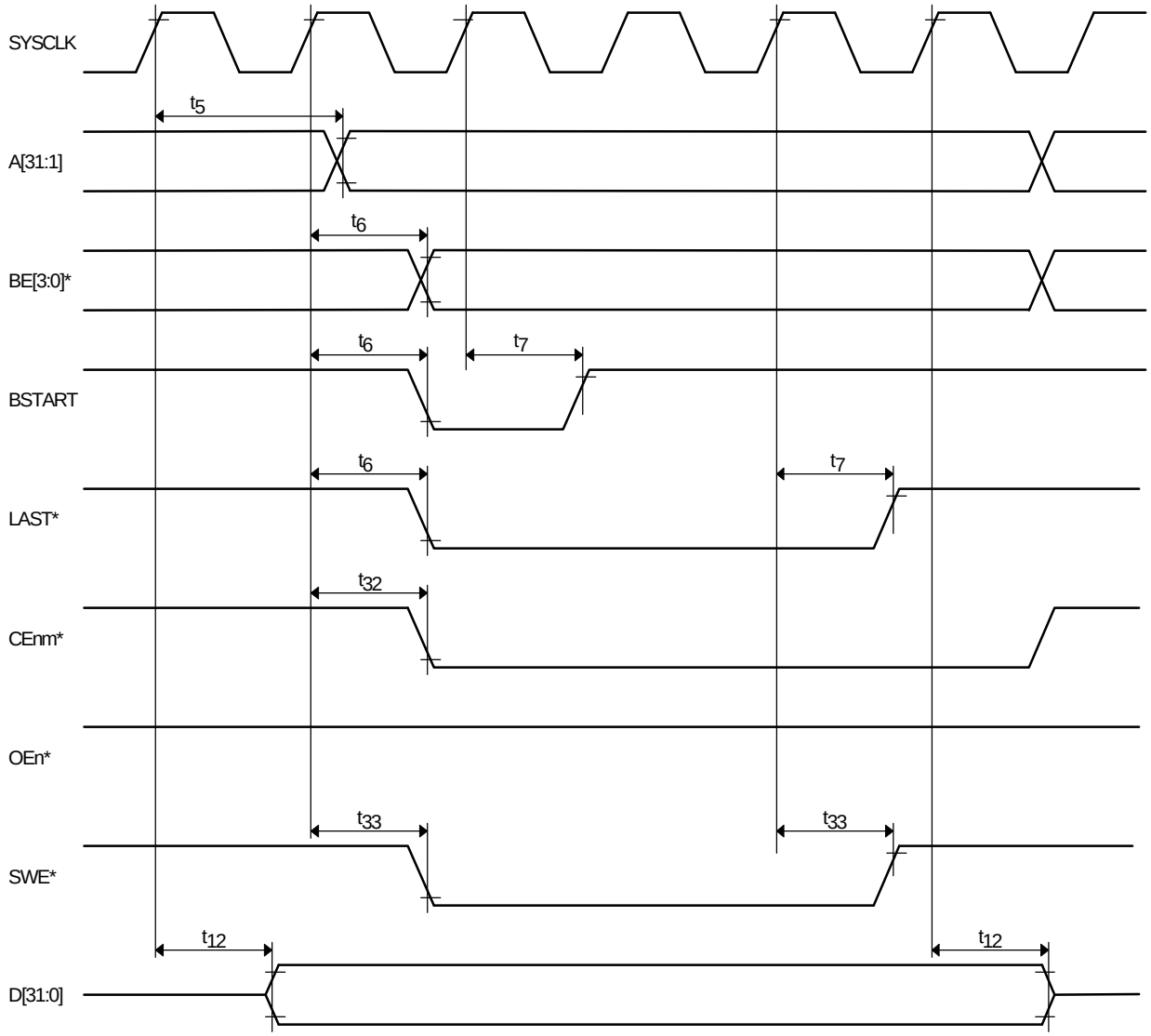
Read operation from DRAM



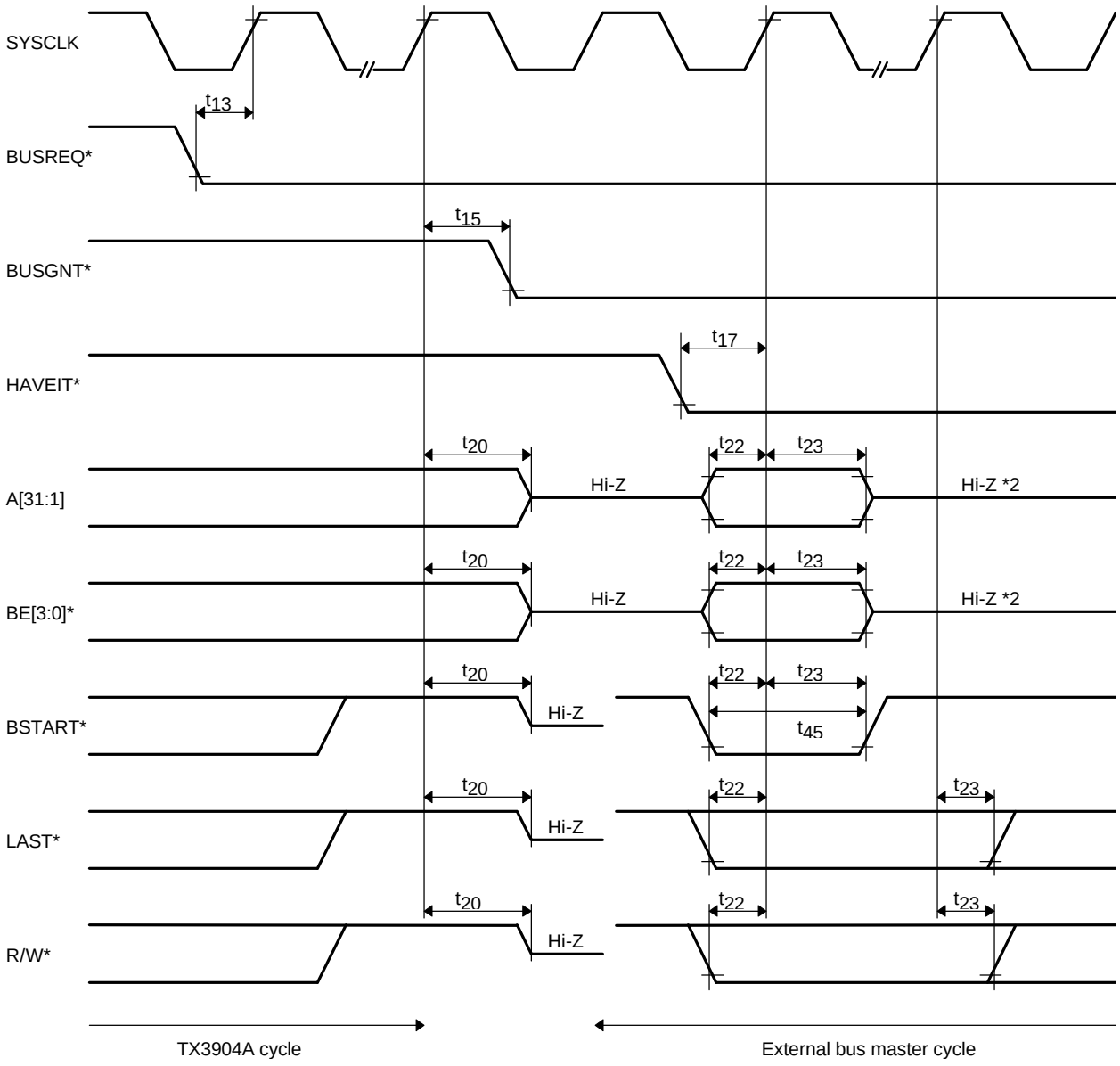
Write operation to DRAM



Read operation from ROM/FLASH/SRAM

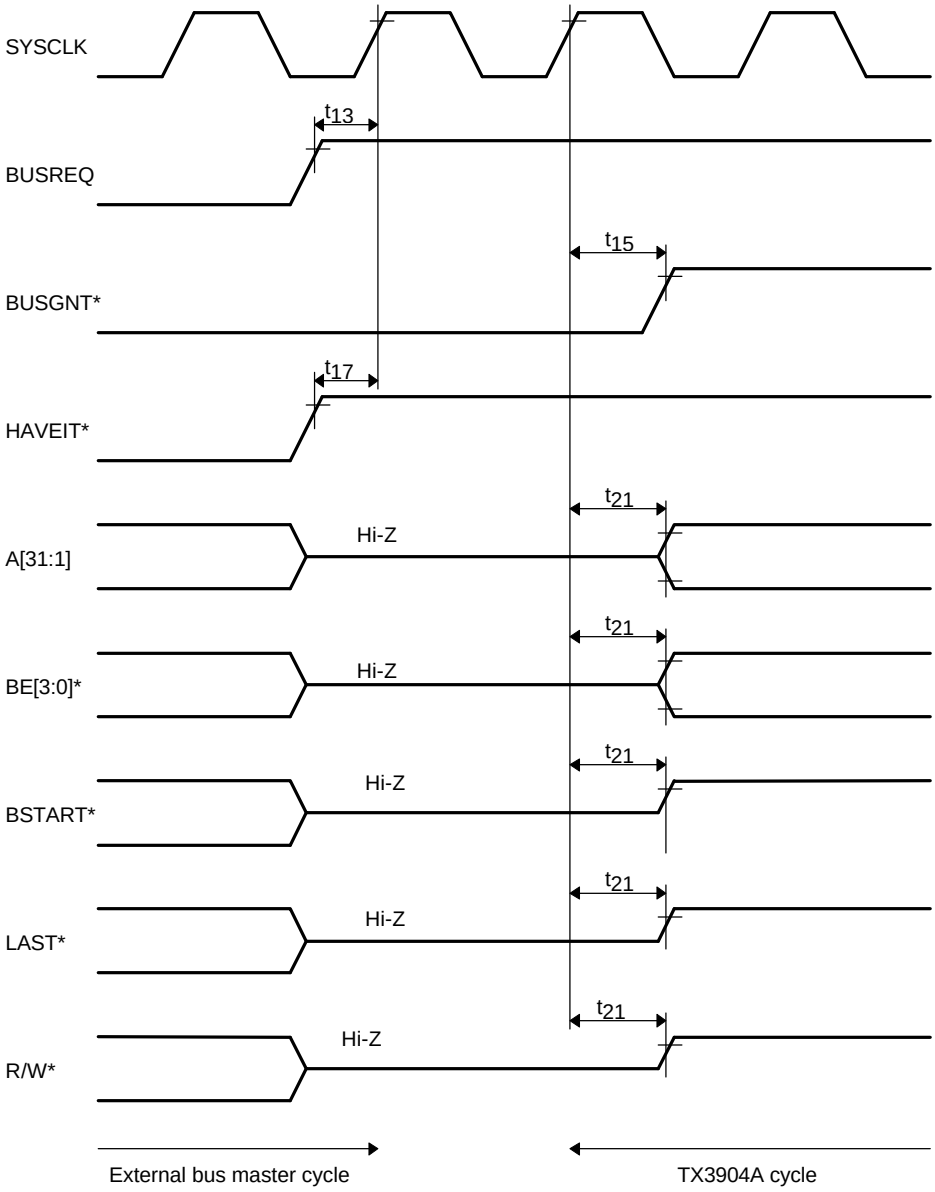


Write operation to FLASH/SRAM

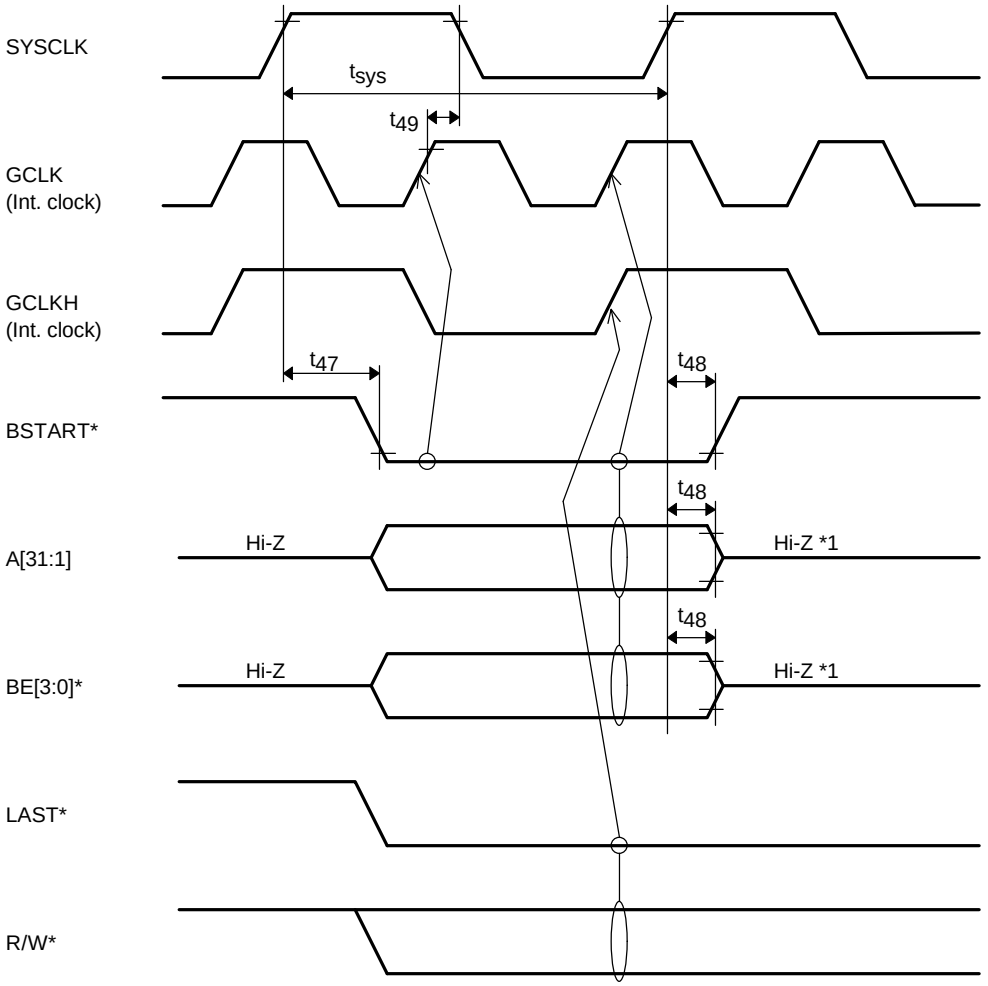


Note 1: A period from asserting BUSREQ* to replying BUSGNT* varies by the status of the TX3904A.
Note 2: When the external bus master uses on-chip DRAMC or ROMC, the external bus master must stop driving A[31:1] and BE[3:0]* at a rising of BSTART*.

Release of bus ownership and External bus master cycle (Full speed bus mode)

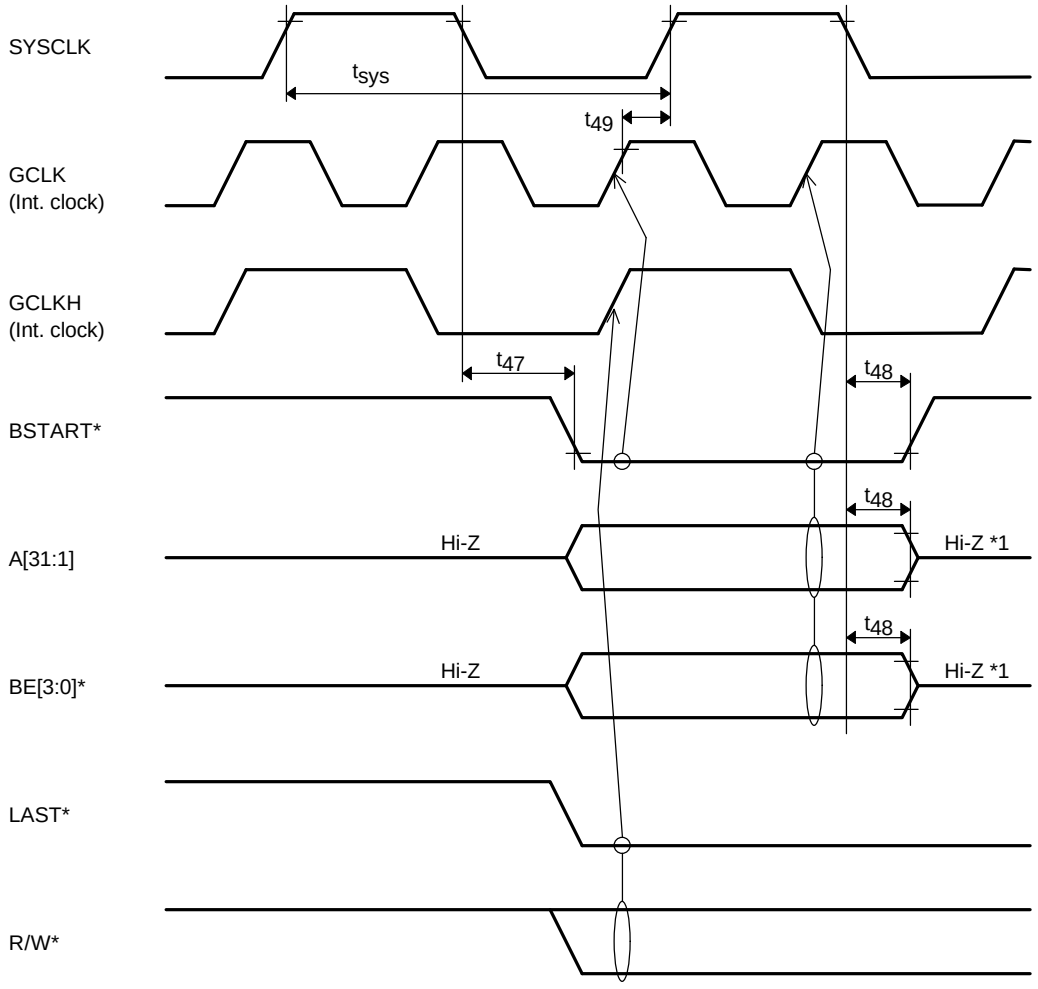


Regaining of bus ownership



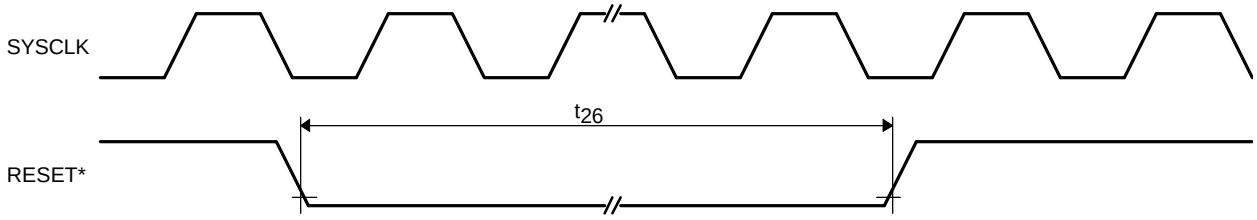
Note 1: When the external bus master uses on-chip DRAMC or ROMC, the external bus master must stop driving A[31:1] and BE[3:0]* at a rising of BSTART*.

External bus master cycle (Half speed bus mode 1)

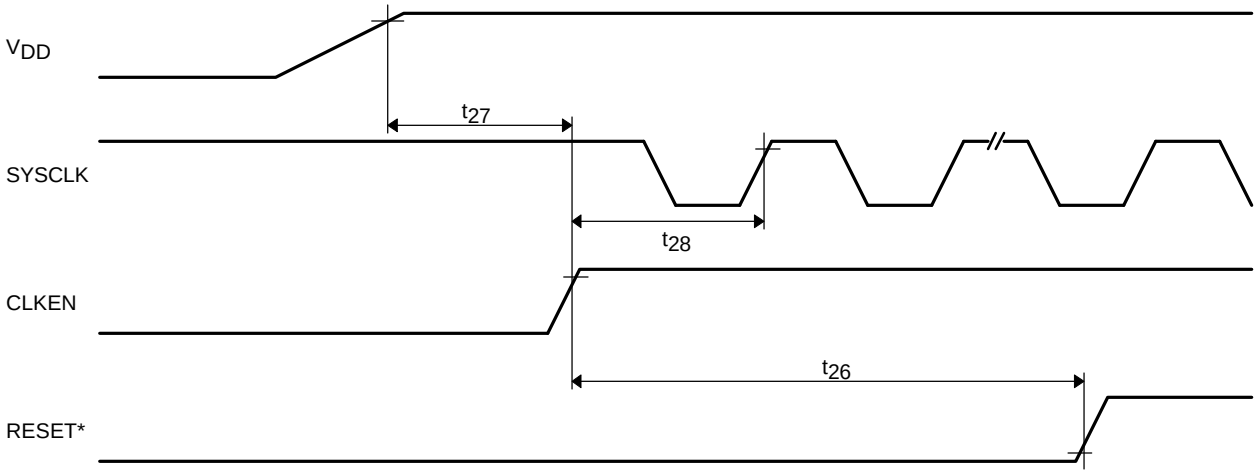


Note 1: When the external bus master uses on-chip DRAMC or ROMC, the external bus master must stop driving A[31:1] and BE[3:0]* at a falling of BSTART*.

External bus master cycle (Half speed bus mode 2)



Reset



t_{27} is not include X'tal oscilation start time (tsta)

Power-on Reset

6. PACKAGE DIMENSION

QFP208-P-2828 Unit: mm