

TC74HC4060AP, TC74HC4060AF

14 - STAGE BINARY COUNTER / OSCILATOR

The TC74HC4060A is a high speed CMOS 14 - STAGE BINARY COUNTER fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The oscillator configuration allows designs using either RC or crystal oscillator circuits, or an external clock may be used.

The clear input resets the counter to a low level on all outputs and disables the oscillator.

A high CLR accomplishes this reset function.

A negative transition on the clock input (ϕI) increments the counter. Ten levels of divided output are provided; 4 stage thru 10 stage and 12 stage thru 14 stage. At the last stage (Q14), a 1/16384 divided frequency is obtained.

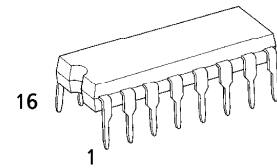
The ϕI input and CLR input are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

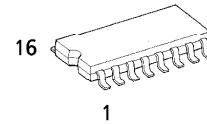
- High Speed..... $f_{MAX} = 58\text{MHz}$ (typ.)
at $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 4\mu\text{A}$ (Max.) at $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (Min.)
- Output Drive Capability 10 LSTTL Loads
- Symmetrical Output Impedance... $|I_{OH}| = I_{OL} = 4\text{mA}$ (Min.)
- Balanced Propagation Delays..... $t_{PLH} \approx t_{PHL}$
- Wide Operating Voltage Range.... V_{CC} (opr.) = 2V ~ 6V
- Oscillator Configuration..... RC or Crystal Oscillator
- Pin and Function Compatible with 4060B

TRUTH TABLE

INPUTS		FUNCTION
ϕI	CLR	
X	H	Counter is reset to zero state. ϕO output goes to high level. $\bar{\phi O}$ output goes to low level.
$\downarrow$	L	Count up one step.
$\uparrow$	L	No change

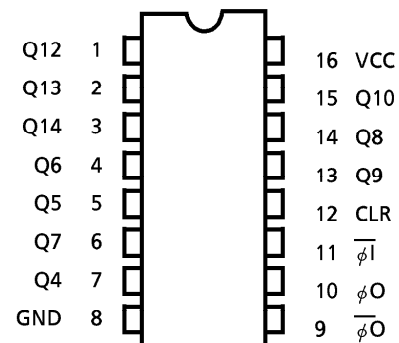


P (DIP16-P-300-2.54A)
Weight : 1.00g (Typ.)



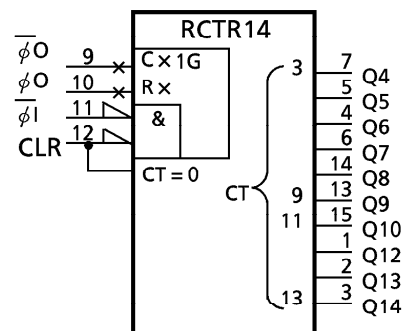
F (SOP16-P-300-1.27)
Weight : 0.18g (Typ.)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



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ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC} /Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	°C

*500mW in the range of $T_a = -40^\circ\text{C} \sim 65^\circ\text{C}$. From $T_a = 65^\circ\text{C}$ to 85°C a derating factor of $-10\text{mW}/^\circ\text{C}$ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	°C
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000 (V_{CC} = 2.0\text{V})$ $0 \sim 500 (V_{CC} = 4.5\text{V})$ $0 \sim 400 (V_{CC} = 6.0\text{V})$	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40 \sim 85^\circ\text{C}$		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}		2.0 4.5 6.0	1.50 3.15 4.20	— — —	— — —	1.50 3.15 4.20	— — —	V
Low - Level Input Voltage	V_{IL}		2.0 4.5 6.0	— — —	— — —	0.50 1.35 1.80	— — —	0.50 1.35 1.80	V
High - Level Output Voltage (Q_n)	V_{OH}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	— — —	1.9 4.4 5.9	— — —	V
		$I_{OH} = -20\mu\text{A}$							
		$I_{OH} = -4 \text{ mA}$ $I_{OH} = -5.2 \text{ mA}$	4.5 6.0	4.18 5.68	4.31 5.80	— —	4.13 5.63	— —	
High - Level Output Voltage ($\phi_O, \bar{\phi}_O$)	V_{OH}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	2.0 4.5 6.0	1.8 4.0 5.5	2.0 4.5 5.9	— — —	1.8 4.0 5.5	— — —	V
		$I_{OH} = -20\mu\text{A}$							
		$I_{OH} = -4 \text{ mA}$ $I_{OH} = -5.2 \text{ mA}$	4.5 6.0	0.17 0.18	0.26 0.26	— —	0.33 0.33	— —	
Low - Level Output Voltage (Q_n)	V_{OL}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	2.0 4.5 6.0	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
		$I_{OL} = 20\mu\text{A}$							
		$I_{OL} = 4 \text{ mA}$ $I_{OL} = 5.2 \text{ mA}$	4.5 6.0	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	
Low - Level Output Voltage ($\phi_O, \bar{\phi}_O$)	V_{OL}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	2.0 4.5 6.0	— — —	0.0 0.0 0.1	0.2 0.5 0.5	— — —	0.2 0.5 0.5	μA
		$I_{OL} = 20\mu\text{A}$							
		$I_{OL} = 4 \text{ mA}$ $I_{OL} = 5.2 \text{ mA}$	4.5 6.0	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC} \text{ or GND}$	6.0	—	—	± 0.1	—	± 1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC} \text{ or GND}$	6.0	—	—	4.0	—	40.0	

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- The information contained herein is subject to change without notice.

TIMING REQUIREMENTS (Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C	UNIT
			V _{CC} (V)	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (ϕ_1)	$t_{W(L)}$ $t_{W(H)}$		2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Pulse Time (CLR)	$t_{W(H)}$		2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Removal Time	t_{rem}		2.0	—	100	125	
			4.5	—	20	25	
			6.0	—	17	21	
Clock Frequency	f		2.0	—	6	5	MHz
			4.5	—	30	24	
			6.0	—	35	28	

AC ELECTRICAL CHARACTERISTICS (C_L = 15pF, V_{CC} = 5V, Ta = 25°C, Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		—	4	8	ns
Propagation Delay Time ($\phi_1 - Q_4$)	t_{PLH} t_{PHL}		—	36	53	
Propagation Delay Time Difference (Q _n - Q _{n+1})	Δt_{pd}	C _L = 50pF (Q _n , Q _{n+1})	—	6	14	
Propagation Delay Time (CLR)	t_{pHL}		—	19	34	
Maximum Clock Frequency	f _{MAX}		33	58	—	MHz

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C		UNIT	
			V _{CC} (V)	MIN.	TYP.	MAX.	MIN.		MAX.
Output Transition Time	t _{TLH} t _{THL}		2.0	—	30	75	—	95	ns
			4.5	—	8	15	—	19	
			6.0	—	7	13	—	16	
Propagation Delay Time ($\overline{\phi}$ 1—Q ₄)	t _{pLH} t _{pHL}		2.0	—	170	300	—	375	
			4.5	—	41	60	—	75	
			6.0	—	30	51	—	64	
Propagation Delay Time Difference (Q _n —Q _{n+1})	Δt _{pd}	C _L = 50pF(Q _n ,Q _{n+1})	2.0	—	32	75	—	95	
			4.5	—	7	15	—	19	
			6.0	—	5	13	—	16	
Propagation Delay Time (CLR)	t _{pLH} t _{pHL}		2.0	—	85	195	—	245	
			4.5	—	23	39	—	49	
			6.0	—	17	33	—	42	
Maximum Clock Frequency	f _{MAX}		2.0	6	12	—	5	—	MHz
			4.5	30	50	—	24	—	
			6.0	35	65	—	28	—	
Input Capacitance	C _{IN}			—	5	10	—	10	pF
Power Dissipation Capacitance	C _{PD} (1)			—	27	—	—	—	

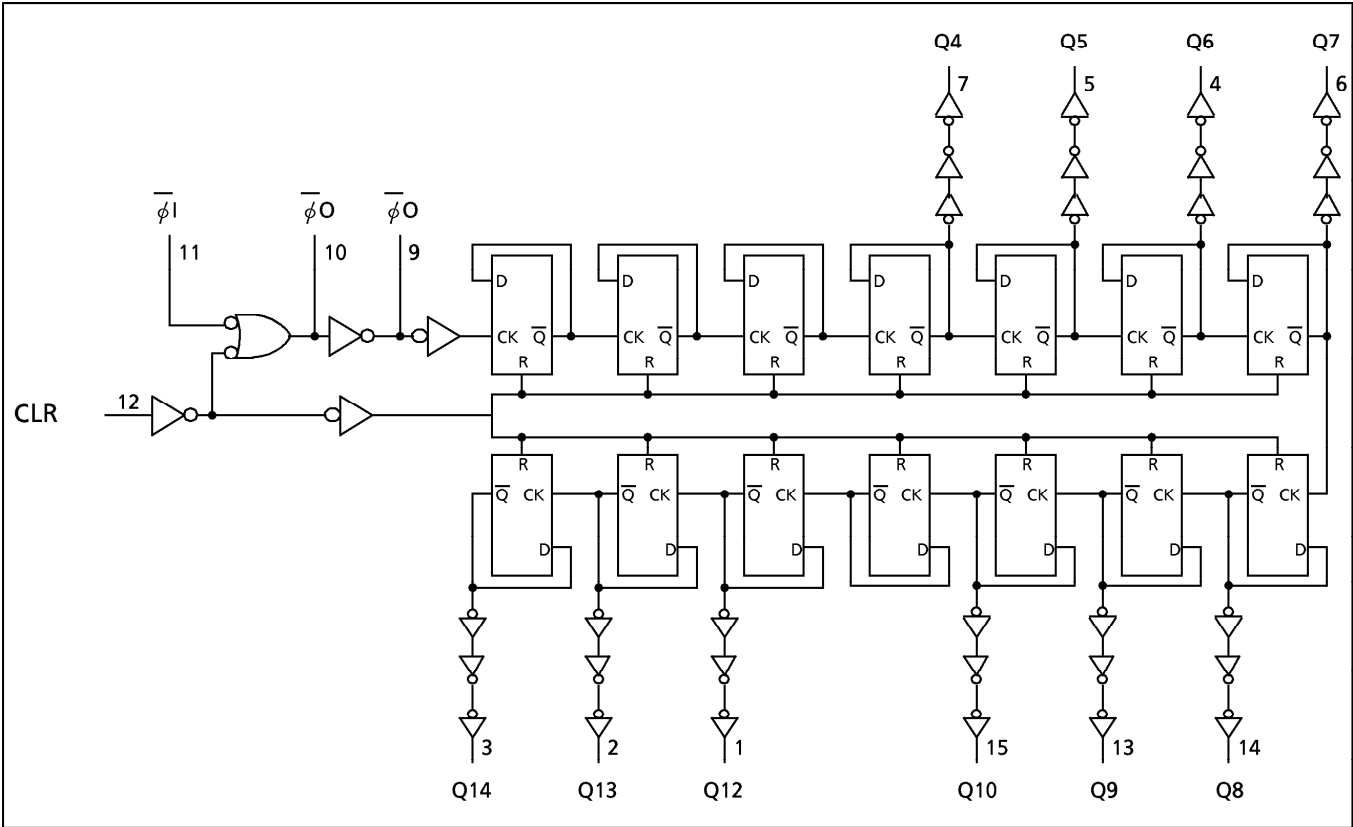
Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

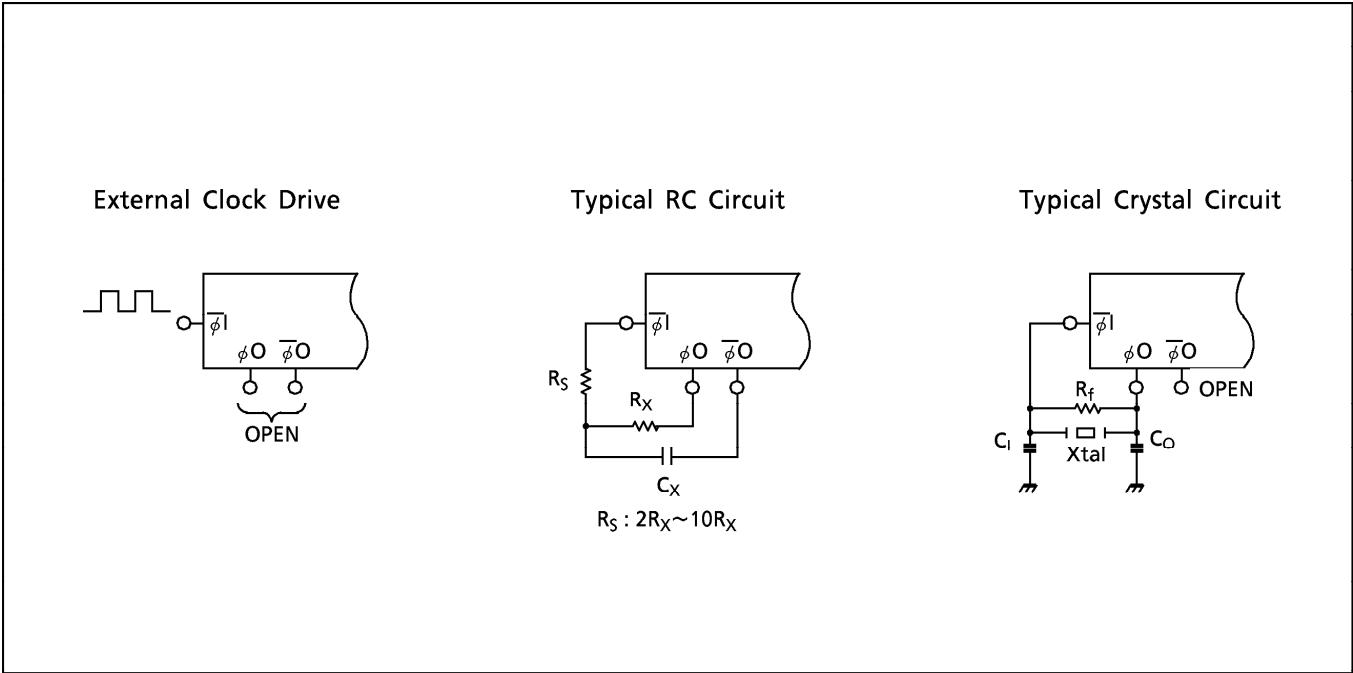
$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

When CR or Crystal oscillation circuit is adopted, the dynamic power dissipation will be greater than the above calculation, because these oscillation circuits spend much supply current.

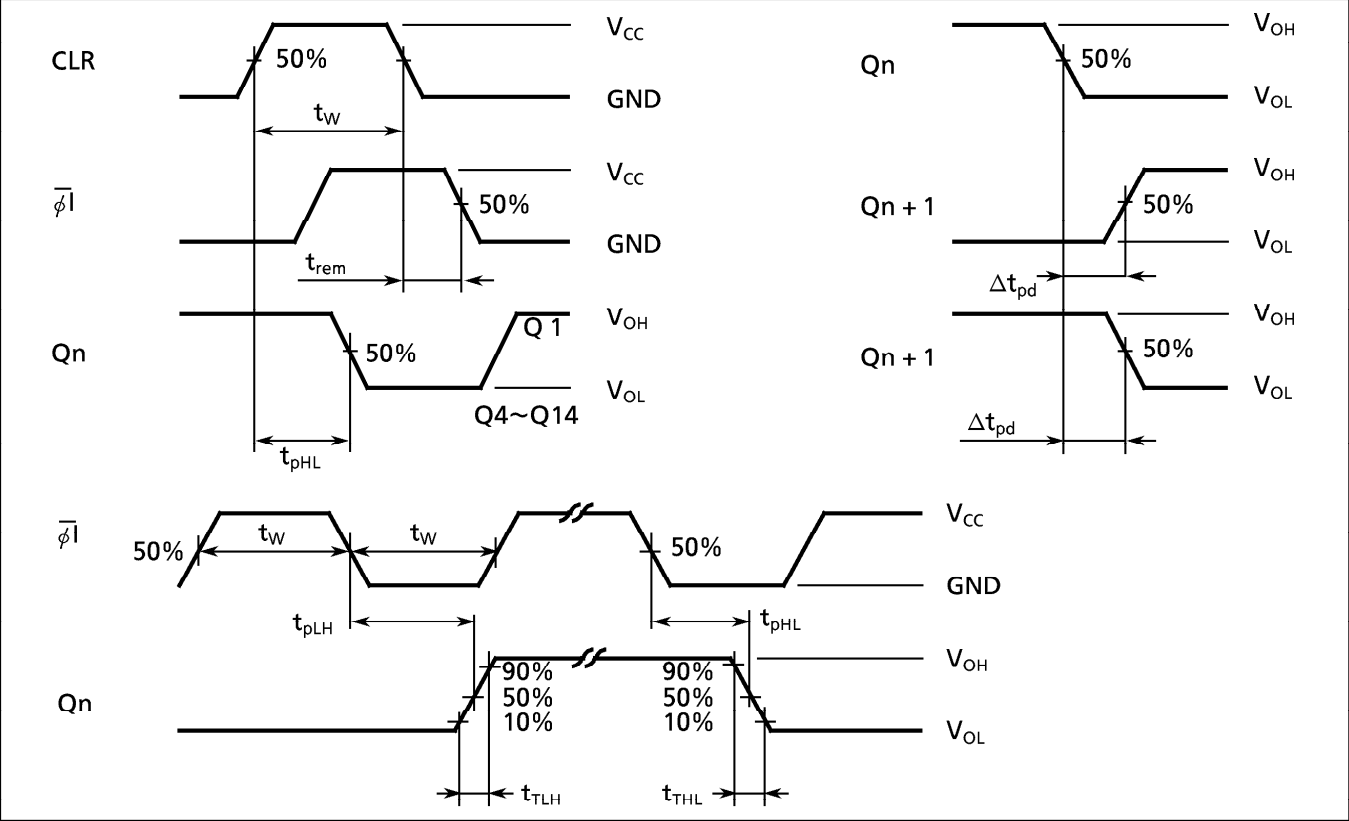
SYSTEM DIAGRAM



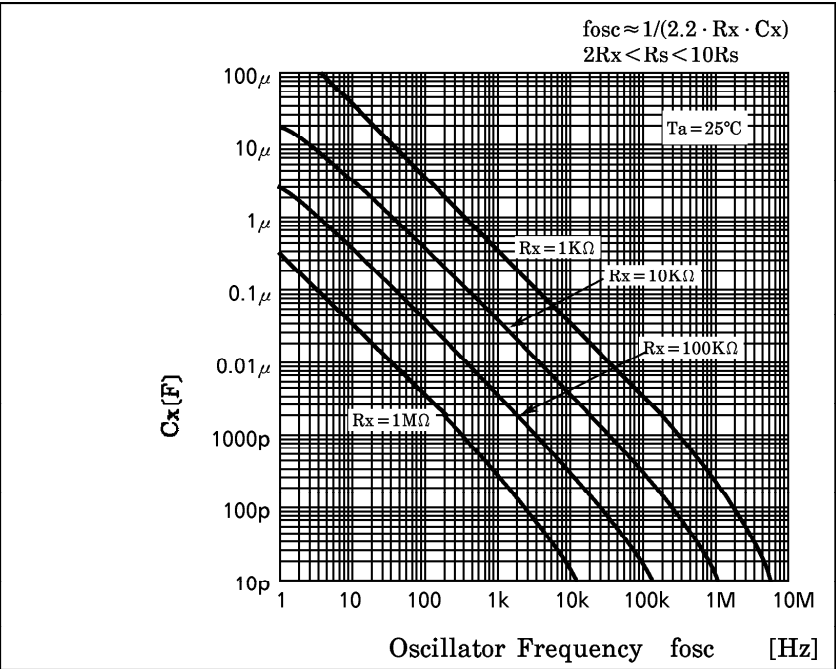
TYPICAL CLOCK DRIVE CIRCUITS



SWITCHING CHARACTERISTICS TEST WAVEFORM

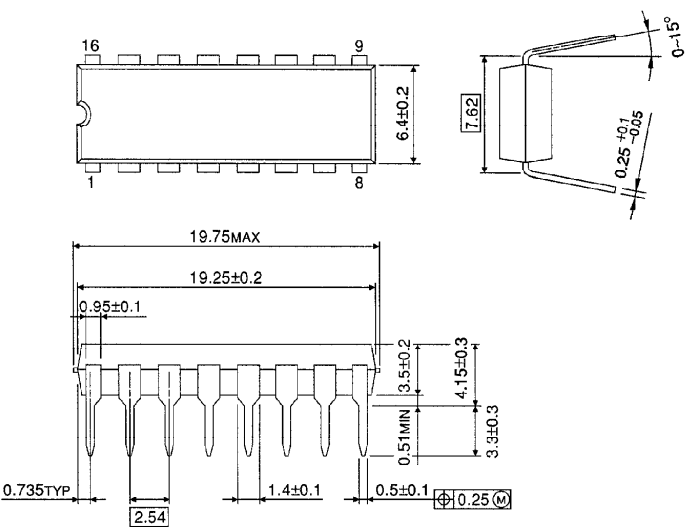


CR Oscillator Characteristics (Typical)



DIP 16PIN OUTLINE DRAWING (DIP16-P-300-2.54A)

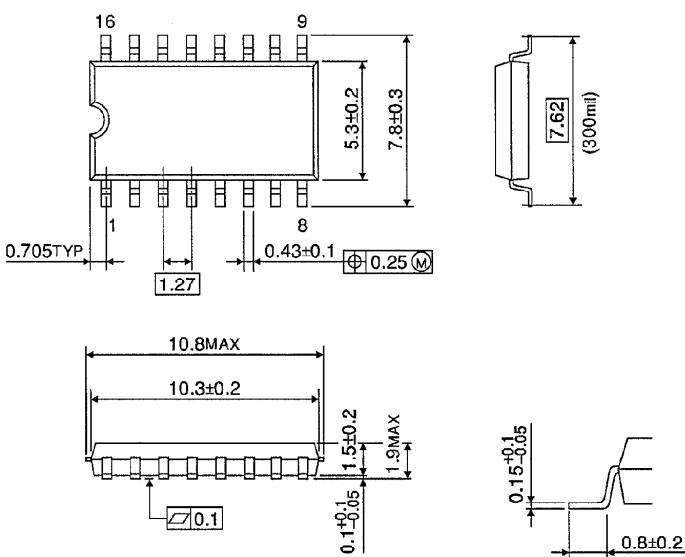
Unit in mm



Weight : 1.00g (Typ.)

SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27)

Unit in mm



Weight : 0.18g (Typ.)