TL3M Device
Triple Level 3 Mapper
TXC-03453

TECHNICAL OVERVIEW
PRODUCT PREVIEW

FEATURES

- Maps up to three independent DS3/E3 line formats into SDH/SONET formats as follows:
  - DS3 to/from STM-1/TUG-3
  - DS3 to/from STS-3/STS-1
  - E3 to/from STM-1/TUG-3
- SDH/SONET bus access:
  - Byte wide drop and add buses
  - Drop bus timing mode (add bus timing derived from drop bus)
  - Add bus timing mode (independent timing for drop/add buses)
- Path overhead byte processing:
  - Microprocessor access
  - External interface
  - B3 generation/detection with test mask
  - B3 bit/block performance counters
  - REI bit/block performance counters
  - C2 mismatch detection
  - C2 unequipped detection and generation
- Alarm indication port
  - Path REI count and RDI status for APS applications
- O-bit channel access via external interface
- Digital desynchronizer with internal pointer leak algorithm
- Line interface:
  - NRZ or P/N rail option for transmit and for receive
  - Monitor NRZ transmit data
- Microprocessor access:
  - Motorola or Intel compatible
  - Hardware interrupt with mask bits
  - Software polling bit
- Testing:
  - Facility or line loopback
  - PRBS generator/analyzer
  - Boundary scan (IEEE 1149.1 standard)
- 3.3 volt power supply, 5 volt tolerant inputs
- 324-lead plastic ball grid array package (23 x 23 mm)

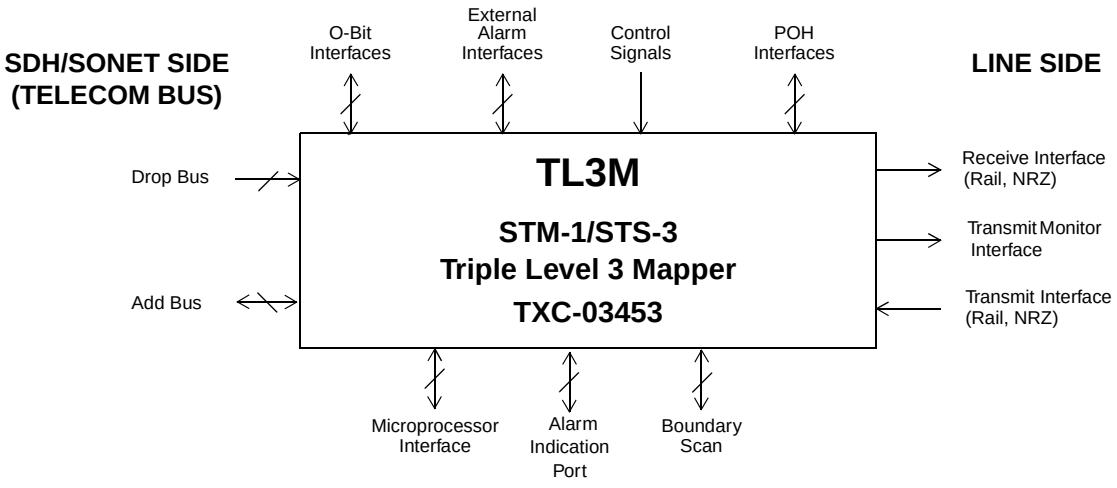
DESCRIPTION

The TL3M maps up to three independent DS3 line signals into an STM-1 TUG-3 or STS-3 STS-1 SPE SDH/SONET signal. An E3 signal is mapped into an STM-1 TUG-3. The TL3M interfaces to an STM-1 or STS-3 SDH/SONET signal using a byte-wide parallel interface in the TranSwitch Telecom Bus format. The TL3M supports drop bus and add bus SDH/SONET timing modes. Drop bus timing provides the timing signals for the add side. Timing for both buses is independent for the add bus timing mode. Individual POH bytes are mapped into a RAM interface for microprocessor access and to an external interface for external processing if required. In the add direction (except for the B3 byte) POH bytes may be inserted individually from RAM locations, from the external interface, or from the local side/alarm indication port. An option is provided to generate an unequipped channel or AIS. An external interface is provided for accessing the O-bits. An alarm indication port is provided for ring operation. The TL3M also uses internal digital desynchronizers that have a built-in pointer leak algorithm. The line side can be configured for a NRZ or positive/negative rail interface.

For testing purposes, the TL3M provides boundary scan, PRBS generators and analyzers, a BIP error mask, and DS3/E3 line and facility loopbacks. The TL3M provides either Motorola or Intel microprocessor access. The interrupt has programmable mask bits. A software polling register is also provided.

APPLICATIONS

- Add/drop multiplexers
- Digital cross connect systems
- Broadband switching systems
- Transmission equipment



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* Please note that TranSwitch provides documentation for all of its products. Current editions of many documents are available from the Products page of the TranSwitch Web site at www.transwitch.com. Customers who are using a TranSwitch Product, or planning to do so, should register with the TranSwitch Marketing Department to receive relevant updated and supplemental documentation as it is issued. They should also contact the Applications Engineering Department to ensure that they are provided with the latest available information about the product, especially before undertaking development of new designs incorporating the product.

LIST OF FIGURES

FEATURES

The TL3M supports the following features. Please note that the convention used here is that the transmit (or add) direction is from the DS3/E3 line signal (rail or NRZ) to the SDH/SONET format, while the receive (or drop) direction is from the SDH/SONET format to the DS3/E3 line.

Bus Timing (Telecom Bus):

The TL3M provides the following bus timing modes for the Telecom Bus modes of operation:

- Drop bus timing
  - Add bus timing is derived from the drop bus
    - Drop bus: C1J1, SPE, optional C1, data, clock, and parity signals leads are inputs
    - Add bus: data, parity, and add indication signal leads are outputs
- Add bus timing
  - Add bus timing is independent of the drop bus
    - Drop bus: C1J1, SPE, clock, optional C1, data, and parity, are drop bus signal lead inputs
    - Add bus: clock, C1J1, and SPE signals are inputs; data, parity, and add indication signal leads are outputs

Mappings:

The TL3M provides the following mapping features:

- Maximum of three channels for either E3 or DS3 line signals
- STM-1 AU-4 VC-4 format
  - E3 or DS3 signal into three TUG-3 formats
- STS-3 format
  - DS3 signal into three STS-1 formats
- Same drop and add bus for all channels
- Add bus Contention Indication (same channel assignment)
- Broadcast mode
  - Drop Bus: multiple channel assignment to the same TUG-3
  - Add Bus: high impedance add bus if there is contention

SDH/SONET Rates:

The TL3M provides the following Telecom Bus rates and format mappings:

- STS-3 STS-1s (19.44 Mbit/s)
- STM-1 VC-4 (19.44 Mbit/s)

Other Telecom Bus Features:

The TL3M provides the following additional bus features:

- SDH/SONET interface drop bus
  - Input parity check with alarm monitoring
    - Odd parity
    - Bus signals
  - Input loss of clock detection
    - Stuck high or low
  - Loss of J1 reference

        - Positive/negative justification count for J1 pulse
    - External path AIS and other alarm (e.g., LOP) indication
- SDH/SONET interface add bus
    - Output parity generation
        - Odd parity
    - Bus indication (active low to indicate bus activity)
    - Ability to High-Z the output bus signals
        - Under processor control
    - Input loss of clock detection
        - Stuck high or low

SDH/SONET Processing Features

- In-band upstream path AIS detection
    - TOH E1 bytes
        - Majority vote
- TUG-3 pointer tracking
    - ETSI-based state machine
        - 8-bit PJ and NJ counters
        - NDF, LOP, and AIS alarm detection
- TUG-3 pointer generation
    - Slaved to drop or add bus J1 pulse
    - Adjusts pointer accordingly
- POH byte processing (TUG-3, STS-1)
    - All receive POH bytes accessible
        - Microprocessor access
        - POH interface
    - J1 byte
        - 64-byte host processor read
    - B3 parity error check
        - Bit or block count
    - G1 byte
        - Single-bit RDI alarm detection with a 5 or 10 event option
        - REI (FEBE) counter (16 bits)
    - C2 byte
        - Signal label mismatch and unequipped detection
- POH byte Insertion (TUG-3, STS-1)
    - All POH bytes
        - Microprocessor access
        - POH interface
            - Control bits to determine source of input bytes
    - J1 byte
        - 64-byte message

  - G1 byte
    - Receive side or alarm indication port
      - REI (FEBE) insertion from B3 byte errors
      - Single-bit RDI insertion
  - C2 byte
    - Path label insertion
- SDH/SONET AIS generation
  - TUG-3s
- Unequipped channel generation
  - TUG-3s
- Desynchronizer
  - Meets ETSI and ANSI performance requirements
    - Pointer test sequence
    - Jitter
  - Internal
    - Digital
    - Internal pointer leak algorithm or microprocessor control

O-Bit (Overhead Communications) Channel Access:

- Microprocessor access (two-bit field)
- Option for two reserved bits in the E3 format
- External serial bit interface (clock and data)
  - Gapped clock
  - Asynchronous

Line AIS Detection:

  - Transmit E3 AIS detection per ITU G.775

Line AIS Generation:

- Transmit and receive sides
- Generate as a result SDH/SONET alarms or line level alarms
  - Mask enable bits
  - Global enable bit
  - Microprocessor control

Line Interface:

- Rail interface
  - Clock, positive and negative rail signals
  - DS3/E3 loss of signal detection in transmit direction
  - BPV counter
  - DS3 B3ZS or E3 HDB3 CODEC function
  - Loss of clock detector
  - Invert clock polarity

- NRZ interface
  - Clock and data
  - Loss of Clock Detector
  - External interface for loss of signal (transmit direction)
  - Invert clock polarity (receive and transmit)
- High-Z receive output leads (quiet mode)
  - Per channel control via host
- Transmit Monitor Port
  - Clock and data

Test Features:

- Boundary Scan that meets IEEE 1149.1 standard (with MEMBIST test instruction for internal RAM)
- High-Z all output leads option
- Loopbacks per channel
  - DS3/E3 line with generate receive AIS output option
  - DS3/E3 facility
- Pseudo-random test generator and analyzer per channel
  - 2^{15}-1, or 2^{23}-1.
  - Uses CV counter to count errors
- B3 BIP-8 error mask
  - RAM value substituted
  - Column error control

Microprocessor Interface:

- Microprocessor
  - Split address/data buses
  - Selectable Intel or Motorola

Alarms And Interrupts:

- Hardware interrupt option
  - Mask bits
  - Positive level
- Software polling bit
- Latched and unlatched alarms
- Saturating or rollover counters option

APPLICATION EXAMPLES

The TL3M can be used in a wide range of telecommunications applications, such as:

- Add/drop multiplexers
- Digital cross connect systems
- Router systems
- Transmission systems

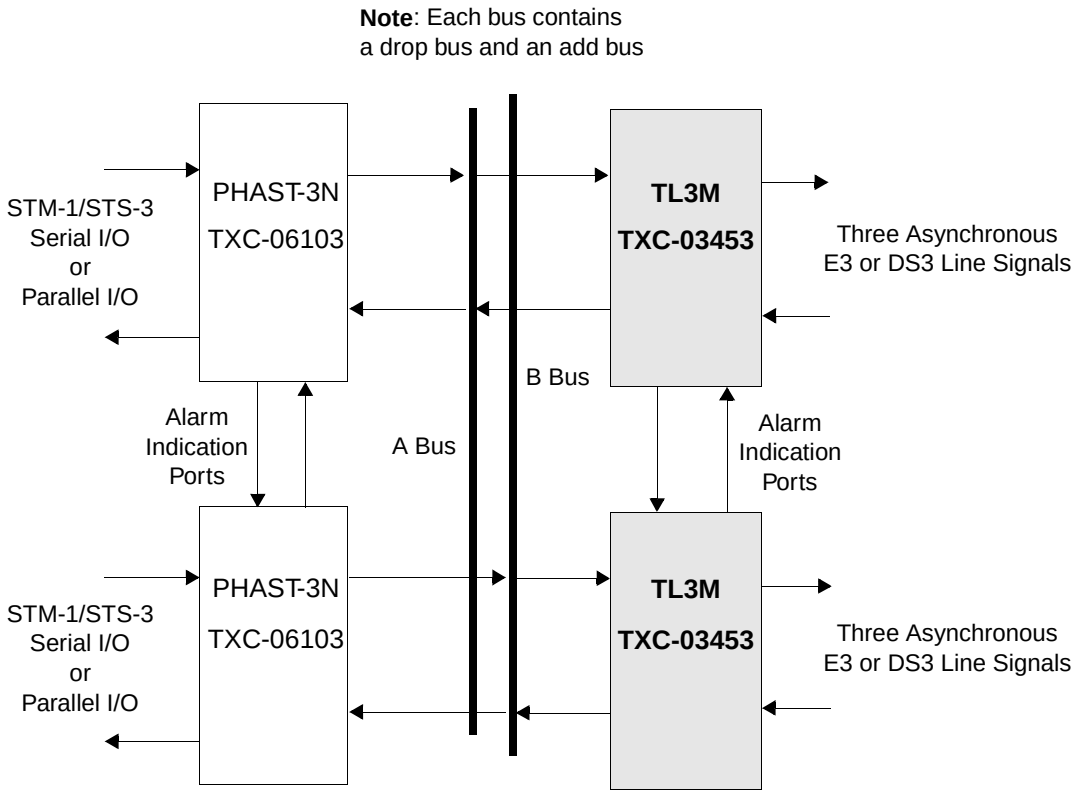


Figure 1. Typical Application using the TL3M and PHAST-3N Devices

Figure 1 shows a Telecom Bus bidirectional E3/DS3 add/drop STM-1/STS-3 multiplexer. The three E3s or DS3s may be dropped from either direction with full time slot reuse in both directions. If required, the asynchronous line interfaces for the two TL3M devices may be tied together. An option is provided in which the output line interface can be forced to the high impedance state.

PRODUCT PREVIEW

FUNCTIONAL DESCRIPTION

The block diagram of the TL3M is shown in Figure 2 below:

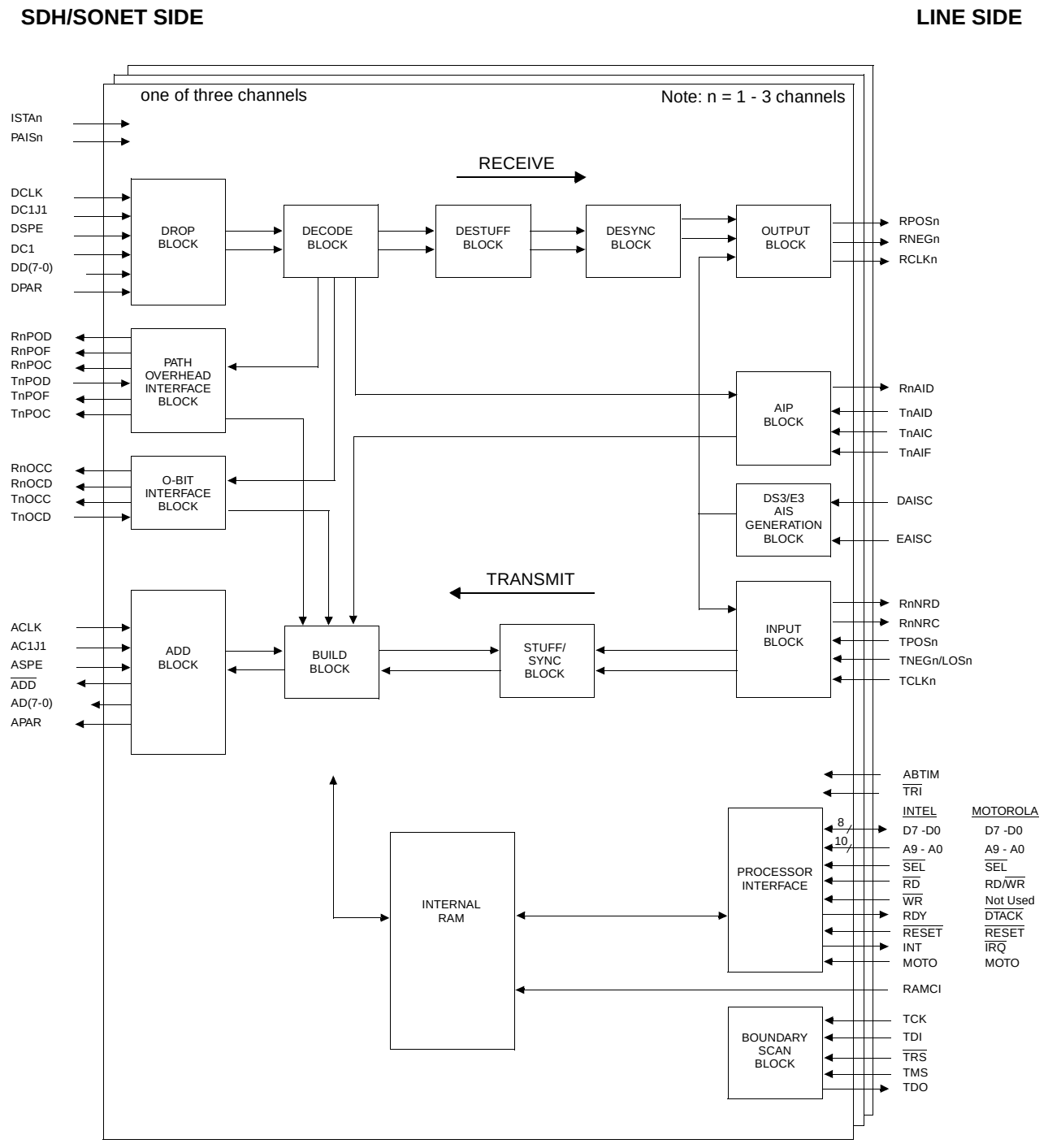


Figure 2. TL3M TXC-03453 Block Diagram

The drop side parallel Telecom Bus interface uses a bus signaling rate of 19.44 MHz. The parallel interface consists of byte-wide input data (DD(7-0)), a C1J1 input indication (DC1J1), an SPE input indication (DSPE), input clock (DCLK), and input parity (DPAR). The C1 (J0) pulse, which is required, is used in conjunction with an active low SPE indication to determine the start of the SDH/SONET frame. The J1 pulse (in the DC1J1 signal) and an active high SPE indication determine the starting location of the VC-4 within the STM-1 format and also the start of each of the STS-1s in the STS-3 format. There are three J1 pulses required for the STS-3 format, and a single J1 pulse required for the STM-1 VC-4 format. The drop bus clock (DCLK) is also monitored for a stuck high or low state. The data lead and other bus leads are calculated for odd parity and compared against the incoming input parity lead (DPAR) to determine if there is a parity error. Other than a parity indication, no action is taken by the TL3M. The C1J1 pulse is also monitored for a loss of J1 pulse. An option is provided in which the C1 pulse can be supplied on a separate lead from the DC1J1 lead.

The Decode block contains the logic for performing the pointer interpretation and tracking for each of the three TUG-3s, when the STM-1 VC-4 format is selected. The H1/H2 pointer bytes in each of the TUG-3s are monitored for loss of pointer, AIS, and a New Data Flag (NDF) indication. The pointer state machines are implemented using the algorithms specified in ETSI and ANSI documents. Performance counters are provided for justification events. The TL3M does not perform pointer tracking for the STS-1 signals, or for the VC-4 formats. Instead, the J1 indication is used as the start of format indication.

This block also performs SDH/SONET E1 byte AIS detection, which may be carrying an upstream in-band AIS indication. The TranSwitch PHAST-3N and SOT-3 devices have an option to generate an in-band line/path AIS indication for the downstream mappers, such as the TL3M, which enables line AIS to be generated without having to perform an additional pointer AIS detection. In addition, two leads are provided for an out-of-band upstream AIS indication, using either the PAISn or ISTAn leads.

The POH bytes from the TUG-3 or the STS-1 formats are provided at POH interfaces for external processing, if required. Each of the three mappers' POH interfaces consists of an output data lead (RnPOD), framing pulse (RnPOF) and a clock signal (RnPOC), where n represents each of three level 3 mappers, starting with channel 1. All the POH bytes in each of the STS-1s and TUG-3s are supplied, including the B3 byte.

All POH bytes from each of the TUG-3s or STS-1s are also written into RAM segments for microprocessor access. In addition, the J1 byte is written into a 64-byte RAM segment on an arbitrary address rotating basis. Each mapper section also performs POH byte processing, which includes RDI detection, C2 mismatch detection and unequipped detection.

The received O-bits for the DS-3 format are provided at an external interface and are also written into a 2-bit RAM location for a microprocessor read cycle. Two reserved bits in the E3 format have been designated as an O-bit channel if required. The bits in the RAM location are updated each frame by the TL3M. There is no synchronous relationship between the SDH/SONET frame and the bits written into these RAM locations. The external interface consists of a serial data lead (RnOCD) and a clock lead (RnOCC).

An alarm indication port is provided for ring configurations. The alarm indication port consists of a data lead (RnAID), which is used with the corresponding POH interface framing pulse (RnPOF) and clock signal (RnPOC). The information on the data lead consists of the REI count and the path RDI alarm summary status. In a ring configuration, this information is inserted from the mate Mapper into the local Mapper G1 byte for transmission.

The Destuff block works in conjunction with the Desync block to remove the stuff columns in the payloads, and also performs the majority logic voting for the DS3 and E3 formats. The majority voting logic uses the justification control bits to determine if the S-bit or bits is carrying a stuffing state or data.

The Desync block, using a digital desynchronizer, is responsible for removing the effects on the output of the DS3 or E3 signals of systemic jitter due to signal mapping and pointer movements. Each of the three desynchronizers has a built-in TranSwitch proprietary pointer leak algorithm, which is transparent to the user. An option is provided in which the pointer leak rate can be programmed by the host processor. The output has an average frequency equal to the source frequency and has jitter characteristics that meet both ITU and ANSI standards.

A line DS3/E3 AIS generator is provided, which enables line AIS to be generated for the various upstream alarms, such as loss of pointer. A control bit is also provided which enables the microprocessor to send line AIS independent of the alarm states. An option is provided which enables line AIS to be generated when a channel is placed in line loopback.

The Output block provides either a positive (RPOSn) and negative (RNEGn) rail line signal or an NRZ line signal (RPOSn) and a clock signal (RCLKn). The receive E3 HDB3 and DS3 B3ZS coder operates independent of the transmitter side. A control bit is provided for inverting the clock output, if required. Also provided is a control bit which enables the receive data and clock leads to be forced to a high impedance state, independent of interface type (rail or NRZ) selected. This permits two interfaces from two different devices to be tied together for ring configurations.

In the transmit direction, the Input block supports either a positive (TPOSn) and negative (TNEGn) rail line signal or an NRZ line signal (TPOSn) and a clock signal (TCLKn). A control bit enables the transmit input clock to be inverted. The Input block performs either the E3 HDB3 or DS3 B3ZS decoder function. Bipolar violations are counted in a 16-bit counter. A choice of bipolar violation sequence detection is also provided. The rail interface also detects an E3 or DS3 loss of signal. The input clock is also monitored for a stuck high or low condition. When the NRZ interface is selected, the unused negative rail input lead can be used to clock in an external loss of signal (LOS) indication from a downstream codec.

Control bits are provided which enable line AIS to be sent when either a loss of signal or input clock failure is detected. A control bit also enables the microprocessor to send line AIS, independent of alarms. Separate NRZ data (RnNRD) and clock (RnNRC) output signals are also provided which may be used for monitoring.

The line signal is connected to the Stuff/Sync block. This block basically consists of a FIFO in which the data is written into the FIFO from the line and is read out by a SDH/SONET clock which is either derived from the add bus (i.e., add bus timing), or by the drop bus (i.e., drop bus timing). The stuffing algorithm for the DS3 signal uses one set of five control bits (C-bits) with one stuffing opportunity bit (S-bit) for frequency justification per subframe (nine subframes). The E3 format uses five pairs of control bits (C1 and C2 bits) to control two stuff opportunity bits (S1 and S2) per subframe (one subframe per three rows for a total of three subframes per frame). A FIFO underflow and overflow alarm indication is provided. Should an underflow or overflow condition occur, the FIFO will immediately reset to a preset value. The FIFO also tracks an incoming line signal having an average frequency deviation as high as ± 20 ppm, and can simultaneously accept the signal with up to 5 UI peak-to-peak jitter (where 1 UI = 1/f).

The Build block formats the data bits into either a SONET STS-3 STS-1 format or an STM-1 VC-4 TUG-3 format. The STS-1 format has two stuff columns and payload plus a column of POH bytes, while the TUG-3 format consists of the payload, plus a column of POH bytes and H1/H2 pointer bytes. The TUG-3 pointer bytes define the start of the J1 POH byte within the TUG-3. A fixed pointer value of 6800 hex is used as the initial value when building a TUG-3 format. There are two levels of pointer movements in the TUG-3 build process. When there is drop or add timing, the transmit pointer value will increment or decrement when there is an STM-1 VC-4 increment or decrement based on the relative position of the J1 pulse in the C1J1. The pointer movement for the TUG-3s will be in the opposite direction. This feature can be disabled.

An O-bit interface value or a value written into RAM by the microprocessor is mapped into the two O-bit positions in the DS3 format. The O-bit interface consists of an output clock signal (TnOCC) and an input data lead (TnOCD). The relationship between the O-bit channel and the SDH/SONET frame in both directions is asynchronous.

The nine individual POH bytes (except the B3 byte) can be inserted into the TUG-3 or STS-1 POH bytes from a value written to RAM by the microprocessor or from the transmit POH interface. The POH interface consists of an input data lead (TnPOD), output framing pulse (TnPOF), and an output clock signal (TnPOC), where n represents each of three level 3 mappers. A control bit enables the POH interface bytes to be written into RAM for microprocessor access when transmitted. In the case of the G1 byte, the value can also be inserted from the local receive side or from the alarm indication port. A test mask is provided for the calculated B3 byte, which permits up to eight errors to be transmitted.

For ring operation, an alarm indication port is provided. The alarm indication port consists of an input data lead (TnAID), input framing pulse (TnAIF), and input clock signal (TnAIC). The information on the data lead consists of the REI count, and the path RDI alarm summary status. In ring operation, this information is inserted into the G1 byte for transmission.

The Add block uses the add or drop timing signals. Add bus timing is enabled by placing a high on control lead ABTIM. When add bus timing is selected, the timing for two buses, add and drop, function independently of each other. When add bus timing is selected, the output add bus signals consist of byte-wide data (AD(7-0)), add indication ($\overline{\text{ADD}}$), and odd parity (APAR). The add bus input timing signals consist of a 19.44 MHz clock (ACLK), C1J1 indication (AJ1C1) and a SPE active indication (ASPE). The output add bus signals consist of byte-wide data (AD(7-0)), Add Indication ($\overline{\text{ADD}}$), and odd parity (APAR). The active add indication ($\overline{\text{ADD}}$) indicates the location of all time slots being added to the add bus. The add bus clock is also monitored for a stuck high or low state when add bus timing is selected. A bus contention alarm is provided if more then one channel is assigned to the same TUG-3 or STS-1.

Drop bus timing is enabled by placing a low on control lead ABTIM. When drop bus timing is selected, the timing for the add bus depends upon the drop bus input signals for operation. When drop bus timing is selected, the output add bus signals consist of byte wide data (AD(7-0)), add indication ($\overline{\text{ADD}}$), and odd parity (APAR).

All of the control registers and performance counters, as well as the status and alarm indications, are accessible via a microprocessor interface. The TL3M supports both Intel and Motorola microprocessor bus interfaces, with hardware and software interrupts. Mask bits are provided for the latched status and alarm indications, to control whether each of them will generate an interrupt when active. The counters may be configured as either rollover or saturating. Saturating counters are cleared automatically when they are read.

For board testing, boundary scan and the ability to force all the output signals to a high impedance state are provided. For network and device debugging, facility and line loopbacks are provided for the line interfaces. Each channel also has a PRBS test analyzer and generator.

SELECTED PARAMETER VALUES

ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

Parameter	Symbol	Min	Max	Unit	Conditions
Supply voltage	V_{DD}	-0.3	+3.9	V	Note 1
DC input voltage	V_{IN}	-0.5	+5.5	V	Note 1
Storage temperature range	T_S	-55	150	^oC	Note 1
Ambient Operating Temperature	T_A	-40	+85	^oC	0 ft/min linear airflow
Moisture Exposure Level	ME	5		Level	per EIA/JEDEC JESD22-A112-A
Relative Humidity, during assembly	RH	30	60	%	Note 2
Relative Humidity, in-circuit	RH	0	100	%	non-condensing
ESD Classification	ESD	absolute value 2000		V	Note 3

Notes:

1. Conditions exceeding the Min or Max values may cause permanent failure. Exposure to conditions near the Min or Max values for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the “CAUTION” label on the drypack bag in which devices are supplied.
3. Test method for ESD per MIL-STD-883D, Method 3015.7.

Thermal Characteristics

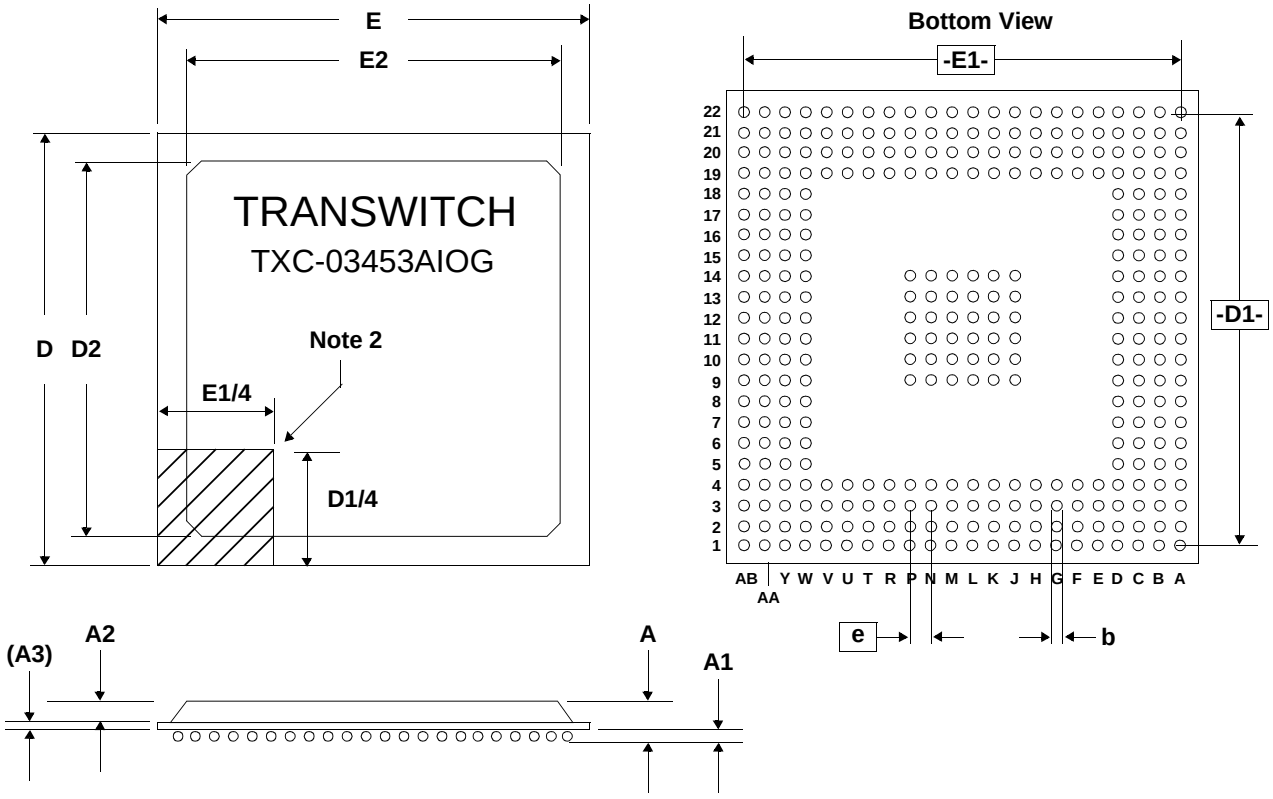
Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal resistance: junction to ambient			23	$^oC/W$	0 ft/min linear airflow

Power Requirements

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	3.15	3.30	3.45	V	
I_{DD}		346		mA	
Power Dissipation, P_{DD}		1142		mW	

PACKAGE INFORMATION

The TL3M device is packaged in a 324-lead plastic ball grid array package suitable for surface mounting, as illustrated in Figure 3.



Notes:
1. All dimensions are in millimeters. Values shown are for reference only.
2. Identification of the solder ball A1 corner is contained within this shaded zone. This package corner may be a 90° angle, or chamfered for A1 identification.
3. Size of array: 22 x 22, JEDEC code MO-151-AAJ-1.

Dimension (Note 1)	Min	Max
A	2.02	2.44
A1	0.40	0.60
A2	1.12	1.22
A3 (Ref.)	0.50	0.62
b	0.40	0.60
D	23.00	
D1 (BSC)	21.00	
D2	19.45	20.20
E	23.00	
E1 (BSC)	21.00	
E2	19.45	20.20
e (BSC)	1.00	

Figure 3. TL3M TXC-03453 Package Diagram

ORDERING INFORMATION

Part Number:	TXC-03453AIOG	324-lead plastic ball grid array package

RELATED PRODUCTS

TXC-02030, DART VLSI Device (Advanced E3/DS3 Receiver/Transmitter). DART performs the transmit and receive line interface functions required for transmission of E3 (34.368 Mbit/s) and DS3 (44.736 Mbit/s) signals across a coaxial interface.

TXC-02302B, SYN155C VLSI Device (155-Mbit/s Synchronizer, Clock and Data Output). Transmits and receives at STS-3/STM-1 rates. Provides the complete STS-3/STM-1 frame synchronization function. Connects directly to optical fiber interface components.

TXC-03001B, SOT-1 VLSI Device (SONET STS-1 Overhead Terminator). This device performs section, line and path overhead processing for STS-1 SONET signals. Has programmable STS-1 or STS-N modes.

TXC-03003B, SOT-3 VLSI Device (STM-1/STS-3/STS-3c Overhead Terminator). This device performs section, line and path overhead processing for STM-1/STS-3/STS-3c signals. Compliant with ANSI and ITU-TSS standards.

TXC-03303, M13E VLSI Device. Single-chip with extended features multiplex/demultiplex device provides the complete interfacing function between a single DS3 signal and 28 independent DS1 signals.

TXC-03305, M13X VLSI Device (DS3/DS1 Mux/Demux). This single-chip device provides the functions needed to multiplex and demultiplex 28 independent DS1 signals to and from a DS3 signal with either an M13 or C-bit frame format. It includes some enhanced features relative to the M13E device.

TXC-03452B, L3M VLSI Device (Level 3 Mapper). Maps a 44.736 Mbit/s DS3 or 34.368 Mbit/s E3 asynchronous line signal into an STM-1/STS-3/STS-1 formatted synchronous signal. Separate add/drop bus timing is available for loop multiplexers. The L3M provides the overhead processing for the mapped signal.

TXC-06103, PHAST-3N VLSI Device (SDH/SONET STM-1, STS-3 or STS-3c Overhead Terminator) This PHAST-3N VLSI device provides a Telecom Bus interface for downstream devices and operates from a power supply of 3.3 volts.

TXC-06125, XBERT VLSI Device (Bit Error Rate Generator Receiver). Programmable multi-rate test pattern generator and receiver in a single chip with serial, nibble, or byte interface capability.

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- NOTES -


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Please fold, tape and mail this page (see other side) or fax it to Marketing Communications at 203.926.9453.

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