TEMx28™ Device
21/28 Channel Dual Bus High Density Mapper
TXC-04222

TECHNICAL OVERVIEW
PRODUCT PREVIEW

FEATURES

- Add/drop 21/28 E1, DS1, or VT/TU payloads from two add and two drop STM-1/VC4, STS-3 buses
- Add bus and drop bus timing modes
- Cross mapping applications (DS1 mapped to/from VT2/TU-12s)
- Selectable HDB3/B8ZS/AMI positive/negative rail, NRZ, or VT/TU interfaces per channel
- H4 multiframe option in place of Telecom Bus V1 pulse
- Digital desynchronizer
- Drop buses are monitored for parity, loss of clock, and upstream AIS
- Performance counters for pointer movements, BIP-2 errors, REI and coding violations
- Single-bit or three-bit RDI operation per channel
- Tandem connection capability per ETSI standards
- J2 trail trace comparison option
- Processor access to H1/H2, H4 overhead bytes, and V1/V2 and V4 bytes
- Selectable positive, negative or positive/negative alarm transition interrupt options
- Line and facility loopbacks, generation of BIP-2 and REI errors, PRBS generator and analyzer per channel
- Polling registers and global summary alarm status
- One second measurements: counters and alarms
- IEEE 1149.1 standard boundary scan
- +3.3 V and 1.8 Vpower supplies, 5 V tolerant I/O leads
- 376-lead plastic ball grid array (PBGA) package (23 mm x 23 mm)

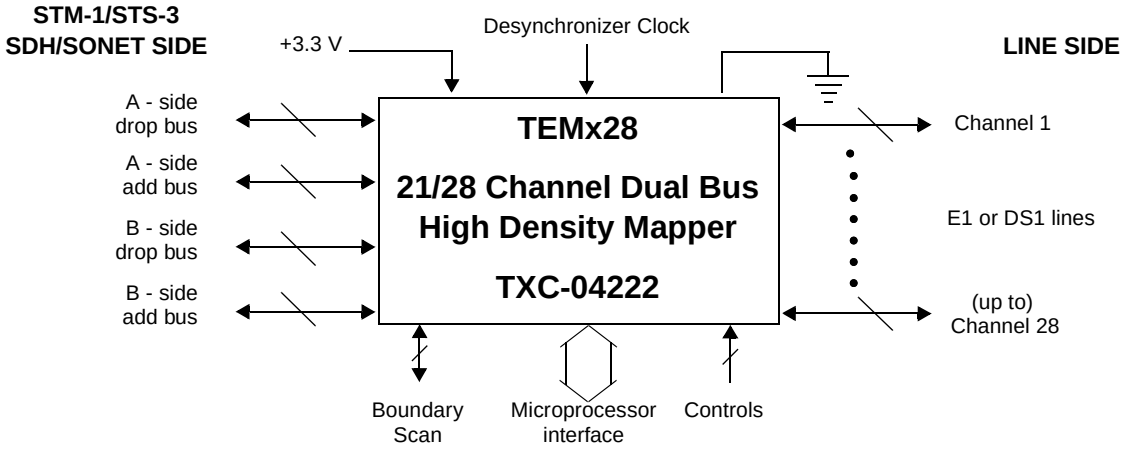
DESCRIPTION

The TEMx28™ device is designed for add/drop multiplexer, terminal multiplexer, and dual and single unidirectional ring applications. Up to 28 E1, DS1, or VT/TU payloads are mapped to and from VT1.5/TU-11s and VT2/TU-12s carried in an STM-1 VC-4 or STS-3 format. The device interfaces to a multiple-segment, byte-parallel SDH/SONET-formatted bus at the 19.44 Mbit/s byte rate. The E1 and DS1 signals can be HDB3 or B8ZS/AMI rail signals, or NRZ signals. The VT/TU interface can be provided with or without the overhead bytes for virtual concatenation applications. The TEMx28 performs pointer tracking and overhead byte processing, including single-bit or three-bit RDI operation, and optional tandem connection capability. All overhead bytes, including the V1/V2/V4 bytes, are provided for microprocessor access.

The TEMx28 can generate receive and transmit line AIS, transmit unequipped and supervisory unequipped channels, and transmit VT/TU AIS, in addition to standards-compliant overhead byte monitoring. It also provides test features and a microprocessor interface.

APPLICATIONS

- STS-3/STM-1 to 1.544 Mbit/s and 2.048 Mbit/s add/drop mux/demux
- Unidirectional or bidirectional ring applications
- STS-3/STM-1 termination terminal mode multiplexer
- STS-3/STM-1 test equipment



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LIST OF FIGURES

OVERVIEW

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The TEMx28 can generate receive and transmit line AIS, transmit unequipped and supervisory unequipped channels, and transmit VT/TU AIS, in addition to standards-compliant overhead byte monitoring.

For testing, the device provides IEEE 1149.1 boundary scan, a PRBS generator and analyzer, and both line and facility loopbacks. The TEMx28 supports split bus access for either Intel or Motorola microprocessors. Its performance counters can be configured to be either saturating or roll over. Interrupts can be generated by alarms that latch on positive, negative, or both positive and negative status transitions, and they can be disabled via mask bits. A software polling register and summary alarm bit status are also provided. One second measurements are performed for alarms and counters.

FEATURES

The following is a detailed list of features supported by the TEMx28:

- Bus Modes of operation (Each Channel)
  - Drop Mode Only
    - Drop from A or B
  - Add Mode only
    - Add to A or B
    - Add to A and B
  - Single Unidirectional Ring
    - Drop from A, Add to A
    - Drop from B, Add to B
  - Multiplexer
    - Drop from A, Add to B
    - Drop from B, Add to A
  - Dual Protection Ring
    - Drop from A, Add to A and B
    - Drop from B, Add to B and A

- Bus Timing
  - Drop Bus Timing
    - Add Bus Timing Derived from the same named Drop Bus
  - Add Bus Timing
    - Add Bus Timing is independent of the Drop Bus
  - Lead Selectable

- SONET/SDH COMBUS Interface
  - Drop Bus Timing Enabled
    - Drop Bus: C1J1V1, SPE, Byte Wide Data, Clock, Parity
    - Add Bus: Byte Wide Data, Parity, Add Indicator
      - Option: Clock, C1J1V1, and SPE are Outputs
  - Add Bus Timing Enabled
    - Drop Bus: C1J1V1, SPE, Byte Wide Data, Clock, Parity
    - Add Bus: Clock, C1J1V1, SPE are inputs; Byte Wide Data, Parity, Add Indicator are Outputs.

- Mappings
  - Maximum of 21/28 Channels
    - DS1/E1 Line Asynchronous Formats, or VC-11/VC-12s
    - Independent VT1.5/TU-11 or VT2/TU12 Selection per Channel for both Drop and Add Buses
    - Cross Mapping: DS1 mapped into VT1.5/TU-12

- SONET/SDH Operating Formats
  - STS-3 STS-1 (19.44 Mbit/s)
  - STM-1 VC-4/TUG-3/TUG-2 (19.44 Mbit/s)
  - STM-1 AU-3s (19.44 Mbit/s)

- Other Bus Features
  - Drop Buses
    - Input Parity Check with Alarm Indication
      - Odd, or Even
      - Data Only, or Bus Signals
    - Input Loss Of Clock Detection
      - Stuck High or Low
  - Add Buses
    - Output Parity Generation
      - Odd, or Even
      - Data Only, or Bus Signals
    - Add to Bus Indicator
    - High Z Output Bus Signals Control
    - Individual Channel High Z VT/TU Time Slots

- SONET/SDH Features
  - In-band upstream AIS Detection
    - H1/H2 Pointer Bytes
    - E1 Bytes using Majority Voting
  - H4 Byte Multiframe Detectors or V1 pulse (C1J1V1) reference input
    - Determines Location of V1/V2 Pointer Bytes
  - Pointer Tracking
    - ETSI/ITU/ANSI State Machine
    - Wrong Size Bits Detection
    - Positive/Negative Justification and NDF 8-bit Counters
  - Microprocessor Access to
    - V1/V2 Pointer Bytes (Each Channel)
    - H4 POH Bytes (Both Buses, VC-4 or Three STS-1s)
    - E1 (used for Upstream AIS Indication) Bytes (Both Buses, VC-4 or Three STS-1s)
    - H1/H2 Pointer Bytes (Both Buses, VC-4 or Three STS-1s)

- VT/TU Overhead Byte Processing
  - J2 Byte
    - 64 Byte Read Segment with Optional CR/LF Alignment
    - 16 Byte Read Segment with Optional Trail Trace Message Comparison
  - V5/K4 Byte
    - Three Bit or Single Bit RDI (Programmable for Each Channel)
      - Detection/Recovery Selection: 5 or 10 event Option
    - REI Error Counter
    - RFI Detector
    - BIP-2 Bit/Block Error Counter Option
    - Signal Label Mismatch, Unequipped, and VC AIS detection
      - Detection/Recovery: 5 events
  - N2 Byte
    - Tandem Connection Option
    - Trail Trace Message Comparison against Microprocessor Written Message

- Overhead Byte Access
  - Both A and B Buses

- Desynchronizer
  - Meets ANSI/ETSI/ITU Requirements
    - Pointer Test Sequences
    - Jitter/MTIE
  - External Clock (Common to Both Rates)
  - Leak Rate Control
    - Microprocessor Control - 10 Bits

- Line AIS (DS1/E1) Generation
  - Mask Bits for Individual Alarms
  - Global Mask Bit for all Alarms
  - Microprocessor Control

- VT/TU Overhead Byte Insertion (per Channel)
  - J2 Byte
    - 64 or 16 byte Microprocessor Written Message
    - J2 Forced to 0 Option
  - V5/K4 Byte
    - REI Insertion (from Drop Side VT/TU)
    - RFI Value from Microprocessor
    - BIP-2 Calculation and Insertion
    - RDI Insertion
      - Single or Three Bit
    - RDI Generated for a Minimum of 20 Multiframes
      - Mask bits for Alarms
      - Global Mask Bit for all Alarms
      - Microprocessor Control
  - K4 Byte
    - Input Bits 1 and 2 from External VT/TU interface
  - N2 Byte
    - Tandem Connection Option
      - 16 Mbyte Message Insertion
      - Mask Alarm Bits or Microprocessor for TC ODI and RDI Generation
      - Internal Multiframe Generation
      - TC AIS Generation
      - TC Unequipped Generation

- Overhead Single Byte Insertion
  - All Bytes
  - Test purpose

- Unequipped Generation (per Channel)
  - Supervisory Unequipped Generation Option
- Transmit AIS Generation

- TU/VT AIS
  - Microprocessor Control
- DS1 or E1 AIS
  - Alarms with mask Bits
  - Microprocessor Control

- O-bit Access
  - Drop and Add both A and B Buses

- Line Interface
  - NRZ
    - External Loss Of Signal or Coding Violation Input
  - Rail
    - CODEC
      - AMI/B8ZS/HDB3
      - Coding Violation Counter
    - Loss Of Signal Detector
  - VT/TU Interface
    - Add Bus Timing Mode Only
    - Fixed C1J1 Locations in Add Direction
    - Two Modes: With or Without (Gapped Clock) Overhead Bytes
    - Transmit Direction: Fixed Framing References and Clock Outputs, Data in
      - Bits 1 and 2 in K4 byte clocked in with data for symmetrical clock

- Microprocessor Interface
  - Intel or Motorola Split Bus
    - LDS lead Option (683XX Processors)
    - READY/$\overline{\text{DTACK}}$ Leads
    - Interrupt Structure
  - Positive, Negative, Positive/Negative Alarm Transitions
  - Polling Registers with Mask Bits
    - Alarm Summary Bits with Mask Bits
    - One Second Measurements
  - Counters
    - Roll Over or Saturating
    - One Second Measurements
- Test features
  - Boundary Scan
  - DS-1/E1 loopbacks
    - Facility
    - Line
- High Z all Leads (except Boundary Scan Output)
- PRBS Generator and Analyzer
  - 2^{15}-1 as defined in O.151 and T1M1.3/92-006R3 or QRSS (2^{20}-1) as defined in ANSI T1.403-1195)
  - Drop or Add Direction Placement
- Single Bit Error Generation for Transmit REI and BIP-2

APPLICATION EXAMPLE

The application diagram in Figure 1 below shows a fully configured bidirectional add/drop fiber multiplexer. Using the four-bus capability of the TEMx28, channels may be dropped from either direction with full time slot reuse in both directions. Using only the B Drop and the A Add buses provides add/drop service back to the network source only, and eliminates the block marked “East Terminal” for a terminal configuration.

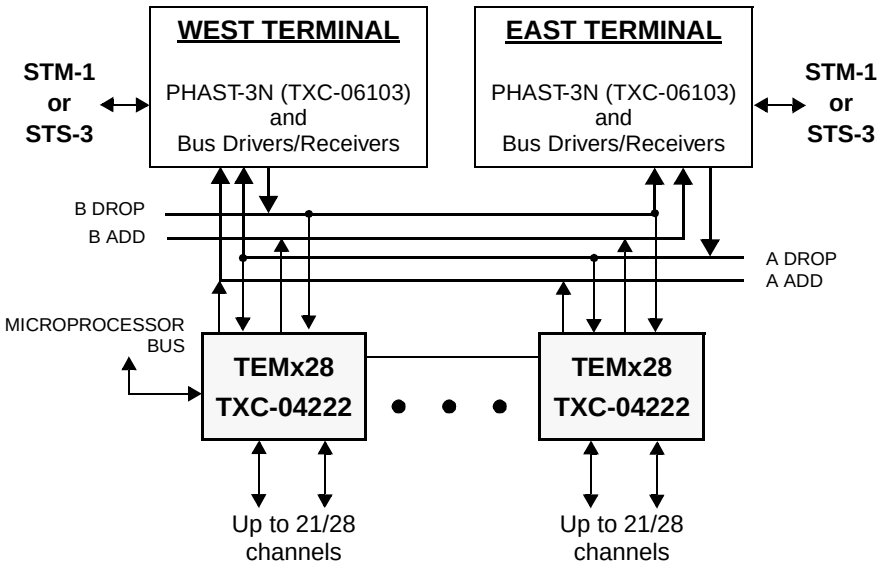


Figure 1. Application Using the TEMx28 TXC-04222

INTEROPERABILITY

The TEMx28 works directly with the following TranSwitch devices:

- QT1F-*Plus* (TXC-03103)
- T1Fx8 (TXC-03108)
- E1Fx8 (TXC-03109)
- QE1F-*Plus* (TXC-03114)
- PHAST-3N (TXC-06103)

PRODUCT PREVIEW

FUNCTIONAL DESCRIPTION

A block diagram of the TEMx28 device is shown in Figure 2. Further information on device operation and the interfaces to external circuits is provided in the following paragraphs.

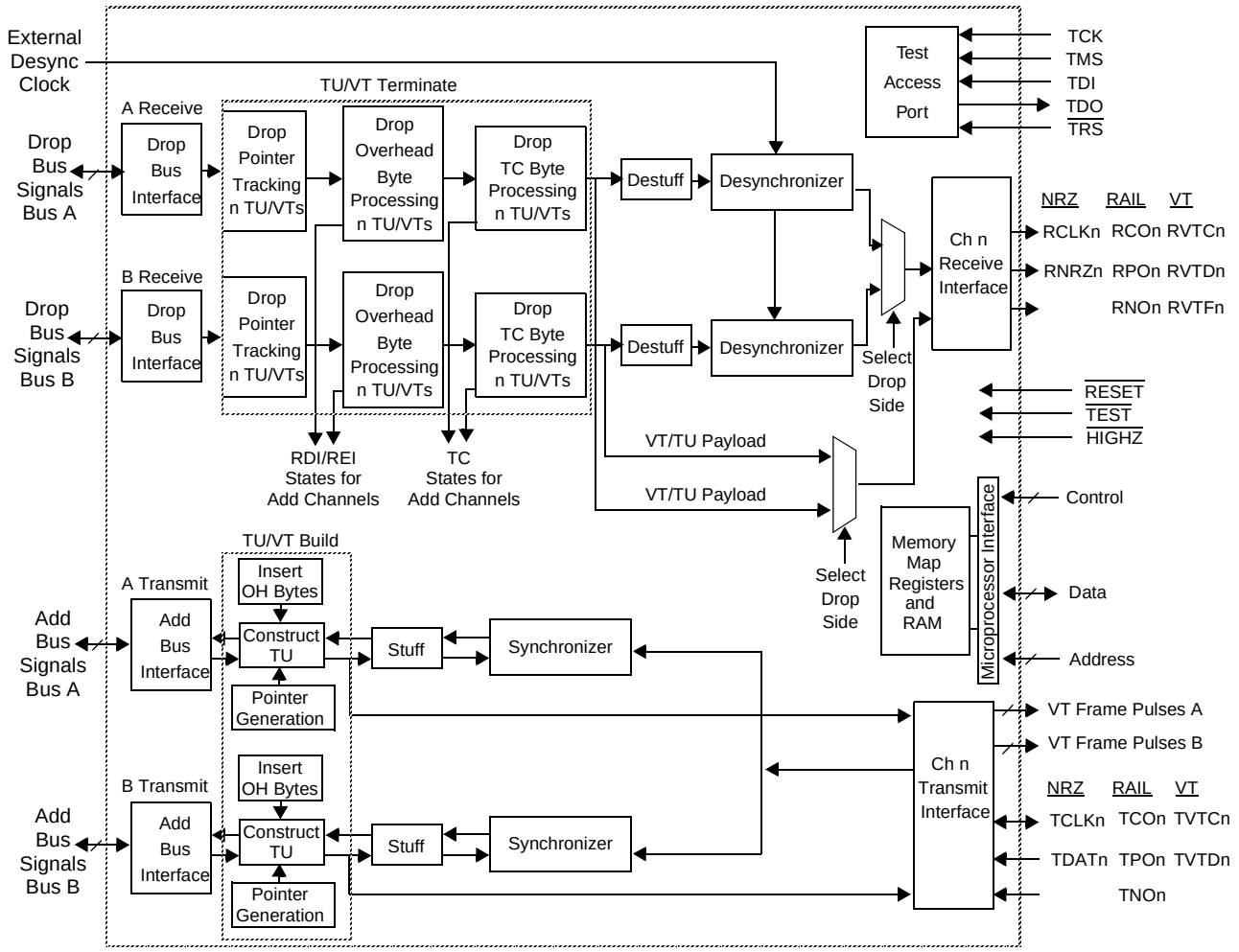


Figure 2. TEMx28 TXC-04222 Block Diagram

As illustrated in Figure 2, the TEMx28 interfaces to four buses, designated as A Drop, B Drop, A Add, and B Add. The four buses run at the STM-1/STS-3 rate of 19.44 Mbyte/s. For North American applications, asynchronous DS1 signals are carried in a floating Virtual Tributary 1.5 (VT1.5) format, while E1 signals are carried in a floating Virtual Tributary 2 (VT2) format. A maximum of 28 VT1.5 and 21 VT2 signals are carried in a Synchronous Transport Signal - 1 (STS-1) format. Three STS-1s are in turn carried in a STS-3 signal. For ITU-T applications, asynchronous E1 signals are carried in floating mode Tributary Unit - 12 (TU-12) format and

DS1 signals are carried in floating mode Tributary Unit - 11 (TU-11) format. The TU-12s and TU-11s are carried in an STM-1 Virtual Container - 4 (VC-4) structure using Tributary Unit Group - 3 (TUG-3), or in the STM-1 Virtual Container - 3 (VC-3) structure using Tributary Unit Group - 2 (TUG-2) mapping schemes. Up to 28 DS1 or 21 E1 signals, or a combination of DS1 and E1 signals, can be dropped from one bus (A Drop or B Drop) to the DS1 or E1 lines. A maximum of 28 asynchronous DS1 or 21 asynchronous E1 signals are converted into TU-1.5/TU-12 or VT1.5/VT2 format and are added to either of the add buses, or both, depending upon the mode of operation.

The TEMx28 can provide, on a per channel basis, the Virtual Container - 11 (VC-11), or the E1 Virtual Container - 12 (VC-12) formats in place of the DS1 or E1 signals for Virtual Concatenation applications. The VC format contains the payload and overhead bytes associated with the TU-11 and TU-12 formats.

The TEMx28 also supports the cross mapping feature specified in ITU Recommendation G707. This feature enables a DS1 asynchronous line signal to be carried in a TU-12/VT2 payload. This feature is supported in the TEMx28 on a per channel basis.

When the TEMx28 is configured for drop bus timing, the add buses are, by definition, byte- and multiframe-synchronous with their like-named drop buses, but are delayed by one or two byte times because of internal processing. For example, if a byte in the STM-1 Virtual Container - 4 (VC-4) structure using Tributary Unit Group - 3 (TUG-3), TU-12/VT2 is to be added to the A Add bus, the time of its placement on the bus is derived from the A Drop bus timing, and from software instructions specifying which TU/VT number is being dropped/added. The TU/VT A and B drop bus selection can be different. An option is provided which enables the dropped timing signals to be sent as outputs on the add bus. When the device is configured for add bus timing, the add bus, parity, and add indicator signals are derived from the input add bus clock, C1J1V1 and SPE signals.

In the drop (receive) direction, the A Receive Drop Bus Interface block is identical to the B Receive block. The TU/VT Terminate block, Destuff block and Desychronizer block are repeated 56 times, 28 for each side (A and B sides). The Channel n Receive Interface blocks are repeated 28 times, one for each channel. The interface between a drop bus and the receive block consists of 12 input leads: a 19.44 MHz byte clock, byte-wide data, a C1J1 indicator which may be also carrying a V1 indication making the signal a C1J1V1 indicator, an SPE indicator, and an odd/even parity bit. The Drop C1J1V1 signal is used in conjunction with the Drop SPE signal to determine the location of the various bytes in the SONET/SDH format. The C1 pulse identifies the location of the C1 byte when the SPE signal is low. A single J1 pulse identifies the starting location of the J1 byte in the VC-4 format, when the SPE signal is high. Three J1 pulses are provided for the STS-3 format, each identifying the starting location of the J1 byte in each of the three STS-1 signals.

The TEMx28 can function with either a V1 pulse in the C1J1V1 signal, or it can use an internal H4 detector for determining the location of the V1 pulse. The V1 pulse location is used to determine the location of the pointer bytes V1 and V2. For STM-1 VC-4 operation, if the C1J1V1 signal is used, a single V1 pulse must occur during three drop bus clock cycles every four frames following the J1 pulse when the SPE signal is high. For STS-3 operation, three V1 pulses must be present every four frames. Each of the three V1 pulses must be present three clock cycles after the corresponding J1 pulse, when the SPE signal is high. For example, in a VC-4 signal, the J1 pulse identifies the J1 byte location (defined as the starting location for the VC-4) in the POH bytes. In the next column (first clock cycle) all the rows are assigned as fixed stuff. Similarly, in the next column (second clock cycle) all the rows are assigned as fixed stuff. The next column (third clock cycle) defines the start of TUG-3 A. This column is where the V1 pulse occurs every four frames. However, the actual V1 byte location is six clock cycles after the V1 pulse.

Each drop bus (A and B) is monitored for parity errors, loss of clock, H4 multiframe alignment if selected, and an upstream SDH/SONET AIS indication. The TEMx28 can monitor either the TOH E1 order wire bytes or the H1/H2 bytes for an upstream AIS indication.

Each TU/VT Terminate block (A and B side) performs pointer processing based on the location of the V1 and V2 bytes. The pointer bytes are monitored for loss of pointer, Alarm Indication Signal (AIS), and a New Data Flag (NDF). The pointer tracking process is based on ETSI/ITU-T standards, which also meets ANSI

requirements. Pointer increments and decrements are also counted, and the size bits are monitored for the correct value. This block also processes and monitors the various alarms found in the four overhead bytes. These operations including signal label mismatch detection, unequipped status detection, BIP-2 parity error detection and error counter, REI error counting, and single-bit or three-bit Remote Defect Indications (RDI). The TEMx28 performs a 16-byte J2 trail trace comparison on the channels selected. For 64-byte messages, the bytes are stored in a memory map segment for a microprocessor read cycle. The device also provides the TU tandem connection feature and performs the 16-byte message comparison for the N2 (formerly known as Z6) byte message.

All VT/TU overhead bytes, eight overhead communications channel bits (O-bits), the V1/V2 pointer bytes, and the V4 byte for each channel are available for a microprocessor read cycle. Also, the E1 order wire bytes, the H1/H2 pointer bytes, and the H4 bytes from the upstream circuitry are also available for a microprocessor read cycle.

A control bit for each port selects the TU/VT from either the A Drop or B Drop bus. The TU/VT is destuffed in the Destuff block using majority logic rules for the three sets of three justification control bits to determine if the two S-bits are data bits or frequency justification bits.

The Desynchronizer block removes the effects on the DS1 or E1 output of systemic jitter that might occur because of signal mappings and pointer movements in the network. The Desynchronizer block contains two parts, a pointer leak buffer, and a loop buffer. The pointer leak buffer can accept up to five consecutive pointer movements, and can adjust the effect over time. The Loop Buffer consists of a digital loop filter, which is designed to track the frequency of the received signal and to remove both transmission and stuffing jitter.

The Channel n Receive Interface block of each channel provides either NRZ data, positive and negative rail signal, or a VT/TU interface. Receive data (towards the line), for each of the channels, can be clocked out on either rising or falling edges of the clock. In addition, a control bit is provided for forcing the data and clock signals to a high impedance state (tristate), or to the zero state.

In the add (transmit) direction, the TEMx28 accepts a clock and either NRZ data or positive and negative rail signals. Data, for each of the channels, can be clocked in on either the falling or rising edge of the clock. In the NRZ mode, an external loss of clock indication or external coding violations can be provided. For the rail signal, coding violations are counted, and there is a loss of signal detector. A DS1/E1 AIS detector is also provided.

Each channel can also be configured for VT/TU interface for Virtual Concatenation data applications. When this interface is selected, a clock signal is provided for strobing in data for either the A or B bus. Four framing pulses are also provided which define the starting location of the VT1.5/TU-11 and VT2/TU-12. An option is provided for including the four overhead bytes. However, except for bits 1 and 2 in the K4 bytes, the other bits are ignored. Bits 1 and 2 in the K4 byte carry an extended signal label and information pertaining to the payload position within the Virtual Concatenation channel. The Virtual Concatenation channel will be assigned to n VT/TUs based on the data bandwidth required for the application.

For a NRZ or positive/negative rail transmit interface, the line signal is written into two FIFOs, one for add A side and the other for the B side, in one of the two Stuff/Synchronizer block pairs. Threshold modulation is used for the frequency justification process. Timing information from the A and B drop buses or from the A and B add buses is used to read the FIFO and perform the TU/VT justification process. The Synchronizer block permits tracking of an incoming signal having an average frequency offset as high as 120 ppm, and up to 1.5 UI of peak-to-peak jitter. Since the TEMx28 supports two different network architectures (DS1 and E1), two sets of blocks are provided for each channel. The TU/VT A and B add bus selection can be different. The VT/TU add bus selection can be different from the drop VT/TU selection. A control bit, and transmit line alarms, can also generate DS1/E1 AIS.

The TU/VT Build blocks format the TU/VT into an STS-3 or STM-1 structure for the asynchronous DS1 or E1 signals. The pointer value carried in the V1 and V2 bytes is transmitted with a fixed value of 78 for the VT1.5/TU-11 and 105 for the VT2/TU-12. Transmit access is provided for the eight overhead communications channel bits (O-bits) via the microprocessor. The microprocessor also writes the signal label, and the value of

the J2 message, either as a 16-byte or a 64-byte message. The TEMx28 provides the TU tandem connection feature for the TU-11 or TU-12, including the transmission of the 16-byte message and the various alarms associated with the tandem connection feature. The device provides either single-bit or three-bit RDI using the V5 and K4 bytes. Local alarms, or the microprocessor, can generate the remote payload, server, or connectivity defect indications. The Remote Error Indication (REI) is inserted from the BIP-2 errors detected on the receive side, and BIP-2 parity is generated for the V5 byte. Control bits are provided for generating unequipped status, generating TU/VT AIS, and inserting REI and BIP-2 errors in the V5 byte. Control bits are also provided that enable the microprocessor to insert overhead byte test values, including the V1/V2 pointer bytes and the V4 byte.

The A Transmit block is identical to the B Transmit block. The interface between an add bus and a Transmit block consists of three input leads and ten output leads, when the add bus timing mode is selected. The input leads are a byte clock, a C1J1V1 indicator, and an SPE indicator. The output leads are byte-wide data, and a parity indicator, and an add-to-bus indicator signal. The Add C1J1V1 signal is used in conjunction with the Add SPE signal to determine the location of the various bytes in the SONET/SDH format.

When drop bus timing is selected, the output leads are byte-wide data, a parity indicator, and an add-to-bus indicator. The add bus clock, SPE and C1J1V1 signals, which are derived from the drop bus, can disabled or provided. The selection is performed by a lead.

The Microprocessor Input/Output Interface block consists of an Intel- or Motorola-compatible split address/data bus interface that provides access to assigned TEMx28 memory map addresses. Interrupt capability, interrupt mask bits, alarm summary bits, and software polling bits are also provided. The alarms that cause the interrupt can be set on positive, negative, or both positive and negative transitions.

Control bits are provided which enable a facility or a line loopback. In addition, a PRBS analyzer and generator are provided. A 2^{15}-1 or 2^{20}-1 PRBS pattern is supported. The analyzer and generator can be used in the drop or add line direction for additional testing flexibility.

The Test Access Port (TAP) block provides a five-lead Boundary Scan capability that conforms to the IEEE 1149.1 standard. This standard provides external boundary scan functions to read and write the external Input/Output leads from the TAP for board and component test.

SELECTED PARAMETER VALUES

ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

Parameter	Symbol	Min	Max	Unit	Conditions
Core Supply Voltage, +1.8V nominal	V_{DD2}	-0.3	2.1	V	Notes 1, 4
I/O Supply Voltage, +3.3V nominal	V_{DD1}	-0.3	3.9		Notes 1, 4
DC input voltage	VIN	-0.5	5.5	V	Notes 1, 4
Storage temperature range	T_S	-55	150	°C	Note 1
Ambient operating temperature	T_A	-40	85	°C	0 ft/min. linear airflow
Moisture Exposure Level	ME	5		Level	per EIA/JEDEC JESD22-A112-A
Relative humidity, during assembly	RH	30	60	%	Note 2
Relative humidity, in-circuit	RH	0	100	%	non-condensing
ESD Classification	ESD	absolute value 2000		V	Note 3
Latch-up	LU				Meets JEDEC STD-78

Notes:

1. Conditions exceeding the Min or Max values may cause permanent failure. Exposure to conditions near the Min or Max values for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the "CAUTION" label on the drypack bag in which devices are supplied.
3. Test method for ESD per MIL-STD-883D, Method 3015.7.
4. Device core is 1.8V only.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal resistance - junction to ambient		22		^{o}C/W	0 ft/min linear airflow

POWER REQUIREMENTS

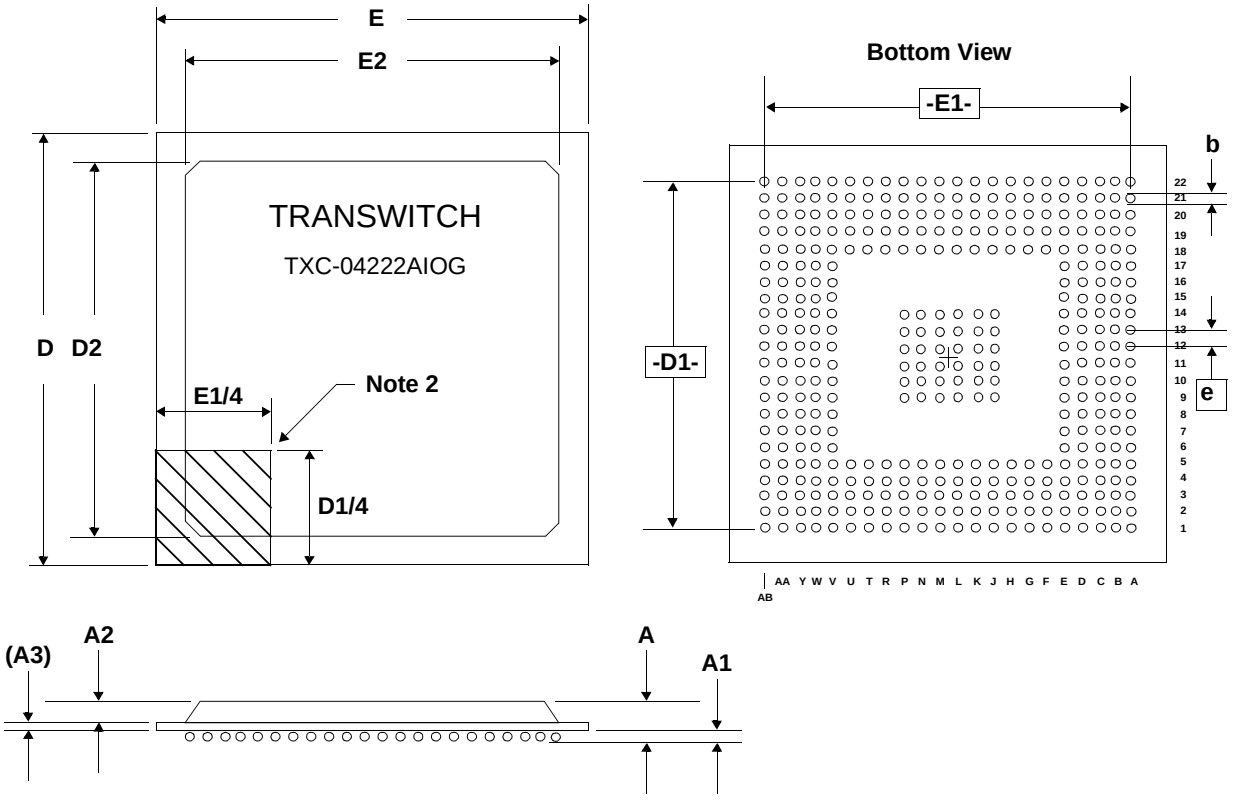
Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD1}	3.15	3.3	3.45	V	
I_{DD1}			TBD	mA	See Notes 1 and 2
P_{DD1}			TBD	W	See Notes 1 and 2
V_{DD2}	1.71	1.8	1.89	V	
I_{DD2}			TBD	mA	See Notes 1 and 2
P_{DD2}			TBD	W	See Notes 1 and 2

Notes:

1. Typical values are based on measurements made with nominal voltages at 25° C.
2. All I_{DD} and P_{DD} values are dependent upon V_{DD}.

PACKAGE INFORMATION

The TEMx28 device is packaged in a 376-lead plastic ball grid array (PBGA) package suitable for surface mounting, as illustrated in Figure 3.



Notes:
1. All dimensions are in millimeters. Values shown are for reference only.
2. Identification of the solder ball A1 corner is contained within this shaded zone. Package corner may not be a 90° angle.
3. Size of array: 22 x 22, JEDEC code MO-151.

Dimension (Note 1)	Min	Max
A A1 A2	2.02 0.40 1.12	2.44 0.60 1.22
A3 (Ref.)	0.56	
b	0.50	0.70
D	23.00	
D1 (Nom)	21.00	
D2	19.45	20.20
E	23.00	
E1 (Nom)	21.00	
E2	19.45	20.20
e (Ref.)	1.00	

Figure 3. TEMx28 TXC-04222 376-Lead Plastic Ball Grid Array Package

ORDERING INFORMATION

Part Number: TXC-04222AIOG 376-lead Plastic Ball Grid Array Package (PBGA)

RELATED PRODUCTS

TXC-03103, QT1F-*Plus* VLSI Device (Quad T1 Framer-*Plus*). A 4-channel framer for voice and data applications. This device handles all logical interfacing functionality to a T1 line. This device requires a 5.0 volt supply. The new TXC-03103C device provides the same functionality but can operate either from a 5 volt supply or from a 3.3 volt supply at lower power dissipation.

TXC-03108, T1Fx8 VLSI Device (8-Channel T1 Framer). An eight-channel DS1 (1544 kbit/s) framer for voice and data communications applications. This device handles all logical interfacing functionality to a T1 line and operates from a power supply of 3.3 volts.

TXC-03109, E1Fx8 Device (8-Channel E1 Framer). The E1Fx8 is an eight-channel E1 (2048 kbit/s) framer designed with extended features for voice and data communications applications. AMI and HDB3 line codes are supported with full alarm detection and generation per ITU-T G.703, G.775 and I.431.

TXC-03114, QE1F-*Plus* VLSI Device (Quad E1 Framer-*Plus*). The QE1F-*Plus* is a four-channel E1 (2048 kbit/s) framer designed for voice and data communications applications. A dual unipolar or NRZ line interface is supported with full alarm detection and generation per ITU-T G.703 and operates from a power supply of 3.3 or 5 volts.

TXC-06103, PHAST-3N VLSI Device (SONET/SDH STM-1, STS-3 or STS-3c Overhead Terminator) The PHAST-3N provides a Telecom Bus interface for downstream devices and operates from a power supply of 3.3 volts.

PRODUCT PREVIEW

REFERENCE DOCUMENTS

- ITU-T, Bellcore TR-253
- ANSI T1.105

- NOTES -

PRODUCT PREVIEW

PRODUCT PREVIEW information documents contain information on products in their formative or design phase of development. Features, characteristic data and other specifications are subject to change. Contact TranSwitch Applications Engineering for current information on this product.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