Crusoe Processor
Model TM5500

Crusoe™ Processor Model TM5500 Features

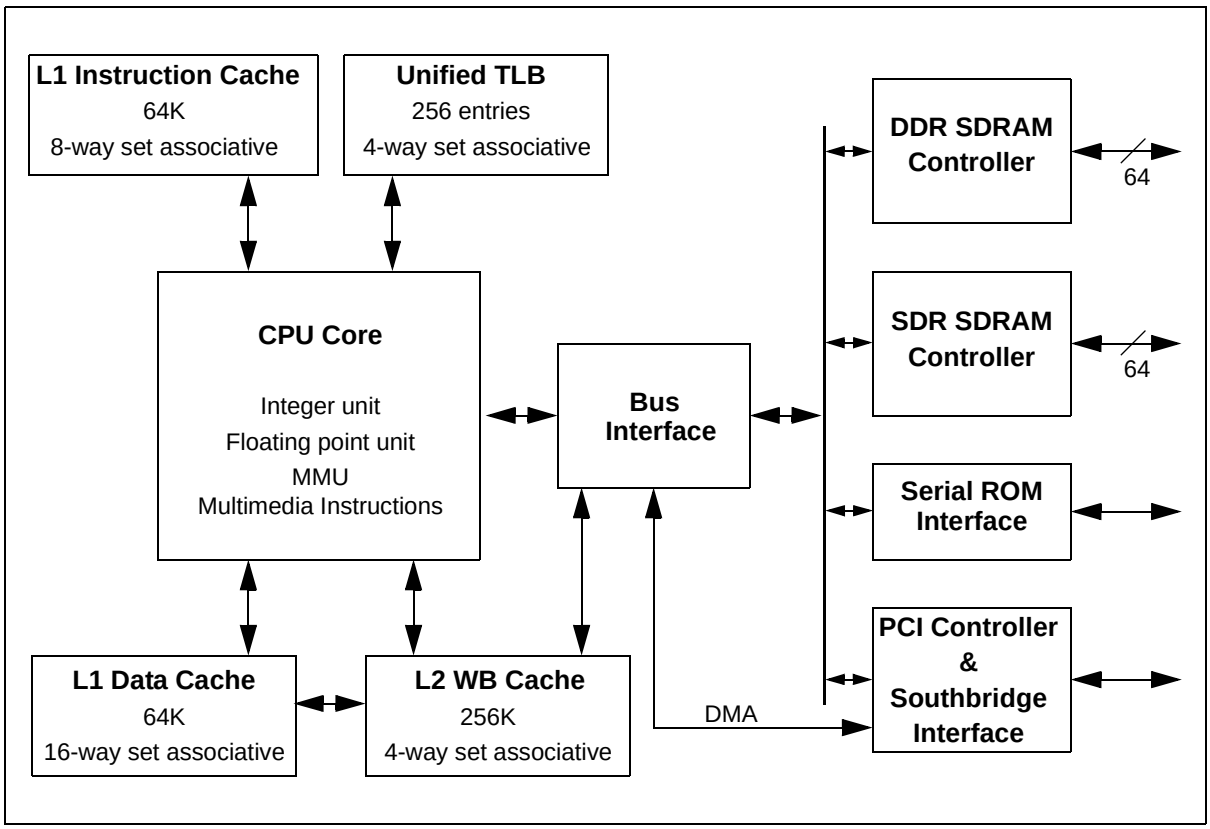
- VLIW processor and x86 Code Morphing™ software provide x86-compatible mobile platform solution
- Processors fabricated in latest 0.13µ process technology operate up to 800 MHz at very low power levels
- Standard product speeds of 667, 700, 733, and 800 MHz
- Integrated 64K-byte L1 instruction cache, 64K-byte L1 data cache, and 256K-byte L2 write-back cache
- Integrated northbridge core logic features facilitate compact system designs
    - DDR SDRAM memory controller with 100-133 MHz, 2.5V interface
    - SDR SDRAM memory controller with 100-133 MHz, 3.3V interface
    - PCI bus controller (PCI 2.1 compliant) with 33 MHz, 3.3V interface
- LongRun™ advanced power management with ultra-low power operation extends mobile battery life
    - 0.4-1.0 W @ 367-800 MHz, 0.9-1.3V running typical multimedia applications
    - 150 mW in deep sleep
- Full System Management Mode (SMM) support
- Compact 474-pin ceramic BGA package is fully pin-compatible with existing TM5400 and TM5600 models

The Transmeta Crusoe processor is an ultra-low power, high-speed microprocessor based on an advanced VLIW core architecture. When used in conjunction with Transmeta's x86 Code Morphing software, the Crusoe processor provides x86-compatible software execution using dynamic binary code translation, without requiring code recompilation. In addition to the VLIW core, the processor incorporates separate 64K-byte instruction and data caches, a large 256K-byte L2 write-back cache, 64-bit DDR SDRAM memory controller, 64-bit SDR SDRAM memory controller, and 32-bit PCI controller. These additional functional units, which are typically part of the core system logic that surrounds the microprocessor, allow the Crusoe processor to provide a highly integrated and cost effective platform solution for the x86 mobile market. The processor core operates from a 0.9-1.3V supply, resulting in extremely low power consumption, even at high operating frequencies. With power consumption during typical operation as low as 150 milliwatts, the Crusoe processor is the most energy efficient high-performance x86-compatible mobile solution ever offered.

1.0 Architecture

The Crusoe processor incorporates integer and floating point execution units, separate instruction and data caches, a level-2 write-back cache, memory management unit, and multimedia instructions. In addition to these traditional processor features, the device integrates a DDR SDRAM memory controller, SDR SDRAM memory controller, PCI bus controller and serial ROM interface controller. These additional units are usually part of the core system logic that surrounds the microprocessor. The VLIW processor, in combination with Code Morphing software and the additional system core logic units, allow the Crusoe processor to provide a highly integrated, ultra-low power, high performance platform solution for the x86 mobile market. The Crusoe processor block diagram is shown in Figure 1.

FIGURE 1 Crusoe Processor Block Diagram - Model TM5500



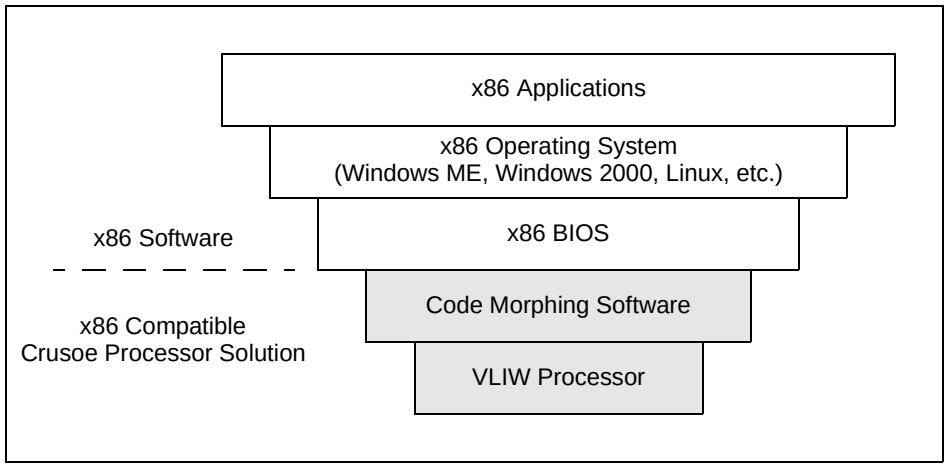
2.0 Processor Core

The Crusoe processor core architecture is relatively simple by conventional standards. It is based on a Very Long Instruction Word (VLIW) 128-bit instruction set. Within this VLIW architecture, the control logic of the processor is kept very simple and software is used to control the scheduling of instructions. This allows a simplified and very straightforward hardware implementation with an in-order 7-stage integer pipeline and a 10-stage floating point pipeline. By streamlining the processor hardware and reducing the control logic transistor count, the performance-to-power consumption ratio can be greatly improved over traditional x86 architectures.

The Crusoe processor includes a 64K-byte 8-way set-associative Level 1 (L1) instruction cache, and a 64K-byte 16-way set associative L1 data cache. The TM5500 model also includes an integrated 256K-byte Level 2 (L2) write-back cache for improved effective memory bandwidth and enhanced performance. This cache architecture assures maximum internal memory bandwidth for performance intensive mobile applications, while maintaining the same low-power implementation that provides a superior performance-to-power consumption ratio relative to previous x86 implementations.

Other than having execution hardware for logical, arithmetic, shift, and floating point instructions, as in conventional processors, the Crusoe processor has very distinctive features from traditional x86 designs. To ease the translation process from x86 to the core VLIW instruction set, the hardware generates the same condition codes as conventional x86 processors and operates on the same 80-bit floating point numbers. Also, the Translation Look-aside Buffer (TLB) has the same protection bits and address mapping as x86 processors. The software component of this solution is used to emulate all other features of the x86 architecture. The software that converts x86 programs into the core VLIW instructions is called Code Morphing software. The combination of Code Morphing software and the VLIW core together act as an x86-compatible solution, as shown in Figure 2.

FIGURE 2 Crusoe Processor Software Hierarchy



The typical behavior of the Code Morphing software is to execute a loop which decodes and executes x86 instructions. The first few times a specific x86 code sequence is executed, Code Morphing interprets the code by decoding the instructions one byte at time and then dispatching execution to corresponding VLIW native instruction subroutines. Once the x86 code has been executed several times, Code Morphing translates the x86 instructions into highly optimized and extremely fast VLIW native instructions, executes the translated code, and caches the native instruction translations for future use. If the same x86 code is required to execute again, the high-performance cached translations are executed immediately and no re-translation is required.

2.1 Integrated DDR SDRAM Memory Controller

The DDR SDRAM interface is the highest performance memory interface available on the Crusoe processor. The DDR SDRAM controller supports only Double Data Rate (DDR) SDRAM and transfers data at a rate that is twice the clock frequency of the interface. The DDR SDRAM controller supports up to two banks, the equivalent of two Dual In-line Memory Modules (DIMMs), of DDR SDRAM using a 64-bit wide interface.

The DDR SDRAM memory can be populated with 64M-bit, 128M-bit, or 256M-bit devices. For highest performance, it is recommended that the DDR SDRAM devices be soldered to the motherboard rather than incorporated on DIMMs. Also, to reduce signal loading, only x8 or x16 devices should be used.

The frequency setting for the DDR SDRAM interface is initialized during the power-on boot sequence. Although the processor supports a DDR interface frequency in the range of 1/2 to 1/15 of the core frequency, the recommended interface frequency is between 100 and 133 MHz.

2.2 Integrated SDR SDRAM Memory Controller

The SDR SDRAM memory controller supports up to four banks, equivalent to two Small Outline Dual In-line Memory Modules (SO-DIMMS), of Single Data Rate (SDR) SDRAM that can be configured as 64-bit SO-DIMMs. These SO-DIMMs can be populated with 64M-bit, 128M-bit or 256M-bit devices. All SO-DIMMs must use the same frequency SDRAMs, but there are no restrictions on mixing different SO-DIMM configurations into each SO-DIMM slot.

The frequency setting for the SDR SDRAM interface is initialized during the power-on boot sequence. Although the processor supports an SDR interface frequency in the range of 1/2 to 1/15 of the core frequency, the recommended interface frequency is between 100 and 133 MHz. It is also recommended that a maximum of 8 devices per SO-DIMM be used in order to operate at the required frequency with the proper signal integrity.

2.3 Integrated PCI Controller

The Crusoe processor includes a PCI bus controller that is PCI 2.1 compliant. The PCI bus is 32 bits wide, operates at 33 MHz, and is compatible with 3.3V signal levels. It is not 5V tolerant, however. The PCI controller on provides a PCI host bridge, the PCI bus arbiter, and a DMA controller.

The PCI bus can sustain 132 Mbytes/sec bursts for reads and writes on 4K-byte blocks. The PCI controller snoops ahead on PCI-to-DRAM reads and writes. The 16-Dword CPU-to-PCI write buffer converts sequential memory mapped I/O writes to PCI bursts. The DMA controller handles PCI-to-DRAM reads and writes. The 16-Dword PCI-to-DRAM write buffer converts one 16-Dword burst to eight separate address/data pairs. The 16-Dword DRAM-to-PCI read ahead buffer permits continuation of read ahead activity after hitting in the buffer. The PCI controller tri-states the PCI bus when hot docking.

2.4 Serial ROM Interface

The Crusoe processor serial ROM interface is a five-pin interface used to read data from a serial flash ROM. The flash ROM is 1M-byte in size and provides non-volatile storage for the Code Morphing software. During the boot process, the Code Morphing code is copied from the ROM to the Code Morphing memory space in SDRAM. Once transferred, the Code Morphing code requires 16M-bytes of memory space. The portion of SDRAM space reserved for Code Morphing software is not visible to x86 code. Transmeta supplies programming information for the flash ROM device. This interface may also be used for in-system reprogramming of the flash ROM.

3.0 Software Compatibility

When used in conjunction with Transmeta's x86 Code Morphing software, the Crusoe processor provides x86-compatible software execution without requiring code recompilation. Systems based on this solution are capable of executing all standard x86-compatible operating systems and applications, including Microsoft Windows 9x, Windows ME, Windows 2000, and Linux.

4.0 Operating Power and Power Management

The Crusoe processor operates from a 0.9-1.3V core voltage supply at extremely low power levels, even while the device is operating at very high performance. The TM5500 model incorporates LongRun adaptive power management technology. LongRun power management dynamically reduces the core CPU power consumption to near-optimal levels in response to processor work load requirements.

LongRun achieves this dynamic power reduction by varying the CPU clock and core power supply voltage in response to adaptive power management protocols that monitor processor load demands and control processor power and performance levels. The LongRun power management approach is particularly effective in applications that run predominantly in the normal (active) power state, as described below.

Additionally, the Crusoe processor supports ACPI-compliant power management modes by incorporating five distinct power states: Normal, Auto Halt, Quick Start, Deep Sleep and Off. These power states may be used to reduce the operating power of the processor during system states that require little or no CPU activity.

Table 1 lists the recommended state of the processor for each of the ACPI global system states. Typical power dissipation for each of the power states is shown in Table 2.

TABLE 1 **Crusoe Processor Power Management System States**

ACPI System State		Processor Power State	DDR, SDR SDRAM	Clock Generator
G0/S0 (Working)	C0	Normal	Normal	Running
	C1	Auto Halt	Normal	Running
	C2	Quick Start	Self Refresh	Running
	C3	Deep Sleep	Self Refresh	Clocks Stopped
G1/S1 (Sleeping)		Deep Sleep	Self Refresh	PLL Shut Down
G1/S2 (Suspend-to-RAM)		Deep Sleep	Self Refresh	PLL Shut Down
G1/S3 (Suspend-to-RAM)		Off	Self Refresh	PLL Shut Down
G1/S4 (Suspend-to-Disk)		Off	Off	Off
G2/S5 (Soft Off)		Off	Off	Off
G3 (Mechanical Off)		Off	Off	Off

TABLE 2 **Crusoe Processor Model TM5500 Specifications**

Crusoe Processor Model	Performance Range	Voltage Range	Thermal Power
TM5500-667 MHz	300 - 667 MHz	0.9 - 1.3 V	5.0 W
TM5500-700 MHz	333 - 700 MHz	0.9 - 1.3 V	5.3 W
TM5500-733 MHz	333 - 733 MHz	0.9 - 1.3 V	5.5 W
TM5500-800 MHz	367 - 800 MHz	0.9 - 1.3 V	6.0 W

TABLE 3 **Crusoe Processor Typical Power Consumption - TM5500 367-800 MHz 0.9-1.3V**

Workload System State	Crusoe Processor CPU Core + Integrated Northbridge	Notes
DVD Playback (C0)	1.049 W	1, 2
MP3 Playback (C0)	0.419 W	1, 3
Auto Halt (C1)	0.312 W	1, 4
Quick Start (C2)	0.197 W	1, 5
Deep Sleep (C3)	0.156 W	1, 6
Off / Instant On	0.000 W	1, 7

Notes:
1. All power supplies at their optimal operating values. Full system power management enabled, including LongRun adaptive power management.
2. Typical DVD power is measured while running the Win DVD® 2000 player under Windows® 2000.
3. Typical MP3 power measured while running MMJukebox under Windows 2000.
4. Auto Halt mode entered by executing a HLT instruction.
5. Quick Start mode entered by asserting STPCLK#.
6. Deep Sleep mode entered by asserting SLEEP# and stopping CLKIN while in Quick Start.
7. Off / Instant On mode is entered in the Suspend to RAM and Suspend to Disk system states.

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