THC63DV151

120MHz 24Bit COLOR DVI Compliant Receiver

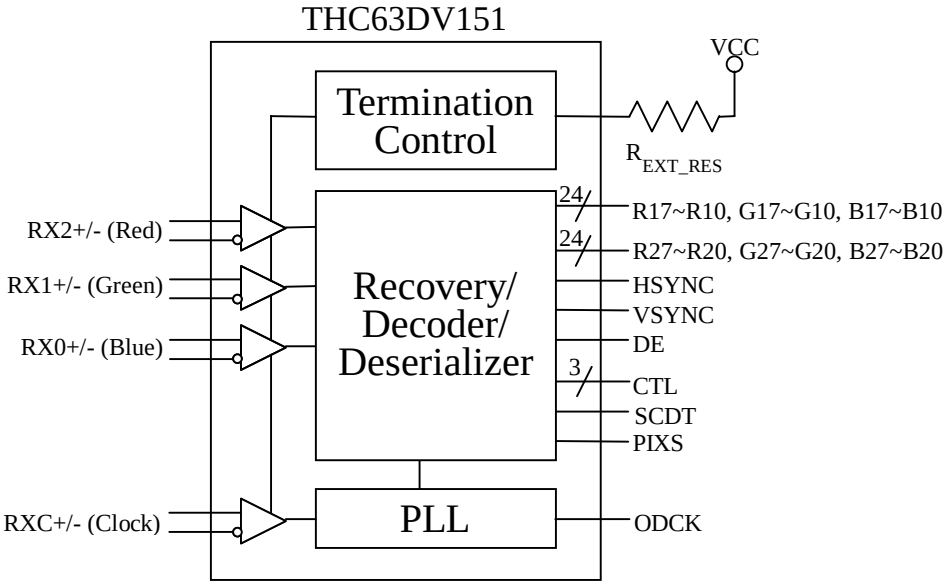
General Description

The THC63DV151 is a receiver compliant with DVI Rev.1.0. The THC63DV151 supports display resolution from VGA to SXGA(25-120MHz), up to 24bit/pixel. The built-in PLL requires no external component. Based on THine's original technologies used in the THine's LVDS products, the THC63DV151 realizes low power and high skew tolerance.

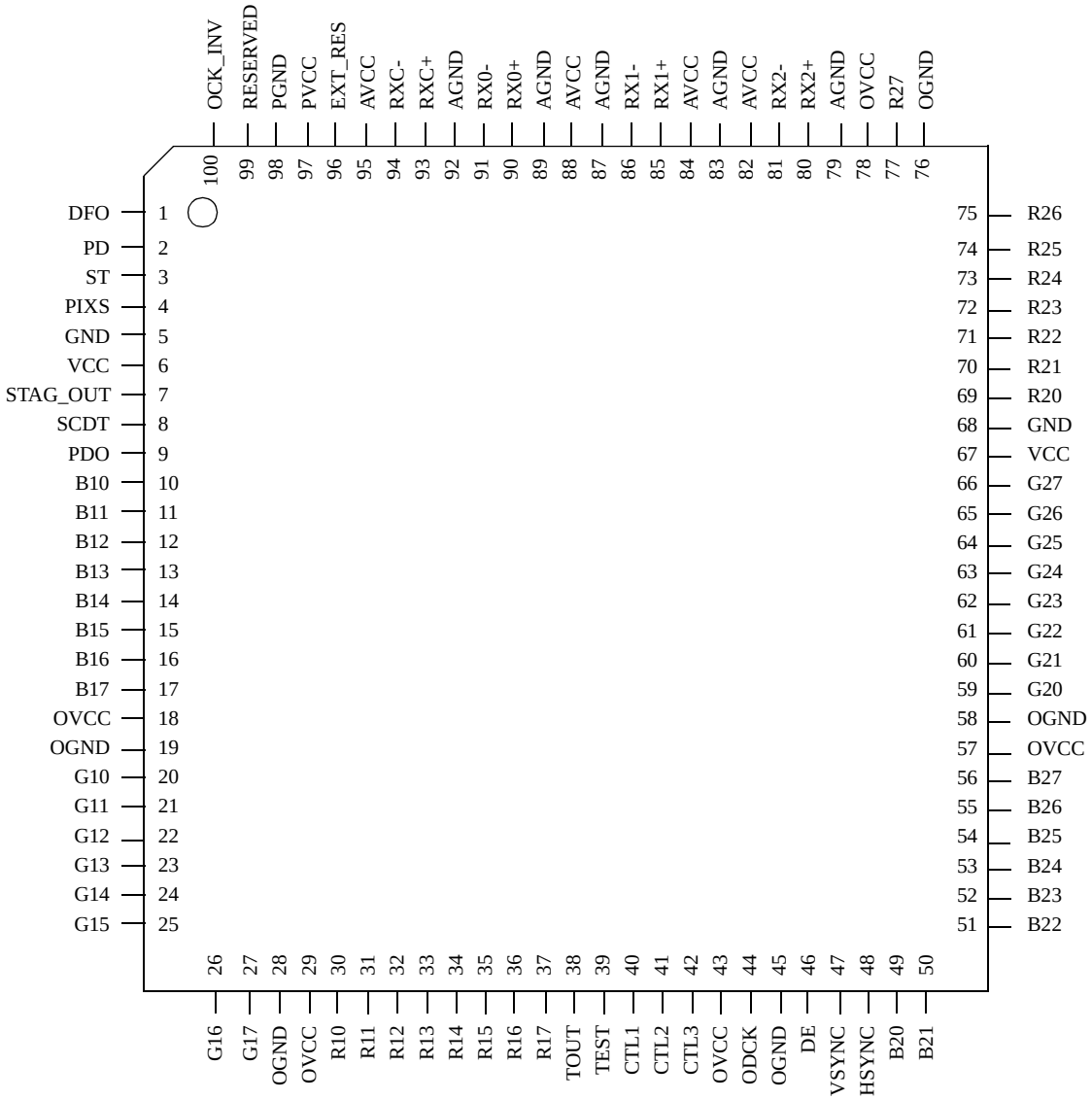
Features

- Compliant with DVI Rev.1.0
- Wide Frequency Range:25MHz-120MHz
- PLL requires No external components
- High Skew Tolerance:1 full input clock cycle
- Programmable Single/Dual Pixel Mode
- Programmable TTL Output Clock Polarity
- Programmable TTL Output Current
- Power down mode
- Low power single 3.3V CMOS design
- 100pin TQFP
- Pin Compatible with the Silicon Image SiI151

Block Diagram



Pin Out



Pin Description

Pin Name	Pin #	Type	Description
RX0+, RX0-	90, 91	In	Differential Data Inputs.
RX1+, RX1-	85, 86	In	
RX2+, RX2-	80, 81	In	
RXC+, RXC-	93, 94	In	Differential Clock Input.
R17 ~ R10	37, 36, 35, 34, 33, 32, 31, 30	Out	First Pixel Data Outputs. These outputs correspond to 24-bit pixel data for 1-pixel/clock mode and to the first 24-bit pixel data for 2-pixels/clock mode. PD=L or PDO=L make the output drivers into a high impedance mode with weak pull-down.
G17 ~ G10	27, 26, 25, 24, 23, 22, 21, 20	Out	
B17 ~ B10	17, 16, 15, 14, 13, 12, 11, 10	Out	
R27 ~ R20	77, 75, 74, 73, 72, 71, 70, 69	Out	Second Pixel Data Outputs. These outputs correspond to the second 24-bit pixel data for 2-pixels/clock mode and are driven low for 1-pixel/clock mode. PD=L or PDO=L make the output drivers into a high impedance mode with weak pull-down.
G27 ~ G20	66, 65, 64, 63, 62, 61, 60, 59	Out	
B27 ~ B20	56, 55, 54, 53, 52, 51, 50, 49	Out	
ODCK	44	Out	Clock Output.
DE	46	Out	Data Enable Output.
VSYNC	47	Out	Vsync Output.
HSYNC	48	Out	Hsync Output.
CTL3~CTL1	42, 41, 40	Out	Control Signal Outputs.
OCK_INV	100	In	ODCK Polarity. H: Inverted L: Normal
PIXS	4	In	Pixel Select. H: Two pixels per clock L: Single pixel per clock
DFO	1	In	Output Data Format. Must be L for all DVI applications
STAG_OUT	7	In	Staggered Output. This function is only available for 2-pixels per clock mode. H: Simultaneous output drive L: Staggered output drive
SCDT	8	Out	Sync Detect. H: All channels establish synchronization with the data streams. Link is active. L: Any channel does not establish synchronization or RXC+/ RXC- pair is not actively toggling. Link is down.
PDO	9	In	Output Drive Power Down. H: Normal operation L: All output drivers except SCDT and CTL1 into a high impedance mode with weak pull-down
ST	3	In	Output Drive Strength. H: High output drive strength L: Low output drive strength

Pin Name	Pin #	Type	Description
PD	2	In	Power Down. H: Normal operation L: Power down mode. All output drivers are disabled with weak pull-down, all circuitries are powered down, and all inputs are disabled.
TEST	39	In	Test pin. Must be L for normal operation.
TOUT	38	Out	Test Output. This pin is in high impedance mode during normal operation and can be tied H for the pin compatibility with the other products.
EXT_RES	96	Analog	Impedance Matching Control. Resistor value should be ten times the termination resistance of each channel.
RESERVED	99	In	Reserved. Must be H for normal operation.
VCC	6, 67	Power	Power Supply Pins for digital core.
GND	5, 68	Ground	Ground Pins for digital core.
OVCC	18, 29, 43, 57, 78	Power	Power Supply Pins for output drive.
OGND	19, 28, 45, 58, 76	Ground	Ground Pins for output drive.
AVCC	82, 84, 88, 95	Power	Power Supply Pins for analog circuitry.
AGND	79, 83, 87, 89, 92	Ground	Ground Pins for analog circuitry.
PVCC	97	Power	Power Supply Pin for PLL circuitry.
PGND	98	Ground	Ground Pin for PLL circuitry.

Absolute Maximum Ratings [1]

Supply Voltage (V_{CC})	-0.3V ~ +4.0V
CMOS/TTL Input Voltage	-0.3V ~ (V_{CC} + 0.3V)
CMOS/TTL Output Voltage	-0.3V ~ (V_{CC} + 0.3V)
TMDS Receiver Input Voltage	-0.3V ~ (V_{CC} + 0.3V)
DC Output Current	-30mA ~ 30mA
Junction Temperature	+125°C
Storage Temperature Range	-55°C ~ +125°C
Lead Temperature (Soldering, 4sec)	+260°C
Maximum Power Dissipation @+25°C	1.4W

Electrical Characteristics

DC Digital I/O Specifications

V_{CC} = 3.0V ~ 3.6V, Ta = 0°C ~ +70°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	High Level Input Voltage		2.0			V
V_{IL}	Low Level Input Voltage				0.8	V
V_{OH}	High Level Output Voltage	I_{OH}= -2mA, -4mA (ODCK) I_{OH}= -1mA, -2mA (Others)	2.4			V
V_{OL}	Low Level Output Voltage	I_{OL}= 2mA, 4mA (ODCK) I_{OL}= 1mA, 2mA (Others)			0.4	V
I_{INC}	Input Current	$0V \le V_{IN} \le V_{CC}$	-10		+10	μA

DC Differential Input Specifications

V_{CC} = 3.0V ~ 3.6V, Ta = 0°C ~ +70°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IDIFF}	Differential Input Voltage		150		1200	mV
V_{ICM}	Input Common Mode Voltage		Vcc-300		Vcc-37	mV

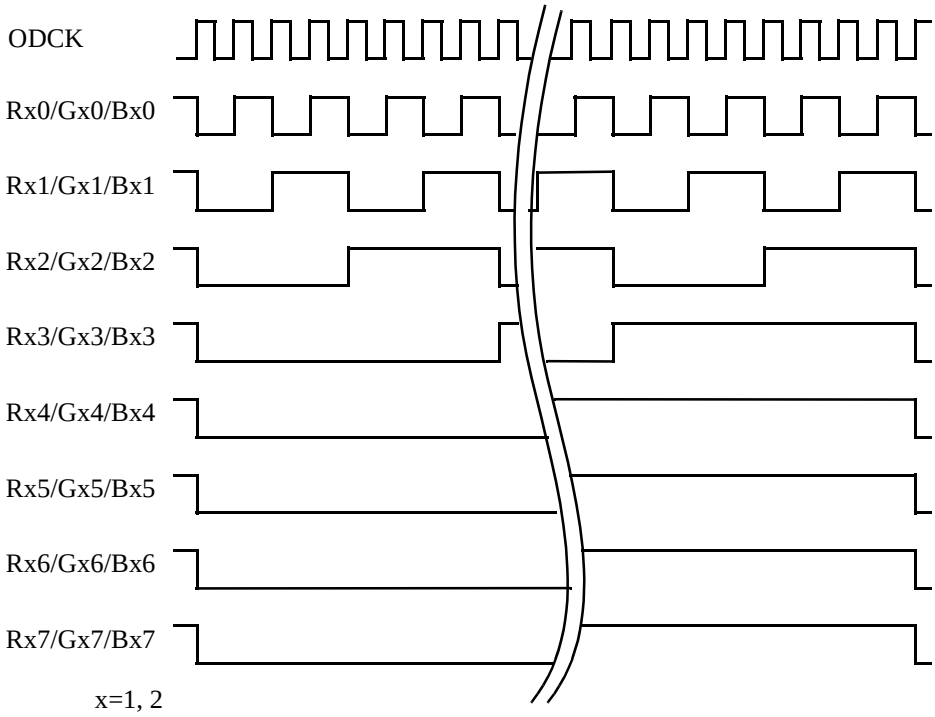
1. "Absolute Maximum Ratings" are those valued beyond which the safety of the device can not be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Supply Current

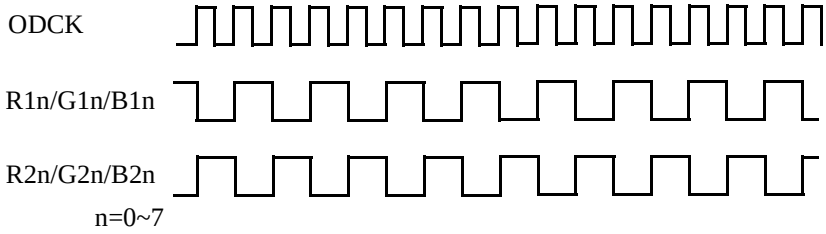
V_{CC} = 3.0V ~ 3.6V, Ta = 0°C ~ +70°C

Symbol	Parameter	Condition	Typ.	Max.	Units
I_{CCRG}	Receiver Supply Current	DCLK=60MHz, 2-pixel/clock mode, C_{LOAD}=10pF, R_{EXT_SWING}=400Ω, Gray Scale Pattern	140	165	mA
I_{CCRW}	Receiver Supply Current	DCLK=60MHz, 2-pixel/clock mode, C_{LOAD}=10pF, R_{EXT_SWING}=400Ω, Worst Case Pattern	205	235	mA
I_{CCRD}	Receiver Disconnected Supply Current	Disconnected or Transmitter Disabled	35		mA
I_{CCRS}	Receiver Power Down Supply Current	PD = L		100	μA

256 Gray Scale Pattern



Worst Case Pattern



AC Specifications

V_{CC} = 3.0V ~ 3.6V, Ta = 0°C ~ +70°C

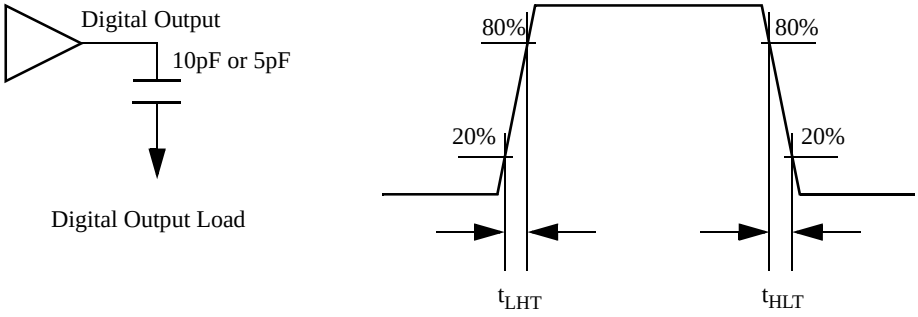
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{DPS}	Intra-Pair Skew				0.4	T_{bit}
t_{CCS}	Inter-Pair Skew				1.0	T_{pixel}
t_{IJIT}	Differential Input Clock Jitter Tolerance				0.3	T_{bit}
t_{LHT}	L-to-H Transition Time Data and Controls	C_{LOAD}=10pF ST=H			3.1	ns
		C_{LOAD}=5pF ST=L			5.0	ns
	ODCK	C_{LOAD}=10pF ST=H			2.0	ns
		C_{LOAD}=5pF ST=L			2.9	ns
t_{HLT}	H-to-L Transition Time Data and Controls	C_{LOAD}=10pF ST=H			2.8	ns
		C_{LOAD}=5pF ST=L			3.9	ns
	ODCK	C_{LOAD}=10pF ST=H			1.5	ns
		C_{LOAD}=5pF ST=L			2.5	ns
t_{RS}	Data, DE, VSYNC, HSYNC, and CTL[3:1] Setup Time to ODCK falling edge (OCK_INV=L, 120MHz, 1-pixel/clock, PIXS=L)	C_{LOAD}=10pF ST=H	3.2			ns
		C_{LOAD}=5pF ST=L	3.5			ns
	Data, DE, VSYNC, HSYNC, and CTL[3:1] Setup Time to ODCK falling edge (OCK_INV=L, 60MHz, 2-pixels/clock, PIXS=H)	C_{LOAD}=10pF ST=H	7.4			ns
		C_{LOAD}=5pF ST=L	7.7			ns
	Data, DE, VSYNC, HSYNC, and CTL[3:1] Setup Time to ODCK rising edge (OCK_INV=H, 120MHz, 1-pixel/clock, PIXS=L)	C_{LOAD}=10pF ST=H	3.2			ns
		C_{LOAD}=5pF ST=L	3.5			ns
	Data, DE, VSYNC, HSYNC, and CTL[3:1] Setup Time to ODCK rising edge (OCK_INV=H, 60MHz, 2-pixels/clock, PIXS=H)	C_{LOAD}=10pF ST=H	7.4			ns
		C_{LOAD}=5pF ST=L	7.7			ns

AC Specifications (continued)

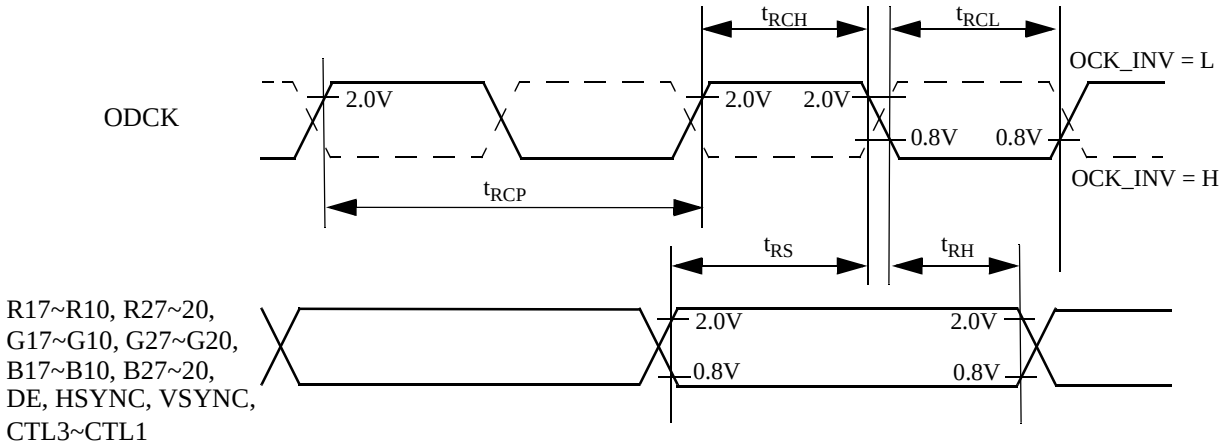
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{RH}	Data, DE, VSYNC, HSYNC, and CTL[3:1] Hold Time to ODCK falling edge (OCK_INV=L, 120MHz, 1-pixel/clock, PIXS=L)	C_{LOAD}=10pF ST=H	3.2			ns
		C_{LOAD}=5pF ST=L	2.9			ns
	Data, DE, VSYNC, HSYNC, and CTL[3:1] Hold Time to ODCK falling edge (OCK_INV=L, 60MHz, 2-pixels/clock, PIXS=H)	C_{LOAD}=10pF ST=H	7.4			ns
		C_{LOAD}=5pF ST=L	7.1			ns
	Data, DE, VSYNC, HSYNC, and CTL[3:1] Hold Time to ODCK rising edge (OCK_INV=H, 120MHz, 1-pixel/clock, PIXS=L)	C_{LOAD}=10pF ST=H	3.2			ns
		C_{LOAD}=5pF ST=L	2.9			ns
	Data, DE, VSYNC, HSYNC, and CTL[3:1] Hold Time to ODCK rising edge (OCK_INV=H, 60MHz, 2-pixels/clock, PIXS=H)	C_{LOAD}=10pF ST=H	7.4			ns
		C_{LOAD}=5pF ST=L	7.1			ns
t_{RCP}	ODCK Cycle Time (1-pixel/clock)		8.33		40	ns
f_{RCP}	ODCK Frequency (1-pixel/clock)		25		120	MHz
t_{RCP}	ODCK Cycle Time (2-pixels/clock)		16.7		80	ns
f_{RCP}	ODCK Frequency (2-pixels/clock)		12.5		60	MHz
t_{RCH}	ODCK High Time (120MHz, 1-pixel/clock, PIXS=L)	C_{LOAD}=10pF ST=H	3.0			ns
		C_{LOAD}=5pF ST=L	1.1			ns
t_{RCL}	ODCK Low Time (120MHz, 1-pixel/clock, PIXS=L)	C_{LOAD}=10pF ST=H	3.5			ns
		C_{LOAD}=5pF ST=L	2.1			ns
t_{PDL}	Delay from PD Low to High impedance outputs				10	ns
t_{FSC}	Link disabled (DE inactive) to SCDT Low			1		µs
	Link disabled (Tx power down) to SCDT Low			1		µs
t_{HSC}	Link enabled (DE active) to SCDT High			25		DE edges
t_{ST}	ODCK High to even data output (OCK_INV=L)			0.25		t_{RCP}
	ODCK Low to even data output (OCK_INV=H)			0.25		t_{RCP}

AC Timing Diagrams

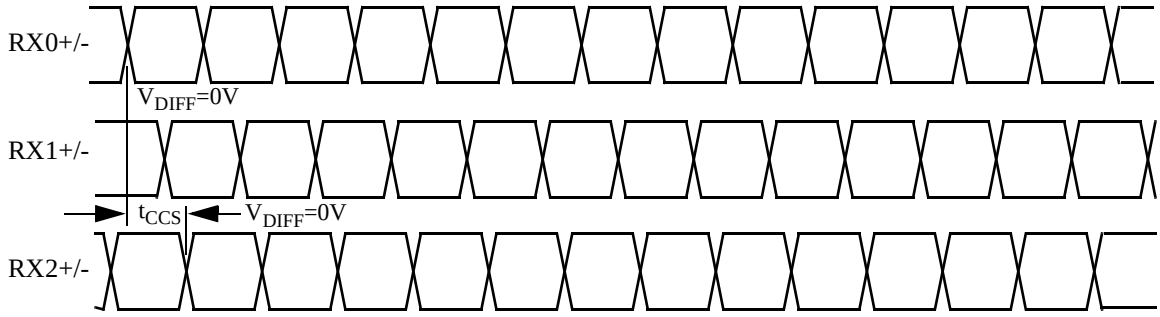
Digital Output Transition Times



Output Timing



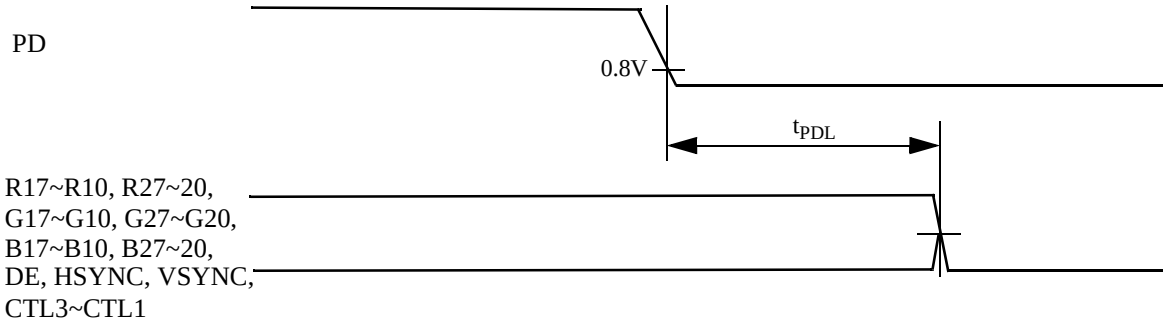
Inter-Pair Skew Timing



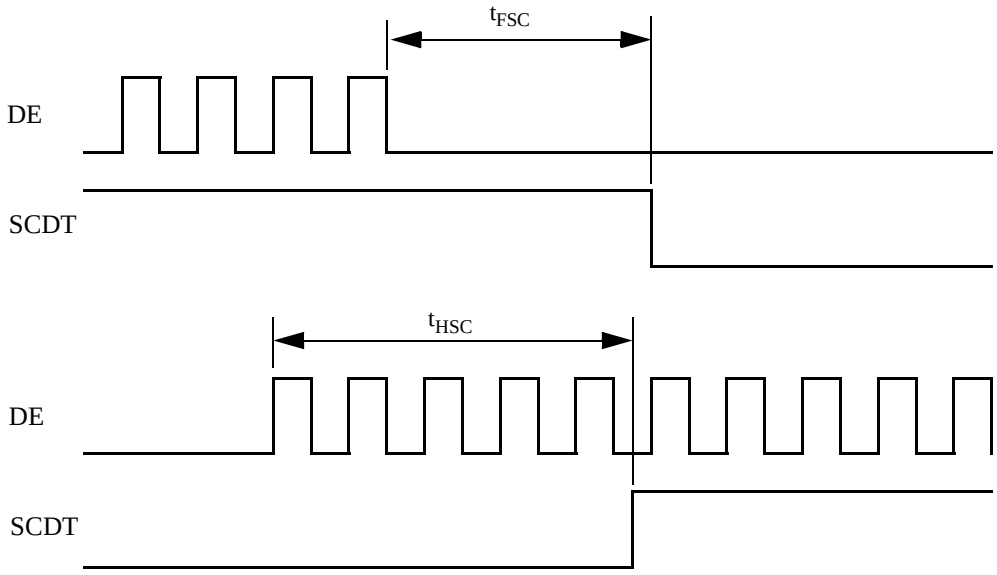
Note:
V_{DIFF} = (RXn+) - (RXn-), (RXC+) - (RXC-)

AC Timing Diagrams (continued)

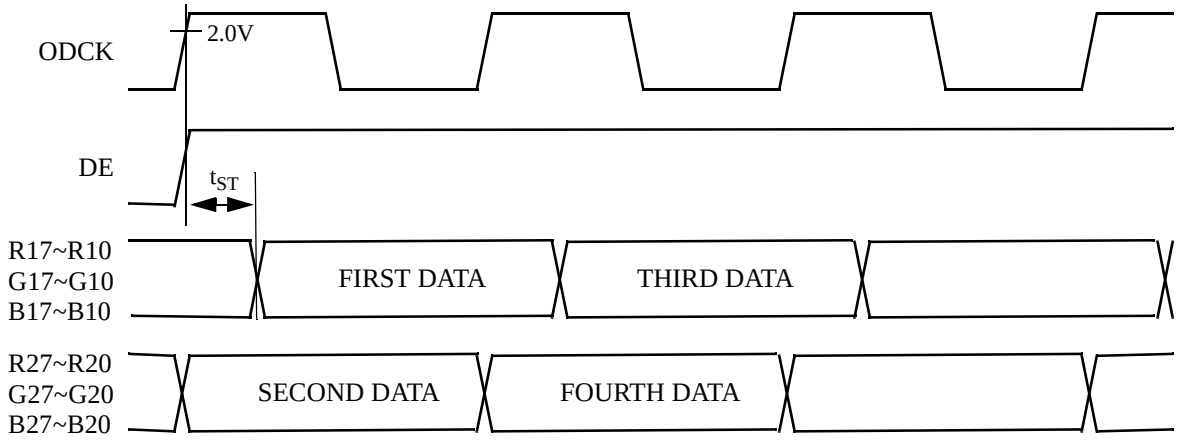
Output Signals Disabled Timing from PD Active



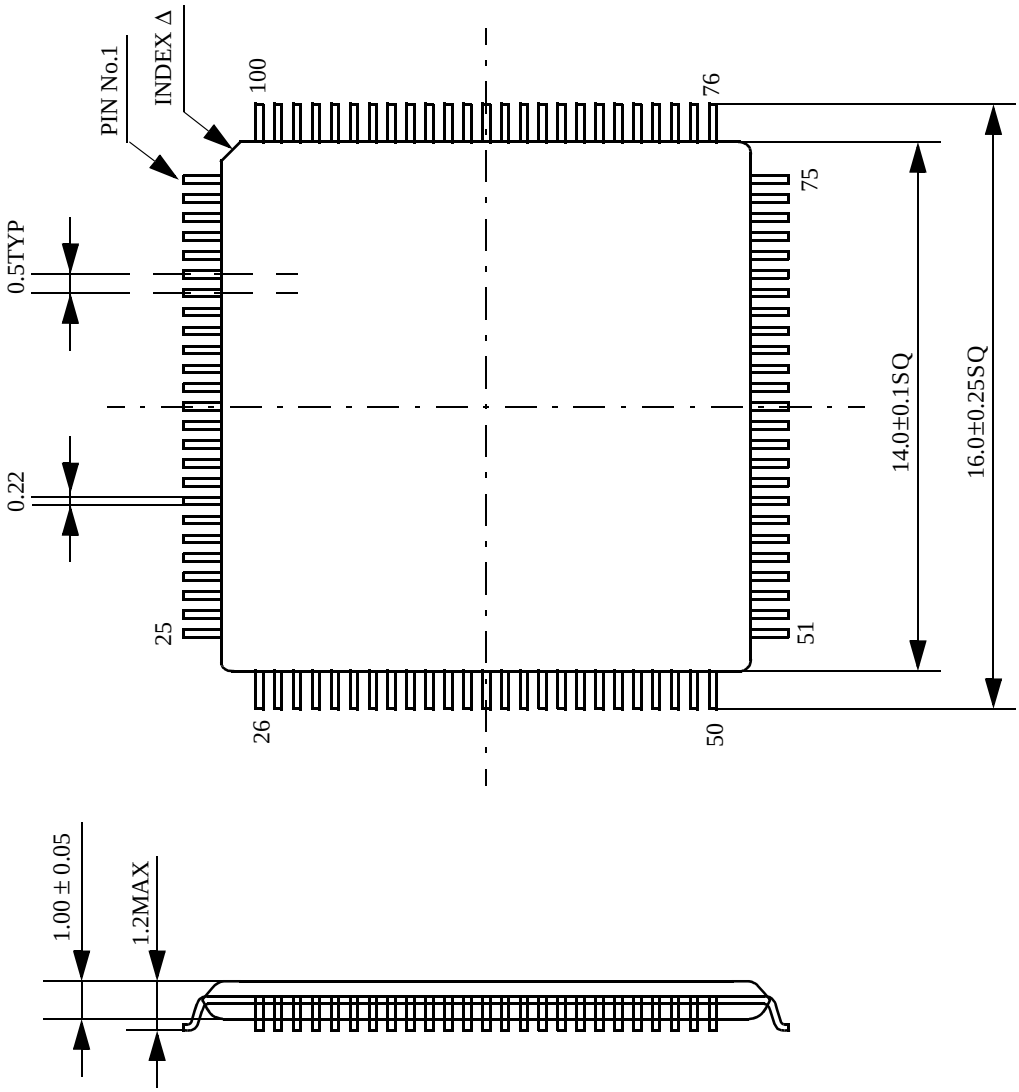
SCDT Timing from DE Inactive/Active



2-Pixels/Clock Staggered Output Timing Diagram



Package



UNITS:mm

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