TNETA1560

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SBus SAR

Networking Business Unit
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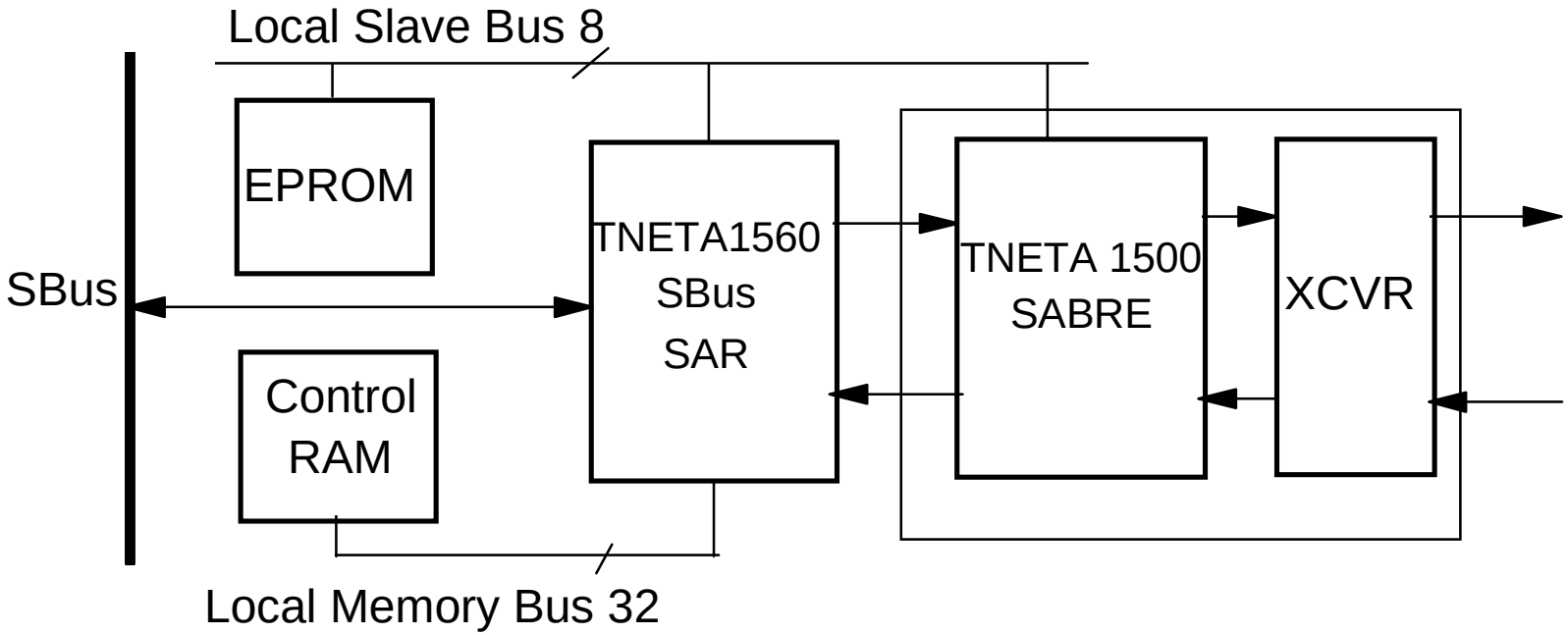
Agenda

- Main Features
- Interfaces
- Architecture
- Data Structures
- Functional Overview
- Registers
- Peripheral Devices

SBus SAR Main Features



- **The SBus SAR is an SBus device that provides an asynchronous transfer mode (ATM) Interface.**
- **Single-chip segmentation and reassembly (SAR) for full-duplex ATM adaptation layer (AAL) processing.**

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Main Features

- On-chip SBus host interface allows use of host memory for packet segmentation and reassembly
- No local packet memory required
- Packet interface managed by efficient descriptor rings
- 53-byte ATM cells are transparent to the user
- Provides complete encapsulation and termination of AAL5 and limited AAL3/4
- Null AAL provides features for constant-bit-rate services
- Supports 1023 unique virtual circuits (VCs)
- Explicit cell-level interleaving between groups of VCs

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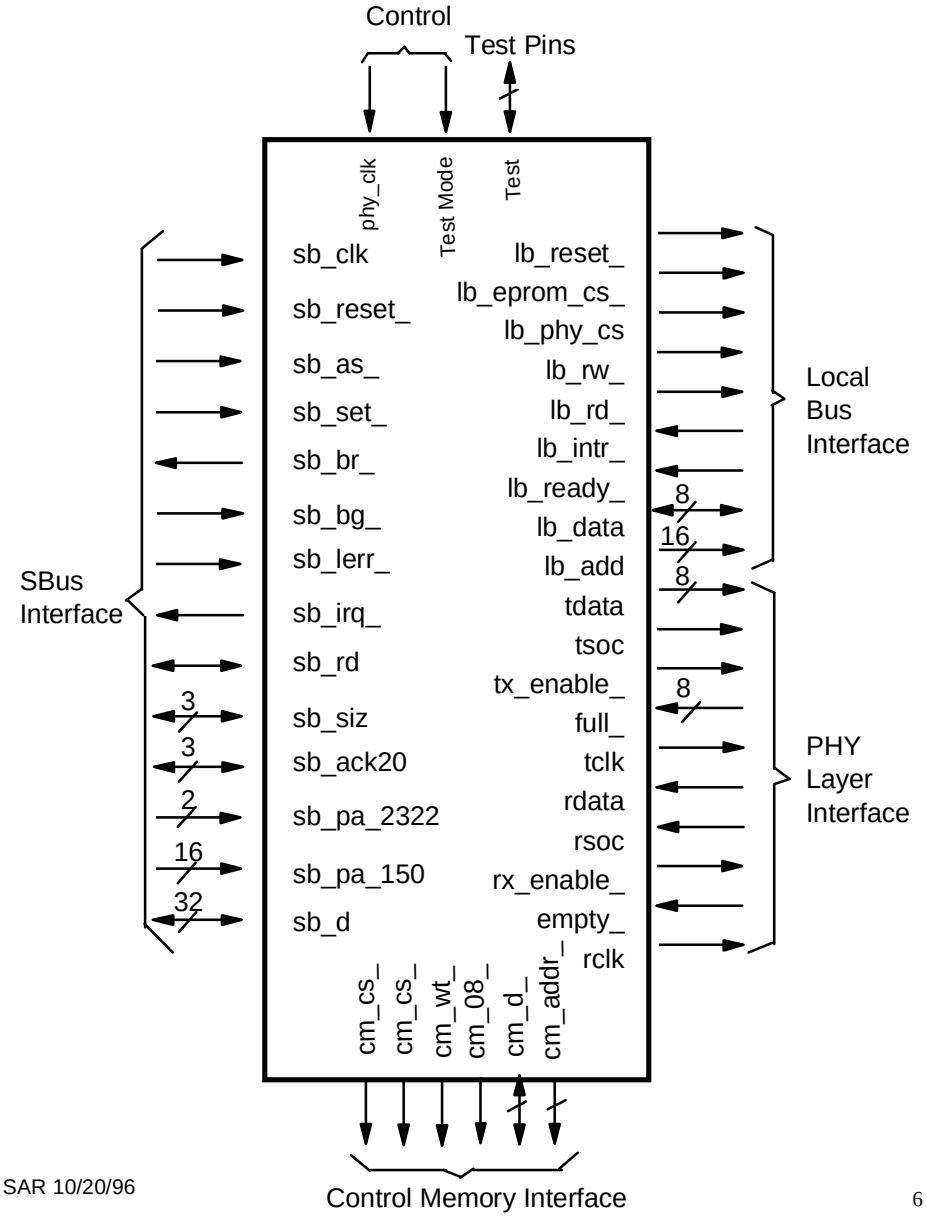
Main Features (cont.)

- **Interfaces directly to TNETA1500 SONET ATM BiCMOS receiver transmitter (SABRE)**
- **Full-duplex physical (PHY) layer interface is compliant with the UTOPIA specification**
- **Supports PHY layer data rates in the range 25.6 to 155.52 Mbits/s**
- **Support provided to recognize ATM layer operations and maintenance (OAM) cells**
- **8-Cell transmit FIFO**
- **32-Cell receive FIFO**
- **No external logic required for host or local buses, ensuring simple design with low external component count**

SBus SAR Interfaces



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SBus Interface

- SBus interface module (SBIM) is responsible for implementing the details of the SBus protocol
- No external host interface logic required to interconnect to a SBus host
- Behaves both as a SBus DVMA master and slave
- Efficient transfer of 48-byte payload using 32- and 16-byte bursts

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Control Memory Interface

- Control memory set up in a 16K x 32 configuration
- Cycle time given by the SBus clock
- Simple design for latched SRAM, no external logic is required, all signals are provided:
  - 32-bit data bus
  - 14-bit address bus
  - cm_wr_ signal determines read/write
  - cm_oe_ output enable signal

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Local Bus Interface

- **All signals are provided to connect the SBus SAR to the EPROM and to the TNETA1500 physical layer.**
- **No external components are required; all necessary signals are provided by the SBus SAR.**
- **The lower 16 bits of the SBus address are directly routed to the local bus address bus.**
- **The SBus SAR ensures that the SBus acknowledgment signal is not asserted until the corresponding local bus transaction is complete.**

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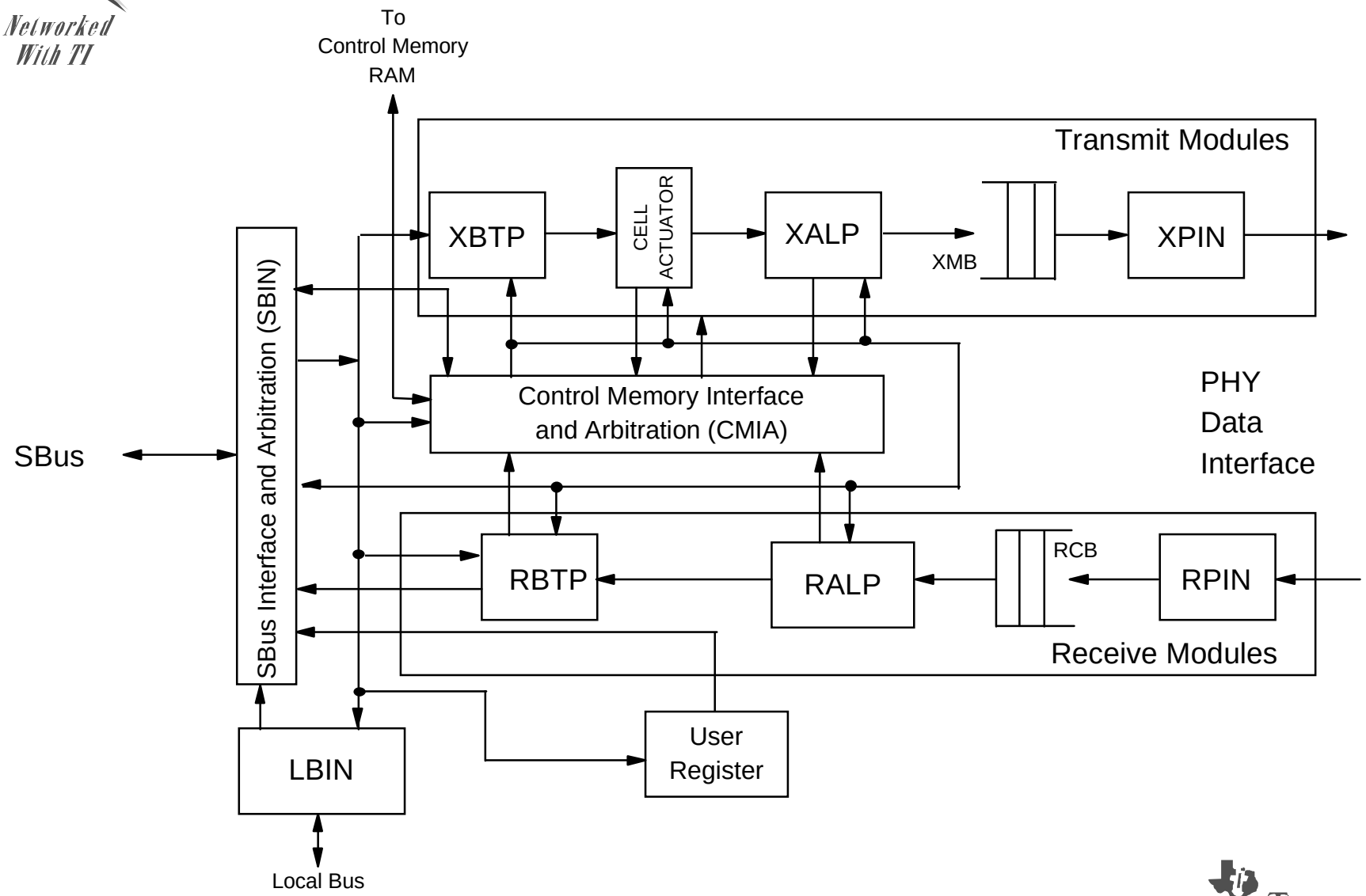
PHY Layer Interface

- **The SBus SAR generates a PHY layer transmit clock at the SBus frequency.**
- **The receive clock for the PHY interface is also driven by the SAR and is equivalent to the internal clock.**
- **The SBus SAR generates output data, along with a start-of-cell indicator in the transmit direction.**

PHY Layer Control Interface

- **The internal SAR clock is driven by an external PHY clock signal. A 19.44-MHz clock is required for 155.52 Mbit/s operation.**

SBus SAR Architecture



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Transmit Modules

- **The transmit host and buffer transaction processor (XBTP) is responsible for host-related transmit functions. It requests 16- and 32-byte transfers from the SBus block.**
- **The cell actuator determines the next VC to be serviced.**
- **The transmit adaptation layer processor (XALP) handles all AAL-related functions and ATM header formation.**
- **The transmit buffer (XMB) is an 8-cell buffer.**
- **The transmit PHY interface (XPIN) performs word-to-byte unpacking and interacts with the PHY layer using the SBus clock.**

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Receive Modules

- The receive PHY interface (RPIN) performs byte-to-word packing, filters idle cells, and interacts with the PHY layer using the PHY layer clock.
- The receive buffer (RCB) provides rate synchronization from the PHY layer clock to the SBus clock and holds up to 32 cells.
- The receive ATM adaptation layer processor (RALP) terminates the AAL5 CRC and processes various end-of-packet (EOP) indicators.
- The RALP block also processes the ATM header and determines which receive DMA is to be used.
- The receive host and buffer transaction processor (RBTP) perform all host-specific receive functions.

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SBus Interface Module

- **The SBus interface module (SBIN) is responsible for implementing the SBus protocol.**
- **The XBTP and RBTP are the only modules that require the SAR to be a master on the SBus.**
- **Hence, the SBus SAR arbitrates requests from these two blocks.**
- **The SAR is an SBus slave for host accesses to EPROM, PHY registers, SAR registers, and control memory.**

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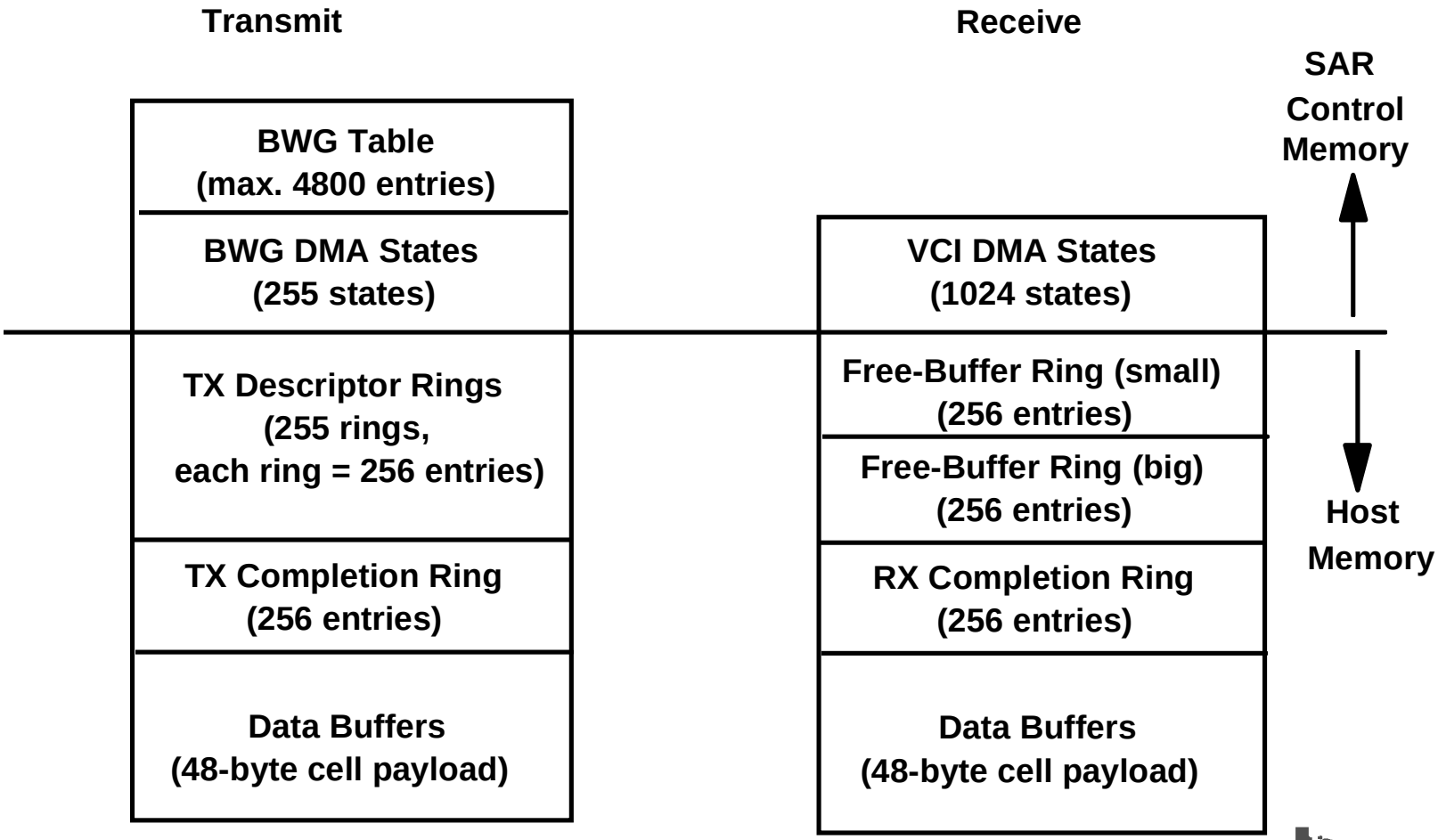
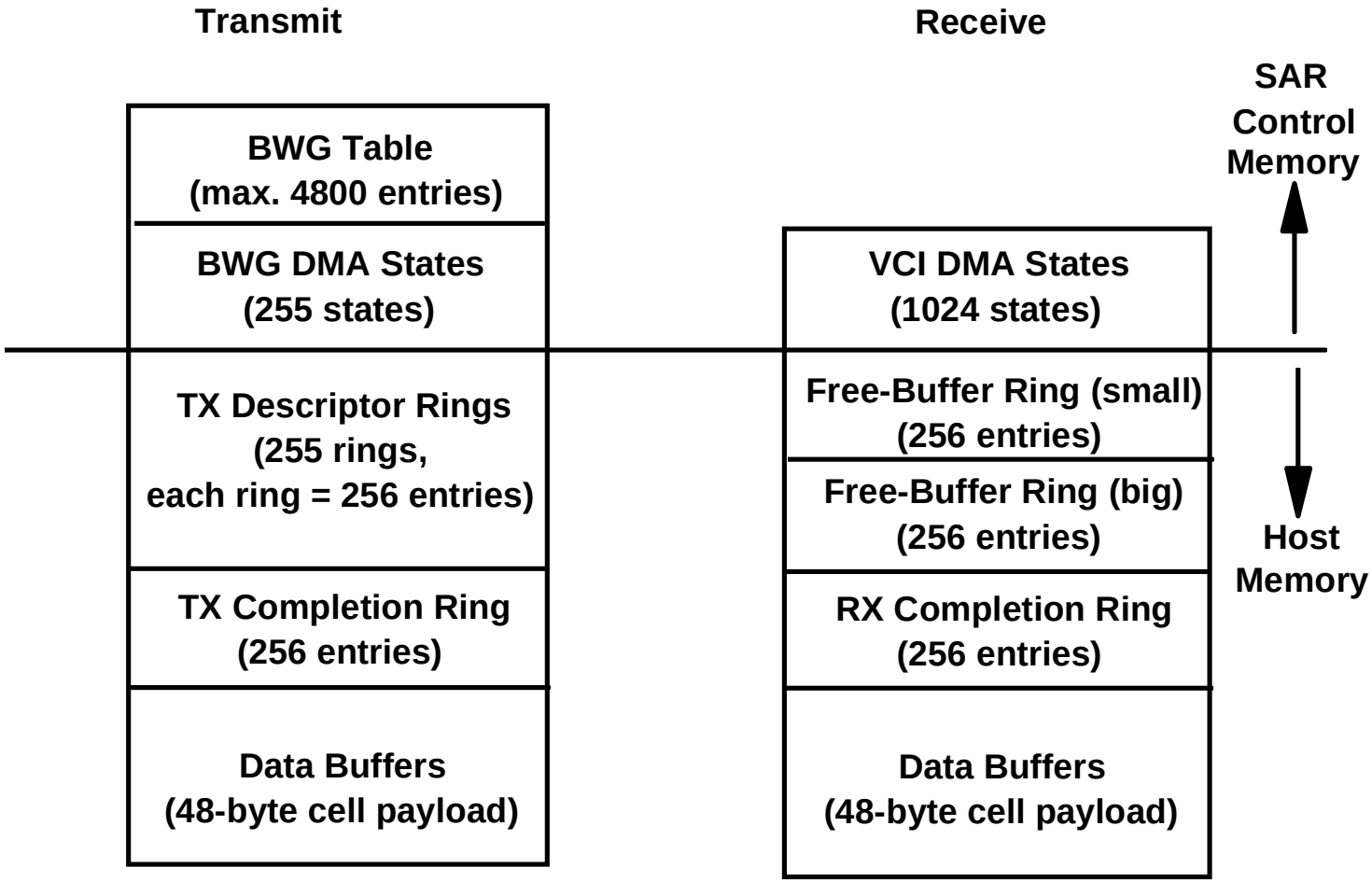
Control Memory Interface and Arbitration

- **The control memory interface and arbitration (CMIA) block imposes a strict priority mechanism for servicing requests from the various blocks, as follows:**
  - **RALP**
  - **XALP**
  - **Cell actuator**
  - **RBTP**
  - **SBTP**
  - **SBIN**
  - **Each access is a one-word access**

SBus SAR Data Structures



Host Memory Data Structures



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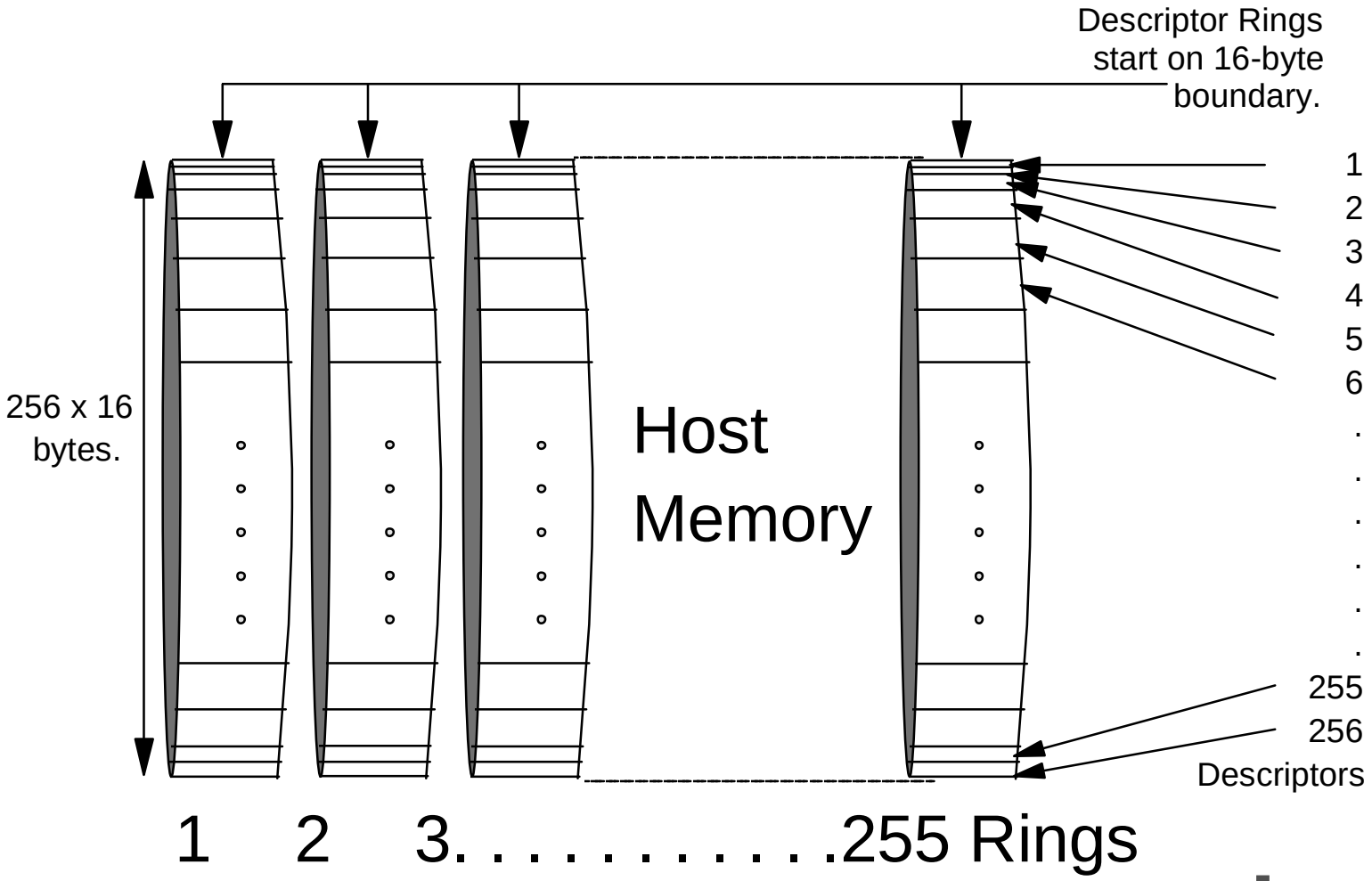
TX Descriptor Rings



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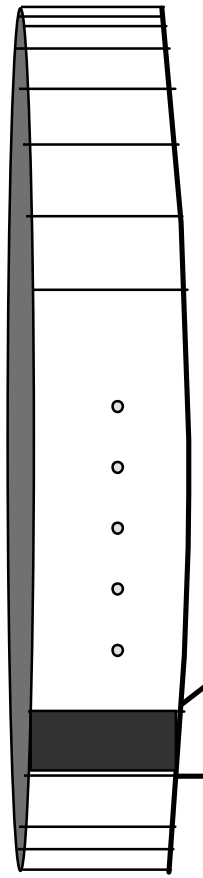
TX Descriptors

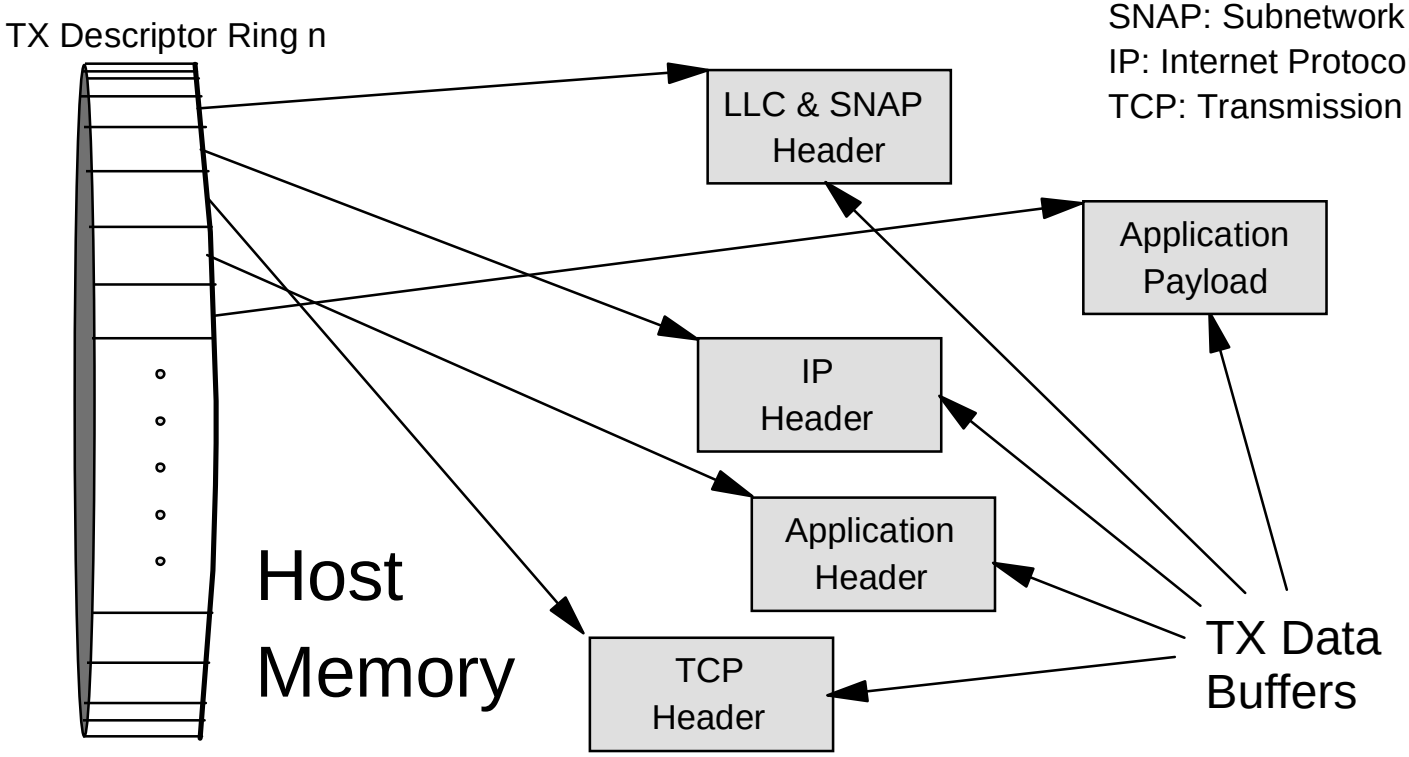


- **Efficient data structures for optimum performance**
- **OWN bit is MSB**
- **Start-of-chain, end-of-chain indications**
- **64K-byte buffers supported**

ENTRY	DESCRIPTION
Word 0	Control field, packet length, buffer length
Word 1	Start-of-buffer pointer – 32 bits
Word 2	4-byte ATM header
Word 3	AAL5 Tail – control and length fields

TX Descriptors

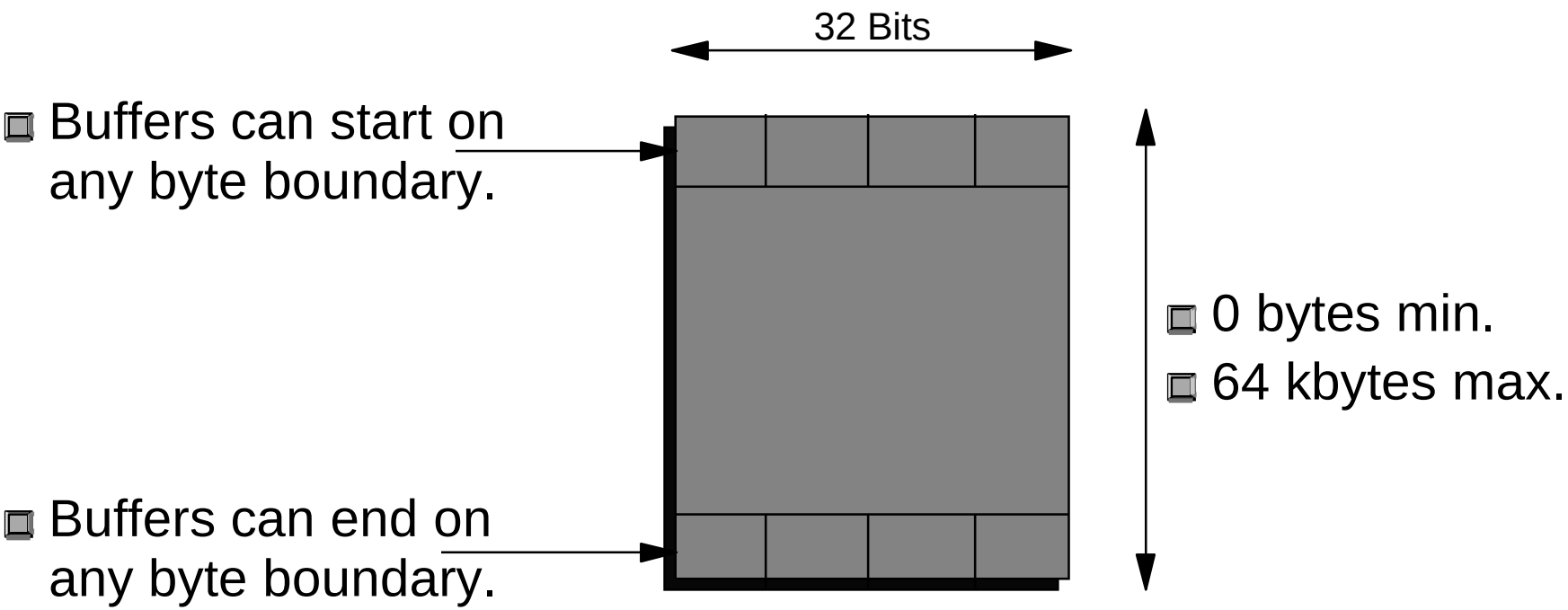
LLC: Logical Link Control
SNAP: Subnetwork Access Protocol
IP: Internet Protocol
TCP: Transmission Control Protocol



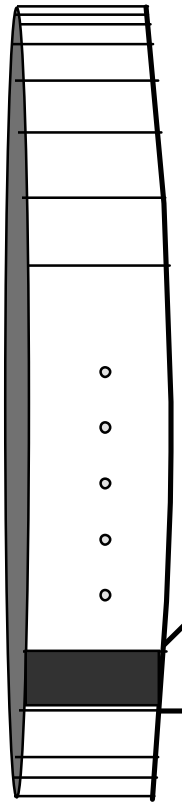
- **Descriptor word 1, start-of-buffer pointer – 32 bits**
- **Buffers can be chained in host memory**

TX Data Buffers

Flexible transmit data buffer structures provide for efficient software.



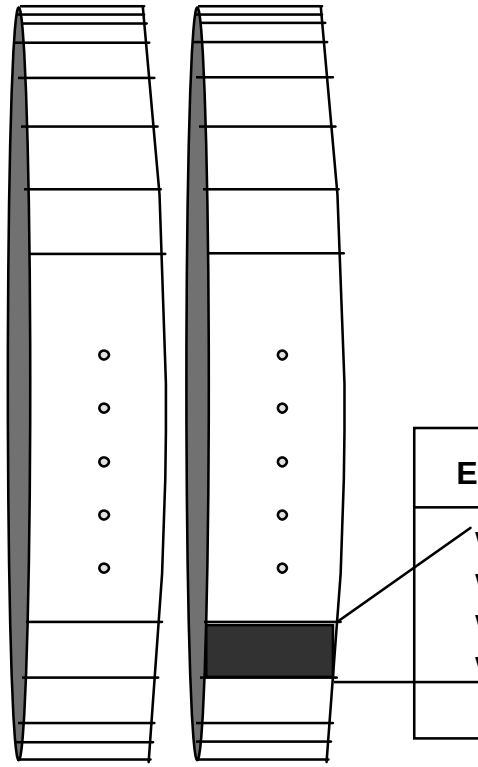
TX Completion Rings



- **Single transmit completion ring**
- **256 entries**
- **Indicates transmission complete**
- **Single descriptor for each packet sent**

ENTRY	DESCRIPTION		
Word 0	Own (31)	Unused (30:8)	BWG index (7:0)
Word 1		Reserved	
Word 2		Reserved	
Word 3		Reserved	

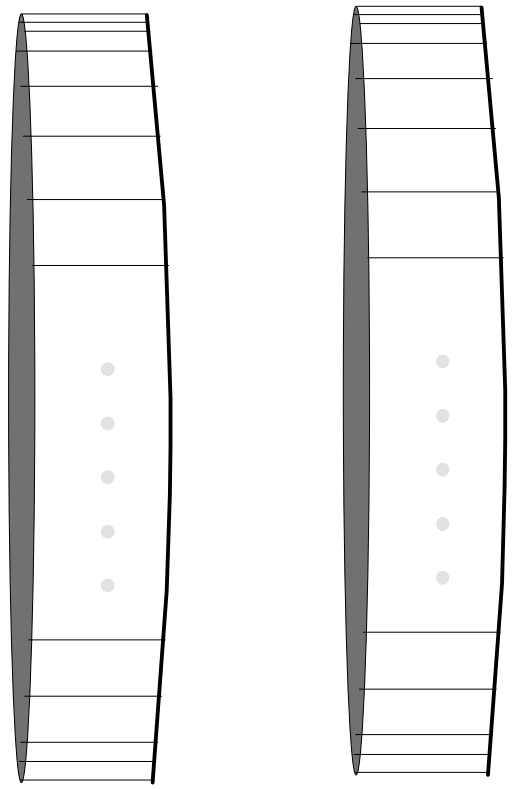
RX Free-Buffer Rings



- **Two free receive buffer rings**
- **Each ring has 256 entries**
- **Use of each ring is application-specific**
- **Example: use one as large and one as small buffer ring**

ENTRY	DESCRIPTION		
Word 0	Own (31)	Unused (30:28)	Start-of-buffer pointer (27:0)
Word 1		Reserved	
Word 2		Reserved	
Word 3		Reserved	

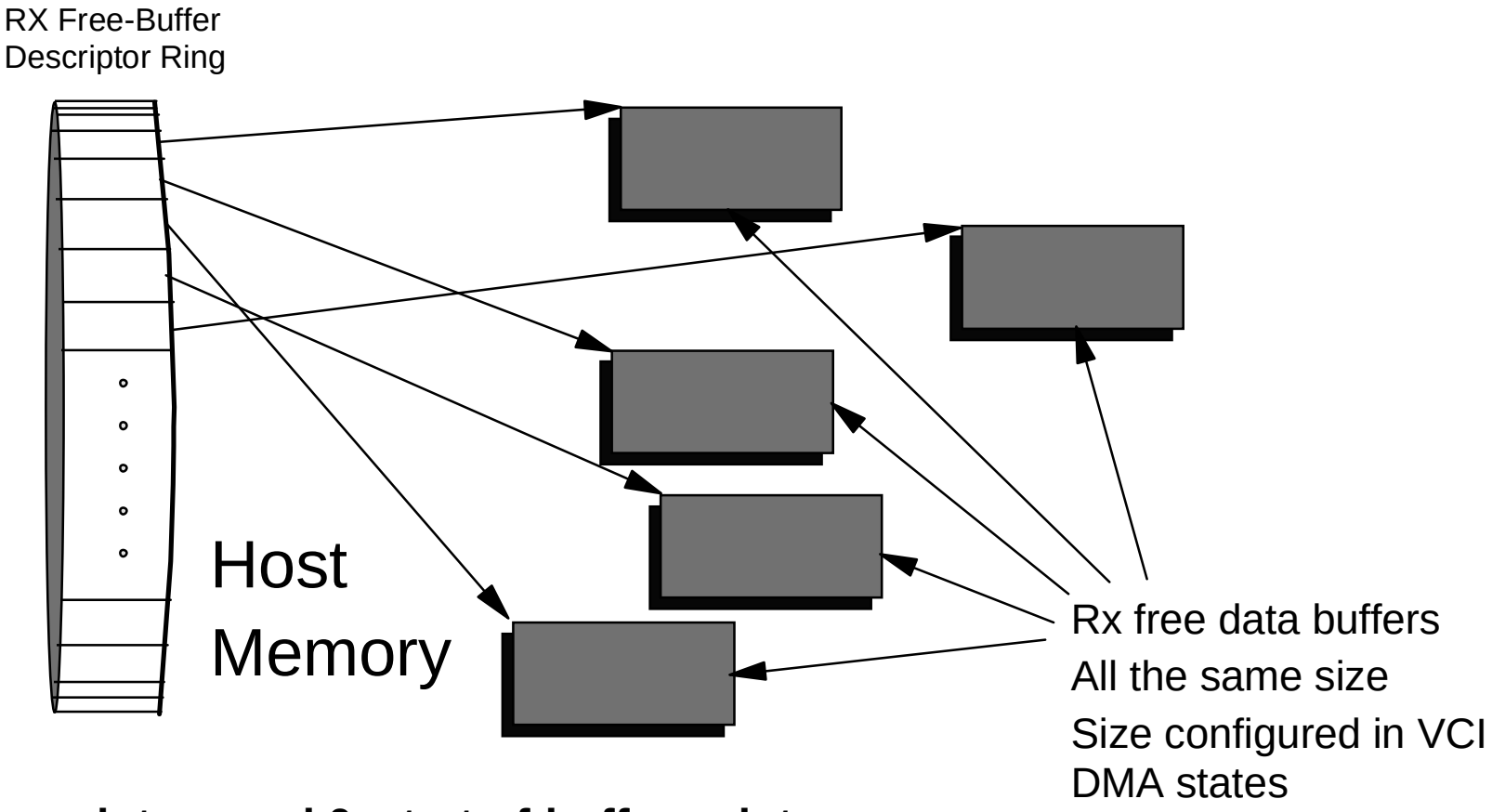
RX Free Buffer Rings Example



Small Buffer Ring Large Buffer Ring

- **Example: use of large/small buffer rings**
- **Small buffer-ring points to 48-byte buffers for constant-bit rate services**
- **Large buffer ring points to 8k-byte buffers for TCP/IP-based applications**
- **VCs set up for CBR applications use small buffer ring**
- **VCs set up for TCP/IP applications use large buffer ring**

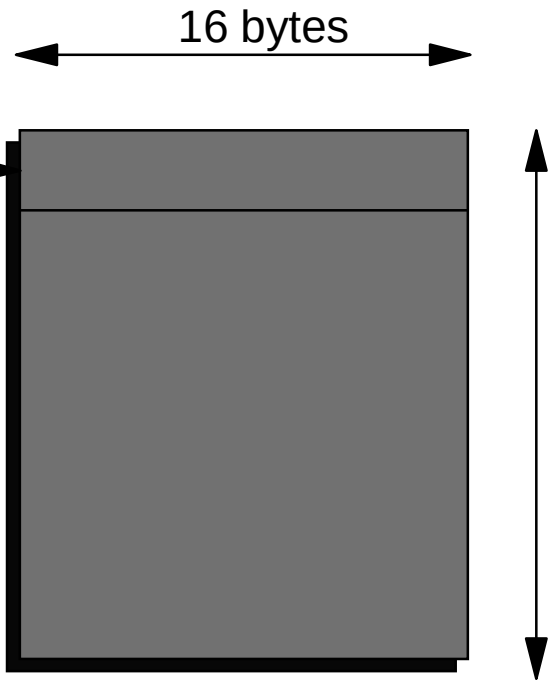
RX Free-Buffer Rings



- **Descriptor word 0, start-of-buffer pointer.**
- **Buffers located in host memory, same size for each ring.**

RX Data Buffers

- Buffers start on 16-byte boundary.



- 48 bytes min.
- 64K bytes max.
- It is efficient to make buffer lengths multiples of 48 bytes.

- **Buffer lengths must all be equal for a given ring and are configurable at initialization time.**

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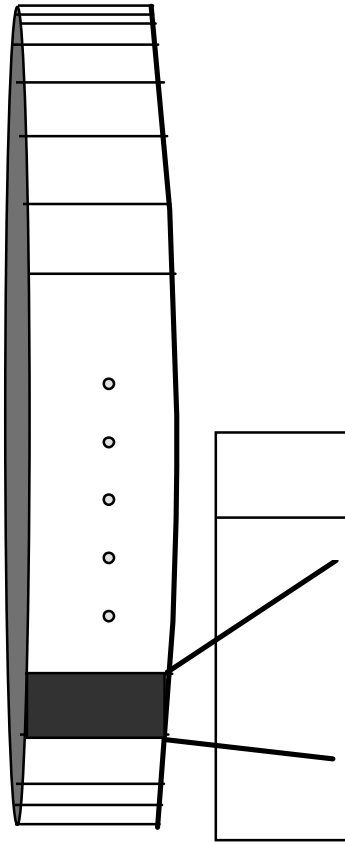
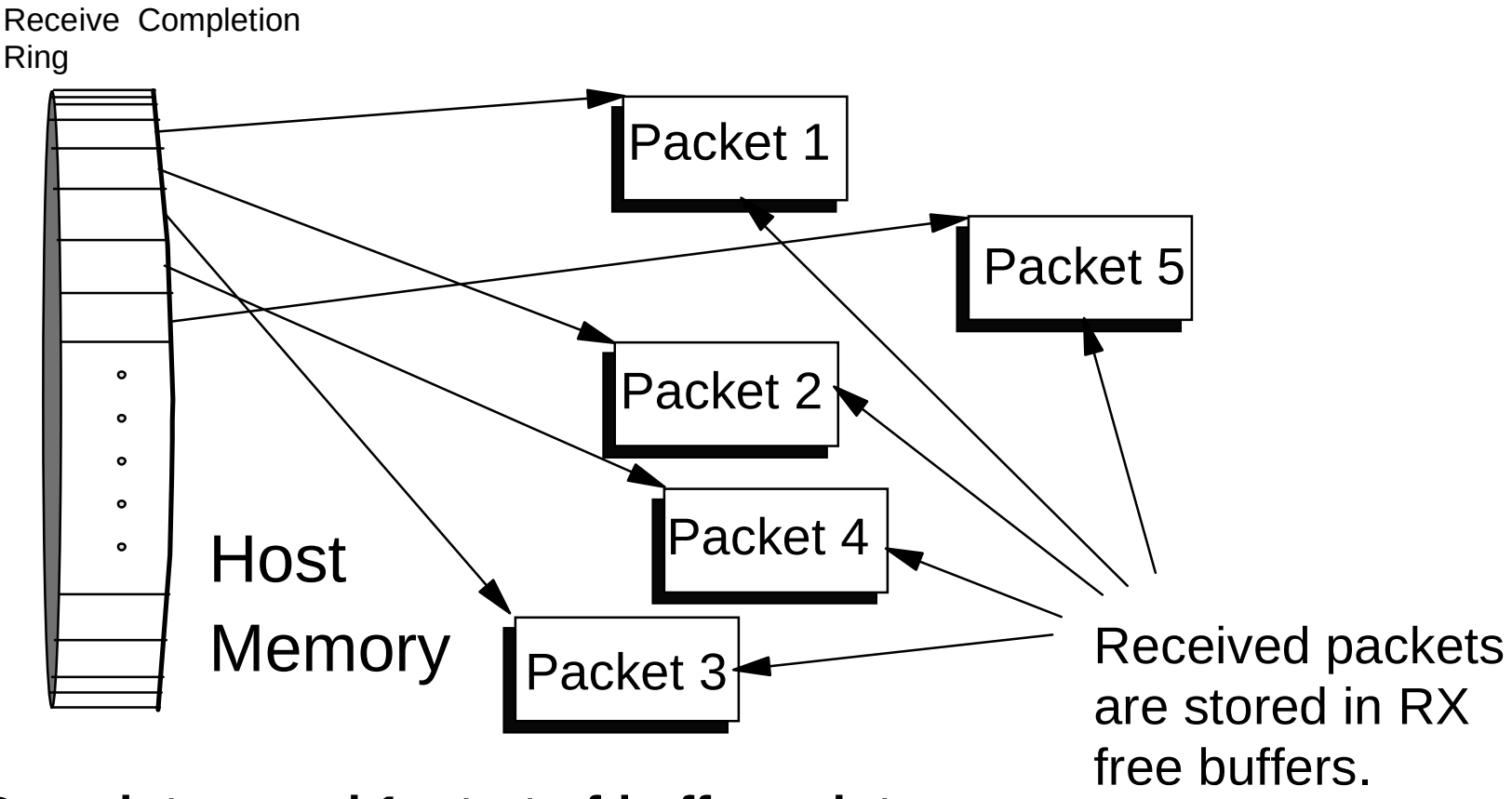
RX Completion Ring



- **Single receive completion ring**
- **256 entries**
- **Indicates packet reception complete**
- **Single descriptor for each packet received**

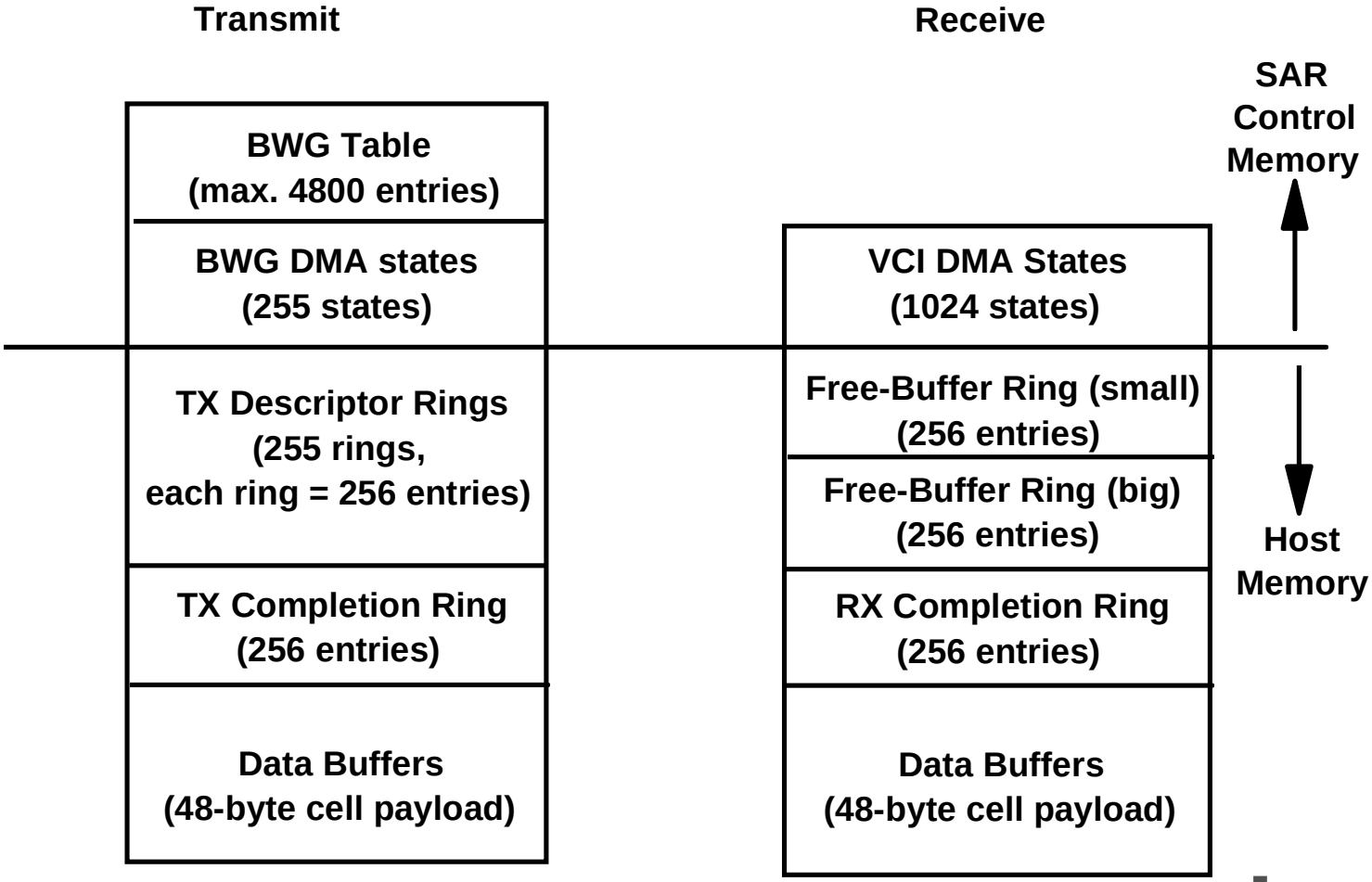
ENTRY	DESCRIPTION
Word 0	Control field, EFCN cells received, packet length
Word 1	Start-of-buffer pointer – 28 bits
Word 2	4-byte ATM header
Word 3	Reserved

RX Completion Ring



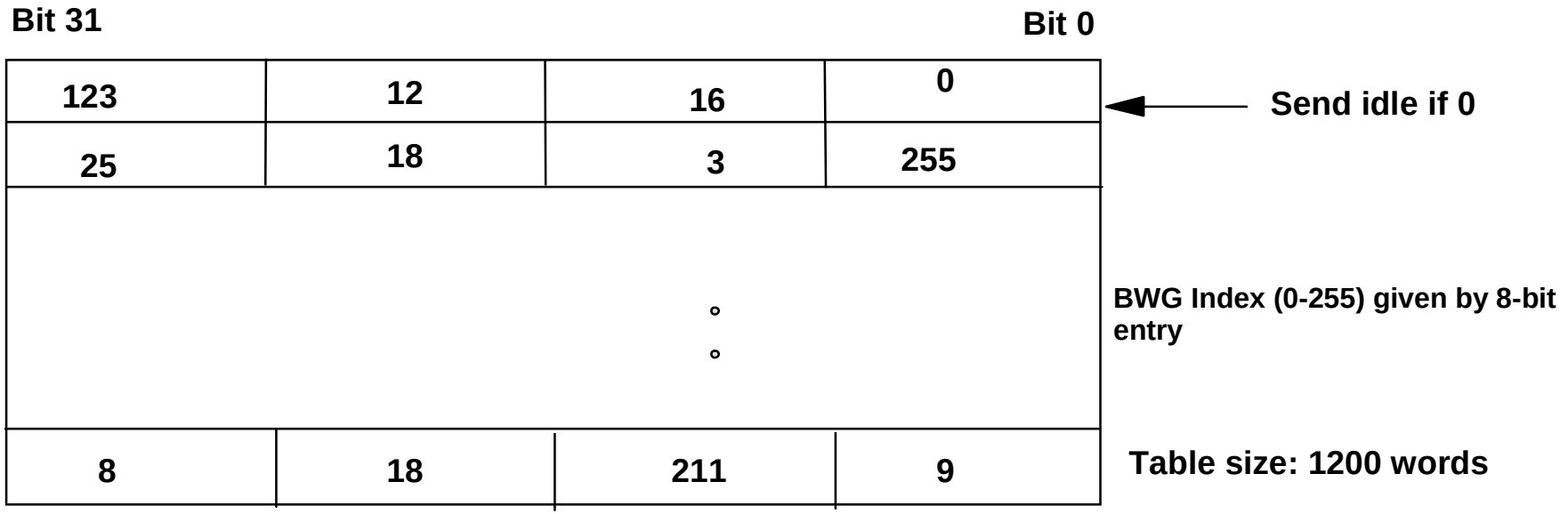
- **Descriptor word 1, start-of-buffer pointer**
- **Received packets must fit in single buffer for reception.**

Control Memory Data Structures



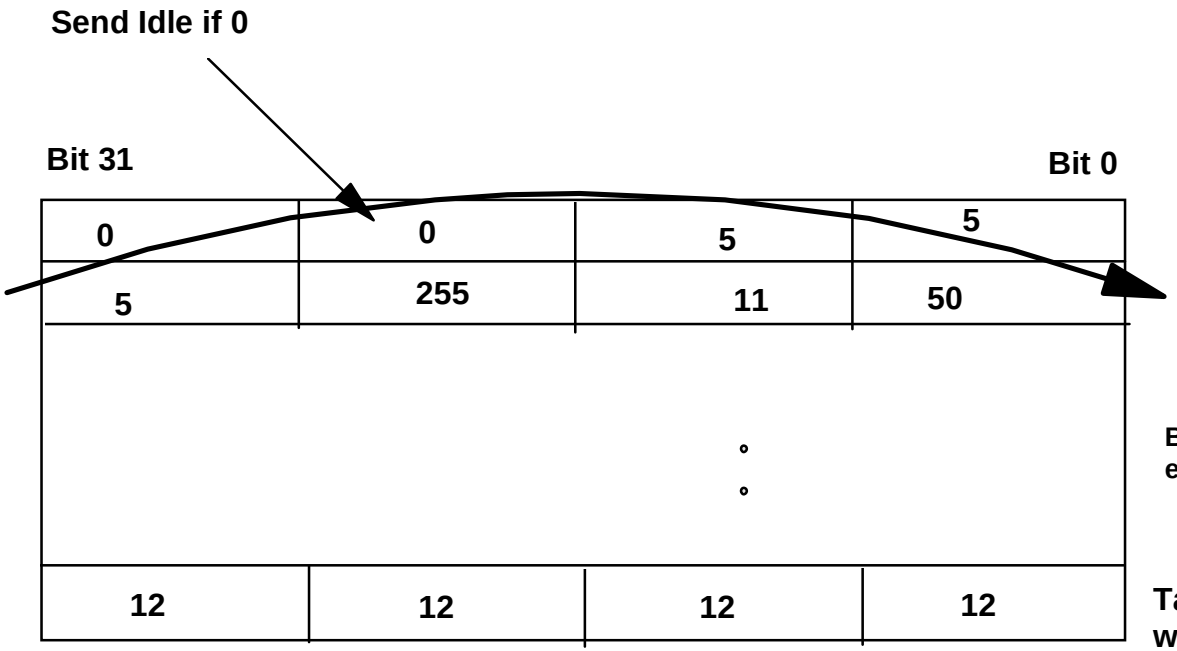
BWG Table

- **The bandwidth group (BWG) control table provides for special bit rate control.**
- **The BWG table is programmable, with a maximum of 4800 entries.**
- **Each entry consists of an 8-bit BWG index.**



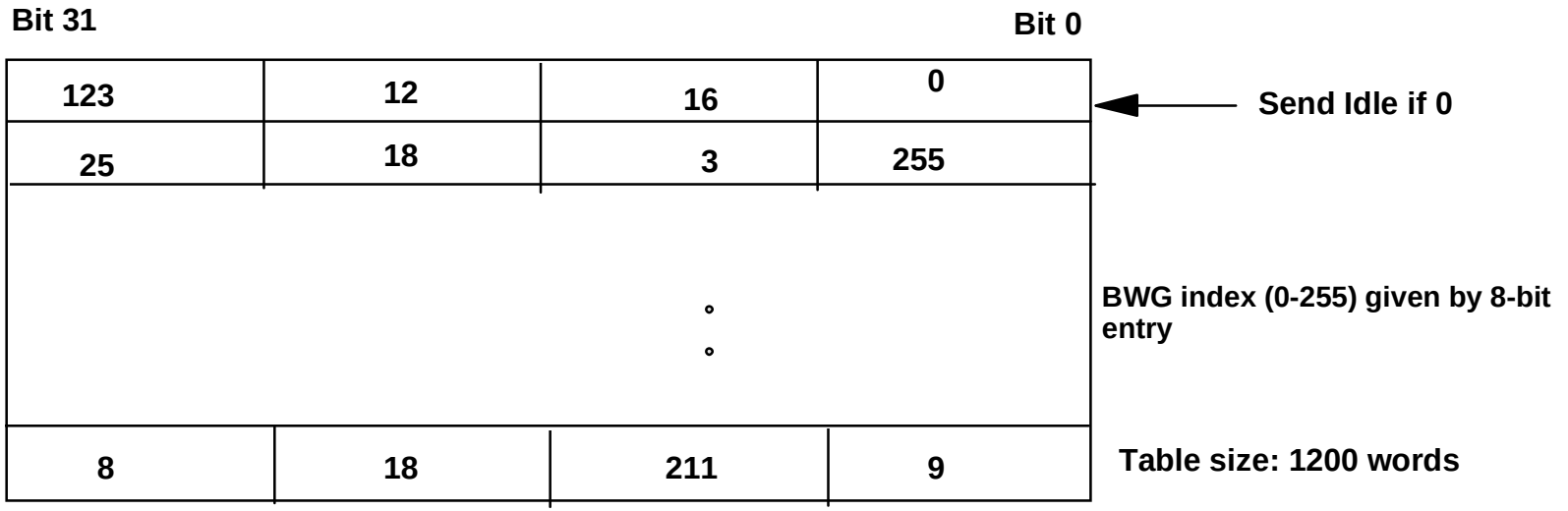
BWG Table Mechanism

- **Each entry must be assigned to a bandwidth group by inserting a BWG index into each entry.**
- **BWG index indicates which transmit descriptor ring should be processed.**
- **BWG index zero indicates idle cells should be sent.**



BWG Table Mechanism

- **Used to allocate a bandwidth to a bandwidth group.**
- **155 Mbit/s / 4800 provides for a granularity of 32 kbit/s.**
- **Bandwidth available to application is approx. 135.63 Mbit/s*. (155.52 less SONET and ATM overhead)**
- **136 Mbit/s / 4800 provides for a granularity of 28,250bit/s*.**



* Figures calculated assuming null AAL; i.e., no AAL overhead is included.

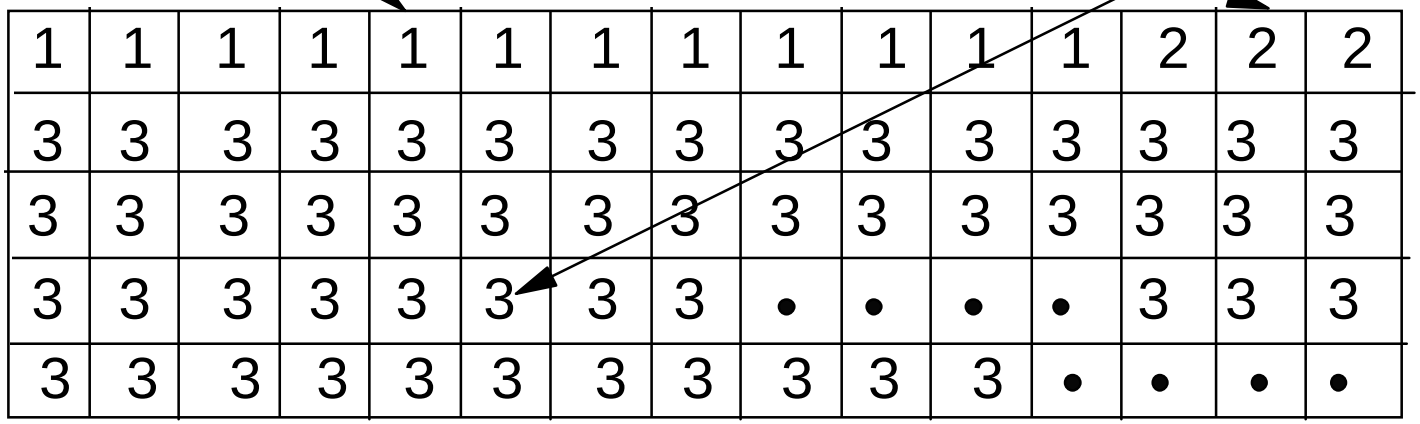
BWG Table Example

- **Application 1 requires 0.32Mbit/s and uses BWG 1**
- **Application 2 requires 64 kbit/s and uses BWG 2**
- **Application 3 requires 10 Mbit/s and uses BWG 3**

Write 1 (for BWG 1) in BWG table 12 times. (12 x 28250 > 0.32Mbit/s)

Write 2 (for BWG 2) in BWG table 3 times. (3 x 28250 > 64kbit/s)

Write 3 (for BWG 3) in BWG table 254 times. (254 x 28250 >10Mbit/s)



1	1	1	1	1	1	1	1	1	1	1	1	2	2	2
3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
3	3	3	3	3	3	3	3	•	•	•	•	3	3	3
3	3	3	3	3	3	3	3	3	3	3	•	•	•	•

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BWG DMA States

- 255 BWG DMA entries, eight words in size, for each of the transmit DMA channels.
- Used as a work area for the DMA state machine.
- Highlight indicates entry copied from transmit descriptor.
- Word 3 is the only host programmable entry.

ENTRY	DESCRIPTION	STATIC/ DYNAMIC
Word 0	Control field, packet length, buffer length	Dynamic
Word 1	Current buffer pointer – 32 bits	Dynamic
Word 2	4-byte ATM header	Dynamic
Word 3	Static bits – BWG on/off	Static
Word 4	BWG data ring pointer, descriptor pointer	Dynamic
Word 5	BWG cell counter place holder – not implemented	Dynamic
Word 6	Partial 32-bit packet CRC	Dynamic
Word 7	AAL5 tail – control and length fields	Static

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VCI DMA States

- **1024 VCI DMA entries, eight words in size, for each of the receive DMA channels**
- **Used as a work area for the DMA state machine**
- **Highlight indicates entry copied from receive free ring**
- **Word 3 is only host-programmable entry**

ENTRY	DESCRIPTION	STATIC/ DYNAMIC
Word 0	Control, status, EFCN cell count, current packet length	Dynamic
Word 1		Dynamic
Word 2	**Current buffer pointer - 28 bits**	**Static**
Word 3	Start-of-buffer pointer - 28 bits	Static
Word 4	Control, packet length	
Word 5	Reserved	Dynamic
Word 6	AAL5 partial CRC - 32 bits	
Word 7	Reserved	
	Reserved	

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VCI DMA States Configuration

- **VC_ON: Enables packet reassembly processing**
- **Buffer type: Small or big**
- **Null AAL indication: Configure VC for null AAL**
- **AAL3/4 indication: Configure VC for AAL 3/4**
- **AAL packet length: Length of receive free buffers**

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SBus SAR Functional Overview

- Packet interface
- AAL5 processing
- AAL3/4 processing
- Null AAL processing
- OAM processing
- Address mapping
- Transmit operation
- Receive operation

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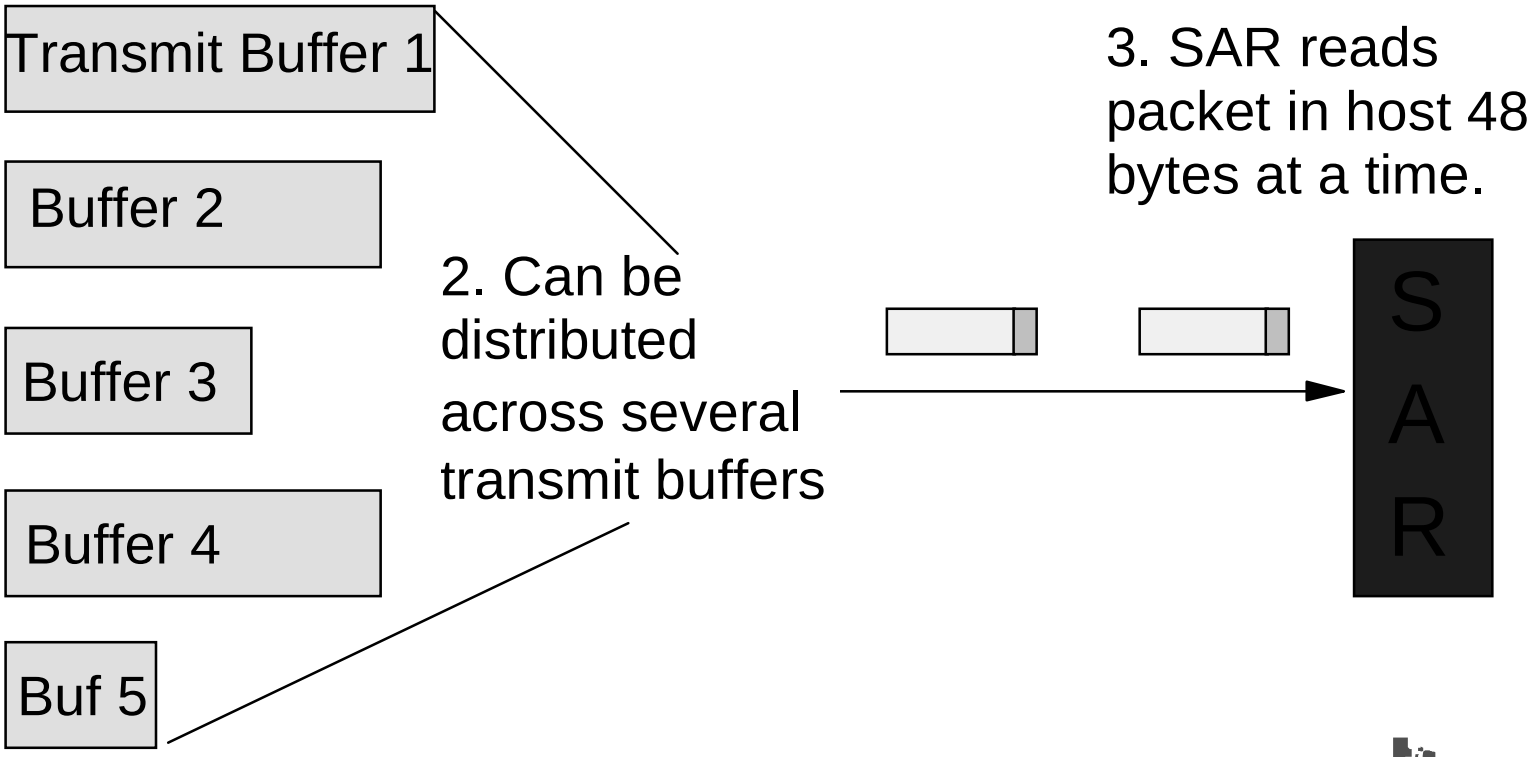
Packet Interface

- **SBus SAR uses host memory to store 48-byte payload units constituting a packet for both transmit and receive.**
- **The device initiates the transfer of these 48-byte payload units.**
- **Each packet queued for transmission can be distributed across multiple buffers.**
- **Each packet received from ATM is placed in a single receive buffer in host memory.**

Packet Interface Transmit

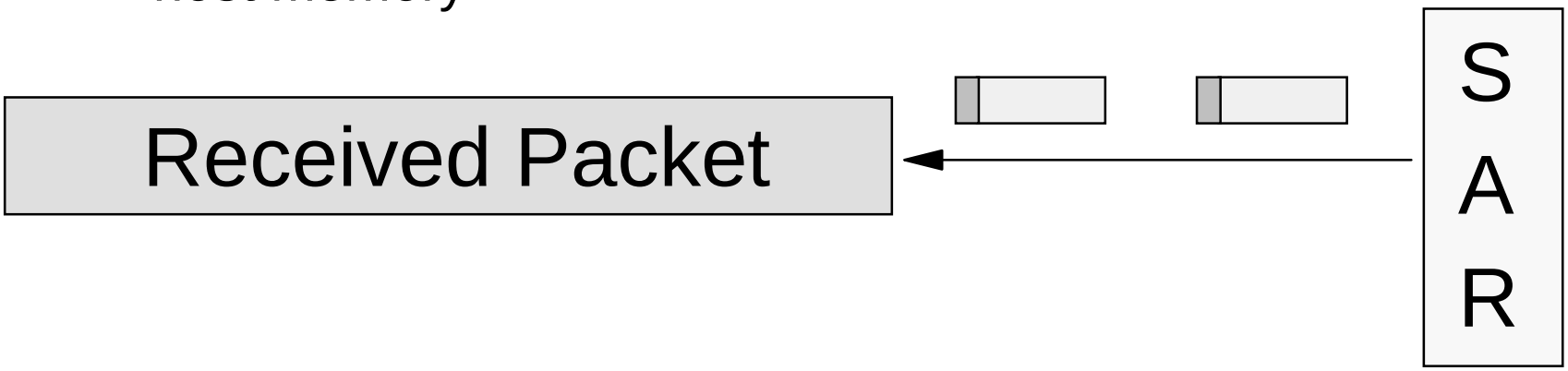
1. Packet in host memory



Packet Interface Receive

2. Received packet stored in a single receive buffer in host memory

1. SAR writes packet to host 48 bytes at a time.



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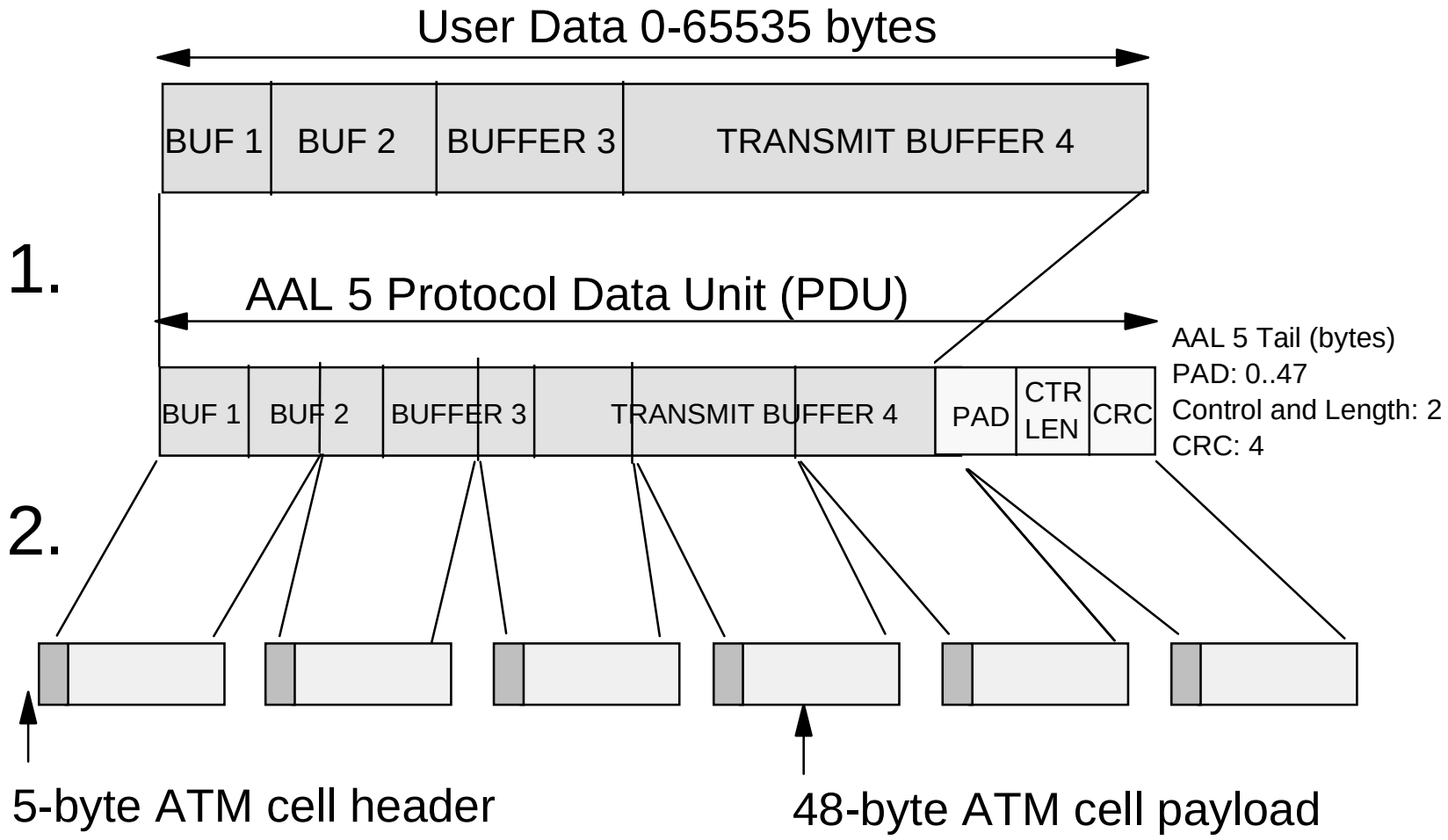
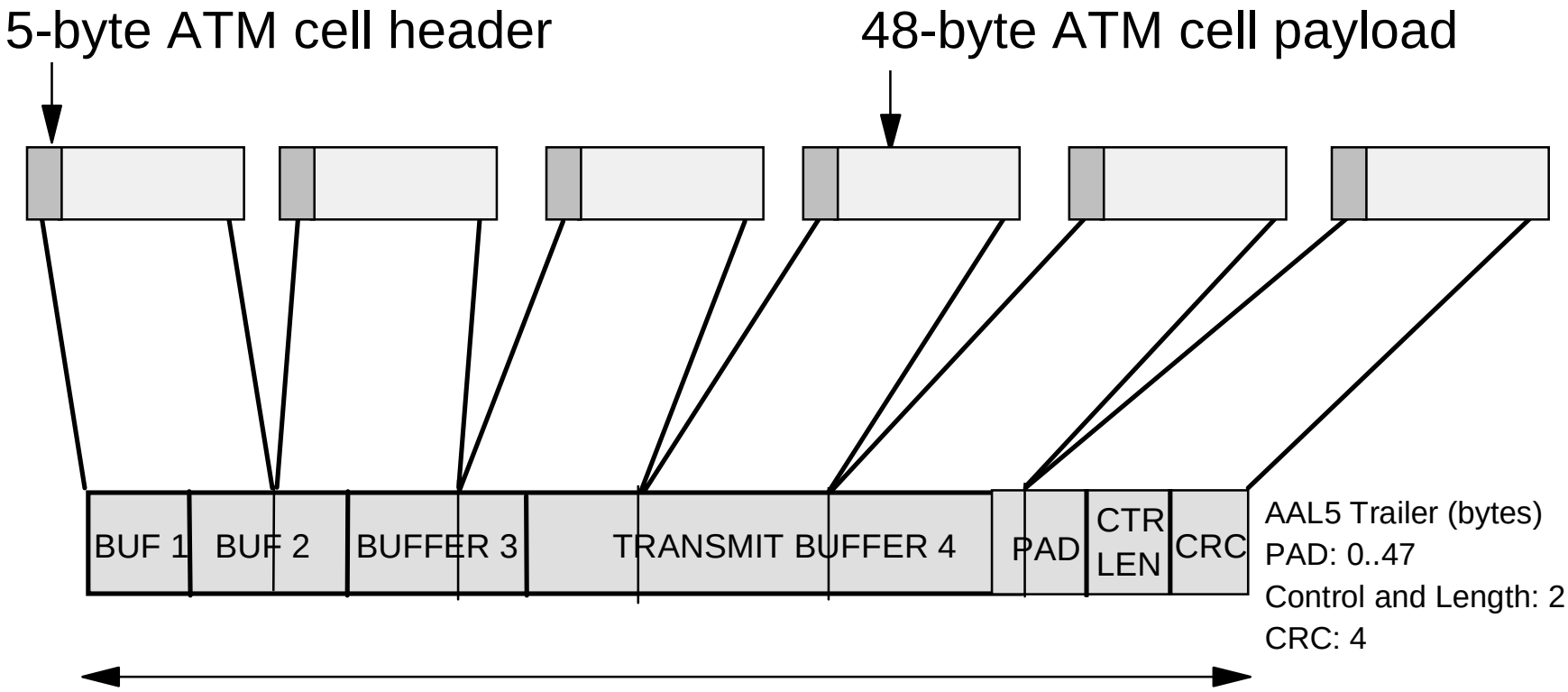
AAL5 Processing

- In-depth support ATM adaptation layer 5 (AAL5)
- AAL5 encapsulation in the transmit direction
  - SAR computes and adds AAL5 protocol trailer
  - SAR segments AAL5 packet into 48-byte ATM payloads and adds ATM cell header
- AAL5 termination in the receive direction
- SAR computes and checks AAL5 CRC
- SAR places entire AAL5 packet in host memory
- Interrupt given for end of packet (AAL5)

AAL5 Encapsulation



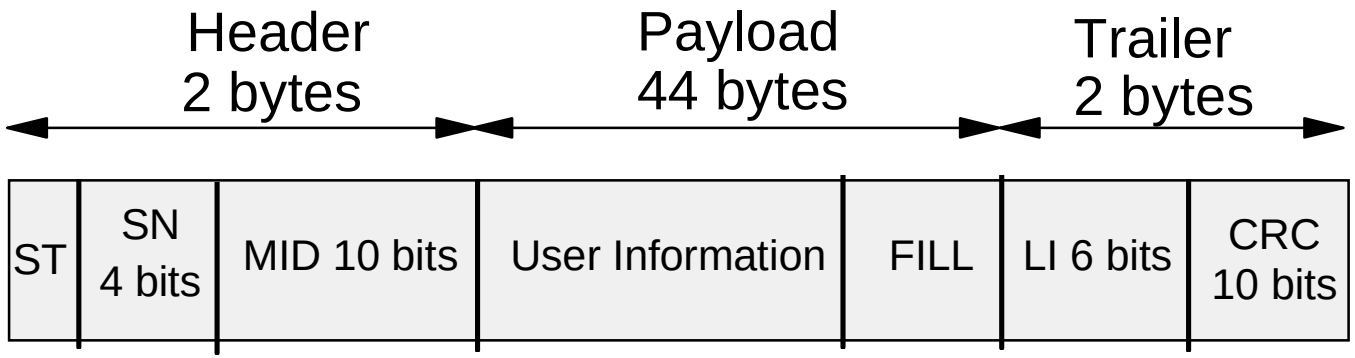
AAL5 Termination



AAL5 Protocol Data Unit (PDU) in Host Memory

AAL3/4 Processing

- **In the transmit direction, AAL5 processing is turned off, in the transmit-buffer descriptors, for AAL3/4 traffic.**
- **All AAL3/4 data packet processing is performed on the host in software.**
- **AAL5 processing is disabled on those VCIs configured for using AAL3/4.**
- **The AAL3/4 end-of-message (EOM) indicator is recognized by the SAR, initiating an interrupt.**



ST: Stream Delimiter
SN: Sequence No.
MID: Multiplex ID
LI: Length ID
CRC: Checksum

Structure of AAL 3/4 PDU

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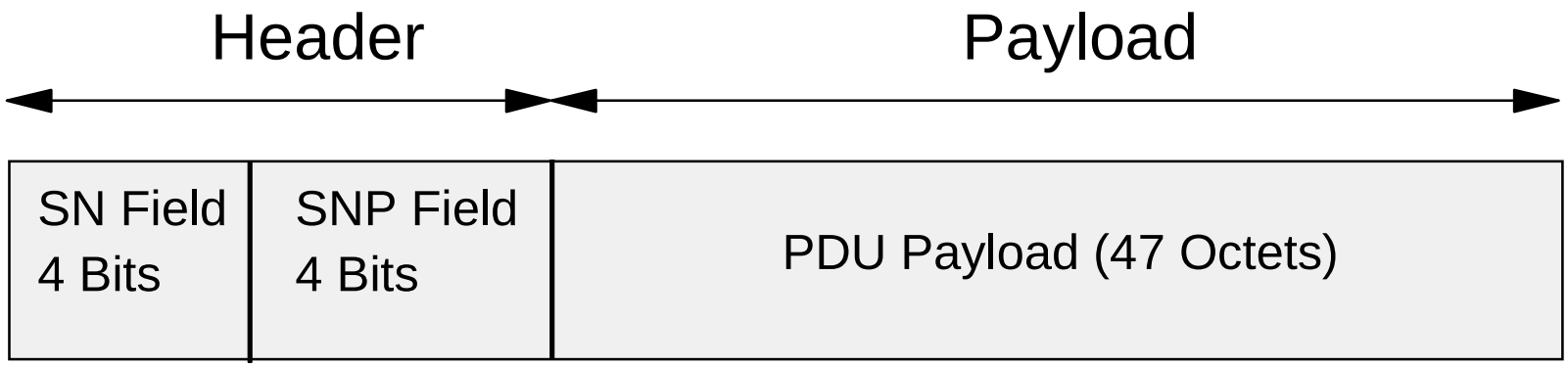
Null AAL Processing

- In the transmit direction, AAL 5 processing is turned off, in the transmit-buffer descriptors for null AAL traffic.
- Null AAL processing is configured for receive direction in the VCI bandwidth group DMA block.
- This bandwidth group is also configured to issue an interrupt after a set number of cells have been received.
- Constant-bit-rate (CBR) services could be implemented using the null AAL feature.

Null AAL Processing Constant-Bit-Rate Example

- **Set up a transmit channel for sending out CBR data in single ATM cells (48-byte payload). Use null AAL.**
- **Set up a receive channel for receiving CBR data in single ATM cells using null AAL (packet count equals one cell).**
- **With these features, AAL1 emulation can be implemented in software.**



Structure of AAL 1 PDU

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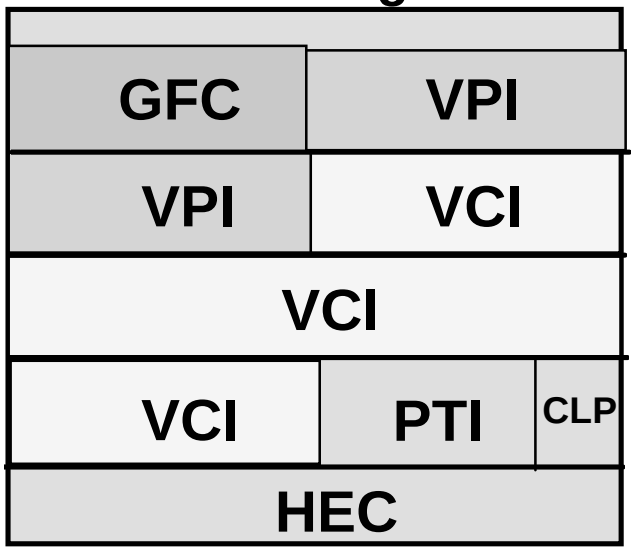
OAM Processing

- **The SBus SAR recognizes all operations and maintenance (OAM) flows; cells are added to the receive complete ring.**
- **VP-level OAM cells are received on VCI 3 and 4 DMA channels (VCI 3 and 4 need to be configured as Null AAL channels).**
- **VC-level OAM cells are diverted to receive DMA channel 0.**

NO.	ITEM	VCI	PTI
1	VP level: link-associated OAM cell	3	--
2	VP level: end-to-end OAM cell	4	--
3	VC level: link-associated OAM cell	Any	4
4	VC level: end-to-end OAM cell	Any	5

Address Mapping

- **The lower 10 bits of the VCI field are used to encode the 1023 possible VCIs that are supported by this device.**
- **The upper-order bits of the VCI and the VPI field are programmable on a per-VC basis for transmit.**
- **The GFC field is always zero.**
- **The upper-order bits on the VCI, the VPI field, and the GFC field are ignored on all cells that are received.**



The ATM UNI Cell Header

GFC: Generic flow control
VPI: Virtual path identifier
VCI: Virtual channel identifier
PTI: Payload type identifier
CLP: Cell loss priority
HEC: Header error control

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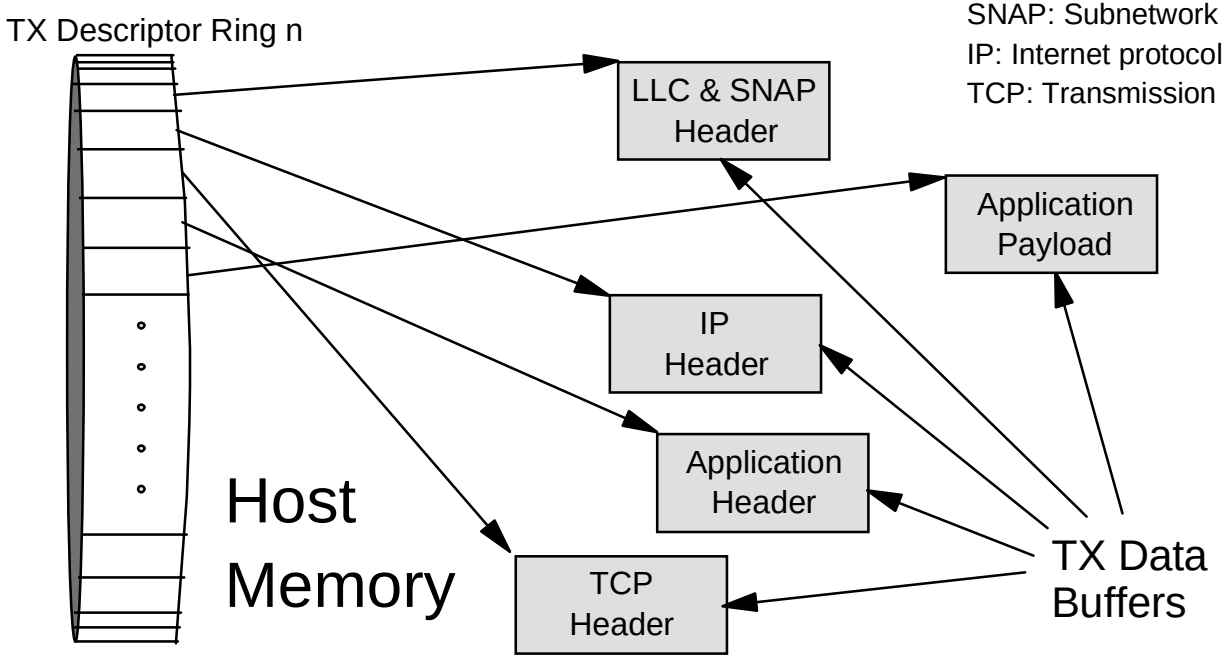
Address Mapping (cont.)

- Note that if bits in these fields are set, then:
  - Such cells would only be passed to the SAR if the HEC field is correct.
  - Hence, the upper-order bits are correct and the cell was intentionally routed to the SAR, or...
  - The cell was misrouted, the probability of which is small. (Such an event would be detected by a CRC failure at the AAL5 or AAL3/4 layer).
- Hence, the SAR takes advantage of this and supports any VPI/VCI combination as long as the lower 10 bits of the VCI are unique.

Transmit Operation

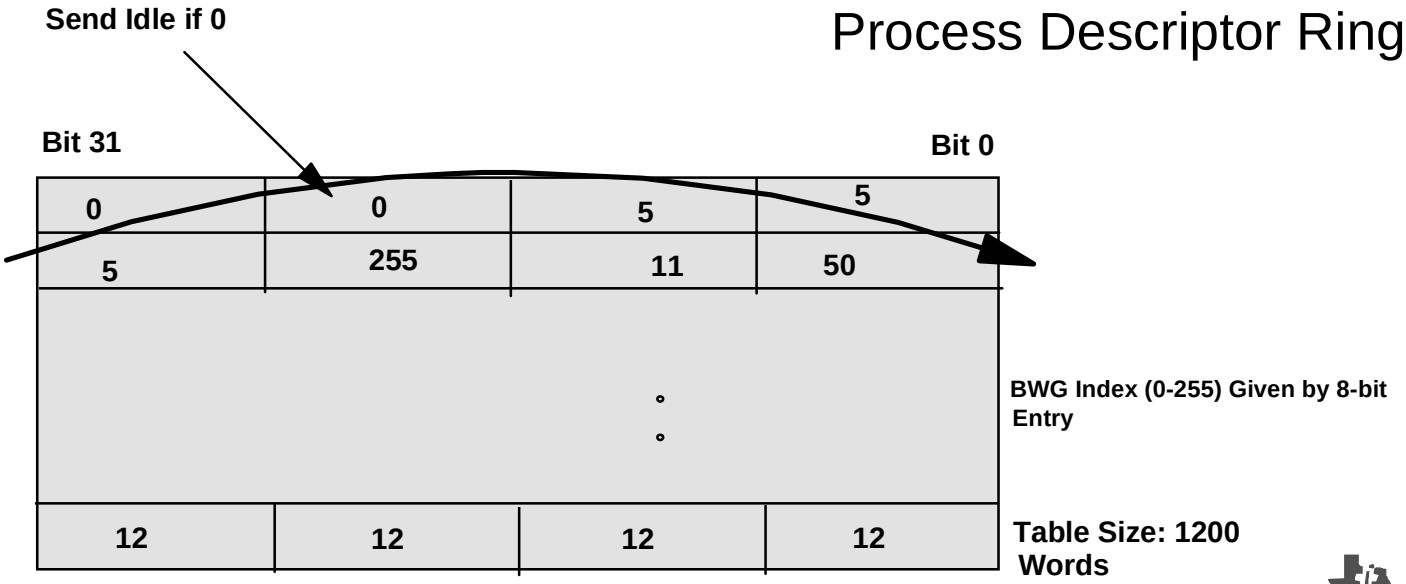
- **Host application places data in host memory.**
- **Host protocol software adds protocol layers.**
- **Host SAR driver builds descriptors in ring n.**
- **SAR driver passes control to SAR when OWN bits are set. Set OWN bits in zipper-up fashion.**

LLC: Logical link control
SNAP: Subnetwork access protocol
IP: Internet protocol
TCP: Transmission control protocol

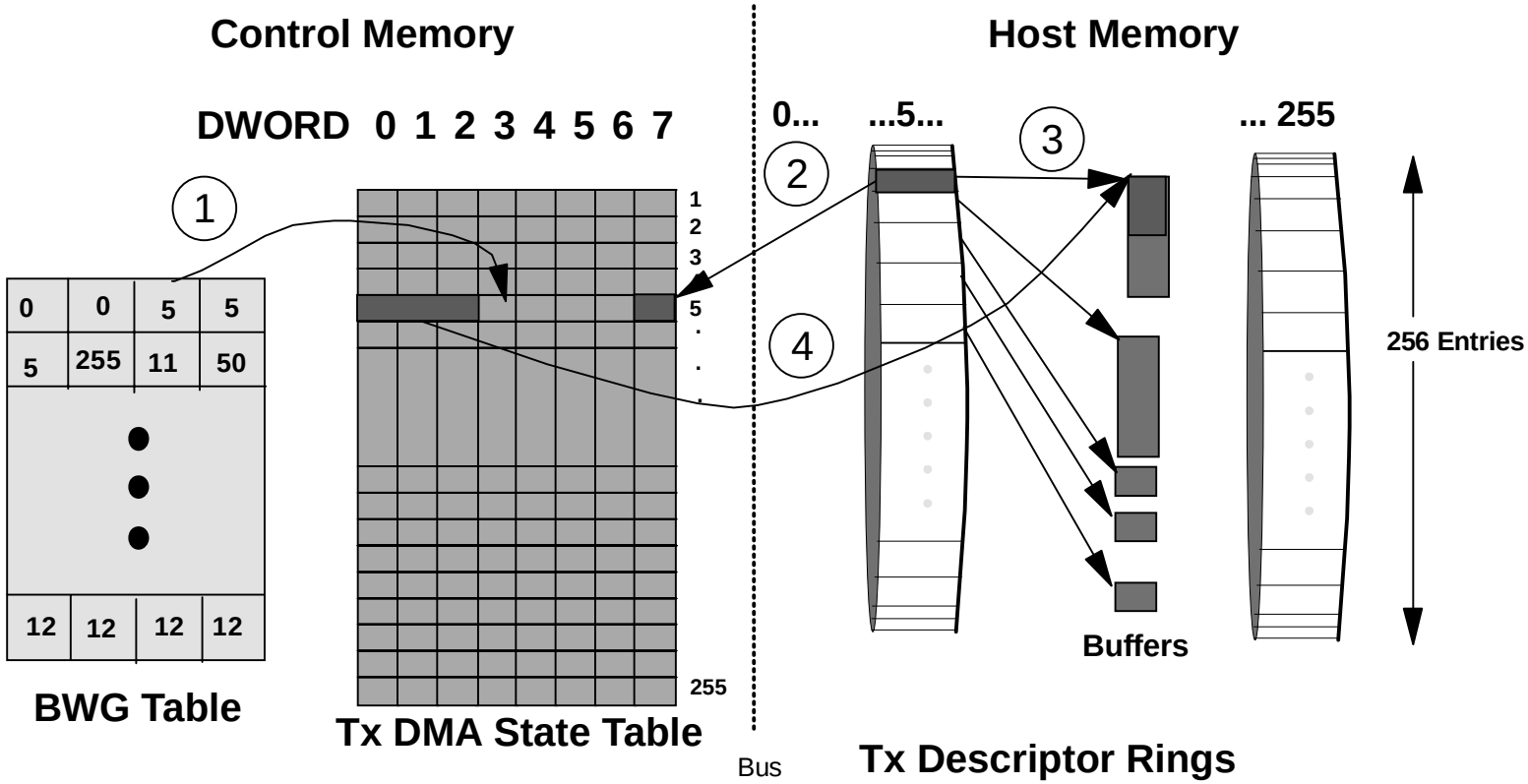


Transmit Operation

- **The SBus SAR cycles through the BWG table.**
- **A single cell is sent for each entry.**
- **Entries contain indexes that reference transmit descriptor rings and transmit DMA blocks.**
- **An index of zero indicates null ATM cells should be generated and transmitted by the SAR (VPI,VCI = 0).**



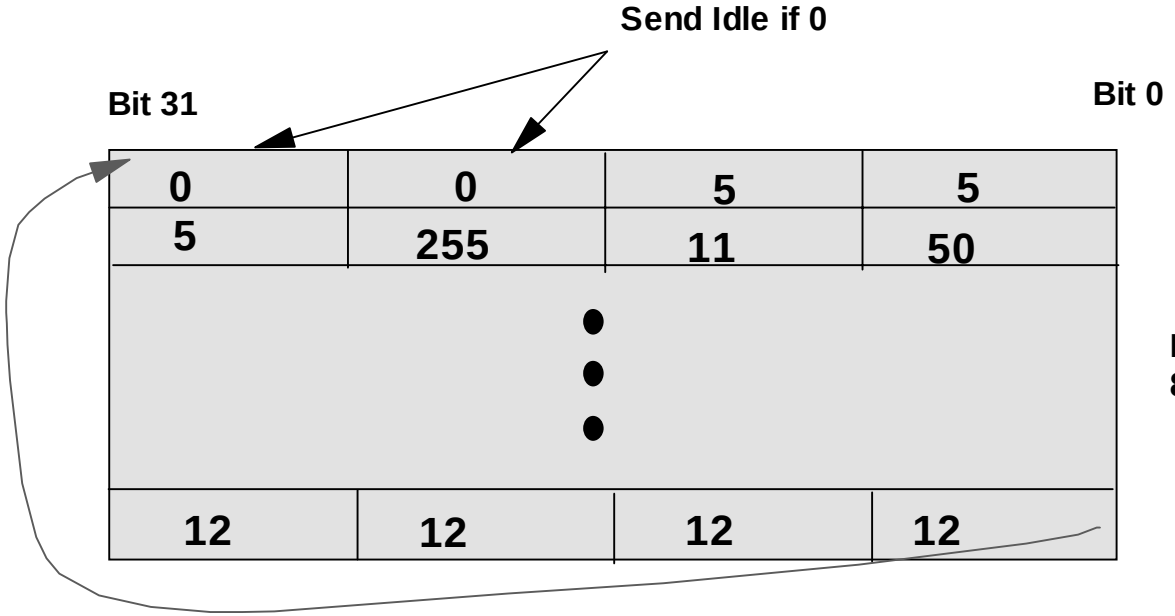
Transmit Operation



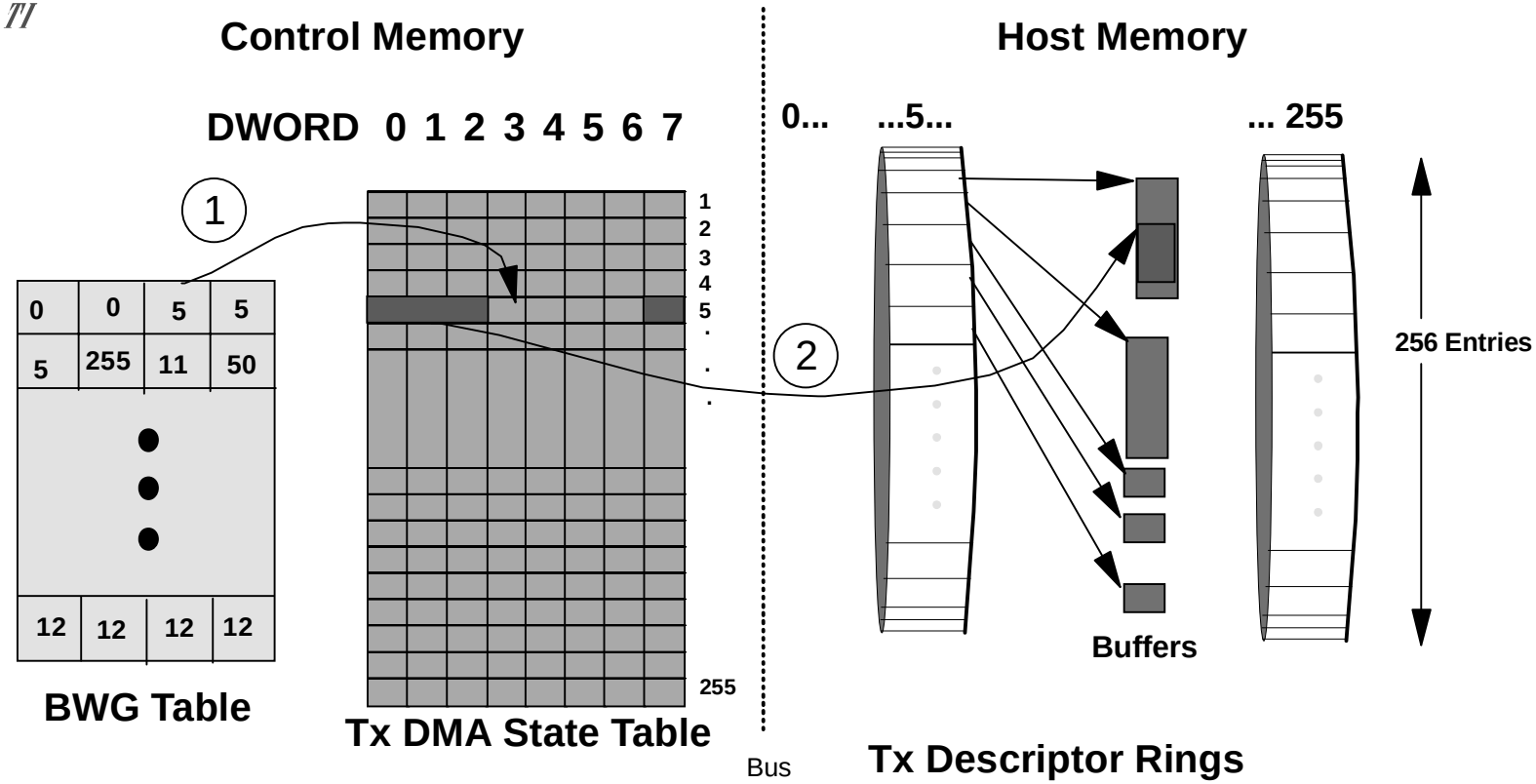
- The SAR cycles through the BWG table. It looks at word 3 for each entry within the BWG state table. If the BWG is turned on, the SAR processes a packet of data.
- The SAR loads the first descriptor into the BWG DMA state table (register 5).
- Four 32-bit words are loaded as illustrated.
- The SAR then reads a single cell payload (48 bytes) from the first TX data buffer.

Transmit Operation

- **The PCI SAR returns to the BWG Table.**
- **The SAR processes the next entry in the ring; for our example, it will process descriptor ring 5 again. If a packet is currently being processed, a single cell is transmitted.**
- **If the ring is empty (OWN bit not set), the SAR sends an IDLE cell and returns to the BWG table to find the next BWG index.**
- **Eventually, the SAR loops around the BWG table and returns to the entry that points to descriptor ring 5.**

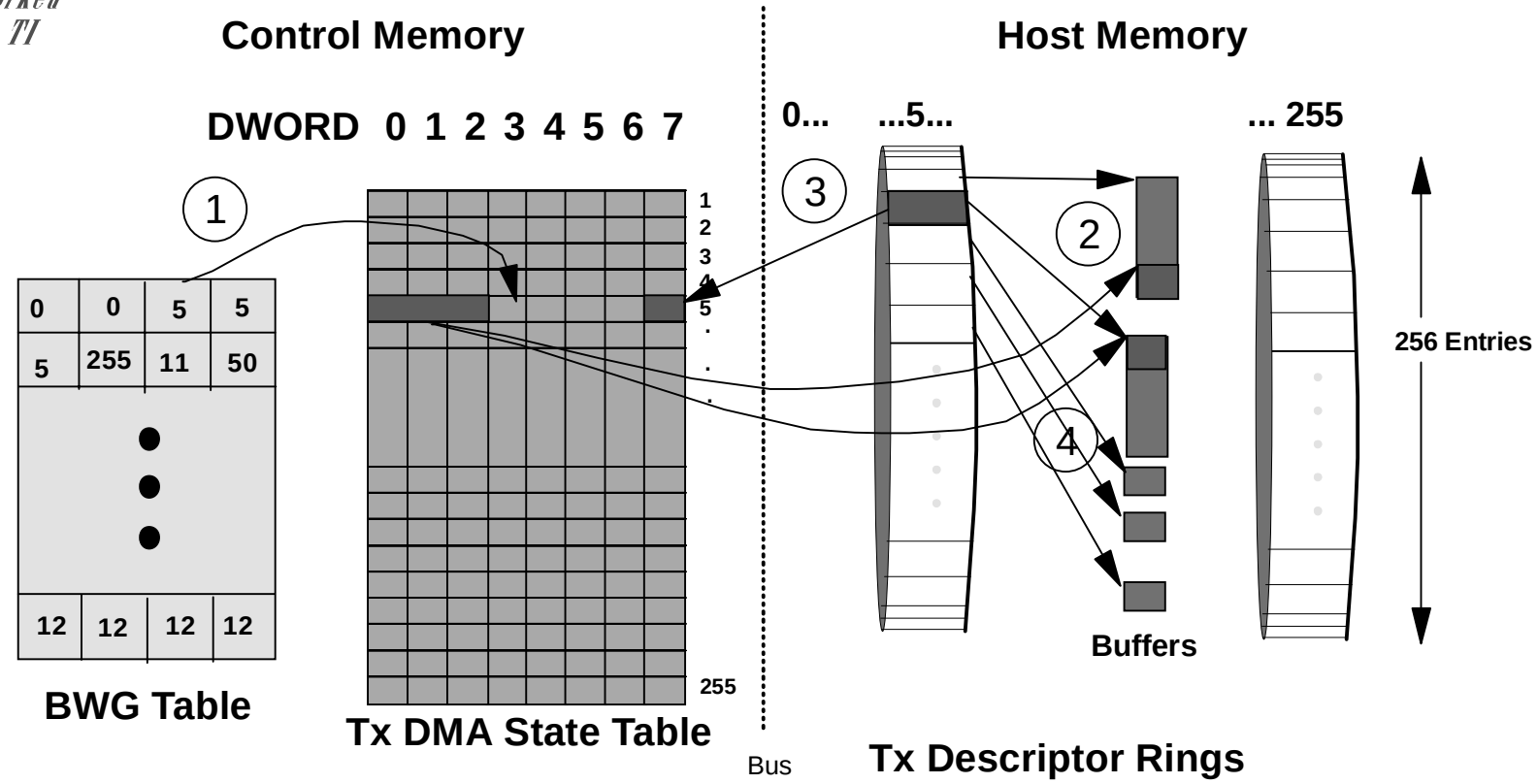


Transmit Operation



- **The BWG DMA state 5 contents indicate a packet currently is being processed.**
- **The SAR then reads another cell payload from the first TX data buffer.**

Transmit Operation

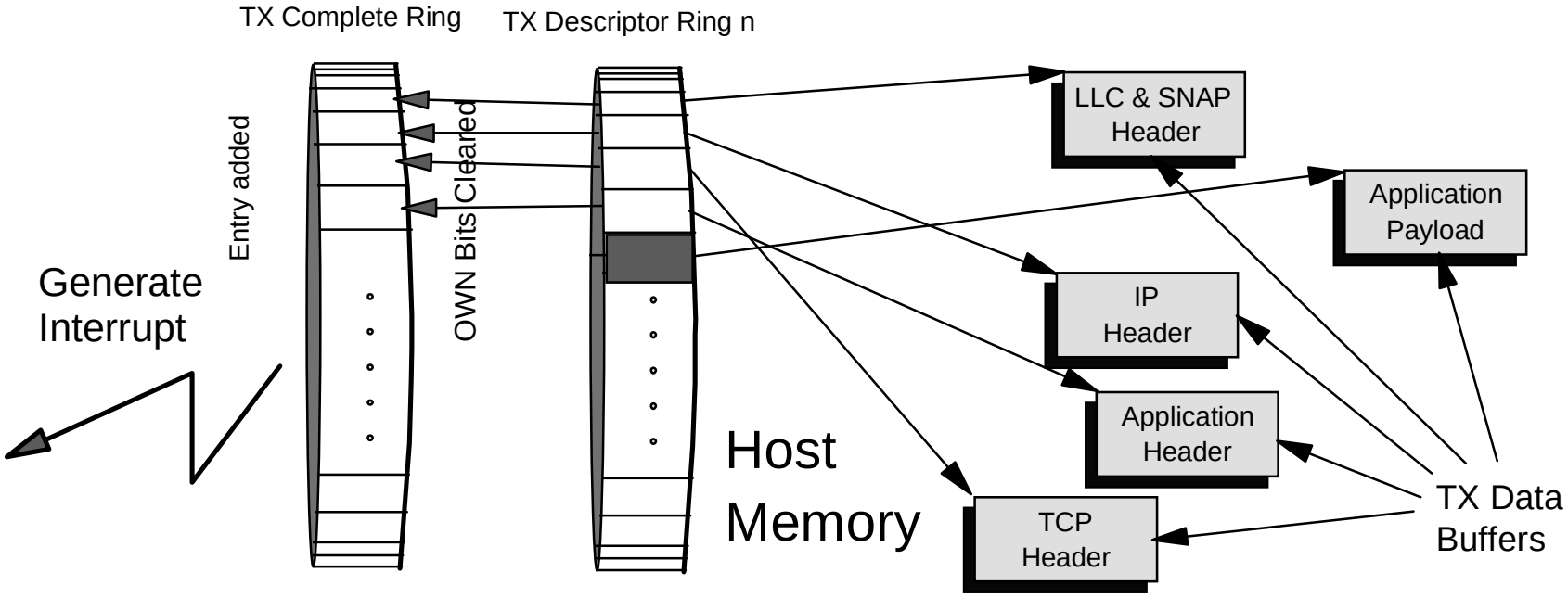


- **If a data packet contains many buffers, the buffers do not have to contain a multiple of 48 bytes. The SAR finishes processing the previous buffer and starts processing the next buffer.**
- **The SAR cycles through the BWG table and transmits all the buffers within a packet.**

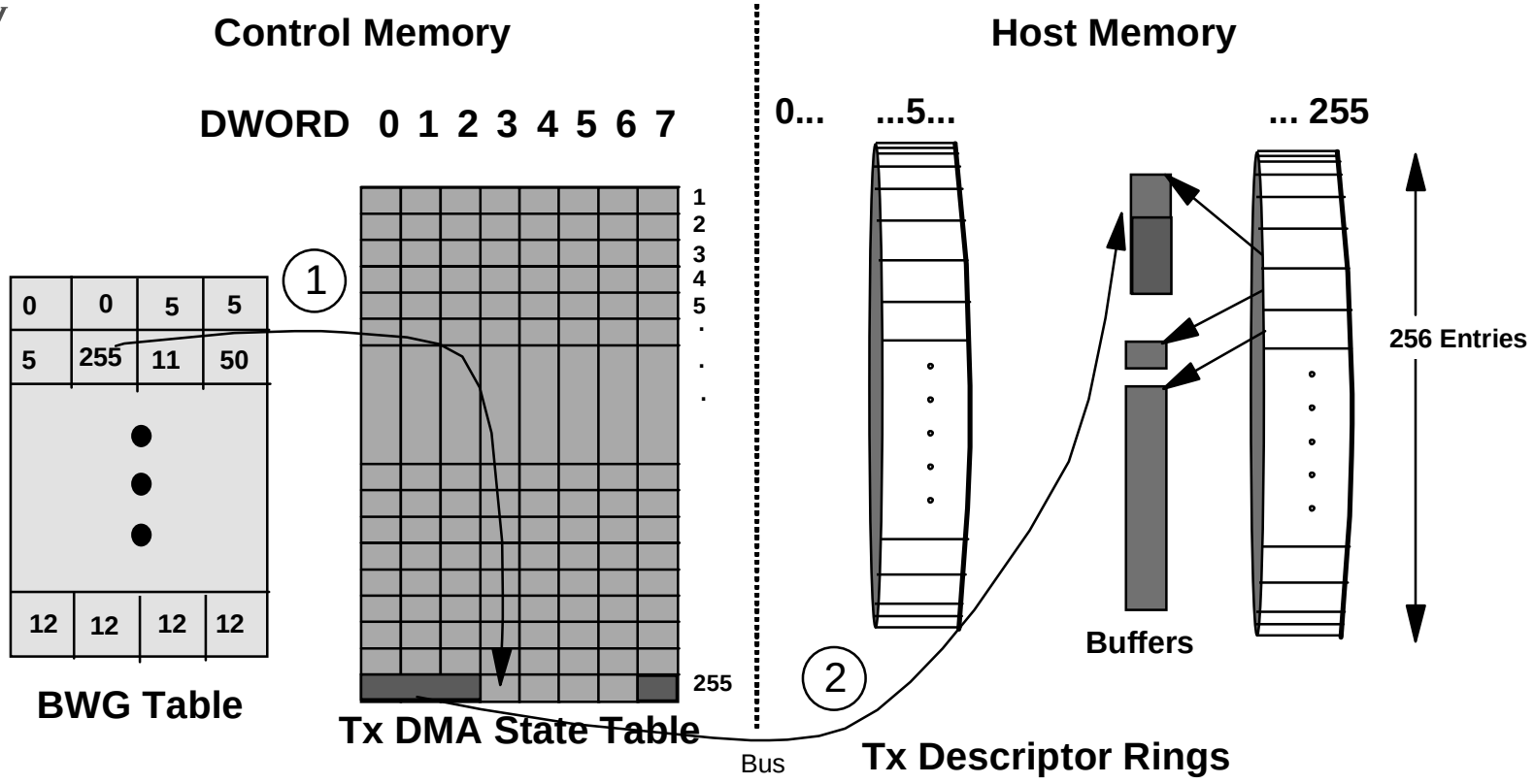
Transmit Operation

Once the entire packet has been transmitted:

- **OWN bits are cleared for all descriptors for that packet.**
- **A completion ring entry is posted.**
- **An interrupt is generated to the host.**



Transmit Operation



- **The SAR then processes the next BWG. The SAR again checks to see if the BWG is turned on.**
- **The 48 bytes are transmitted and the SAR updates the DMA states table.**

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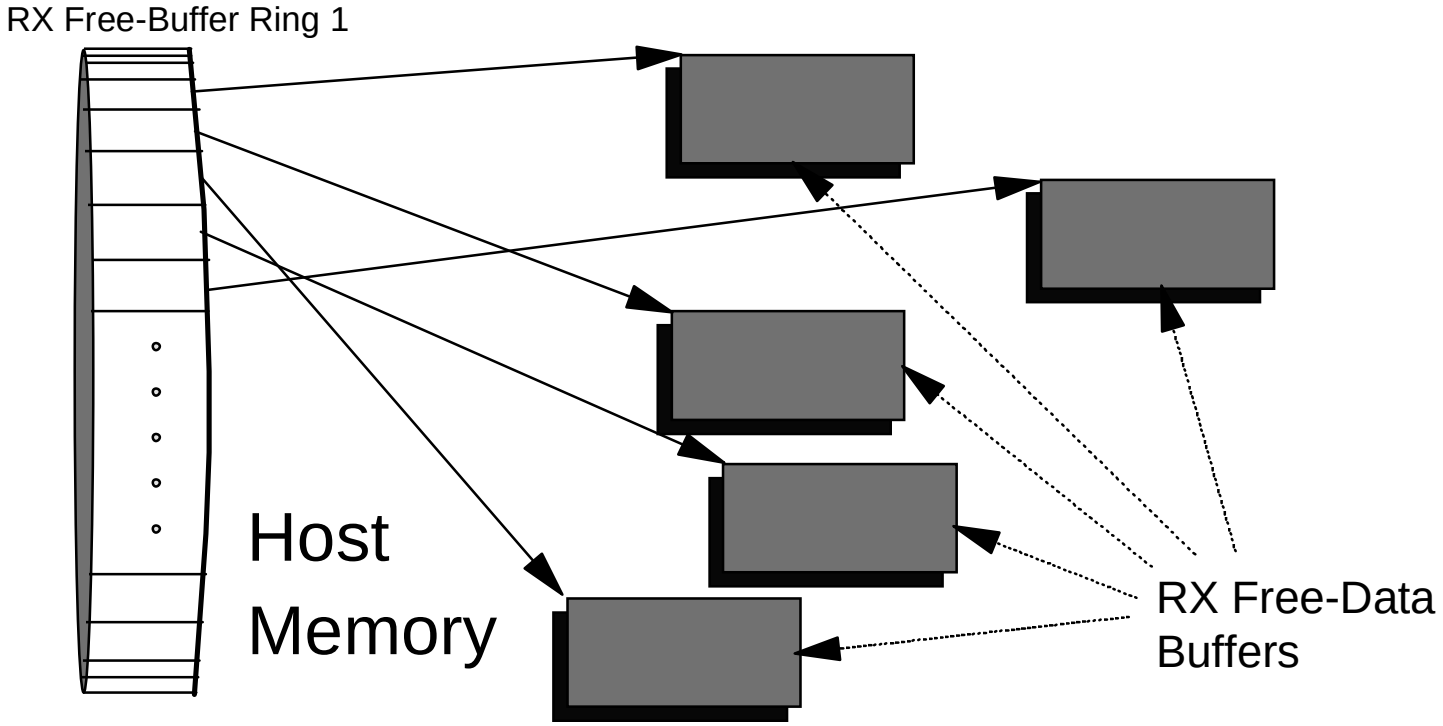
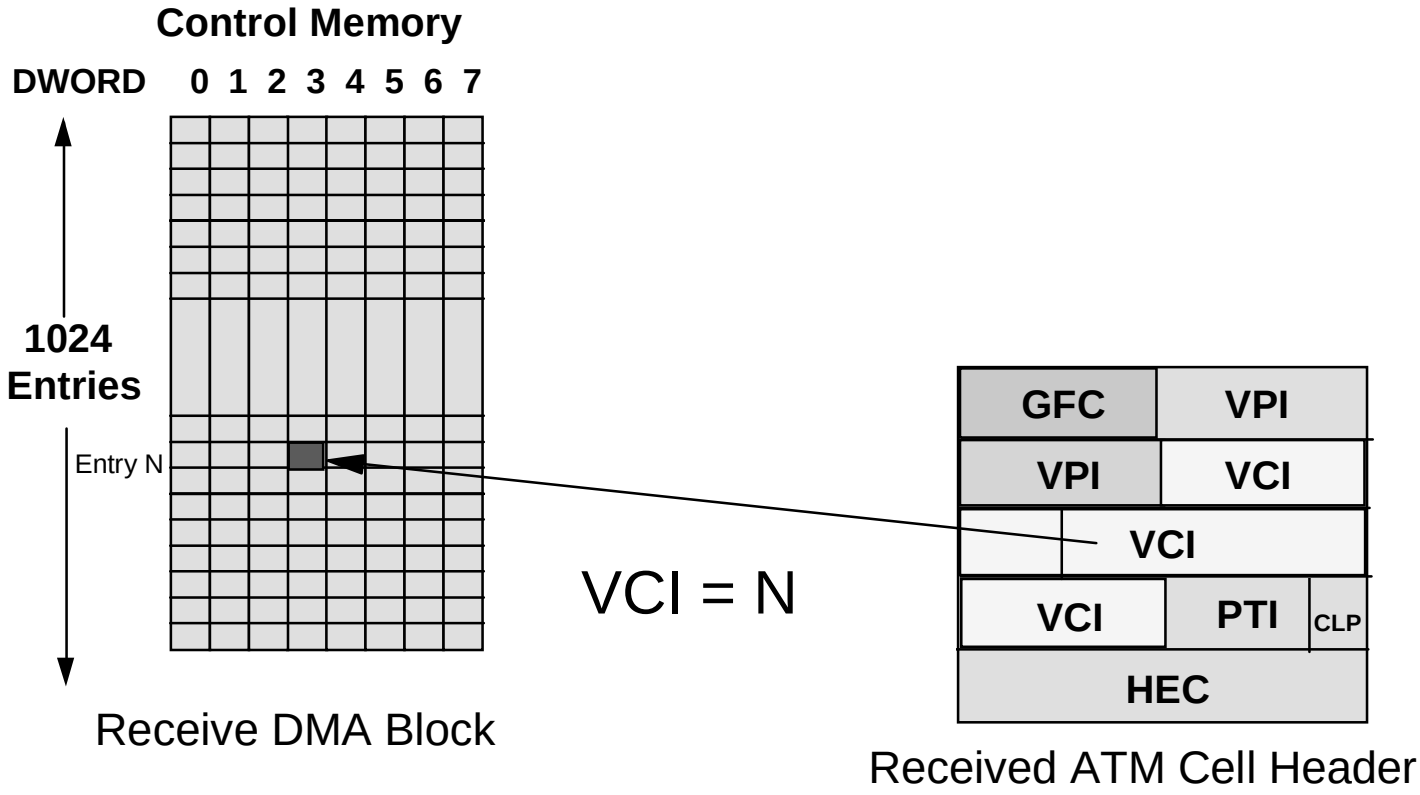
Receive Operation

- **Host SAR driver allocates free buffers in host memory.**
- **SAR driver builds descriptors in free-buffer rings.**
- **SAR driver passes buffers to SAR when OWN bits are set.**

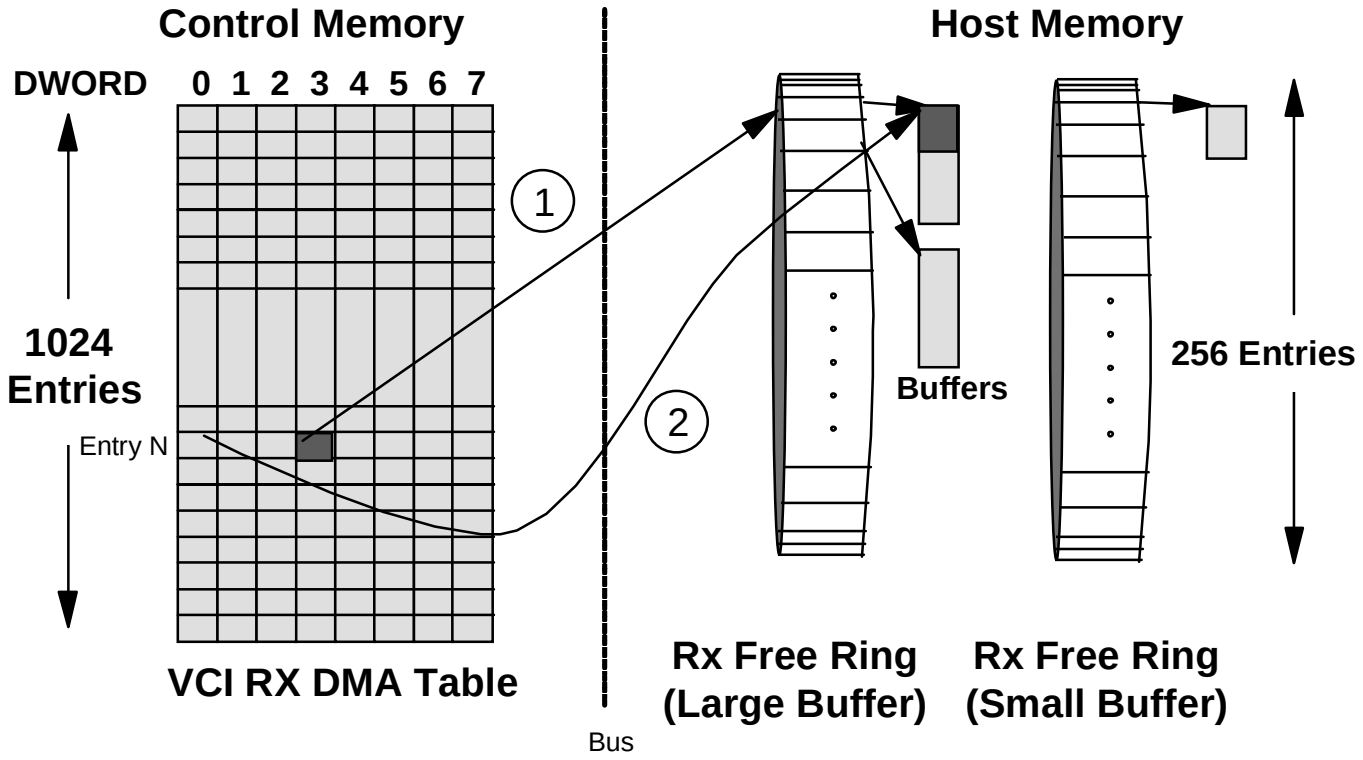


Receive Operation

- **10-bit VCI from incoming cells is used to index into the receive DMA block.**

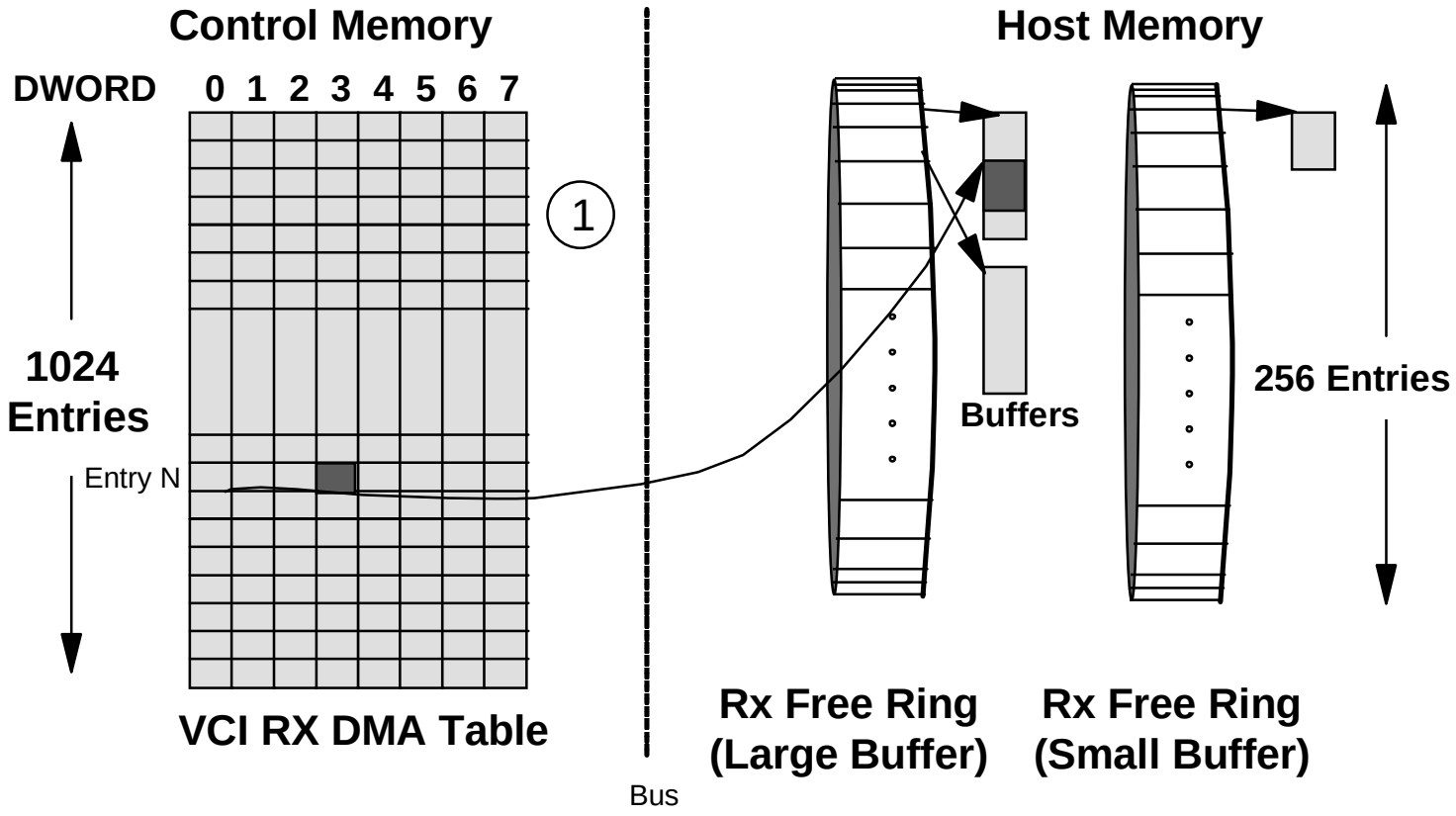


Receive Operation



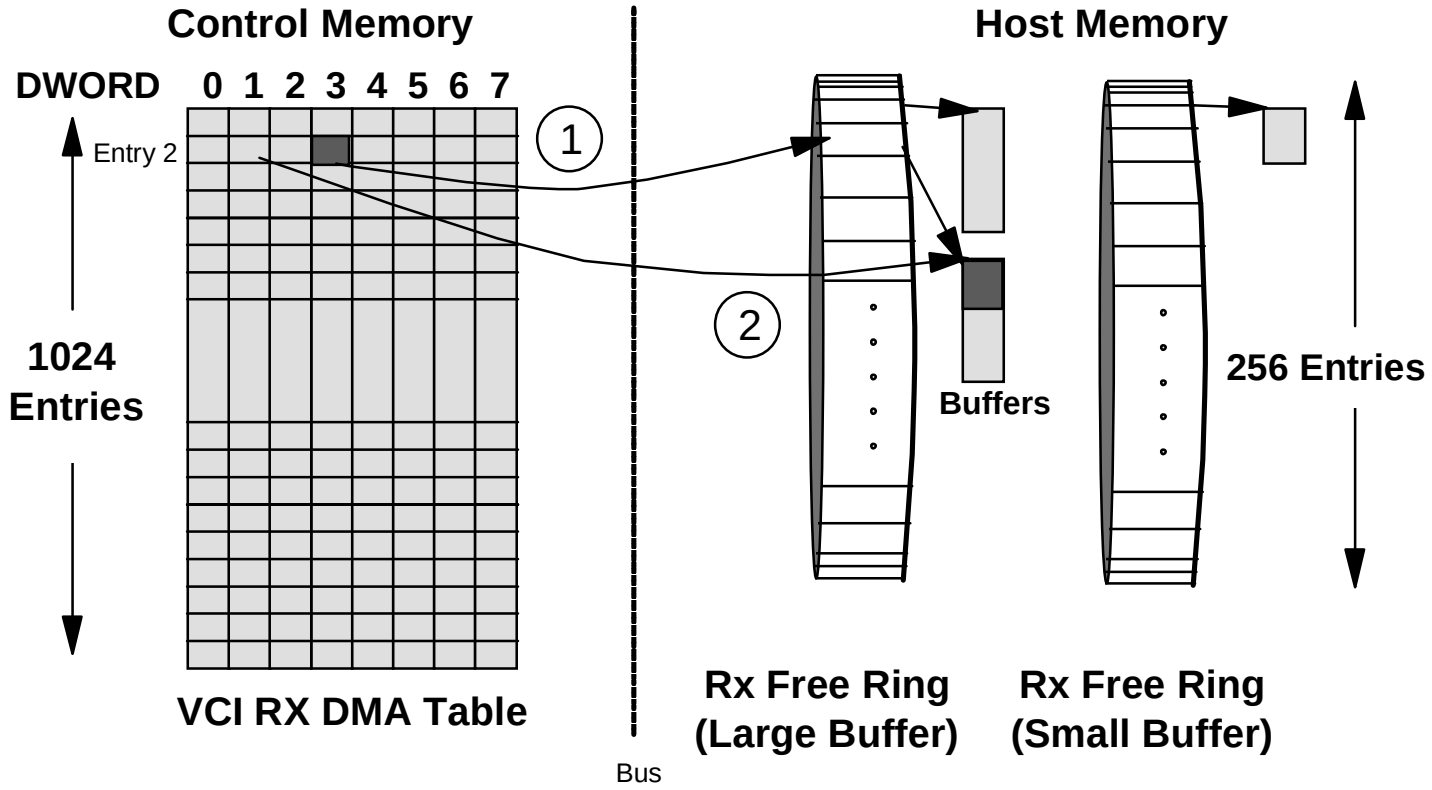
- **The receive DMA entry for this particular VCI indicates which free buffer ring is to be used and if the VCI is "on."**
- **Word 0 indicates if a packet currently is being processed.**

Receive Operation



- **Upon receiving the next 48 bytes (VCI=N), the SAR examines the receive DMA table and determines if a buffer is currently being processed. If a buffer is being processed, the SAR writes the data into host memory and updates the receive DMA control table.**

Receive Operation

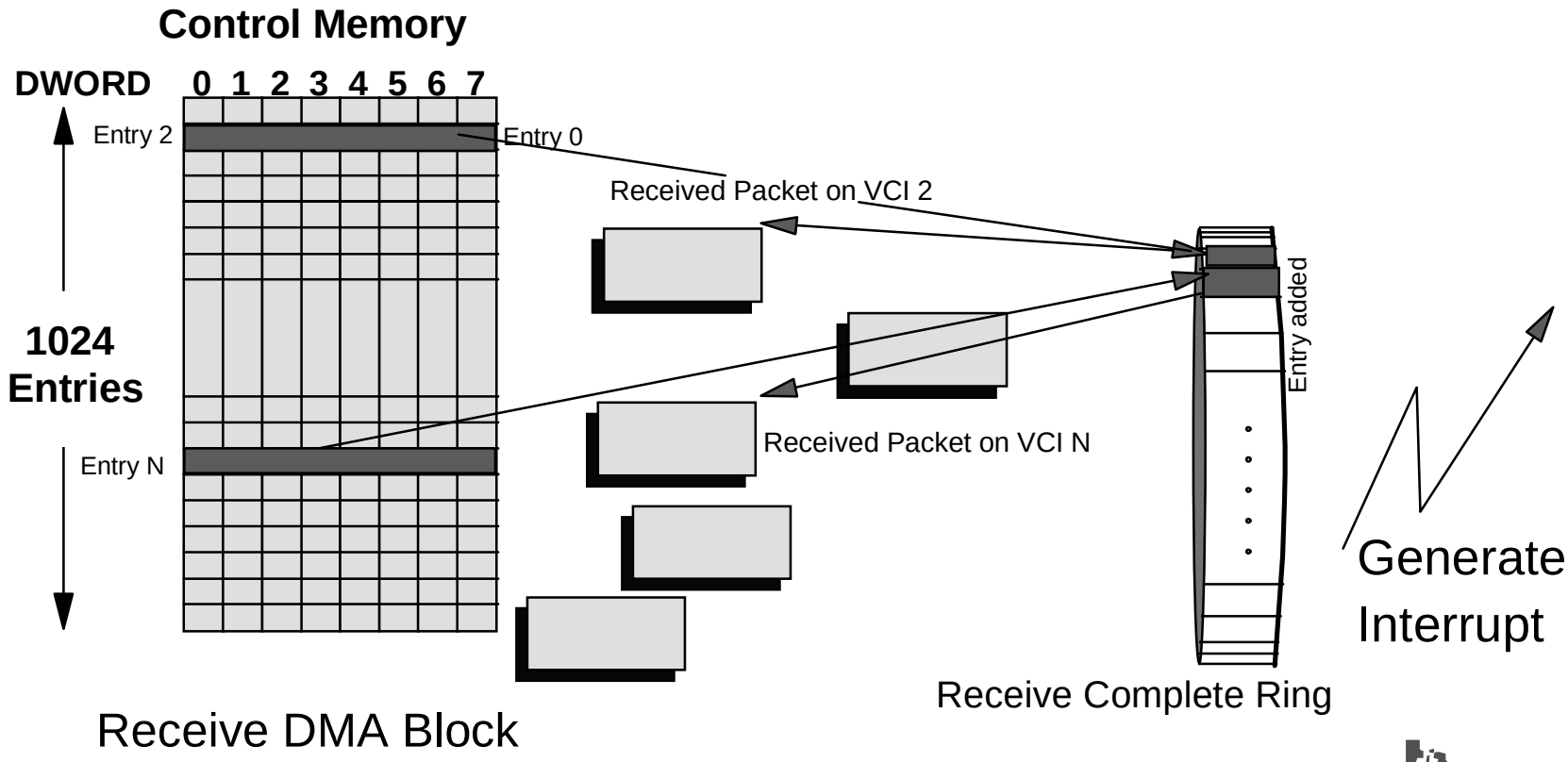


- The SAR then processes the next received cell.
- This cell has a different VCI from the previous cell.
- The descriptor is loaded for the next free buffer.
- The payload is then loaded.

Receive Operation

Once the entire packet is received:

- **A completion ring entry is posted**
- **An interrupt is generated to the host**



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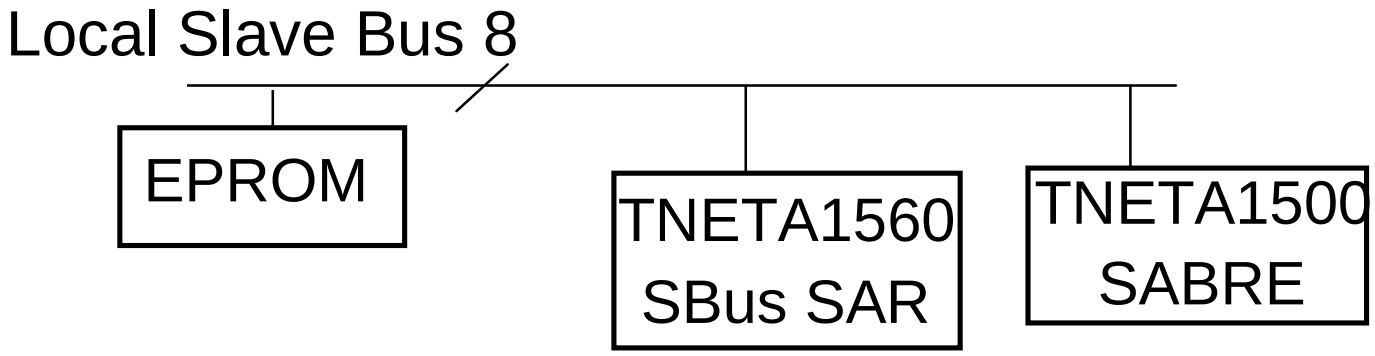
SBus SAR Registers

OFFSET-8 BIT (hex)	DESCRIPTION	READ/WRITE
00	Software reset	Write only
04	Status register	Read only
08	Interrupt mask register	Read/write
0C	Configuration register	Read/write
14	BWG table size register	Read/write
18	TX/RX FIFO maximum depth register	Read/write
20	Clear transmit freeze command	Write only
24	Clear receive freeze command	Write only

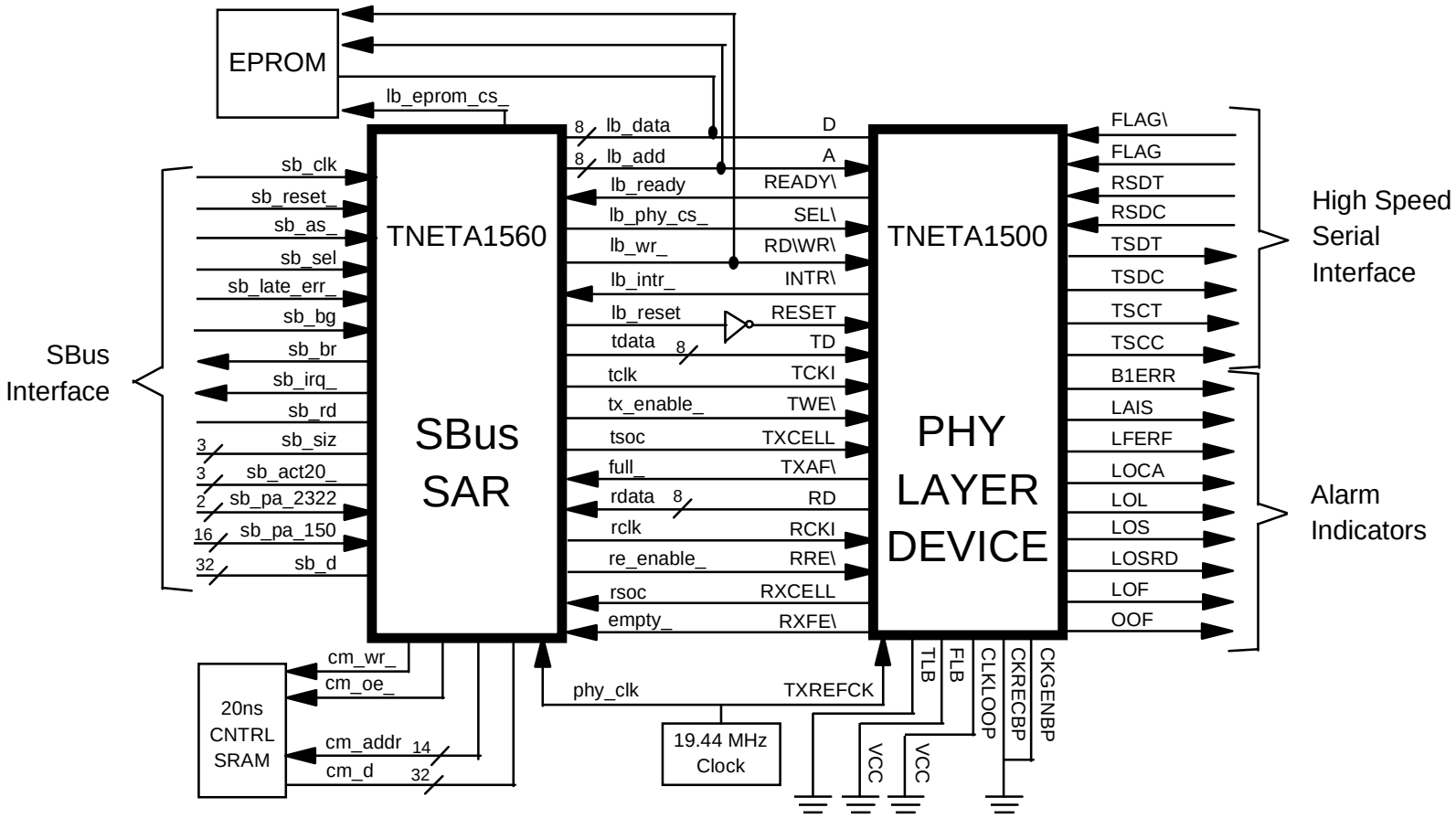
SBus SAR Peripheral Devices

- **Access to the SBus SARs peripheral devices is through the address map illustrated below.**
- **No external logic is required to connect external EPROM, PHY (chip select signals, etc., are provided by the SAR).**

ADDRESS – 24 BITS (hex)	DESCRIPTION	ADDRESS BITS	READ/WRITE
000000-00FFFF	EPROM addresses	16	Read only
400000-40FFFF	PHY layer register addresses	16	Read/write
C00000-C03FFF	Control memory addresses	14	Read/write



SBus SAR, SABRE Interconnect



TNETA1560 Tools

- **32-bit PCI evaluation module**
  - **With TNETA1560 and TNETA1500 SONET device**
  - **Capability to exercise both the TNETA1560 and TNETA1500**
- **SUN™ SOLARIS™ 2.x-based software utility**
  - **Transmit and receive ATM data**
  - **Monitor incoming traffic**
  - **Try different configurations**
  - **Test error and alarm conditions**
- **Software drivers (third-party software)**
  - **Provides solutions**
  - **Improves time-to-market**
- **Application note (1560/1500 interface)**

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Summary

- **Samples available now**
- **Production 8/15/95**
- **Evaluation board and software available now**