TOSHIBA PHOTOCOUPLER GaAs IRED & PHOTO-TRIAC

TLP3051, TLP3052

OFFICE MACHINE

HOUSEHOLD USE EQUIPMENT

TRIAC DRIVER

SOLID STATE RELAY

The TOSHIBA TLP3051 and TLP3052 consist of a photo-triac optically coupled to a gallium arsenide infrared emitting diode in a six lead plastic DIP package.

• Peak Off-State Voltage : 600V (Min.)

• Trigger LED Current : 15mA (Max.) (TLP3051)

10mA (Max.) (TLP3052)

• On-State Current : 100mA (Max.)

• UL Recognized : UL1577, File No. E67349

Isolation Voltage : 5000Vrms (Min.)

• Option (D4) type

Insulation Thickness:

VDE Approved : DIN VDE0884/08.87,

Certificate No. 68329

Maximum Operating Insulation Voltage: 630VpK Highest Permissible Over Voltage: 6000VpK

(Note) When a VDE0884 approved type is needed, please designate the "Option (D4)"

7.62mm pich 10.16mm pich standard type (LF2) type

Creepage Distance : 7.0mm (Min.) 8.0mm (Min.)

Clearance : 7.0mm (Min.) 8.0mm (Min.)

0.5mm (Min.)

0.5mm (Min.)

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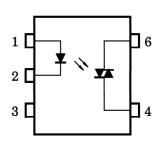
Unit in mm

3 2 1
4 6
8.64 ± 0.25
8 7.62
11.9A2

TOSHIBA 11-9A2

Weight: 0.44g

PIN CONFIGURATION (TOP VIEW)



1 : ANODE 2 : CATHODE

3 : NC

4 : TERMINAL 1 6 : TERMINAL 2

2001-06-01

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT	
(D	Forward Current		$I_{\mathbf{F}}$	50	mA
	Forward Current Derating (Ta≥53°C)		⊿I _F /°C	-0.7	mA/°C
	Peak Forward Current (100 µs pulse, 100 pps)		I _{FP}	1	A
LED	Power Dissipation		P_{D}	100	mW
	Power Dissipation De (Ta≥25°C)	erating	△P _D /°C	-1.0	mW/°C
	Reverse Voltage		v_{R}	5	V
	Junction Temperature	е	T_{j}	125	°C
	Off-State Output Terminal Voltage		$v_{ m DRM}$	600	V
	On-State RMS Current	Ta = 25°C Ta = 70°C	I _T (RMS)	100 50	mA
ror	On-State Current Derating (Ta≥25°C)		ΔI _T /°C	-1.1	mA/°C
DETECTOR	Peak On-State Current (100 µs pulse, 120 pps)		I_{TP}	2	A
DE,	Peak Nonrepetitive S Current (P _w =10ms,	_	I_{TSM}	1.2	A
	Power Dissipation		$P_{\mathbf{D}}$	300	mW
	Power Dissipation De (Ta≥25°C)	erating	$_{\Delta \mathrm{P_D}/^{\circ}\mathrm{C}}$	-4.0	mW/°C
	Junction Temperatur	е	$T_{ m j}$	115	°C
Sto	Storage Temperature Range		$\mathrm{T}_{\mathrm{stg}}$	-55~150	°C
Operating Temperature Range			$T_{ m opr}$	-40~100	°C
Lead Soldering Temperature (10s)			${ m T_{sol}}$	260	°C
Total Package Power Dissipation			P_{T}	330	mW
	tal Package Power Dis rating (Ta≥25°C)	$\Delta P_{\mathrm{T}}/{^{\circ}\mathrm{C}}$	-4.4	mW/°C	
	lation Voltage C, 1 min., R.H.≦60%)	$BV_{\mathbf{S}}$	5000	Vrms	

(Note 1) Device considered a two terminal device: Pins 1, 2 and 3 shorted together and pins 4 and 6 shorted together.

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	v_{AC}		ı	240	Vac
Forward Current	$ m I_{ m F}$ *	15	20	25	mA
Peak On-State Current	$I_{ ext{TP}}$	_	_	1	A
Operating Temperature	$T_{ m opr}$	-25	_	85	°C

 \times In the case of TLP3052

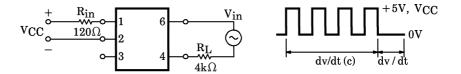
INDIVIDUAL	FI FCTRICAL	CHARACTERISTICS	$(Ta = 25^{\circ}C)$
INDIVIDUAL		CHANACILINISHOS	10-23 ()

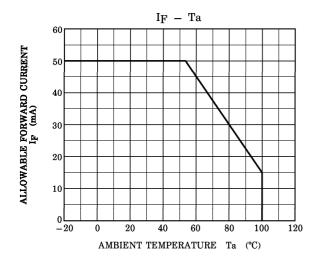
	CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
LED	Forward Voltage	$ m V_{ m F}$	$I_{ m F} = 10 { m mA}$	1.0	1.15	1.3	V
	Reverse Current	$I_{\mathbf{R}}$	$V_R = 5V$	_	_	10	μ A
	Capacitance	C_{T}	V=0, f=1MHz	_	30	_	pF
DETECTOR	Peak Off-State Current	${ m I}_{ m DRM}$	$V_{DRM} = 600V$	_	10	1000	nA
	Peak On-State Voltage	$ m V_{TM}$	$I_{ extbf{TM}} = 100 ext{mA}$	_	1.7	3.0	V
	Holding Current	${ m I_H}$	ı	_	1.0	_	mA
	Critical Rate of Rise of Off-State Voltage	dv/dt	V_{in} =240Vrms, Ta=85°C (Fig.1)	_	500	_	V/μs
	Critical Rate of Rise of Commutating Voltage	dv / dt (c)	V_{in} =60Vrms, I_T =15mA (Fig.1)	_	0.2	_	V/μs

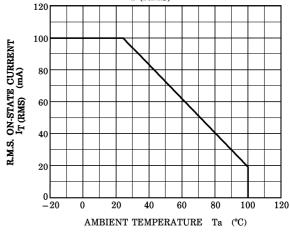
COUPLED ELECTRICAL CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Trigger LED Current	TLP3051	- I _{FT}	$V_{\mathrm{T}}=6V$	_	_	15	mA	
	TLP3052			_	5	10		
Capacitance Input to Output		c_{S}	$V_S=0$, $f=1MHz$	_	0.8	_	pF	
Isolation Resistance		$R_{\mathbf{S}}$	$V_S = 500V (R.H. \le 60\%)$	5×10^{10}	10^{14}	_	Ω	
Isolation Voltage		BV_S	AC, 1 minute	5000	_		Vrms	
			AC, 1 second, in oil	_	10000	_	VIIIS	
			DC, 1 minute, in oil	_	10000	_	v_{dc}	

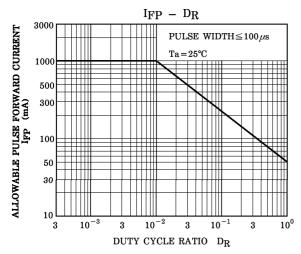
Fig. 1 dv/dt TEST CIRCUIT

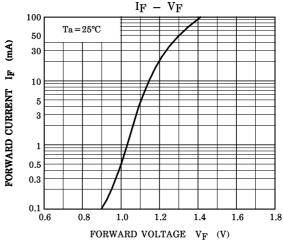


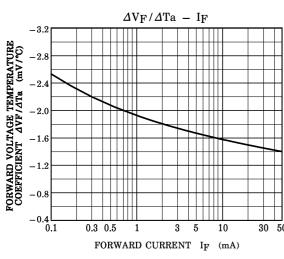


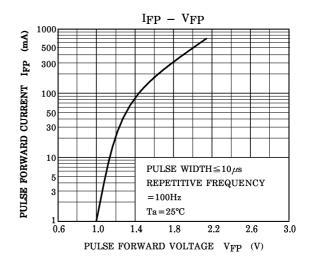


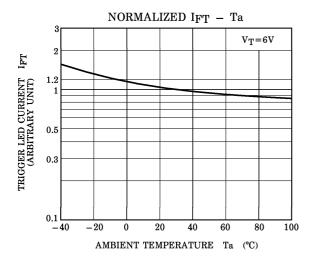
IT (RMS) - Ta

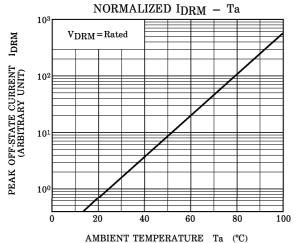


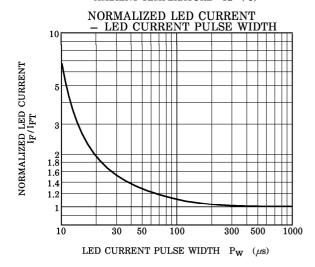


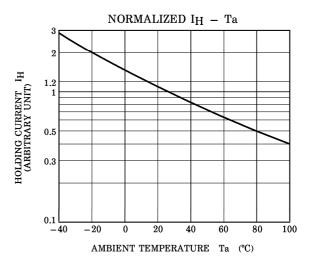


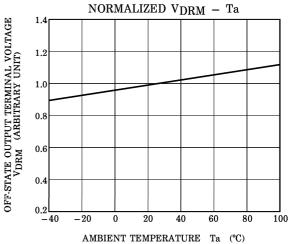












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