

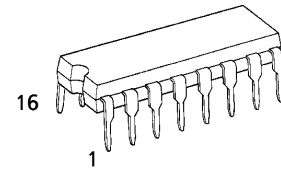
TC4094BP, TC4094BF, TC4094BFN

TC4094B 8 - STAGE SHIFT - AND - STORE BUSREGISTER

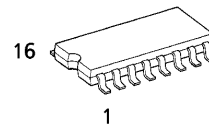
TC4094B is a SHIFT and STORE REGISTER that consists of an 8-bit shift register and an 8-bit latch. The read data in the shift register can be taken in the latch through the asynchronous STROBE input; therefore, the data transfer mode can hold output. And, since the parallel outputs is of 3-state construction, it can be directly connected to the 8-bit busline.

This register can be applied to Serial - to - parallel conversion, data receivers, etc.

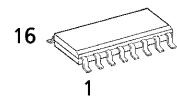
(Note) The JEDEC SOP (FN) is not available in Japan.



P (DIP16-P-300-2.54A)
Weight : 1.00g (Typ.)



F (SOP16-P-300-1.27)
Weight : 0.18g (Typ.)

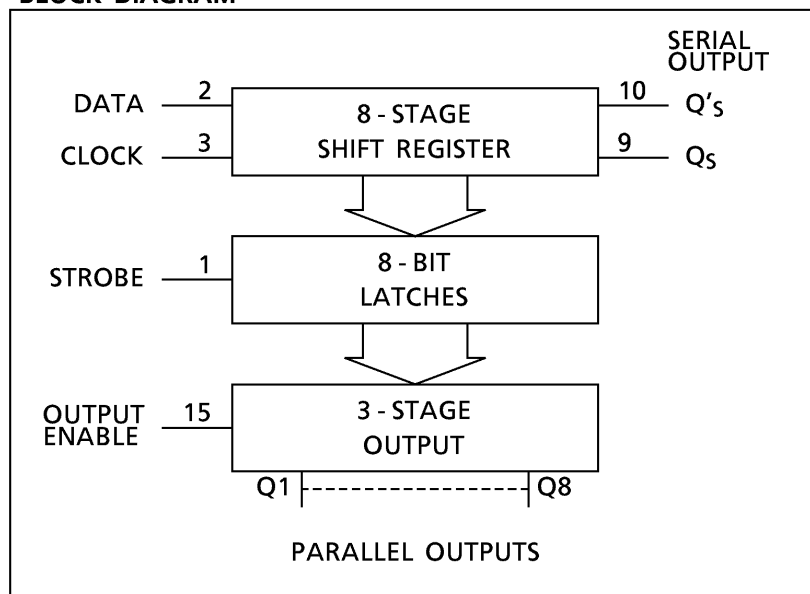


FN (SO16-P-150-1.27)
Weight : 0.13g (Typ.)

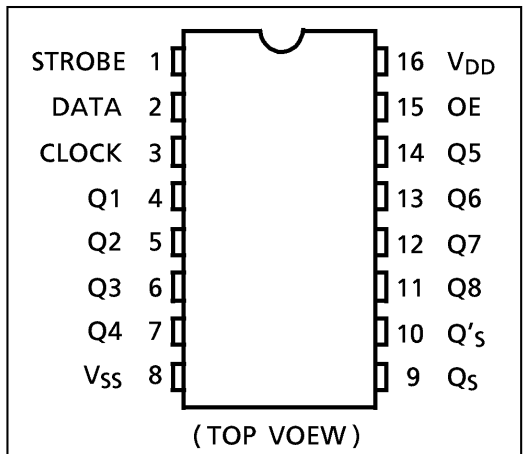
MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	$V_{SS} - 0.5 \sim V_{SS} + 20$	V
Input Voltage	V_{IN}	$V_{SS} - 0.5 \sim V_{DD} + 0.5$	V
Output Voltage	V_{OUT}	$V_{SS} - 0.5 \sim V_{DD} + 0.5$	V
DC Input Current	I_{IN}	± 10	mA
Power Dissipation	P_D	300 (DIP) / 180 (SOIC)	mW
Operating Temperature Range	T_{opr}	$-40 \sim 85$	$^{\circ}\text{C}$
Storage Temperature Range	T_{stg}	$-65 \sim 150$	$^{\circ}\text{C}$

BLOCK DIAGRAM



PIN ASSIGNMENT



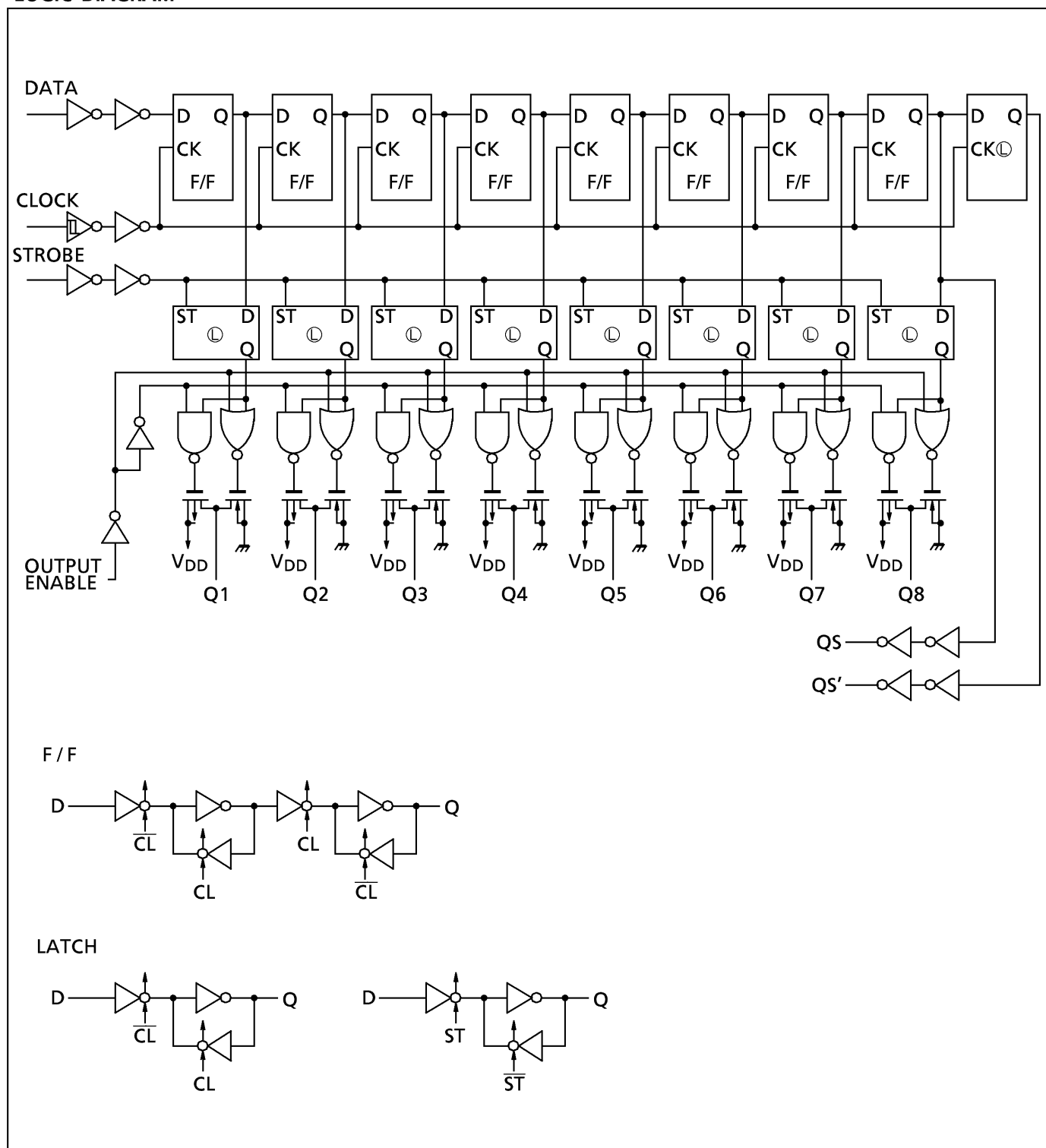
TRUTH TABLE

CL	OE	ST	D	PO		SO	
				Q1	Qn	Qs	Q's
	H	H	L	L	Qn - 1	Q7	NC
	H	H	H	H	Qn - 1	Q7	NC
	H	L	X	NC	NC	Q7	NC
	L	X	X	HZ	HZ	Q7	NC
	H	X	X	NC	NC	NC	Qs
	L	X	X	HZ	HZ	NC	Qs

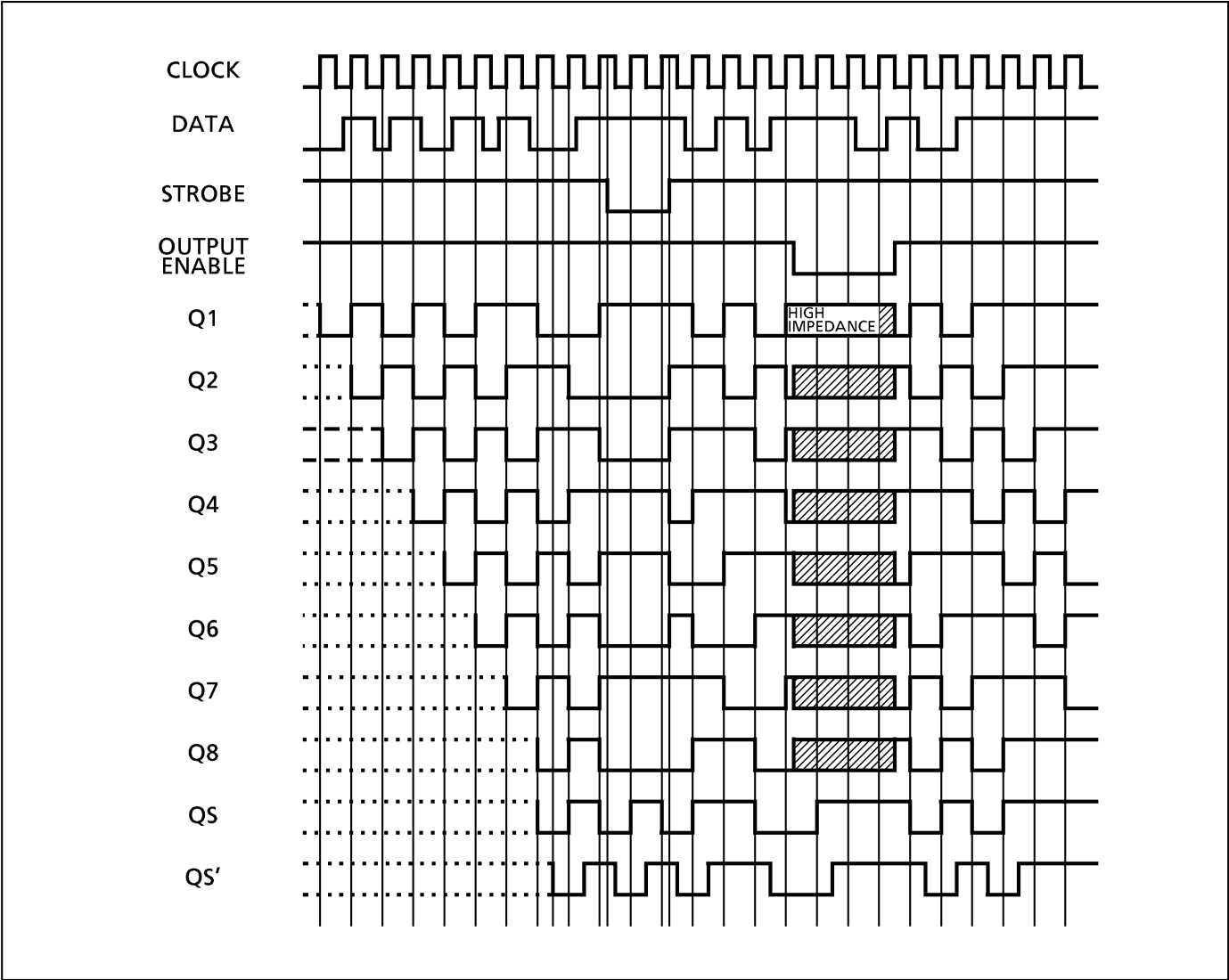
CL = Clock
OE = Output Enable
ST = Strobe
D = Data
PO = Parallel Outputs
SO = Serial Output

X = Don't Care
NC = No Change
HZ = High Impedance

LOGIC DIAGRAM



TIMING CHART



RECOMMENDED OPERATING CONDITIONS ($V_{SS} = 0V$)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
DC Supply Voltage	V_{DD}		3	—	18	V
Input Voltage	V_{IN}		0	—	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS ($V_{SS} = 0V$)

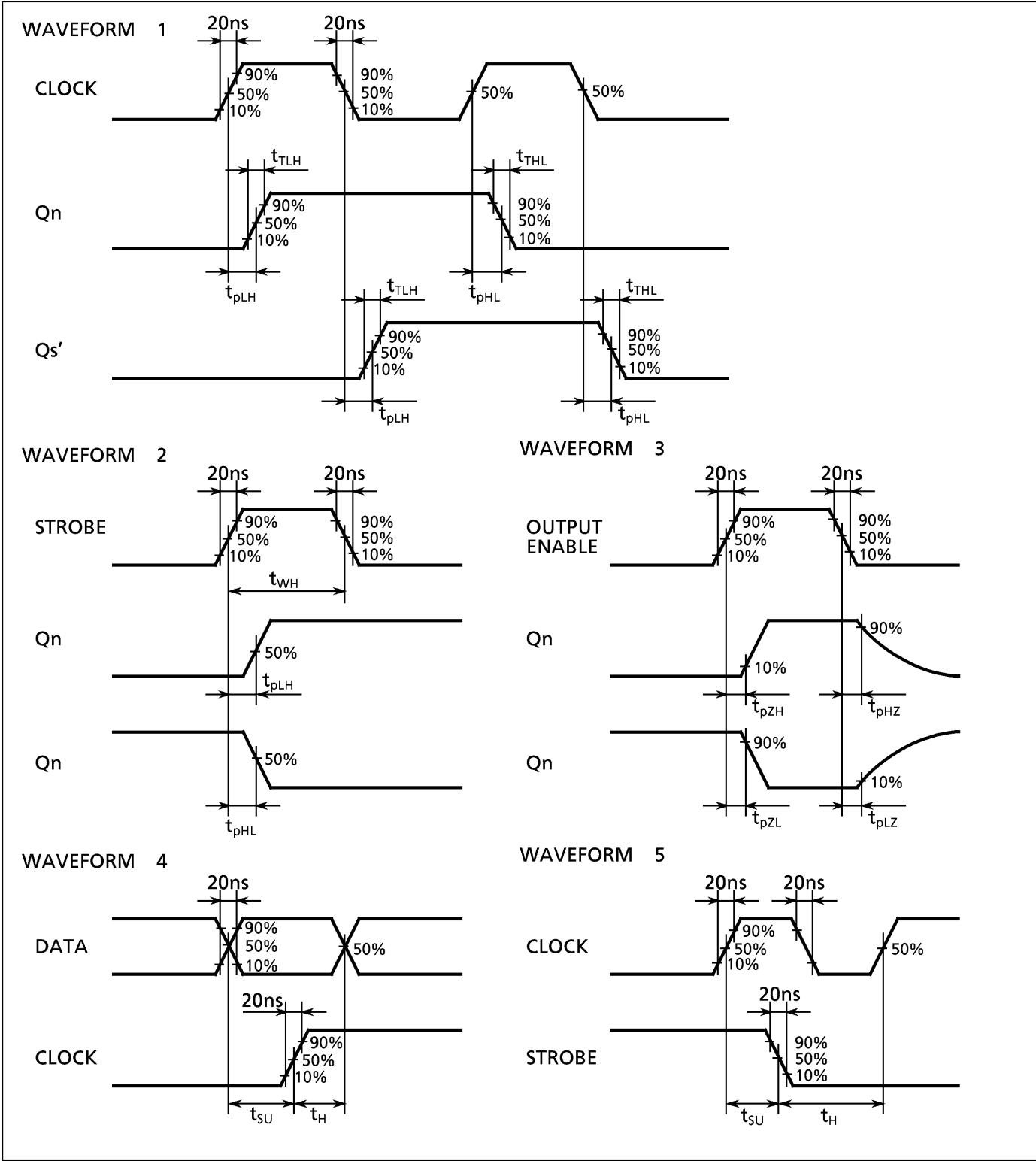
CHARACTERISTIC	SYM-BOL	TEST CONDITION	V_{DD} (V)	- 40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Output Voltage	V_{OH}	$ I_{OUT} < 1\mu A$ $V_{IN} = V_{SS}, V_{DD}$	5	4.95	—	4.95	5.00	—	4.95	—	V
			10	9.95	—	9.95	10.00	—	9.95	—	
			15	14.95	—	14.95	15.00	—	14.95	—	
Low-Level Output Voltage	V_{OL}	$ I_{OUT} < 1\mu A$ $V_{IN} = V_{SS}, V_{DD}$	5	—	0.05	—	0.00	0.05	—	0.05	V
			10	—	0.05	—	0.00	0.05	—	0.05	
			15	—	0.05	—	0.00	0.05	—	0.05	
Output High Current	I_{OH}	$V_{OH} = 4.6V$	5	-0.61	—	-0.51	-1.0	—	-0.42	—	mA
		$V_{OH} = 2.5V$	5	-2.50	—	-2.10	-4.0	—	-1.70	—	
		$V_{OH} = 9.5V$	10	-1.50	—	-1.30	-2.2	—	-1.10	—	
		$V_{OH} = 13.5V$	15	-4.00	—	-3.40	-9.0	—	-2.80	—	
		$V_{IN} = V_{SS}, V_{DD}$									
Output Low Current	I_{OL}	$V_{OL} = 0.4V$	5	0.61	—	0.51	1.2	—	0.42	—	mA
		$V_{OL} = 0.5V$	10	1.50	—	1.30	3.2	—	1.10	—	
		$V_{OL} = 1.5V$	15	4.00	—	3.40	12.0	—	2.80	—	
		$V_{IN} = V_{SS}, V_{DD}$									
Input High Voltage	V_{IH}	$V_{OUT} = 0.5V, 4.5V$	5	3.5	—	3.5	2.75	—	3.5	—	V
		$V_{OUT} = 1.0V, 9.0V$	10	7.0	—	7.0	5.50	—	7.0	—	
		$V_{OUT} = 1.5V, 13.5V$	15	11.0	—	11.0	8.25	—	11.0	—	
		$ I_{OUT} < 1\mu A$									
Input Low Voltage	V_{IL}	$V_{OUT} = 0.5V, 4.5V$	5	—	1.5	—	2.25	1.5	—	1.5	V
		$V_{OUT} = 1.0V, 9.0V$	10	—	3.0	—	4.50	3.0	—	3.0	
		$V_{OUT} = 1.5V, 13.5V$	15	—	4.0	—	6.75	4.0	—	4.0	
		$ I_{OUT} < 1\mu A$									
Input Current	"H" Level	I_{IH}	$V_{IH} = 18V$	18	—	0.1	—	10^{-5}	0.1	—	μA
	"L" Level	I_{IL}	$V_{IL} = 0V$	18	—	-0.1	—	-10^{-5}	-0.1	—	
3-State Output Leakage Current	"H" Level	I_{DH}	$V_{OUT} = 18V$	18	—	0.4	—	10^{-4}	0.4	—	μA
	"L" Level	I_{DL}	$V_{OUT} = 0V$	18	—	-0.4	—	-10^{-4}	-0.4	—	
Quiescent Supply Current	I_{DD}	$V_{IN} = V_{SS}, V_{DD} *$	5	—	5	—	0.005	5	—	150	μA
			10	—	10	—	0.010	10	—	300	
			15	—	20	—	0.015	20	—	600	

* All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta = 25°C, Vss = 0V, CL = 50pF)

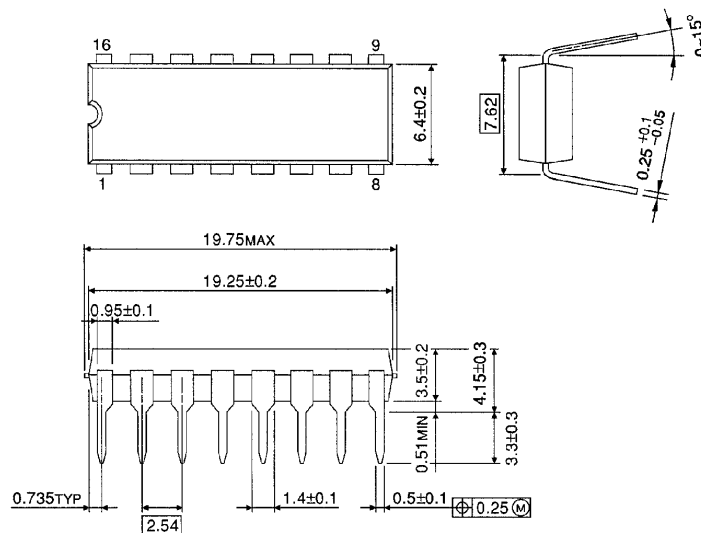
CHARACTERISTIC	SYMBOL	TEST CONDITION	V _{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t _{TLH}		5 10 15	— — —	70 35 30	200 100 80	ns
Output Transition Time (High to Low)	t _{THL}		5 10 15	— — —	70 35 30	200 100 80	
Propagation Delay Time (CLOCK - Q _S)	t _{pLH} t _{pHL}		5 10 15	— — —	150 75 55	600 250 190	
Propagation Delay Time (CLOCK - Q _S ')	t _{pLH} t _{pHL}		5 10 15	— — —	155 75 55	460 220 150	
Propagation Delay Time (CLOCK - Q _n)	t _{pLH} t _{pHL}		5 10 15	— — —	190 90 65	840 390 270	
Propagation Delay Time (STROBE - Q _n)	t _{pLH} t _{pHL}		5 10 15	— — —	150 70 50	580 290 200	
Three State Disable Time (OUTPUT ENABLE - Q _n)	t _{pHZ} t _{pZH}	R _L = 1kΩ	5 10 15	— — —	60 35 30	200 100 80	
Three State Disable Time (OUTPUT ENABLE - Q _n)	t _{pLZ} t _{pZL}	R _L = 1kΩ	5 10 15	— — —	70 40 35	200 100 80	
Min. Clock Pulse Width	t _w		5 10 15	— — —	45 20 15	200 100 80	
Min. Pulse Width (STROBE)	t _{WH}		5 10 15	— — —	40 20 15	200 80 70	
Max. Clock Frequency	f _{CL}		5 10 15	1.25 2.50 3.00	6 12 16	— — —	MHz
Min. Set-up Time (DATA - CLOCK)	t _{SU}		5 10 15	— — —	0 0 0	125 55 35	ns
Min. Hold Time (DATA - CLOCK)	t _H		5 10 15	— — —	10 10 5	40 20 15	
Min. Set-up Time (CLOCK - STROBE)	t _{SU}		5 10 15	— — —	90 40 30	200 100 80	
Min. Hold Time (CLOCK - STROBE)	t _H		5 10 15	— — —	— — —	0 0 0	
Max. Clock Input Rise Time Max. Clock Input Fall Time	t _{rCL} t _{fCL}		5 10 15	No Limit			μs
Input Capacitance	C _{IN}			—	5	7.5	pF

WAVEFORMS FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS



DIP 16PIN PACKAGE DIMENSIONS (DIP16-P-300-2.54A)

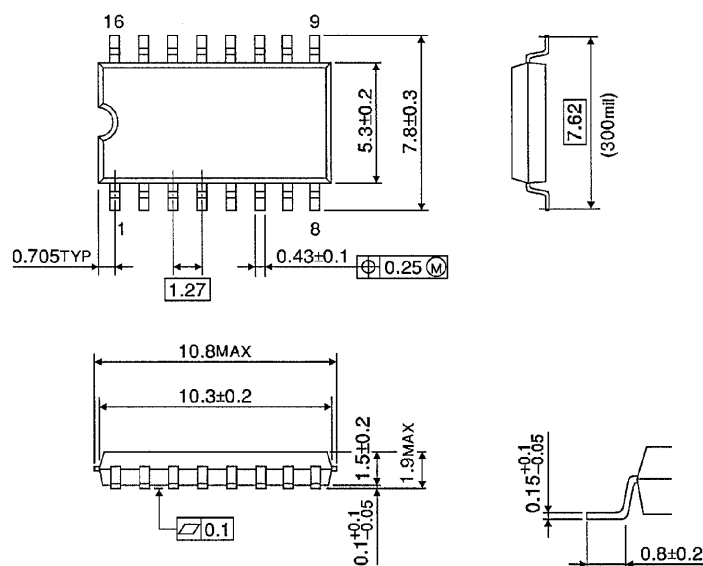
Unit in mm



Weight : 1.00g (Typ.)

SOP 16PIN (200mil BODY) PACKAGE DIMENSIONS (SOP16-P-300-1.27)

Unit in mm

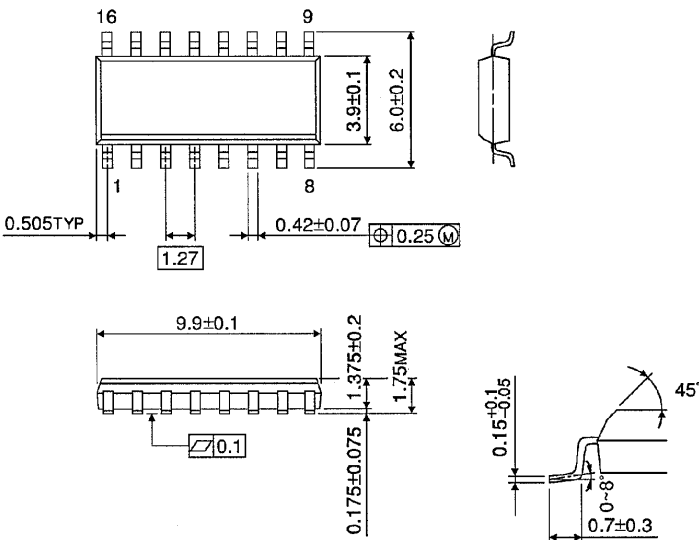


Weight : 0.18g (Typ.)

SOP 16PIN (150mil BODY) PACKAGE DIMENSIONS (SOL16-P-150 -1.27)

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)

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000707EBA

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