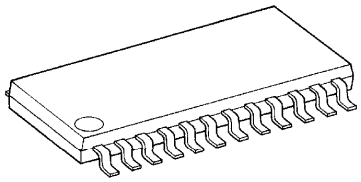
TENTATIVE TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC9400F, TC9400N

Σ-Δ MODULATION SYSTEM DA CONVERTER WITH A BUILT-IN 8-TIMES OVER SAMPLING DIGITAL FILTER / DIGITAL ATTENUATOR

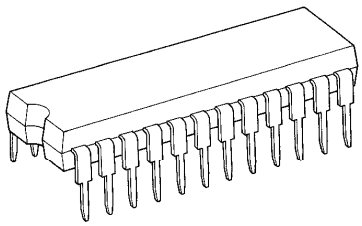
The TC9400F and TC9400N are a 2'nd order Σ-Δ modulation system 1-bit DA converter incorporating an 8-times oversampling FIR type digital filter and digital attenuator developed for digital audio equipment.
Because the IC is small package (SSOP24, SDIP24) and the de-emphasis filter has been incorporation, it is possible to constitute reducing the size and cost of the DA converter.

TC9400F



SSOP24-P-300-1.00

TC9400N



SDIP24-P-300-1.78

Weight
SSOP24-P-300-1.00 : 0.31 g (Typ.)
SDIP24-P-300-1.78 : 1.2 g (Typ.)

FEATURES

- Built-in 8-times over sampling FIR type digital filter
- DA converter over sampling ratio (OSR) : 192 fs
- Built-in digital de-emphasis filter
- In serial control mode, output amplitude can be set in 128 steps of resolution using microcontroller commands
- In parallel control mode, soft mute can be set for the output signal in 128 steps in 20 ms
- Simultaneous outputs Left and Right channel
- Sampling frequency : 44.1 kHz, 32 kHz, 48 kHz
- Support double speed operation
- Built-in digital zero detection output circuit
- Characteristics of the digital filter and DA converter are as follows :

Digital filter

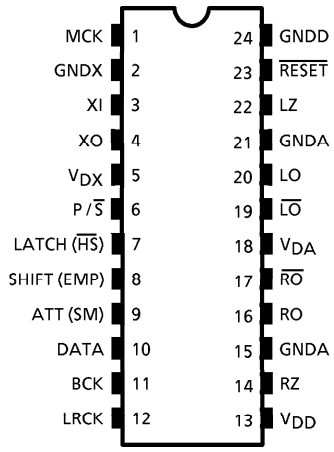
	DIGITAL FILTER	PASS-BAND RIPPLE	TRANSIENT BAND WIDTH	STOP-BAND SUPPRESSION
Standard Operation	8 fs	± 0.15 dB	20 k~24.1 kHz	– 40 dB
Double Speed Operation	8 fs	± 0.15 dB	20 k~24.1 kHz	– 40 dB

DA converter (V_{DD} = 5 V)

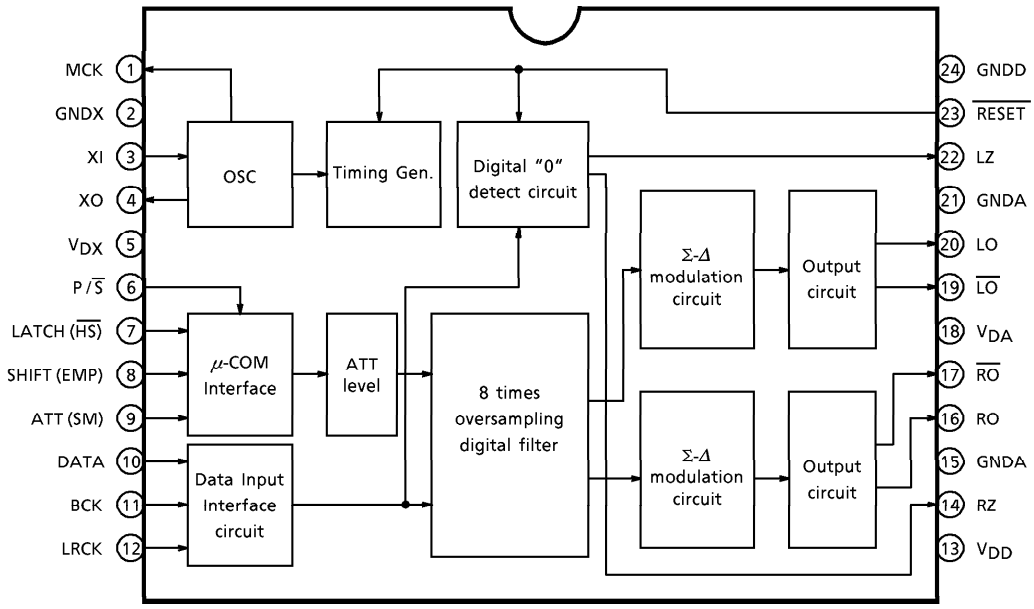
	OSR	NOISE DISTORTION	S / N RATIO
Standard Operation	192 fs	– 90 dB (Typ.)	100 dB (Typ.)
Double Speed Operation	192 fs	– 87 dB (Typ.)	98 dB (Typ.)

- 2 kinds of package, Pin 24 flat package and Pin 24 DIP shrunk package.

PIN CONNECTION



BLOCK DIAGRAM



PIN FUNCTION

PIN No.	SYMBOL	I/O	FUNCTION & OPERATION	REMARKS
1	MCK	O	System clock output pin	
2	GNDX	—	Crystal oscillator GND pin	
3	XI	I	Crystal oscillator connecting pins.	
4	XO	O	Generate the clock required by the system.	
5	V_{DX}	—	Crystal oscillator power supply pin	
6	P/$\overline{S}$	I	Parallel/serial mode select pin	Shumitt input Pull-up resister
7	LATCH ($\overline{HS}$)	I	Serial mode : Data latch signal input pin Parallel mode : Standard/Double speed operation control pin	Shumitt input Pull-up resister
8	SHIFT (EMP)	I	Serial mode : Shift clock input pin Parallel mode : De-emphasis filter ON/OFF control pin	Shumitt input Pull-up resister
9	ATT (SM)	I	Serial mode : Data input pin Parallel mode : Soft mute control pin	Shumitt input Pull-up resister
10	DATA	I	Audio data input pin	Shumitt input
11	BCK	I	Bit clock input pin	Shumitt Input
12	LRCK	I	LR clock input pin	Shumitt input

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Power Supply Voltage		V_{DD}	−0.3~6.0	V
		V_{DA}	−0.3~6.0	
		V_{DX}	−0.3~6.0	
Input Voltage		Vin	−0.3~V_{DD} + 0.3	V
Power Dissipation	TC9400F	PD	200	mW
	TC9400N		300	
Operating Temperature		T_{opr}	−35~85	°C
Storage Temperature		T_{stg}	−55~150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta = 25°C V_{DD} = V_{DX} = V_{DA} = 5 V)

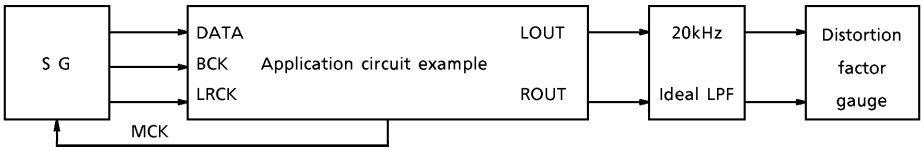
DC CHARACTERISTICS

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Power Supply Voltage		V_{DD}	—	Ta = −35~85°C	4.5	5.0	5.5	V
		V_{DX}			4.5	5.0	5.5	
		V_{DA}			4.5	5.0	5.5	
Power Dissipation		I_{DD}	—	XI = 16.9 MHz	—	30	40	mA
Input Voltage	"H" Level	V_{IH}	—		V_{DD} × 0.7	—	V_{DD}	V
	"L" Level	V_{IL}			0	—	V_{DD} × 0.3	
Input Current	"H" Level	I_{IH}	—		−10	—	10	μA
	"L" Level	I_{IL}						

AC CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Noise Distortion	THD + N	1	1 kHz Sine wave, full-scale input	—	−90	−80	dB
S/N Ratio	S/N	1		90	100	—	dB
Dynamic Range	DR	1	1 kHz Sine wave, −60 Input conversion	90	95	—	dB
Cross-talk	CT	1	1 kHz Sine wave, full-scale input	—	−95	−90	dB
Operating Frequency	f_{opr}	—		12	16.9344	18.5	MHz
Input Frequency	f_{LR}	—	LRCK duty cycle = 50%	30	44.1	100	kHz
	f_{BCK}		BCK duty cycle = 50%	1.0	2.1168	6.2	MHz
Rise Time	t_r	—	LRCK, BCK (10~90%)	—	—	15	nS
Fall Time	t_f			—	—	15	nS
Delay Time	t_d	—	BCK↓ Edge → LRCK, DATA	−50	—	50	nS

- **TEST CIRCUIT-1** : With the use of a sample application circuit

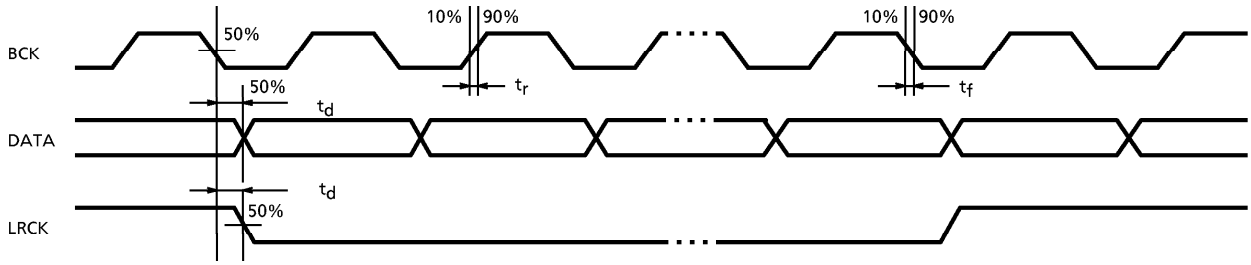


SG : ANRITSU : MG-22A or equivalent
LPF : SHIBASOKU : 725C internal filter
DISTORTION : SHIBASOKU : 725C or equivalent

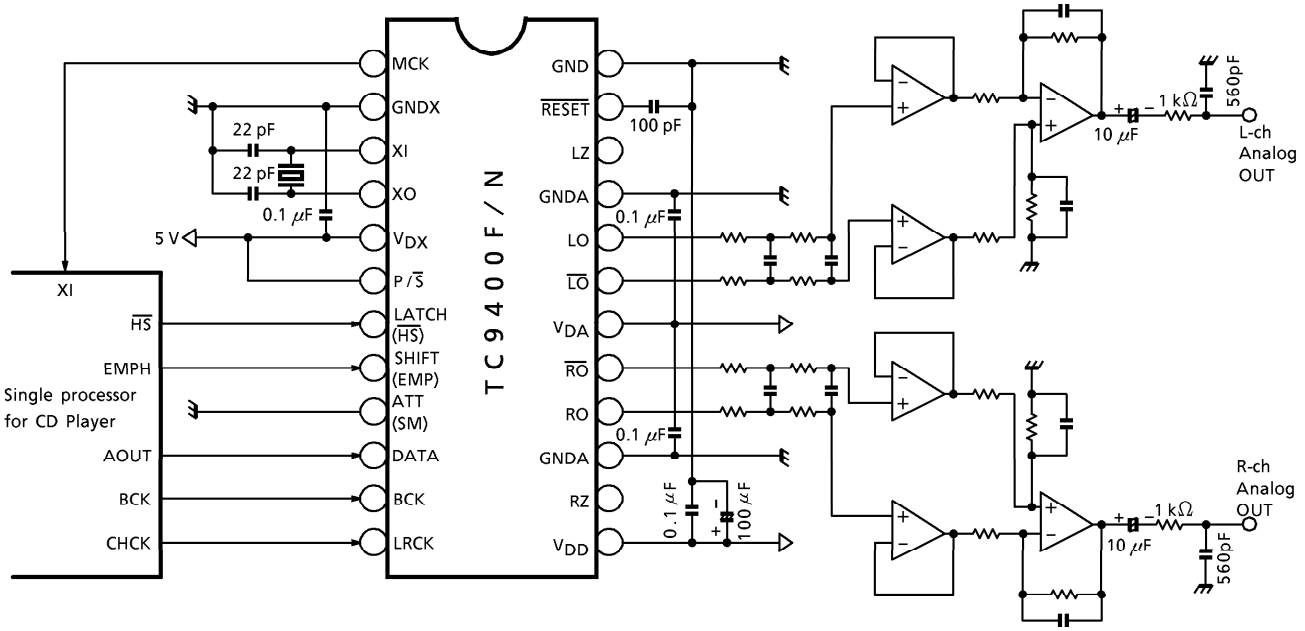
MEASURING ITEM	DISTORTION FACTOR GAUGE FILTER SETTING A WEIGHT
THD + N, CT	OFF
S/N, DR	ON

A weight : IEC-A or equivalent

- **AC CHARACTERISTICS STIPULATED POINT** : (Input signal stipulation : LRCK, BCK, DATA)

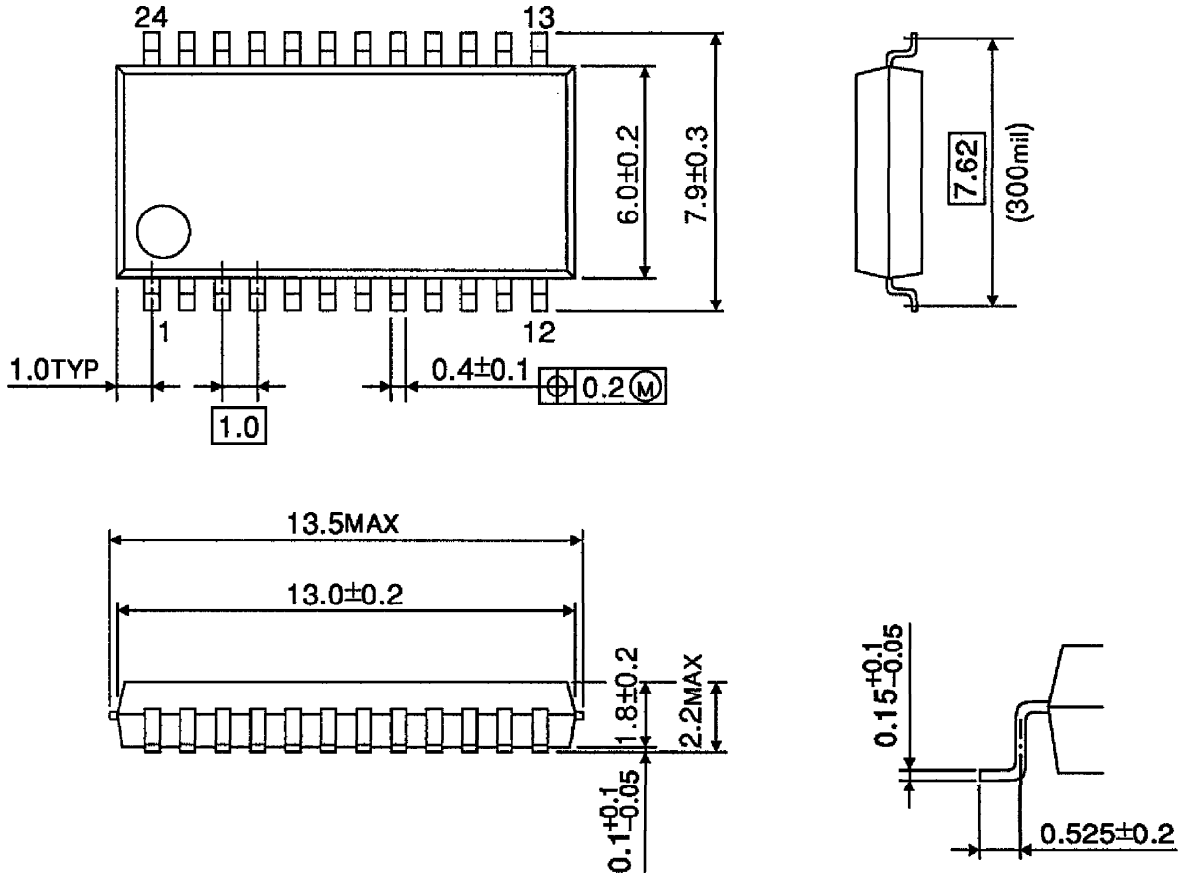


Application Circuit Example



PACKAGE DIMENSIONS

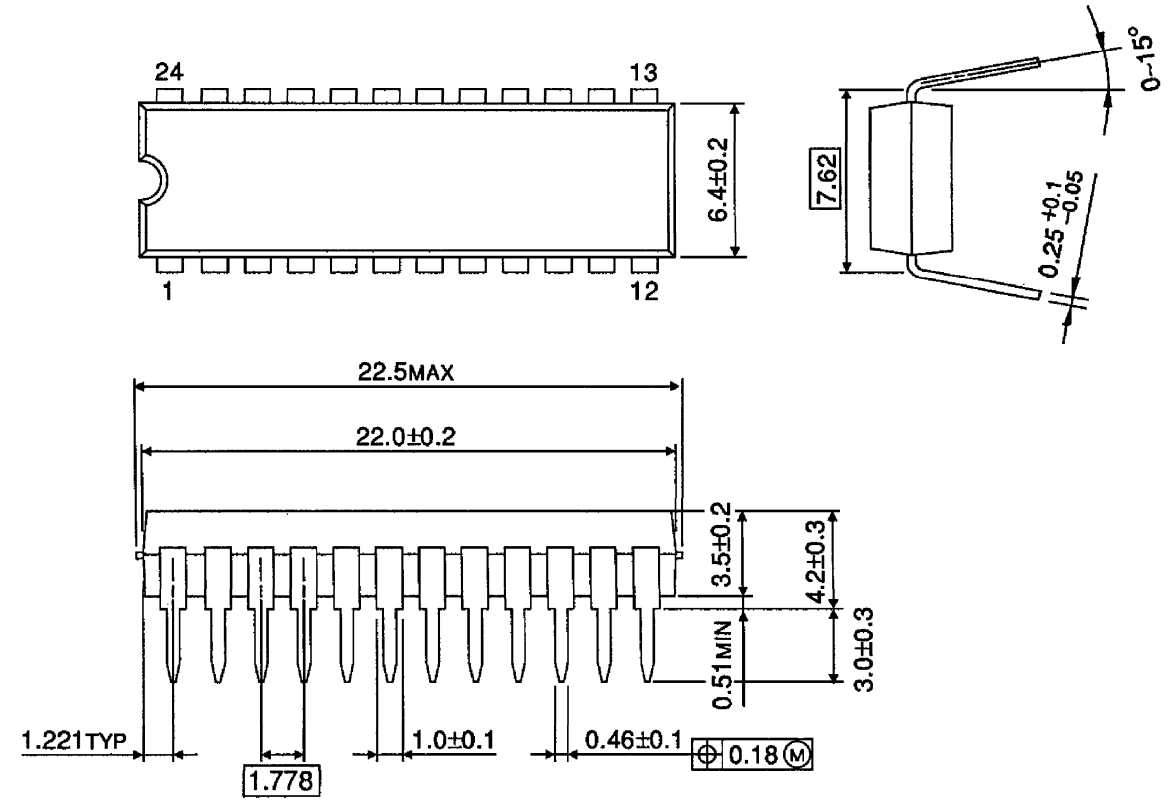
SSOP24-P-300-1.00 Unit : mm



Weight : 0.31 g (Typ.)

PACKAGE DIMENSIONS

SDIP24-P-300-1.78 Unit : mm



Weight : 1.2 g (Typ.)

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