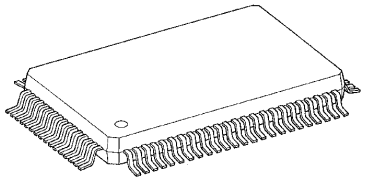
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC9314F

SINGLE-CHIP DTS MICROCONTROLLER (DTS-22)

TC9314F is a 4bit CMOS microcontroller for single-chip digital tuning systems with built-in prescaler, PLL and LCD driver.
The CPU has 4bit parallel addition / subtraction (eg, AI and SI instructions), logical operations (eg, OR and AN), several bit judge and compare instructions (eg, TM and SL), and time base functions.
The device is in an 80pin mini flat package. It includes abundant I / O ports controlled by powerful input and output instructions (IN1-3, OUT1-3) exclusive key input ports, abundant LCD output ports, interrupts, a BUZR port, 6bit A / D and D / A converters, serial interface, and IF counter.
With CMOS architecture for low power consumption, TC9314F is ideal for providing digital tuning for multiband radios, radio-cessatte players and other portable equipment.



QFP80-P-1420-0.80A

Weight : 1.57g (Typ.)

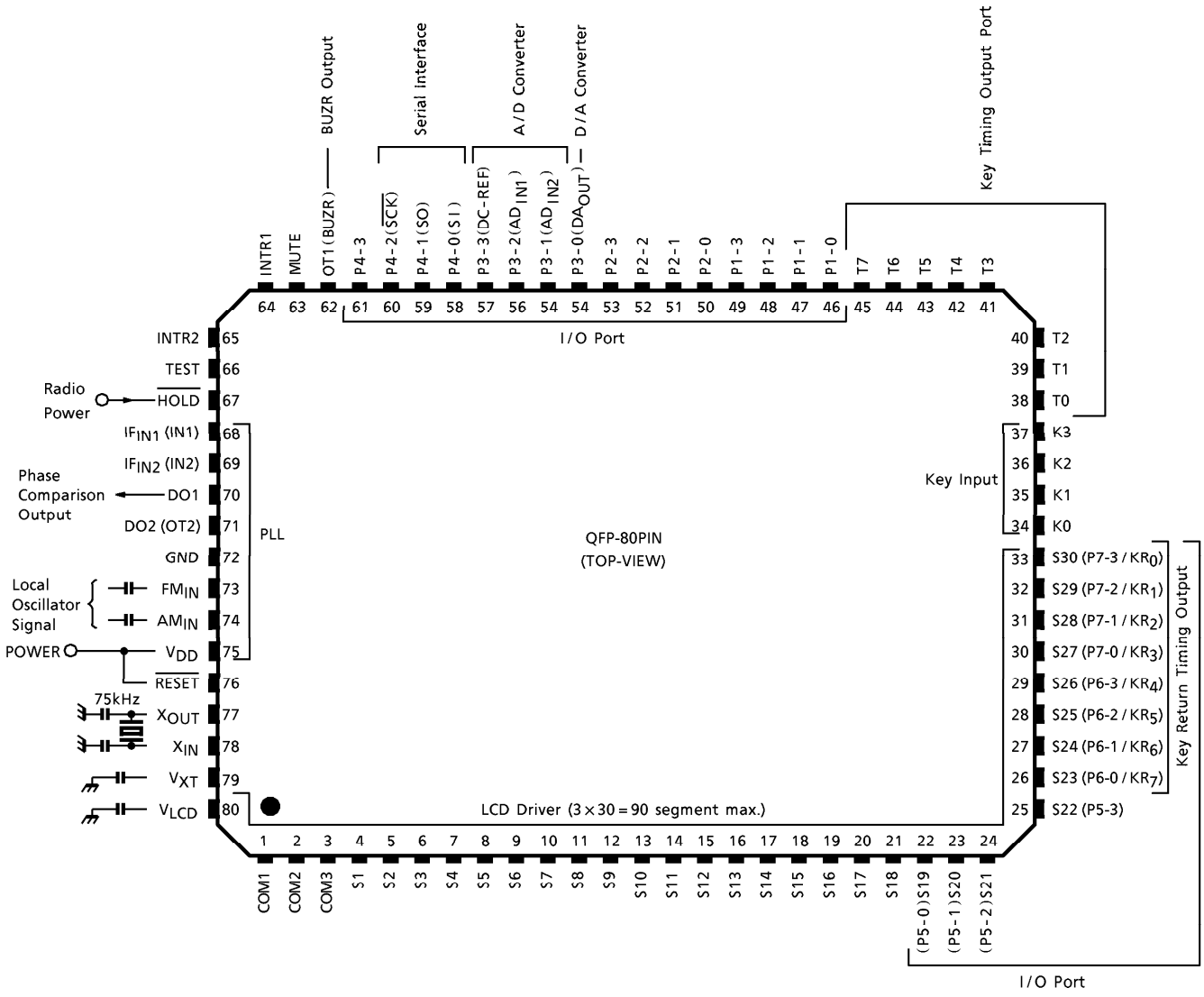
FEATURES

- 4bit microcontroller for single-chip digital tuning systems
- Operating voltage V_{DD} of 2.7~5.5V, with CMOS architecture for low power consumption
- On-chip prescaler (fixed to 1 / 2 frequency division + 2-modulus prescaler : fmax ≧ 130MHz)
- 1 / 3-duty, 1 / 2-bias driven LCD driver, with on-chip 3V constant-voltage display circuit
- Easy backup of data memory (RAM) and various ports
- Program ROM : 16 bits × 6144 steps
- Data memory (RAM) : 4 bits × 384 words
- Powerful instruction set with 54 1-word instructions
- Instruction execution time of 40μs (75kHz crystal connected; 80μs for MVGS and DAL instructions)
- 4 add and 4 subtract instructions

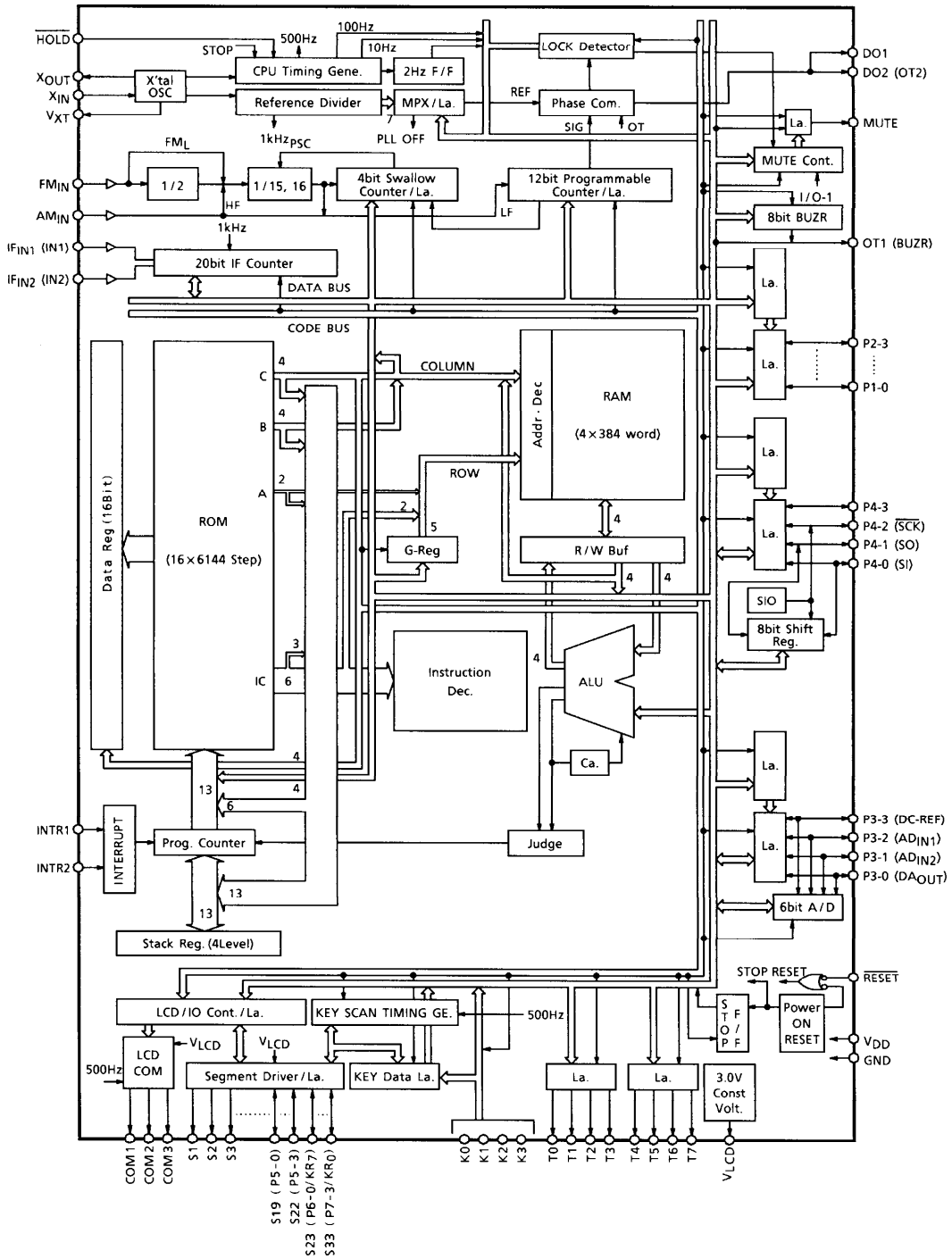
(Note) This device is vulnerable to surge voltage. Take it into account when using this device in your system.

- Powerful compound judge instructions (TMTR, TMFR, TMT, TMF, TMTN and TMFN)
- Data transfer at the same row address (MVSR instruction)
- Register indirect transfer available (MVGD and MVGS instructions)
- 16 powerful general registers assigned in RAM
- Stack levels : 4
- No concepts of pages or fields in program ROM. Features 6144 steps that allow JUMP or CAL instructions at any point.
- 16bit contents of any address in 1024 steps of the program ROM can be referenced freely. (DAL instruction)
- Independent FM_{IN} and AM_{IN} pins for FM and AM frequency input and two phase comparison outputs (DO1 and DO2).
- Choice of seven reference frequencies by program
- Powerful input and output instructions (IN1~3 and OUT1~3)
- Input-only ports (K0~K3) for key inputs and 33 LCD drive pins (90 segments maximum).
- 26 I/O ports (16 ports specifiable in units of bits, 10 output-only ports). Three pins (IF_{IN1}, IF_{IN2} and DO2) can be switched using instructions for use as input-only ports IN1 and IN2, and output-only port OT2, respectively. In addition LCD output pins S19~S30 can be switched to I/O ports in units of bits.
- 2 external interrupt input ports.
  These are able to switch for use as general input ports by program.
- Three backup modes can be implemented using instructions : CPU operation only, clock generation only or clock stop.
- Features a built-in 2Hz timer flip-flop and 10/100Hz interval pulse output (internal time-based port)
- Detection of PLL locked state supported.
- 8 of the LCD segment outputs (S23~S30) can also be used as key return timing outputs (KR_0~KR_7), so that output ports are not monopolized by key return outputs and are available for other uses.
- Built-in 20bit general-purpose IF counter counts central frequencies for each band, providing station detection during automatic tuning.
- Built-in 8bit buzzer output circuit supports generation of 254-level tone signals.
- Built-in 2-channel, 6bit A/D converter and 1-channel, 6bit D/A converter.
- Low-voltage detection circuit stops the CPU when power supply voltage drops below 1.5V to prevent malfunction.
- OTP Product : TC93P14F

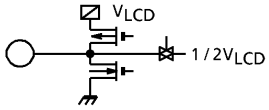
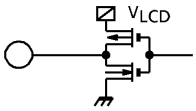
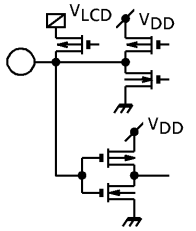
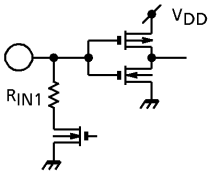
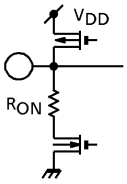
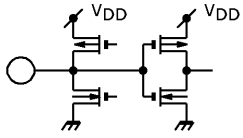
PIN CONNECTION

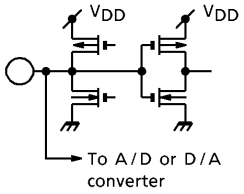


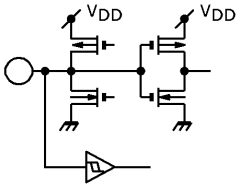
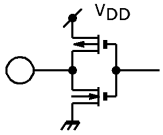
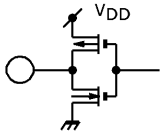
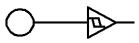
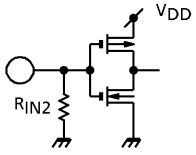
BLOCK DIAGRAM

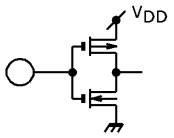
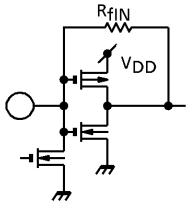


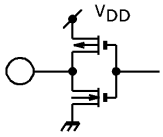
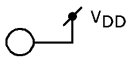
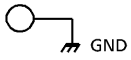
PIN FUNCTION

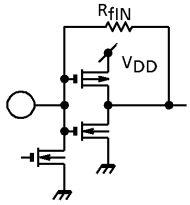
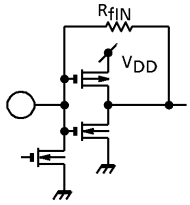
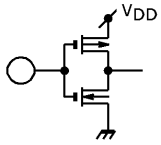
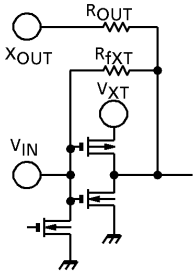
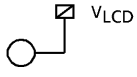
PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
1	COM1	LCD common outputs	Common output pins for the LCD panel. Can display up to 90 segments in a matrix with S1-S30. Three value levels, V_{LCD}, $1/2V_{LCD}$ and GND, are output at 2ms intervals at an 83Hz cycle. After system reset or clock stop are released, $1/2V_{LCD}$ is output, setting the DISP OFF bit to 0 and outputting the common signal.	
2	COM2			
3	COM3			
4~21	S1~S18	LCD segments outputs	Segment signal output pins for the LCD panel. Together with COM1, COM2 and COM3, a matrix is formed that can display a maximum of 90 segments. Pins S19~S30 can programmed as I/O ports. The signals for the key matrix and the segment signals from S23/KR7~S30/KR0 are output on a time division basis. 4×8=32 key matrix can be configured with key input ports K0~K3.	
22~25	S19/P5-0 ~ S22/P5-3	LCD segment outputs/ I/O ports		
26~33	S23/P6-0/KR7 ~ S30/P7-3/KR0	LCD segment outputs/ I/O ports/key return timing outputs		
34~37	K0~K3	Key input ports	4bit port for key-matrix inputs. In combination with key return timing outputs KR_0~KR_7 for the LCD segment pins, these ports support data input for up to 4×8=32 keys. Pull-down resistors are built in. A key matrix can also be configured using key timing output ports T0~T7.	
38~45	T0~T7	Key timing output ports	Key matrix timing signal output ports. To configure the key matrix, N-channel load resistors are built in. When keys are connected, the matrix diodes can be omitted.	
46~53	P1-0 ~ P2-3	I/O ports 1 and 2	8bit I/O port. Input or output can be programmed for each bit.	

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
54~57	P3-0 / DA_{OUT} P3-1 / AD_{IN2} P3-2 / AD_{IN1} P3-3 / DC-REF	I/O port 3 / D/A analog voltage output /A/D analog voltage input /A/D analog voltage input /reference voltage input	4bit I/O port. Input or output can be programmed for each bit. Pins P3-0 through P3-2 serve as the analog inputs and outputs for the built-in A/D and D/A converters. The A/D converter operates by successive comparison method based on software control. Pins can be set to A/D, D/A analog input/output in units of bits as necessary. P3-3 can be set to reference voltage input. Reference voltage can be set to the internal supply voltage (V_{DD}). It is also possible to input V_{EED} to the A/D analog input, enabling measurement of battery voltage and the like. The D/A converter outputs analog voltage through the operating amplifier with shared the comparison voltage generator circuit used by the A/D converter. To share the reference voltage generator circuit with the A/D converter, D/A converter output is set to high impedance during A/D conversion. It is necessary at such times to connect an analog voltage hold capacitor to the D/A output pin. The A/D and D/A converters, as well as their controls, are all programmable.	

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
58~61	P4-0 / SI P4-1 / SO P4-2 / $\overline{SCK}$ P4-3	I / O port 4 / serial data input / serial data output / serial clock input / output I / O port 4	4bit I / O port. Input or output can be programmed for each bit. Pins P4-0 through P4-2 also serve as input / output pins for the serial interface circuit (SIO). SIO inputs 4bit or 8bit serial data at the clock edge of the $\overline{SCK}$ pin; outputs data from the SO pin. The serial operating clock ($\overline{SCK}$) allows selection between internal and external, and between rising and falling clock edge shift. The SO pin can be switched to serial input (SI), facilitating control of a variety of LSIs and communication between controllers. All SIO inputs have built-in Schmittcircuits. All SIOs and their controls can be used or set by program.	
62	OT1 / BUZR	General-purpose output port / buzzer output	1bit output port that also serves as the built- in buzzer circuit output. Buzzer buzzes in 254 levels from 18.75kHz to 147Hz, with a duty factor of 50%. Buzzer output control can be used or set by program.	
63	MUTE	Muting output port	1bit output port. Normally used for output of the muting control signal. It allows the internal MUTE bit to be set to 1 based on I / O port 1 input state. It can also change MUTE bit output logic and output PLL phase differences.	
64 65	INTR1 INTR2	External interrupt input	External interrupt input pins. Can be used for remote control signal input or tape travel detection input. Can also be programmed as general-purpose input ports.	
66	TEST	Test mode control input	Input pin for controlling test mode. When the pin is high, test mode; when low, normal operation. Normally used low or in the NC state. (pull-down resistance built in)	

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
67	$\overline{HOLD}$	Hold mode control input	Input pin used to request / cancel a hold state. Normally used for the radio mode select signal input or for the battery detection signal input. Hold states can be either clock stop mode (crystal oscillation stopped) or wait mode (CPU stopped). The mode is set by a CKSTP or WAIT instruction. When CKSTP instruction is executed, the hold state request / cancel differs depending on the internal MODE bit. When the MODE bit is 0 (MODE-0), executing the CKSTP instruction while the $\overline{HOLD}$ pin is low stops the clock generator and the CPU, and enters memory backup state. When the MODE bit is 1 (MODE-1), executing the CKSTP instruction regardless of whether the $\overline{HOLD}$ pin is high or low enters memory backup state. This state is canceled in MODE-0 when the $\overline{HOLD}$ pin changes to high; in MODE-1, when the input at the $\overline{HOLD}$ pin changes. When a WAIT instruction is executed, the state is cancelled by changes in inputs at this pin. During memory backup, current consumption is reduced (to 1μA or less) and all output pins (display outputs, output ports, etc.) automatically are set to low.	
68 69	IF_{IN1} / IN1 IF_{IN2} / IN2	IF signal input / input port	IF signal input pin for the IF counter; counts the IF signals for the FM and AM bands and detects autostop. Input frequency is 0.3~12MHz ($0.2V_{p-p}$min). The built-in input amplifier operates at small amplitude withcapacitors connected. The IF counter is a 20bit counter with gate time selectable to 1, 4, 16 or 64 ms, allowing 20 bits of data to be loaded to memory directly. This input pin can be programmed as an input port (IN port). When set to IN port, input is CMOS level.	

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
70 71	DO1 DO2 / OT2	Phase comparator output Phase comparator output / output port	PLL phase comparator output pin. Tri-state output. When the divider output of the programmable counter is higher than the reference frequency, high level is output; when lower, low level is output. When they accord, the output is at high impedance. DO1 and DO2 are parallel outputs, allowing optimized design of filter constants for both the FM and AM bands. The DO2 pin can also be set to high impedance or as an output port (OT2) by program. Thus these two pins can be used to improve lockup time, or to provide effective use of pins as output ports.	
75	V_{DD}	Power supply pins	Pin for applying the power supply. Normally, a V_{DD} of 2.7~5.5V is applied during PLL operation. When PLL is stopped, a V_{DD} of 1.8~5.5V is applied. During backup (at execution of the CKSTP instruction), voltage can be reduced to 1.2V. If voltage drops below 1.5V with the CPU in operation, the CPU is stopped to prevent CPU malfunction (stop mode) and is restarted when the voltage reaches 1.5V. The STOP F / F bit detects whether stop mode is in effect or not, so that initialization or clock modification may be programmed as desired. To detect and control CPU malfunction using an external circuit, stop mode operation can be programmed invalid, at which time all 4 bits of the internal test port are set to 1. If a voltage of 0V to 1.8V or more is applied to this pin, the system is reset and the program starts from address 0 (power on reset). (Note) Due to the power on reset operation, use the device with a supply voltage rise time of between 10ms and 100ms.	
72	GND			

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
73	FM_{IN}	FM broadcast signal input	A programmable counter input pin for the FM band. Either the 1/2+pulse swallow method (FM_H mode) or the pulse swallow method (FM_L mode) can be selected by program. In FM mode, a 50 to 130MHz ($0.3V_{p-p}$min) locally oscillated output (VCO output) is input. The built-in input amplifier operates at small amplitude with capacitors connected. (Note) In PLL off mode and when AM_{IN} input is set, input is pulled down.	
74	AM_{IN}	AM broadcast signal input pin	A programmable counter input pin for the AM band. Either the pulse swallow method (HF mode) or the direct frequency division method can be selected by program. In HF mode, a 1 to 60MHz ($0.3V_{p-p}$min) locally oscillated output (VCO output) is input; in LF mode, 0.5 to 10MHz ($0.2V_{p-p}$min). The built-in input amplifier operates at small amplitude with capacitors connected. (Note) In PLL off mode and when FM_{IN} input is set, input is pulled down.	
76	$\overline{RESET}$	Reset input	System reset signal input pin. When a reset occurs while $\overline{RESET}$ is low, the pin is set to high and the program starts from address 0. Normally, if a voltage of 0V to 1.8V or more is supplied to V_{DD}, the system is reset (power on reset) so use this pin fixed to high.	
77	X_{OUT}	Crystal oscillator pin	Crystal oscillator pin. A 75kHz reference crystal oscillator is connected to the X_{IN} and X_{OUT} pins. Oscillation stops during execution of a CKSTP instruction. The V_{XT} pin is the power supply for the crystal oscillator. Connect a capacitor (0.47μF Typ.) for stabilization.	
78	X_{IN}			
79	V_{XT}			
80	V_{LCD}	3V constant-voltage output pin	3V constant-voltage output pin for driving the LCDs. Connect a capacitor (1.0μF Typ.) for stabilization.	

(Note 1) When a device is reset (V_{DD} from 0V to 1.8V or more, or $\overline{RESET}$ from low to high), the I/O ports are set to input; the LCD output and I/O port common pins are set to LCD output, the I/O ports and common pins with additional functions (eg, SIO, A/D converter) are set to I/O port input pins; the IF_{IN} pin is set to IF input.

(Note 2) In PLL off mode (all 4 bits of the internal reference port are set to 1), IF_{IN} and the FM_{IN} and AM_{IN} pins are pulled down, and DO1 and DO2 are at high-impedance.

(Note 3) In clock stop mode (during execution of the CKSTP instruction), output ports and LCD output pins are all set to low. The constant-voltage circuit (V_{LCD}) and clock generator power supply (V_{XT}) are turned off.

(Note 4) When a device is reset, the contents of output ports and internal ports are undefined. Therefore, initialize by program as required.

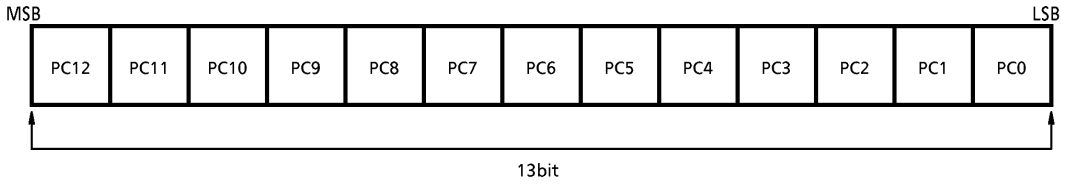
EXPLANATION OF OPERATION

○ CPU

CPU is composed of program counter, stack register, ALU, program memory, data memory, G-register, carry F/F and judging circuit.

1. Program counter (PC)

   Program Counter is a block to designate the address of program memory (ROM), and is composed of 13 bits binary up counter. This is cleared by system reset, and the program starts from zero address.
   Usually, it's increment is made one by one everytime the one instruction is executed, but when JUMP instruction or CAL instruction is executed, the address designated at operand part of that instruction is loaded.
   Further, when the instruction (SLT1, TMT, SKP, RNS instructions, etc.) having skip function is executed, two increments of program counter is made if the result is the condition to be skipped, and the succeeding instruction is skipped.



2. Stack register (STACK)

   This is a register composed of 4×13 bits during the execution of subroutine call instruction, the [illegible] housed. The content of stack register is loaded on the program counter by the execution of return instruction. (RN, RNS instructions)
   This stack level is 4 level, and nesting is 4 level.

3. ALU

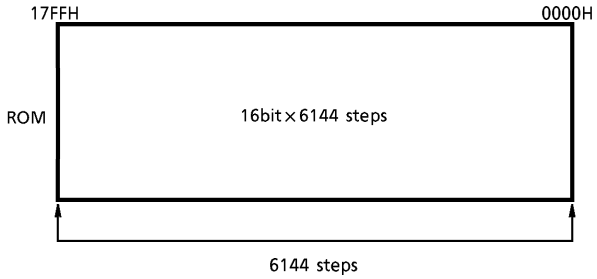
   ALU has binary 4 bits parallel addition and subtraction, logical operation, comparison and plural bit judge functions.
   This CPU has no accumulator, and all operations directly treat the contents of data memory.

4. Program memory (ROM)

Program memory is composed of 16bit×6144 steps and is the address of 0000H~17FFH.
Program memory has no concept of page or field, so JUMP instruction and CAL instruction can be freely used among 6144 steps.
Further, it is possible to use optional address of program memory as data area, and its content, 16 bits, can be loaded to the data register by executing DAL instruction.

(Note) Provide the data area at the address outside the program loop in the program memory.

(Note) In DAL instruction, the address of program memory can be designated as the data area becomes 1024 steps of 0000H~03FFH.



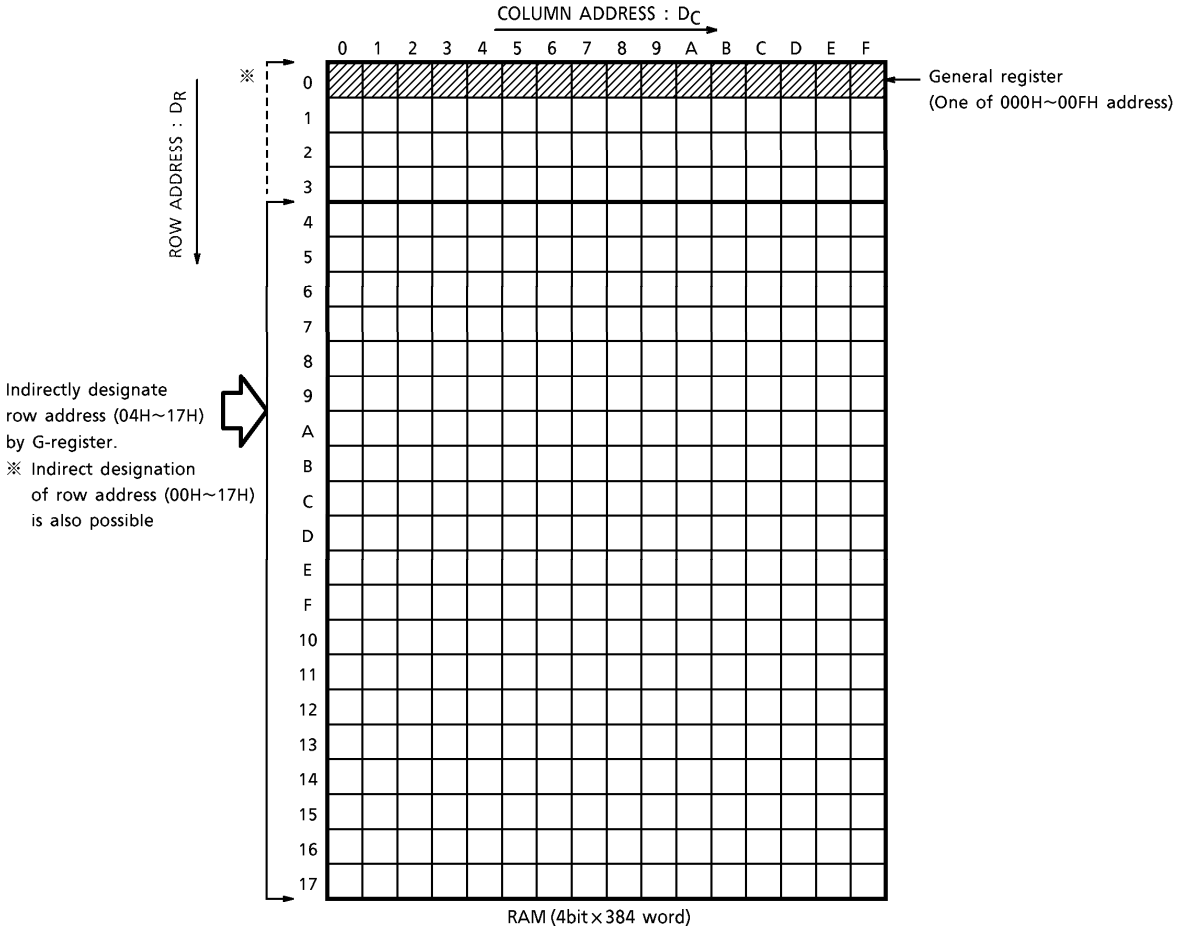
5. Data memory (RAM)

Data memory is composed of 4bit×384 words and used for storing data.
This 384 words are expressed with row address (5 bits) and column address (4 bits).
320 words (row address = 04H~17H) among the data memory are indirect addressing by G-register. For this reason, when carrying out data processing within this territory, it is necessary to designate row address by G-register beforehand Area of 000H~00FH address in data memory is called general register, and can be used only by designating column address (4 bits). These 16 general registers can be used for operation and transfer between data memories. Further, it can also be used as ordinary data memory.

(Note) The column address (4 bits) to designate general register becomes register number of the general register.

(Note) It is also possible to indirectly designate all of row address (= 00H~17H) by G-register.

(Note) 256 words (row address = 00H~0FH) among the data memory are direct addressing by LD or ST instructions.



6. G-register (G-REG.)

   G-register is a 5 bits register for addressing row address (D_R = 04H~17H) of 320 words in data memory.
   Content of this register is effective during executing MVGD instruction, MVGS instruction, and is not related with the execution of other instructions.
   This register is treated as one of the port, and its content is set by the execution of OUT1 instruction among input and output instructions.
   (refer to register port item 1)
   Content of this register can directly setting by the execution STIG instruction.

7. Data register (DATA REG.)

   This is a register composed of 1×16 bits. In this register, 16 bits data of optional address among the program memory is loaded during executing of DAL instruction. This register is treated as one of the port, and when KEY instruction among input and output instruction is executed, it's content is read in the data memory in 4 bits unit.
   (refer to register port item 2 page 39)

8. Carry F/F (C·F/F)

   This is set when carry or borrow is produced as a result of executing operational instruction, and is reset when it is not produced. Content of carry F/F changes only when addition and subtraction instruction is executed, and does not change during the execution of other instructions.

9. Judging circuit (J)

When a instruction with skip function is executed, this circuit judges it's skip condition. When skip condition is satisfied, this circuit makes two increments of program counter, and skips the succeeding instruction.
It is provided with 15 kinds of instructions having abundant skip function.
(refer to Item 11, explanation list of function and operation of instructions, ※ marked instruction)

10. List of instruction set

54 kinds of instruction set are included, all of which consisting of one word instruction. These instructions are expressed with 6 bits instruction code.

Higher Rank 2 bits / Lower Rank 4 bits		00	01	10	11
		0	1	2	3
0000	0	AI M, I	TMTR r, M	CALL $ADDR_1$	SLTI M, I
0001	1	AIC M, I	TMFR r, M		SGEI M, I
0010	2	SI M, I	SEQ r, M		SEQI M, I
0011	3	SIB M, I	SNE r, M		SNEI M, I
0100	4	ORIM M, I	LD r, M*		TMTN M, N
0101	5	ANIM M, I			TMT M, N
0110	6	XORIM M, I			TMFN M, N
0111	7	MVIM M, I			TMF M, N
1000	8	AD r, M	ST M*, r	JUMP $ADDR_1$	IN1 M, C
1001	9	AC r, M			IN2 M, C
1010	A	SU r, M			IN3 M, C
1011	B	SB r, M			OUT1 C, M
1100	C	ORR r, M	CLT r, M		OUT2 C, M
1101	D	ANDR r, M	CLTC r, M		OUT3 C, M
1110	E	XORR r, M	MVGD r, M		DAL $ADDR_2$, r
1111	F	MVSR M1, M2	MVGS M, r		SHRC M RORC M STIG I* SKP, SKPN, RN, RNS WAIT P SKSTP XCH M NOOP

11. Explanation list of function and operation of instructions (Explanation of symbols)

M	:	Data memory address Normally, one of 000H~03FH address of data memory.
M*	:	Data memory address (256 word) One of 000H~0FFH address of data memory (Available at executing ST and LD instruction)
r	:	General register One of 00H~0FH address of data memory.
PC	:	Program counter (13bit)
STACK	:	Stack register (13bit)
G	:	G-register (5bit)
DATA	:	Data register (16bit)
I	:	Immediate data (4bit)
I*	:	Immediate data (5bit)
N	:	Bit position (4bit)
—	:	All "0"
C	:	Code No. of port (4bit)
C_N	:	Lower rank 3bit of port code No. (4bit)
R_N	:	General register No. (4bit)
$ADDR_1$	:	Program memory address in page 0 or 1 (13bit)
$ADDR_2$	:	Higher rank 6bit of program memory address in page 0
Ca	:	Carry
b	:	Borrow
IN1~IN3	:	Port treated during the execution IN1~IN3 instruction
OUT1~OUT3	:	Port treated during the execution OUT1~OUT3 instruction
( )	:	Register or data memory content
$[\ ]_C$	:	Content of port indicated by code No. C (4bit)
[ ]	:	Content of data memory indicated by the content of register or data memory
$[\ ]_P$	:	Content of program memory (16bit)
IC	:	Instruction code (6bit)
※	:	Instruction having skip function
D_C	:	Data memory column address (4bit)
D_R	:	Data memory row address (2bit)
D_R*	:	Data memory row address (4bit) (Available at executing ST and LD instruction)
(M) b0~(M) b3	:	Bit data for content of data memory

INST. GR.	MNEMONIC	SKIP FUNCTION	EXPLANATION OF FUNCTION	EXPLANATION OF OPERATION	MACHINE LANGUAGE (16bit)			
					IC (6bit)	A (2bit)	B (4bit)	C (4bit)
ADDITION INSTRUCTION	AI M, I		Add immediate data to memory	M← (M) + I	000000	D_R	D_C	I
	AIC M, I		Add immediate data to memory with carry	M← (M) + I + ca	000001	D_R	D_C	I
	AD r, M		Add memory to general register	r← (r) + (M)	001000	D_R	D_C	R_N
	AC r, M		Add memory to general register with carry	r← (r) + (M) + ca	001001	D_R	D_C	R_N
SUBTRACTION INSTRUCTION	SI M, I		Subtract immediate data from memory	M← (M) − I	000010	D_R	D_C	I
	SIB M, I		Subtract immdediate data from memory with borrow	M← (M) − I − b	000011	D_R	D_C	I
	SU r, M		subtract memory form general register	r← (r) − (M)	001010	D_R	D_C	R_N
	SB r, M		subtract memory form general register with borrow	r← (r) − (M) − b	001011	D_R	D_C	R_N
COMPARISON INSTRUCTION	SLTI M, I	※	Skip if memory is less than immediate data	Skip if (M) < I	110000	D_R	D_C	I
	SGEI M, I	※	Skip if memory is greater than or equal to immediate data	Skip if (M) ≧ I	110001	D_R	D_C	I
	SEQI M, I	※	Skip if memory is equal to immediate data	Skip if (M) = I	110010	D_R	D_C	I
	SNEI M, I	※	Skip if memory is not equal to immediate data	Skip if (M) ≠ I	110011	D_R	D_C	I
	SEQ r, M	※	Skip if general register is equal to memory	Skip if (r) = (M)	010010	D_R	D_C	R_N
	SNE r, M	※	Skip if general register is not equal to memory	Skip if (r) ≠ (M)	010011	D_R	D_C	R_N

INST. GR.	MNEMONIC	SKIP FUNCTION	EXPLANATION OF FUNCTION	EXPLANATION OF OPERATION	MACHINE LANGUAGE (16bit) IC (6bit)	A (2bit)	B (4bit)	C (4bit)
COMPARISON INSTRUCTION	CLT r, M		Set carry flag if general register is less than memory, or reset if not	(CY)←1 if (r) < (M) or (CY)←0 if (r) ≧ (M)	011100	D_R	D_C	R_N
	CLTC r, M		Set carry flag if general register is less than memory with carry or reset if not	(CY)←1 if (r) < (M) + (Ca) or (CY)←0 if (r) ≧ (M) + (Ca)	011101	D_R	D_C	R_N
TRANSFER INSTRUCTION	LD r, M*		Load memory to general register	r← (M*)	0101	D_R* (4bit)	D_C	R_N
	ST M*, r		Store general register to memory	M*← (r)	0110	D_R* (4bit)	D_C	R_N
	MVSR M_1, M_2		Move memory to memory in the same row	(D_R, D_{C1}) ← (D_R, D_{C2})	001111	D_R	D_{C1}	D_{C2}
	MVIM M, I		Move immediate data to memory	M←I	000111	D_R	D_C	I
	MVGD r, M		Move memory to destination memory referring to G-register and general register	[(G), (r)] ← (M)	011110	D_R	D_C	R_N
	MVGS M, r		Move source memory referring to G-register and general register to memory	M← [(G), (r)]	011111	D_R	D_C	R_N
	STIG I*		Move immediate data to G-register	G← I*	111111	0	I* (5bit)	0010
INPUT AND OUTPUT INSTRUCTION	IN1 M, C		Input IN1 port data to memory	M← $[IN1]_C$	111000	D_R	D_C	C_N
	OUT1 C, M		Output contents of memory to OUT1 port	$[OUT1]_C$← (M)	111011	D_R	D_C	C_N
	IN2 M, C		Input IN2 port data to memory	M← $[IN2]_C$	111001	D_R	D_C	C_N
	OUT2 C, M		Output contents of memory to OUT2 port	$[OUT2]_C$← (M)	111100	D_R	D_C	C_N
	IN3 M, C		Input IN3 port data to memory	M← $[IN3]_C$	111010	D_R	D_C	C_N
	OUT3 C, M		Output contents of memory to OUT3 port	$[OUT3]_C$← (M)	111101	D_R	D_C	C_N

INST. GR.	MNEMONIC	SKIP FUNCTION	EXPLANATION OF FUNCTION	EXPLANATION OF OPERATION	MACHINE LANGUAGE (16bit)			
					IC (6bit)	A (2bit)	B (4bit)	C (4bit)
LOGICAL OPERATION INSTRUCTION	ORR r, M		Logical OR of general register and memory	r← (r) ∨ (M)	001100	D_R	D_C	R_N
	ANDR r, M		Logical AND of general register and memory	r← (r) ∧ (M)	001101	D_R	D_C	R_N
	ORIM M, I		Logical OR of memory and immediate data	M← (M) ∨I	000100	D_R	D_C	I
	ANIM M, I		Logical AND of memory and immediate data	M← (M) ∧I	000101	D_R	D_C	I
	XORIM M, I		Logical exclusive OR of memory and immediate data	M← (M) ∀ I	000110	D_R	D_C	I
	XORR r, M		Logical exclusive OR of general register and memory	r← (r) ∀ (M)	001110	D_R	D_C	R_N
BIT JUDGE INSTRUCTION	TMTR r, M	※	Test general register bits by memory bits, then skip if all bits specified are true	Skip if r [N (M)] = all "1"	010000	D_R	D_C	R_N
	TMFR r, M	※	Test general register bits by memory bits, then skip if all bits specified are false	Skip if r [N (M)] = all "0"	010001	D_R	D_C	R_N
	TMT M, N	※	Test memory bits, then skip if all bits specified are true	Skip if M (N) = all "1"	110101	D_R	D_C	N
	TMF M, N	※	Test memory bits, then skip if all bits specified are false	Skip if M (N) = all "0"	110111	D_R	D_C	N

INST. GR.	MNEMONIC	SKIP FUNCTION	EXPLANATION OF FUNCTION	EXPLANATION OF OPERATION	MACHINE LANGUAGE (16bit) IC (6bit)	A (2bit)	B (4bit)	C (4bit)
BIT JUDGE INSTRUCTION	TMTN M, N	※	Test memory bits, then not skip if all bits specified are true	Skip if M (N) = not all "1"	110100	D_R	D_C	N
	TMFN M, N	※	Test memory bits, then not skip if all bits specified are false	Skip if M (N) = not all "0"	110110	D_R	D_C	N
	SKP	※	Skip if carry flag is set	Skip if (CY) = 1	111111	00	—	0011
	SKPN	※	Skip if carry flag is reset	Skip if (CY) = 0	111111	01	—	0011
SUBROUTINE INSTRUCTION	CALL $ADDR_1$		Call subroutine	STACK← (PC) + 1 and PC←$ADDR_1$	100	$ADDR_1$ (13bit)		
	RN		Return to main routine	PC← (STACK)	111111	10	—	0011
	RNS	※	Return to main routine and skip unconditionally	PC← (STACK) and skip	111111	11	—	0011
JUMP INST.	JUMP $ADDR_1$		Jump to the address specified	PC←$ADDR_1$	101	$ADDR_1$ (13bit)		
OTHER INSTRUCTION	SHRC M		Shift memory bits to right direction with carry	0→ (M) b3→ (M) b2→ (M) b1→ (M) b0→ (CY)	111111	D_R	D_C	0000
	RORC M		Rotate memory bits to right direction with carry	→ (M) b3→ (M) b2→ (M) b1→ (M) b0→ (CY)→	111111	D_R	D_C	0001
	XCH M		Exchange memory bits mutually	(M) b3 ↔ (M) b0, (M) b2 ↔ (M) b1	111111	D_R	D_C	0110
	DAL $ADDR_2$, r		Load program memory in page 0 to DATA register	DATA← [$ADDR_2$ + (r)] P in page 0	111110	$ADDR_2$ (6bit)		R_N

INST. GR.	MNEMONIC	SKIP FUNCTION	EXPLANATION OF FUNCTION	EXPLANATION OF OPERATION	MACHINE LANGUAGE (16bit)			
					IC (6bit)	A (2bit)	B (4bit)	C (4bit)
OTHER INSTRUCTION	WAIT P		At P = "0" H, the condition is CPU waiting (Soft wait mode) At P = "1" H, except for clock generator, all function is waiting (Hard wait mode)	Wait at condition P	111111	P	—	0100
	CKSTP		Clock generator stop	Stop clock generator according to MODE condition	111111	—	—	0101
	NOOP		No operation	—	111111	—	—	1111

(Note 1) Among 10 bits of the program memory address assigned by DAL instruction, the lower rank of 4 bits become indirect addressing based on the content of general register.
DAL instruction executing time is 80μs. (2 machine cycles)

(Note 2) MVGS instruction executing time is 80μs. (2 machine cycles)

○ I/O map

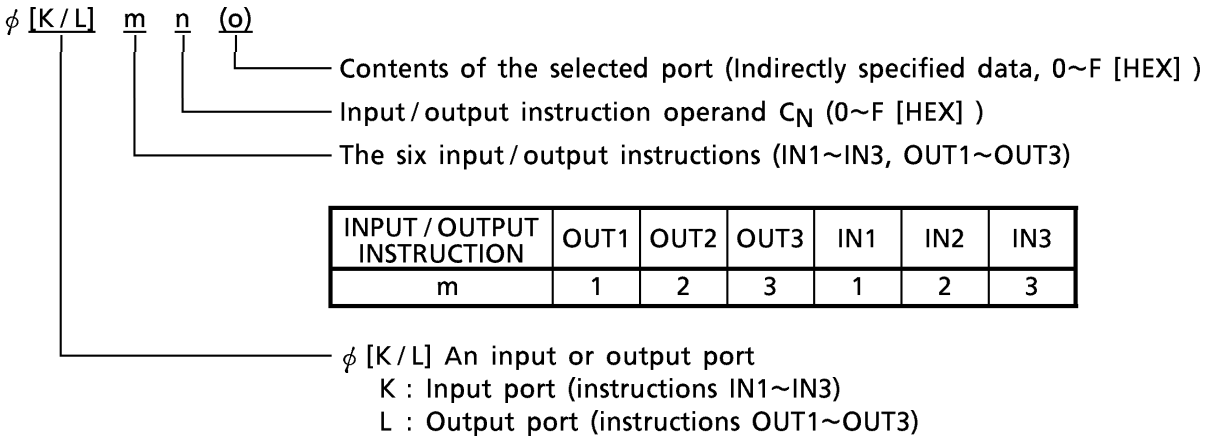
All the ports in the device are accessed by the six input/output instructions (OUT1~OUT3 and IN1~IN3) using the 4bit code number matrices.
The I/O map on the following page shows the port allocation. Horizontally, the I/O map shows the ports manipulated by each input/output instruction. Vertically, the map shows the ports corresponding to each port code number. The G register and the data register are also treated as ports.
Use the OUT1~OUT3 instructions for output ports and the INT1~INT3 instructions for input ports.

(Note 1) The diagonal lines in the I/O map indicate non-existent ports. Executing an instruction to output data to a non-existent output port has no effect on other ports or on data memory contents. Executing an input instruction for a non-existent input port reads all "1" into data memory.

(Note 2) Output ports indicated by an asterisk (*) in the I/O map are unused ports. Data output to these ports are "don't care".

(Note 3) The contents of the ports are represented by four bits where Y1 corresponds to the least significant bit of the data in data memory, and Y8 to the most significant bit.

The ports specified by the six input/output instructions and by code No.C are represented in this document by the following notation.



INPUT/OUTPUT INSTRUCTION	OUT1	OUT2	OUT3	IN1	IN2	IN3
m	1	2	3	1	2	3

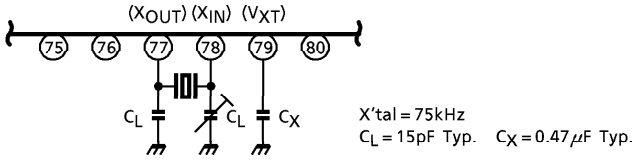
(Example) The G register is set by the OUT1 instruction with codes "D" and "E". Therefore, the notation is "φL1D" and "φL1E".

I/O MAP

I/O	φL1				φL2				φL3				φK1				φK2				φK3			
	OUT1				OUT2				OUT3				IN1				IN2				IN3			
CODE	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8
0		IF offset			DA/AD control				I/O port 1				IF control								I/O port 1			
	HF	+1	−1	FM	DCREF ON	AD1 ON	AD2 ON	DA ON	−0	−1	−2	−3	BUSY	MANUAL	OVER	1					−0	−1	−2	−3
1	Programmable counter				DA REF data 1				I/O port 2				IF data								I/O port 2			
	P0	P1	P2	P3	AR0	AR1	AR2	AR3	−0	−1	−2	−3	F0	F1	F2	F3					−0	−1	−2	−3
2	Programmable counter				DA REF data 2				I/O port 3				IF data								I/O port 3			
	P4	P5	P6	P7	AR4	AR5	SEL0	SEL1	−0	−1	−2	−3	F4	F5	F6	F7	AD OUT	1	1	1	−0	−1	−2	−3
3	Programmable counter				SIO control 1				I/O port 4				IF data								I/O port 4			
	P8	P9	P10	P11	edge	$\overline{SCK}$-INV	$\overline{SCK}$-I/$\overline{O}$	SIO-ON	−0	−1	−2	−3	F8	F9	F10	F11					−0	−1	−2	−3
4	Programmable counter				SIO control 2				I/O port 5				IF data				SIO control				I/O port 5			
	P12	P13	P14	P15	STA	SO-I/$\overline{O}$	8/$\overline{4}$bit	*	−0	−1	−2	−3	F12	F13	F14	F15	BUSY	COUNT	SIO F/F	1	−0	−1	−2	−3
5	Reference selection				SIO output data 1				I/O port 6				IF data				SIO input data 1				I/O port 6			
	R0	R1	R2	R3	SO0	SO1	SO2	SO3	−0	−1	−2	−3	F16	F17	F18	F19	SI0	SI1	SI2	SI3	−0	−1	−2	−3
6	I/F counter control				SIO output data 2				I/O port 7								SIO input data 2				I/O port 7			
	IF 1/$\overline{2}$	SC_{ON}	IF1/$\overline{IN1}$	IF2/$\overline{IN2}$	SO4	SO5	SO6	SO7	−0	−1	−2	−3					SI4	SI5	SI6	SI7	−0	−1	−2	−3
7	I/F counter control				Timer reset		CKSTP	TEST	Output port								Timer			STOP	KEY SCAN digit			
	STA/$\overline{STP}$	MANUAL	G0	G1	2Hz F/F	Clock	Mode	#4	T0	T1	T2	T3					2Hz F/F	10Hz	100Hz	F/F	KS0	KS1	KS2	1
8		MUTE control			Interrupt 1		Interrupt 2		Output port								KEY input data				KEY SCAN input port 0			
	MUTE	I/O	POL	UNLOCK	POL1	INTC1	POL2	INTC2	T4	T5	T6	T7	$\overline{HOLD}$	INTR1	INTR2	1	K0	K1	K2	K3	KS00	KS01	KS02	KS03
9	UNLOCK	DO2 control			Interrupt 1				I/O control 1				UNLOCK		IN port						KEY SCAN input port 1			
	RESET	OTC	OT2	Hz	INT10	INT11	INT12	INT13	−0	−1	−2	−3	F/F	ENA	IN1	IN2					KS10	KS11	KS12	KS13
A	BUZR				Interrupt 1				I/O control 2												KEY SCAN input port 2			
	B0	B1	B2	B3	INT14	INT15	INTE1	INTS1	−0	−1	−2	−3									KS20	KS21	KS22	KS23
B	BUZR				Interrupt 2				I/O control 3												KEY SCAN input port 3			
	B4	B5	B6	B7	INT20	INT21	INT22	INT23	−0	−1	−2	−3									KS30	KS31	KS32	KS33
C					Interrupt 2				I/O control 4				DATA-reg								KEY SCAN input port 4			
					INT24	INT25	INTE2	INTS2	−0	−1	−2	−3	d0	d1	d2	d3					KS40	KS41	KS42	KS43
D	G register				SEG data select				I/O control 5				DATA-reg								KEY SCAN input port 5			
	G0	G1	G2	G3	S1	S2	S4	S8	−0	−1	−2	−3	d4	d5	d6	d7					KS50	KS51	KS52	KS53
E	G register				SEG data 1				I/O control 6				DATA-reg								KEY SCAN input port 6			
	G4	*			COM1	COM1	COM3	*	−0	−1	−2	−3	d8	d9	d10	d11					KS60	KS61	KS62	KS63
F	TEST1				SEG data 2				I/O control 7				DATA-reg								KEY SCAN input port 7			
	#0	#1	#2	#3	COM1	COM2	COM3	SEG I/O	−0	−1	−2	−3	d12	d13	d14	d15					KS70	KS71	KS72	KS73

○ Connecting crystal oscillator

The following diagram shows the connection of the 75kHz crystal oscillator to the device's crystal oscillator pins (X_{IN}, X_{OUT}).
The oscillation signal is supplied to the clock generator, reference frequency divider, and other sub-systems to generate the various CPU timing signals, reference frequency, and other signals. The power supply for the crystal oscillator circuit is the voltage (V_{XT} = 1.5V Typ.) supplied by the built-in constant voltage circuit. This stabilizes the crystal oscillation and reduces the current consumption.



(Note) Use a crystal oscillator with a low CI value and with good startup characteristics.

○ System reset

The system is reset when a low level is applied to the $\overline{RESET}$ pin, or when the voltage supplied to the V_{DD} pin goes from 0V to 1.8V or more (a power on reset). Following a system reset, the program starts from address 0 after a standby period of 100ms.
As the power on reset function is typically used, fix the $\overline{RESET}$ pin to the high level.

(Note 1) During a system reset and during the standby period following the reset, the LCD common and segment outputs are fixed at the low level.

(Note 2) After a system reset, the internal ports shown in the following table are fixed at the specified levels. The states of the other ports after a reset are undefined. Therefore, initialize the ports in the program when necessary.

Fixed internal ports

PORTS SET TO "0"	PORTS SET TO "1"
SC_{ON} bit (ϕL16), MANUAL bit (ϕL17)	Reference port (ϕL15)
I/O, POL, UNLOCK bits (ϕL18)	MUTE bit (ϕL18)
DO2 control port (ϕL19)	IF1/$\overline{2}$, IF1/$\overline{IN1}$, IF2/$\overline{IN2}$ bits (ϕL16)
BUZR ports (ϕL1A, ϕL1B)	
Test ports (ϕL1F, ϕL27, ϕL2FF)	
CKSTP MODE bit (ϕL27)	
DA/AD control ports (ϕL20, ϕL22)	
SIO control ports (ϕL23, ϕL24)	
Timer port (ϕK27)	
V_{LCD} OFF, $\overline{KSSTP}$ bits (ϕL2FF)	
I/O-1~I/O-7 I/O control ports (ϕL39~ϕL3F)	DISP OFF bit (ϕL2FF)
	SEG I/O bit
	(SEG/I/O switching bits : ϕL2F2~ϕL2FD)

○ Backup modes

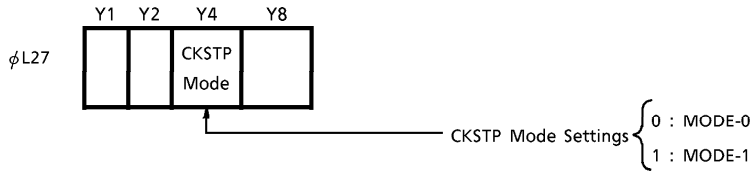
To enter the three backup modes, execute the CKSTP or WAIT instruction.

1. Clock stop mode

Clock stop mode halts the system and maintains the internal state of the system immediately prior to halting. During a halt, the system is maintained with low current consumption (1μA or below, at V_{DD} = 5V). In clock stop mode, the crystal oscillator halts and the output ports and LCD display output pins are all automatically set to the low level or the off state. The supply voltage can be reduced to 1.2V.
When the CKSTP instruction is executed, execution halts at the address of the CKSTP instruction. Therefore, execution starts again from the next instruction when clock stop mode is released (after a standby period of around 100ms).

(1) Setting clock stop mode

Clock stop mode can be set to one of two modes. The CKSTP bit determines which of the two modes is set. Use the OUT2 instruction with the operand [C_N = 7H] to access this bit.



① MODE-0

In mode 0, executing the CKSTP instruction when the $\overline{HOLD}$ pin is low enters clock stop mode. Executing the CKSTP instruction when the $\overline{HOLD}$ pin is high is equivalent to executing a NOOP instruction.

② MODE-1

In mode 1, executing the CKSTP instruction enters clock stop mode regardless of the level of the $\overline{HOLD}$ pin.

(Note) The PLL turns off during execution of the CKSTP instruction.

(2) Releasing clock stop mode

① MODE-0

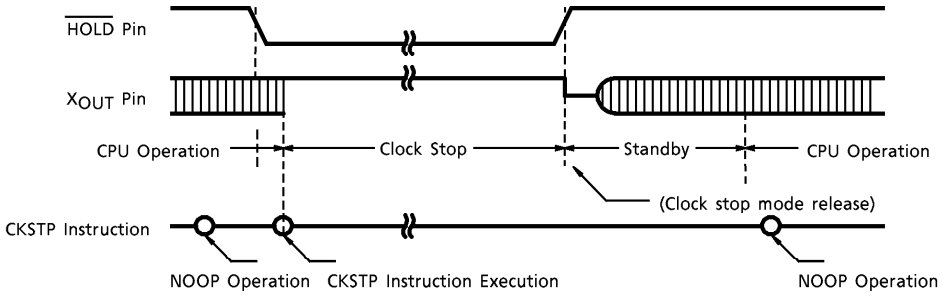
In mode 0, clock stop mode is released when the $\overline{HOLD}$ pin goes to high, or by a change in the input state of any I/O port 1 pin (P1-0~P1-3) set as an input port.

② MODE-1

In mode 1, clock stop mode is released by a change in the input state of the $\overline{HOLD}$ pin or in the input state of any I/O port 1 pin (P1-0~P1-3) set as an input port.

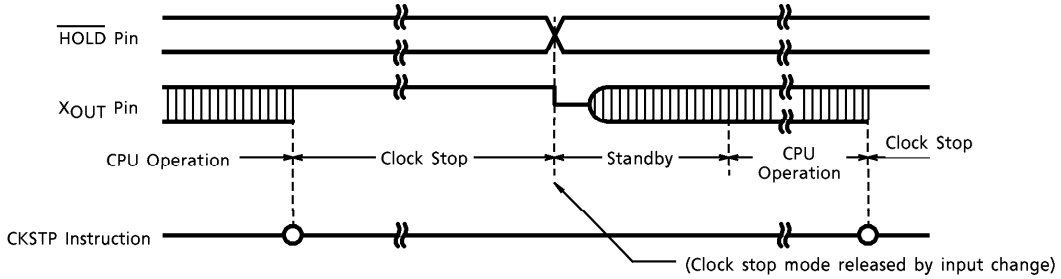
(3) Clock stop mode timing

① MODE-0



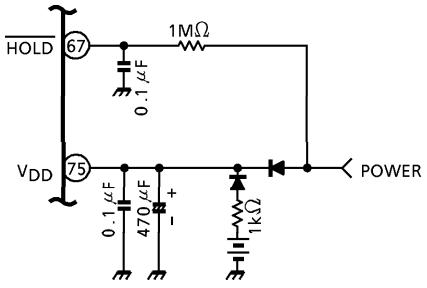
(Executing the CKSTP instruction while the $\overline{HOLD}$ pin input is low sets the device to clock stop mode.)

② MODE-1

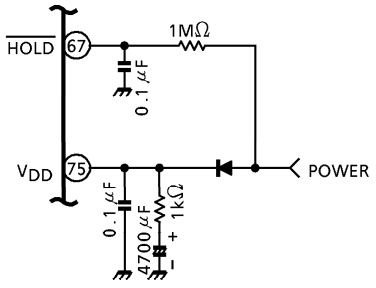


(Executing the CKSTP instruction always sets the device to clock stop mode.)

(4) Circuit example (MODE-0)



Example of backup circuit using battery



Example of backup circuit using capacitor

2. Wait mode

Wait mode halts the system and maintains, with reduced current consumption, the internal state of the system immediately prior to halting. Two wait modes are available : "soft wait" and "hard wait". When the WAIT instruction is executed, execution halts at the address of the WAIT instruction. Therefore, when wait mode is released, execution starts again from the next instruction without delaying for the standby time.

(1) Soft wait mode

Executing the WAIT instruction with the operand [P = 0H] stops only the CPU inside the device. In this mode, the crystal oscillator, display circuit, and other circuitry continue to operate normally. Using soft wait mode in the program for clock functions reduces the current consumed during clock operation.

(Note) The current consumption depends on the program.

(2) Hard wait mode

Executing the WAIT instruction with the operand [P = 1H] stops all operation other than the crystal oscillator. This reduces current consumption still further than soft wait mode. In this state, the CPU and display circuits are halted, and the LCD display output pins are all automatically fixed at the low level. (10μA Typ. at V_{DD} = 5V)

(3) Setting wait mode

Executing the WAIT instruction always sets wait mode.

(Note) In hard wait mode, the PLL turns off, while in soft wait mode, the PLL does not turn off. Accordingly, before setting a soft wait, turn the PLL off by software.

(4) Wait mode release conditions

Wait mode is released by the following conditions.

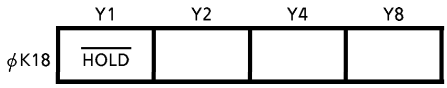
① At a change in the input state of the $\overline{\text{HOLD}}$ pin

② When a high level is input to a key input pin (K0~K3)
(Note : Depends on the key input mode)

③ When the 2Hz timer flip-flop is set to "1". (In soft wait mode only)

④ At a change in the input state of an I/O port (P1-0~P1-3) set as an input port

3. $\overline{\text{HOLD}}$ input port



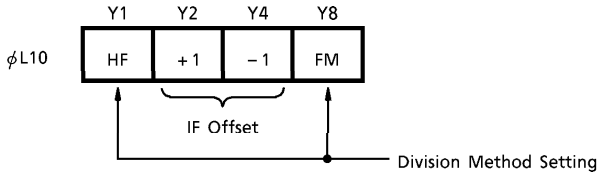
The $\overline{\text{HOLD}}$ pin can be used as an input port. Executing the IN1 instruction with the operand [C_N = 8H] reads the data input from this bit to data memory.
When setting clock stop mode, always access this port prior to executing the CKSTP instruction. Note that if the CKSTP instruction is executed without first accessing this port, the device may not enter clock stop mode.

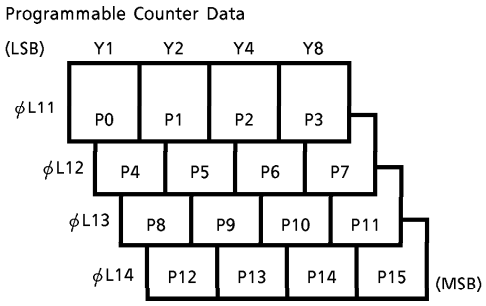
○ Programmable counter

The programmable counter block consists of a 2-modulus prescaler, 4bit and 12bit programmable counters, and the ports used to control the block.
The programmable counters can be turned on and off by the contents of the reference ports.

1. Programmable counter control ports

These ports control the divisor, division method, and the IF correction (IF offset) for the FM band.





Access the division method and the IF offset using the OUT1 instruction with the operand [C_N = 0H]. Access the divisor settings using the OUT1 instruction with the operands [C_N = 1H~4H]. Set the divisor by writing to bits P0~P15. When the programmable counter data (P12~P15) are set, all the data from P0 to P15 are updated. Therefore, always access P12~P15 to set the data, even when changing only a portion of the data.

2. Setting division method

The HF and FM bits select the pulse swallow or direct division method.
As the following table shows, there are four methods. Select the appropriate method in accordance with the frequency band used.

MODE	HF	FM	DIVISION METHOD	EXAMPLE OF RECEPTION BAND	OPERATING FREQUENCY RANGE	INPUT PIN	DIVISOR (Note)
LF	0	0	Direct division method	MW / LW	0.5~10MHz	AM_{IN}	n
HF	1	0	(1 / 15 or 1 / 16) Pulse swallow method	SW	1~60MHz	AM_{IN}	n
FM	0	1	(1 / 15 or 1 / 16) Pulse swallow method	FM	50~130MHz	FM_{IN}	n
	1	1	1 / 2 × (1 / 15 or 1 / 16) Pulse swallow method	FM	50~130MHz	FM_{IN}	2·n

(Note) n indicates the programmed divisor.

3. IF correction function for FM band

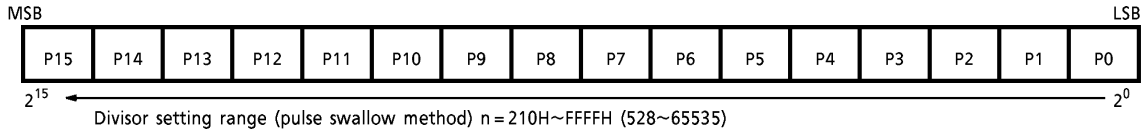
When the pulse swallow method is selected, the ΔIF ± 1 ports allow the actual divisor to be varied by ± 1 without changing the programmed divisor. This can be used for IF offset in FM. When the direct division method is selected, the IF offset function does not operate.

ΔIF + 1	ΔIF − 1	DIVISOR (At FM_H)	DIVISOR (At FM_L, HF)
0	0	2·n	n
0	1	2· (n − 1)	n − 1
1	0	2· (n + 1)	n + 1
1	1	Prohibited	Prohibited

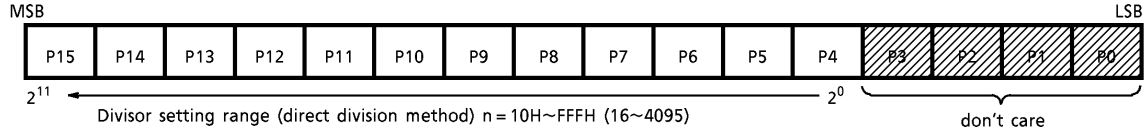
4. Setting divisor

Set the divisor of the programmable counter as a binary value in bits P0~P15.

- Pulse swallow method (16 bits)



- Direct division method (12 bits)

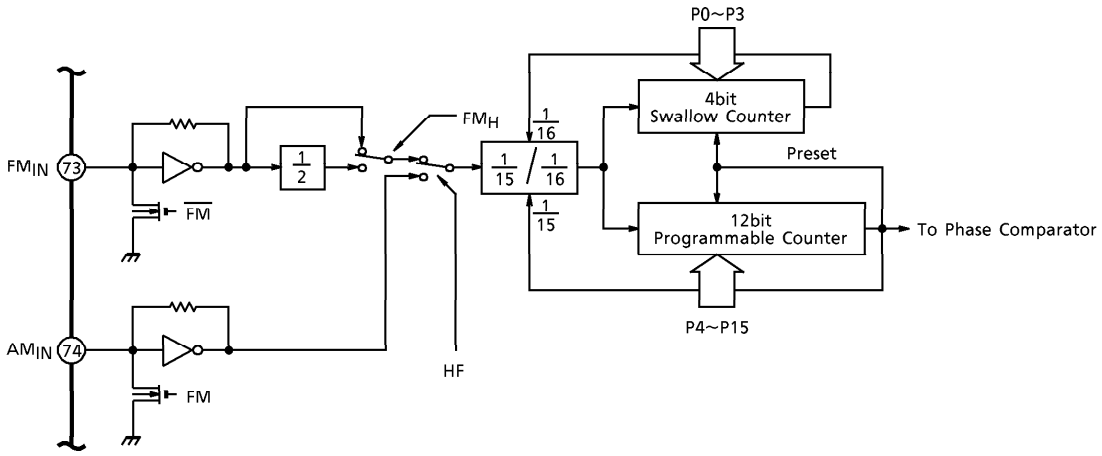


(Note) In FM_H mode, the divisor is double the programmed divisor.

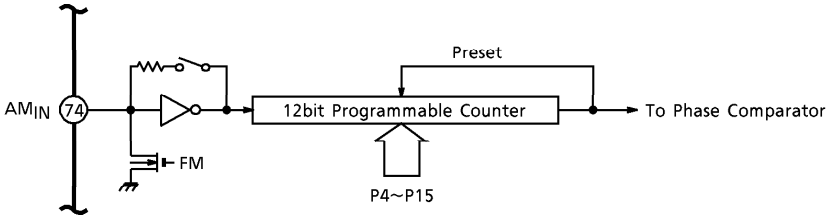
5. Programmable counter circuit structure

- Pulse swallow method circuit structure

The programmable counter circuit is made up of a 1/15 or 1/16 2-modulus prescaler, a 4bit swallow counter, and a 12bit binary programmable counter. In FM_H mode, a 1/2 divider is inserted before the prescaler.



- Direct division method circuit structure
  This circuit bypasses the prescaler and uses the 12bit programmable counter.



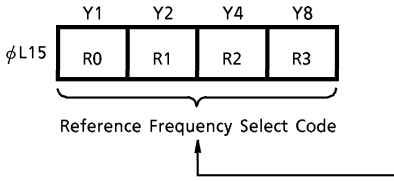
(Note) The FM_{IN} and AM_{IN} pins incorporate amps. Connecting a capacitor permits low-amplitude operation. The input pins not selected by the division method are pulled down. In PLL off mode (set by the reference port), the inputs are also pulled down.

○ Reference frequency divider

The reference frequency divider divides the frequency of the external 75kHz crystal oscillator to generate seven PLL reference frequency signals : 1kHz, 3kHz, 3.125kHz, 5kHz, 6.25kHz, 12.5kHz, and 25kHz. The frequency signal is selected by the reference port data.
The selected signal is supplied as the reference frequency for the phase comparator, which is described next. The PLL is turned on or off by the reference port setting.

1. Reference port

The reference port is an internal port used to select the reference frequency signal (from the seven frequencies). Use the OUT1 instruction with the operand [C_N = 5H] (ϕL15) to access this port. When the contents of the reference port are all "1", the programmable counter, IF counter, and reference counter are halted, and the PLL is turned off.

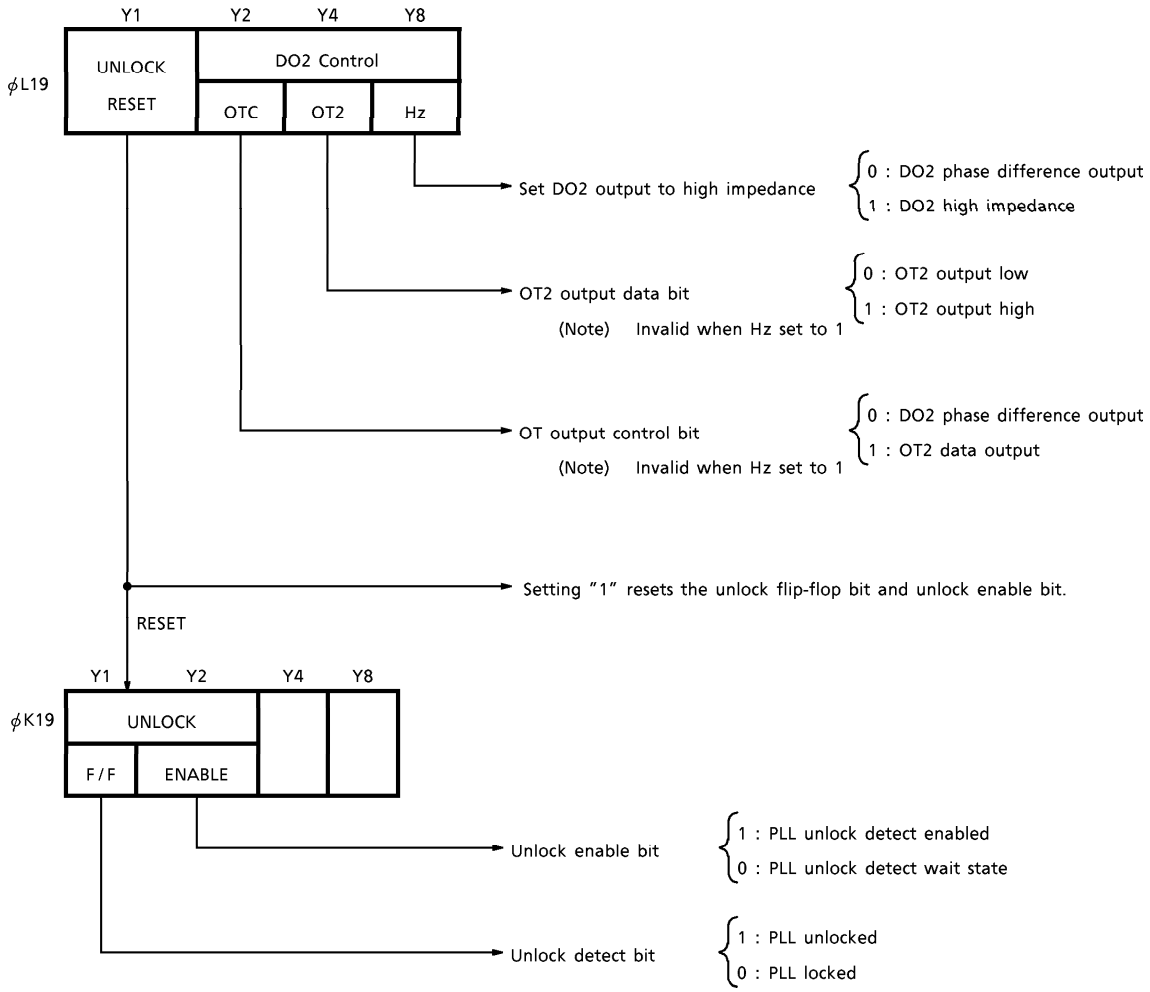


R3	R2	R1	R0		REFERENCE FREQUENCY
0	0	0	0	0	1kHz
0	0	0	1	1	3kHz
0	0	1	0	2	3.125kHz
0	0	1	1	3	5kHz
0	1	0	0	4	6.25kHz
0	1	0	1	5	12.5kHz
0	1	1	0	6	25kHz
0	1	1	1	7	Prohibited
⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	0	E	Prohibited
1	1	1	1	F	PLL off

○ Phase comparator, Clock detection port

The phase comparator compares the reference frequency signal supplied by the reference frequency divider with the divided signal output by the programmable counter, and outputs the phase difference. The output of the phase comparator is used to control the VCO via the low pass filter so as to eliminate the frequency and phase difference between the two signals.
Data are output from the phase comparator to the tristate buffered DO1 and DO2 pins in parallel. This enables the optimal filter constants to be designed for both FM and AM bands.
Also, the DO2 pin can be set for general-purpose output by the DO2 control port. The DO2 pin can also be set to high impedance. By using the DO1 and DO2 pins, PLL loop characteristics, such as the lockup time, can be improved.
The lock detection port can be used to detect the PLL lock state.

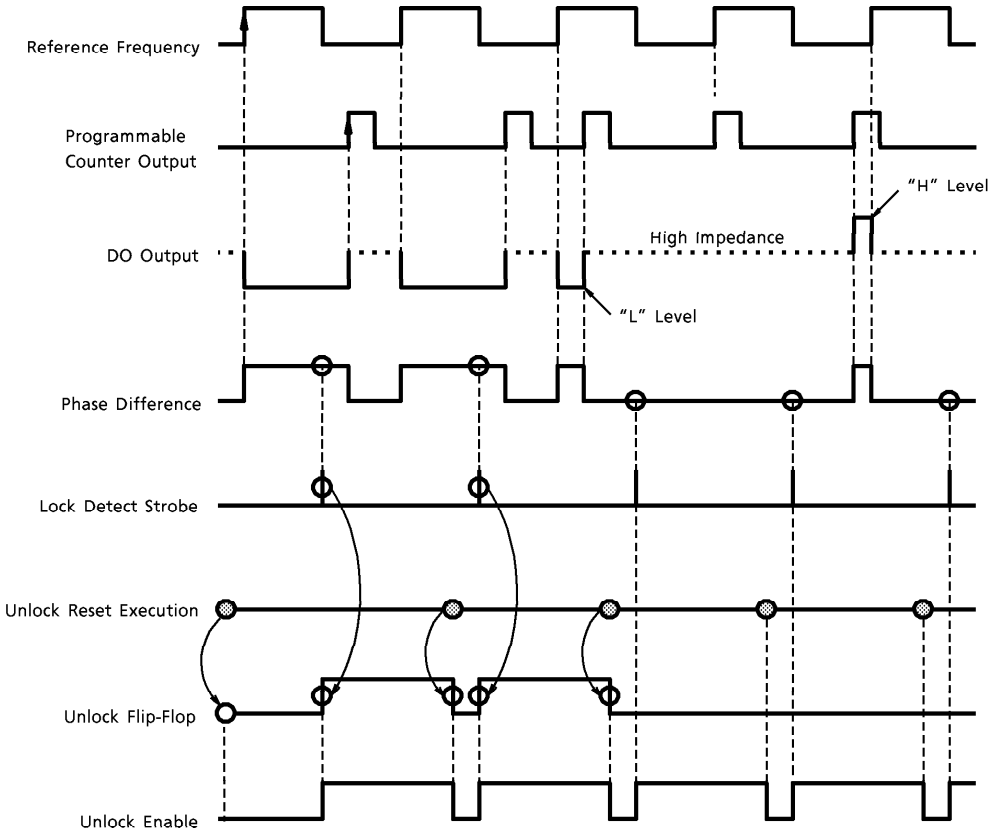
1. DO2 control port, Unlock detection port



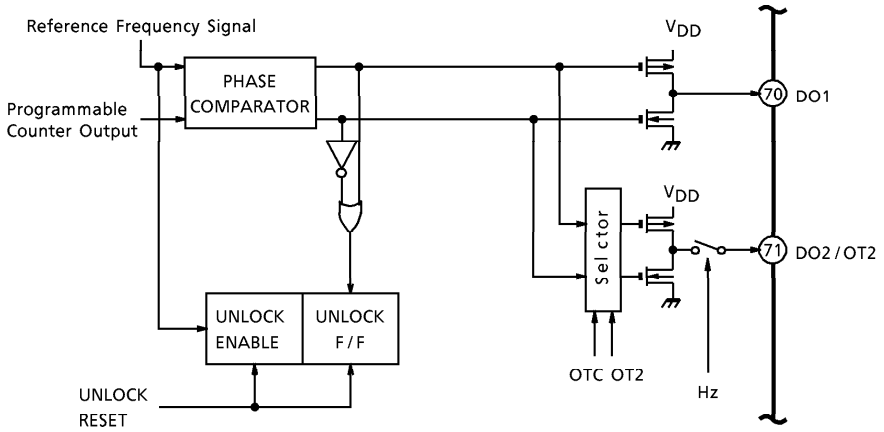
The OTC, OT, and Hz control bits of the DO2 control port set the DO2 output pin as a general-purpose output port, and control whether DO2 goes to high impedance instead of outputting the phase difference. Set these bits to the required values by program.
When the phase is approximately 180°, the unlock flip-flop bit detects the phase difference between the divided output of the programmable counter and the reference frequency. If the phase difference does not match, that is, if the PLL is unlocked, the unlock flip-flop is set. Also, setting the unlock reset bit to "1" resets the unlock flip-flop.
To detect the phase difference during the reference voltage period, reset the unlock flip-flop, then access the unlock flip-flop after waiting for a time longer than the reference frequency period. An enable bit is supplied for this purpose. After confirming that the unlock enable bit is set to "1", access the unlock flip-flop.
Setting the unlock reset bit to "1" resets the unlock enable bit.
Use the OUT1 and IN1 instructions with the operand [$C_N = 9$] to control these ports, and to load data.

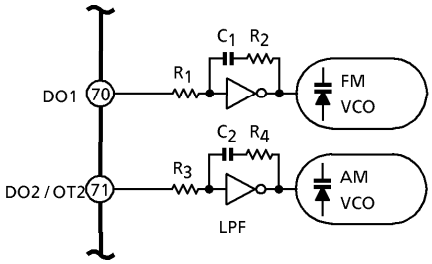
(Note) When the PLL is off, the DO output is set to high impedance. However, when DO2 is set as an output port (OT2 output), the data are output from the port without change.

2. Phase comparator, Unlock port timing

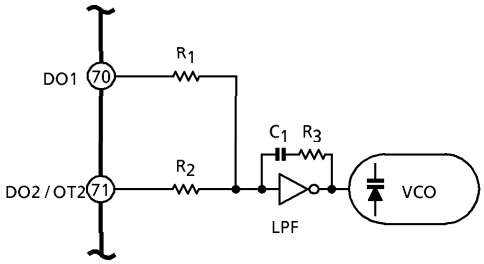


3. Phase comparator, Unlock port circuit structure





When setting different filter constants for each band

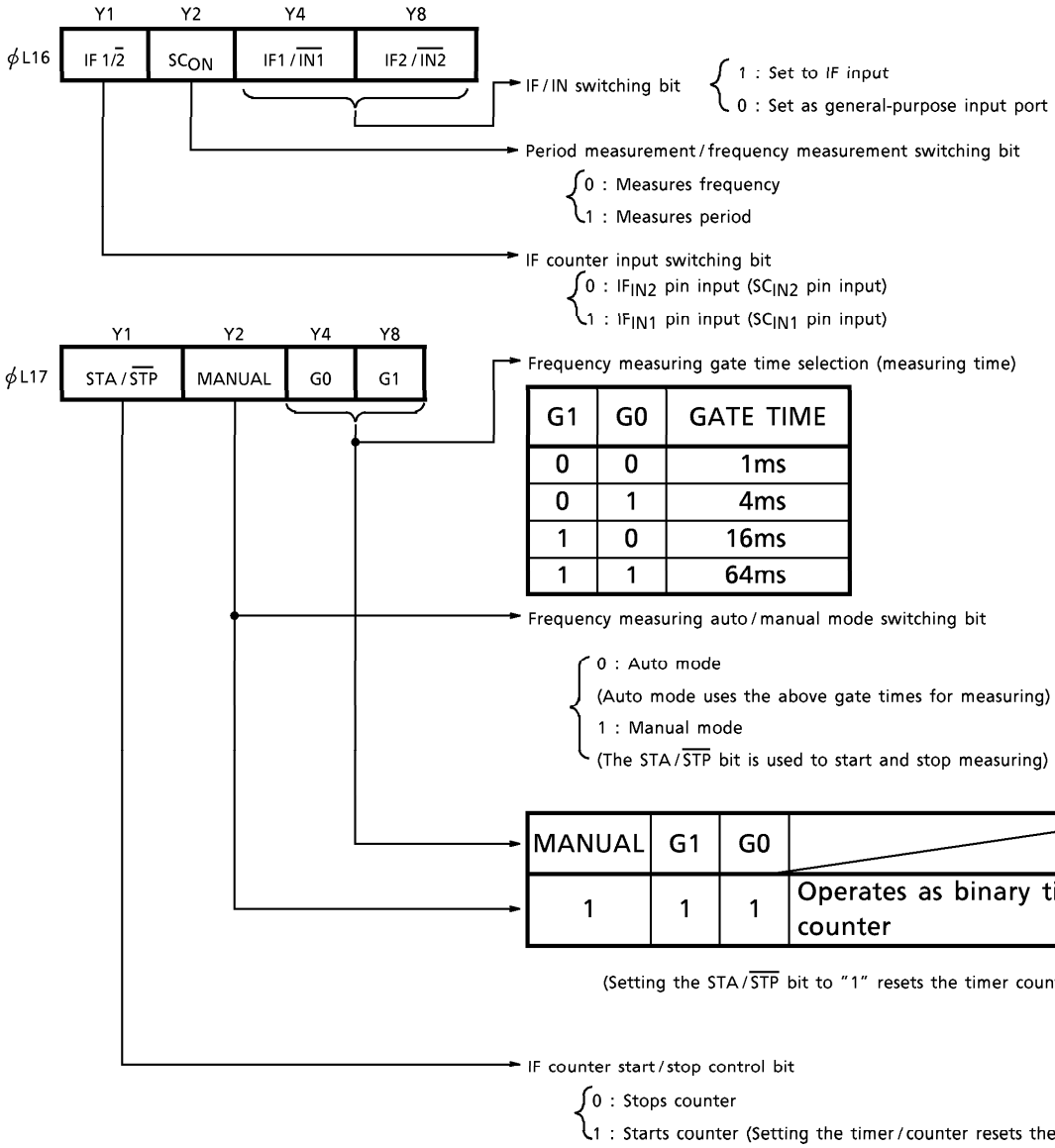


When using the same low pass filter for both bands (Set DO2 to high impedance to switch the filter constant)

○ IF counter

This is a 20bit general-purpose intermediate frequency (IF) counter used for such purposes as counting the FM or AM intermediate frequency during auto-tuning or detecting the auto-stop signal. The IF counter also has a period measuring function for measuring the period of low-frequency pilot signals, for example.
When the general-purpose IF counter is not being used for counting, for example, the intermediate frequency, it can be used as a timer.
The IF counter block consists of a 20bit binary counter and a control port.

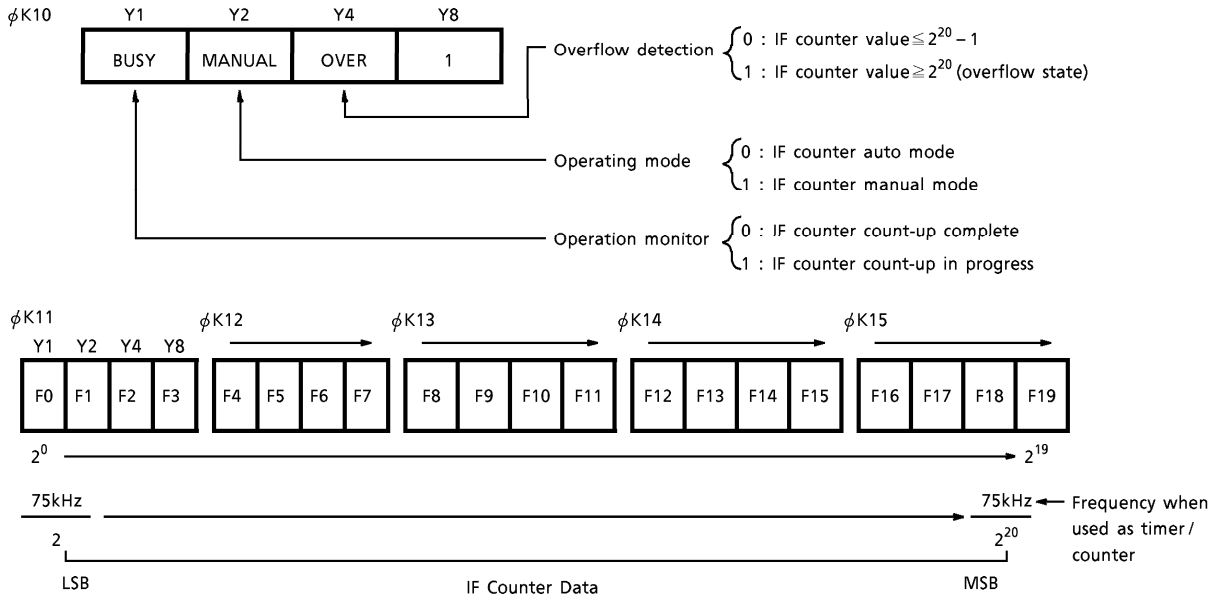
1. IF counter control port, Data port



G1	G0	GATE TIME
0	0	1ms
0	1	4ms
1	0	16ms
1	1	64ms

MANUAL	G1	G0	
1	1	1	Operates as binary timer counter

(Setting the STA / STP bit to "1" resets the timer counter)



(Note) When the PLL is off, the IF counter is disabled.
(When the timer / counter is in use, the IF counter is enabled.)

(1) IF counter auto mode (Frequency measuring)

To use IF counter auto mode, use the IF / $\overline{IN}$ switching bit to set the IF pin to IF input, and set the SC_{ON} bit to frequency measuring mode "0". Then, set the IF_{IN1} or IF_{IN2} pin using the IF counter input switching bit.
Set the gate time based on the IF input frequency band. Set the MANUAL bit to "0" and the STA / $\overline{STP}$ bit to "1" to start the IF counter.
As a result, the clock for the 20bit binary counter is input from the IF pin for the specified gate time. The IF counter counts the number of input pulses. To determine when the IF counter has finished counting, check the BUSY bit. When the count equals or exceeds 2^{20} input pulses, the OVER bit is set to "1".
To measure the frequency input to the IF input pin, load the F0~F19 IF data when the BUSY and OVER bits are both "0".

(2) IF counter manual mode (Frequency measuring)

Use manual mode to measure the frequency using the IF frequency by controlling the gate time using an internal time base (eg, 10Hz).
Perform the same IF counter input settings as for auto mode, and set the G0 and G1 bits to other than "1". Set the MANUAL bit to "1" and the STA / $\overline{STP}$ bit to "1" to start the count. Setting the STA / $\overline{STP}$ bit to "0" terminates the count and loads the data in binary format.

(3) IF counter period mode (Period measuring)

Use this mode to measure low frequencies that cannot be otherwise be measured.
The frequency is measured by inputting the reference clock (75kHz) to the 20bit binary counter for one input period. Use the number of pulses to determine the period of the input.
This input pin can also be used as the IF input pin. Setting the SC_{ON} bit to "1" sets the pin as the SC_{IN} pin.
The IF $1/\overline{2}$ bit switches between SC_{IN1} and SC_{IN2} input in the same way as for IF counter frequency measurement. Set the MANUAL, G0, and G1 bits to "0".
As in frequency measuring, to start period measuring, use the BUSY bit to confirm the operation state, then load the count data.

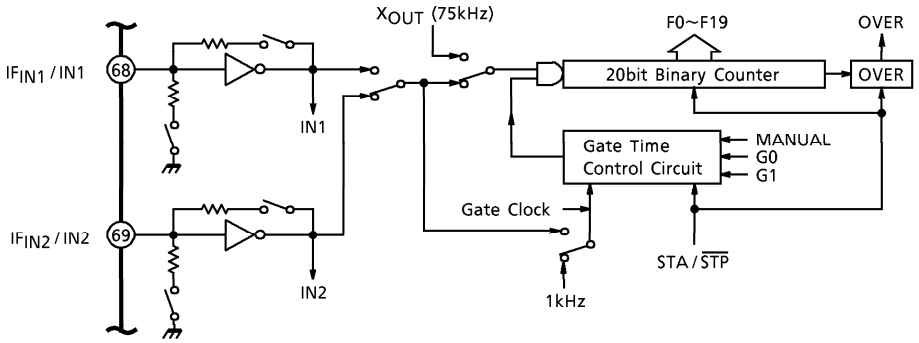
(Note) When SC_{IN} input is selected, input the square wave signals DC coupled.

(Note) Note that the BUSY bit is not cleared to "0" if no clock is input to SC_{IN}.

(4) Timer / Counter mode

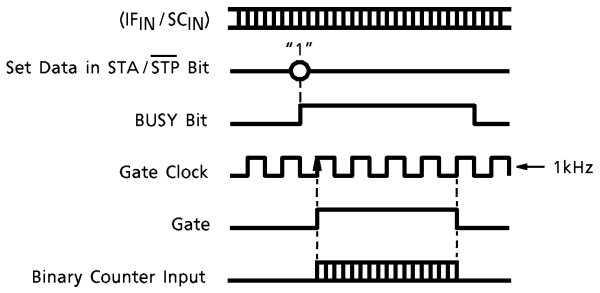
When not using the IF counter, the block can be used as a timer or binary counter. Set the MANUAL, G0, and G1 bits to "1" to start binary counting using the 75kHz frequency as the reference clock.
Setting the STA / $\overline{STP}$ bit to "1" resets the counter.

2. IF counter circuit structure

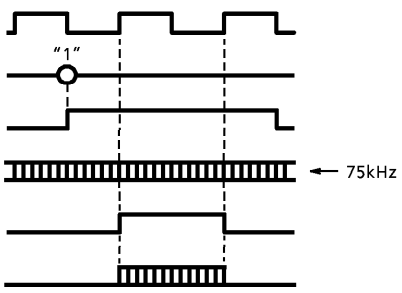


The IF counter block consists of an input amp, a gate timer control circuit, and a 20bit binary counter.
When the PLL is turned off, the IF counter is off. However, the block can still operate when set as a timer / counter.

(Note) The IF_{IN1} and IF_{IN2} pins incorporate amps. Connecting the pins via a capacitor permits low-amplitude operation.



Frequency measuring auto mode

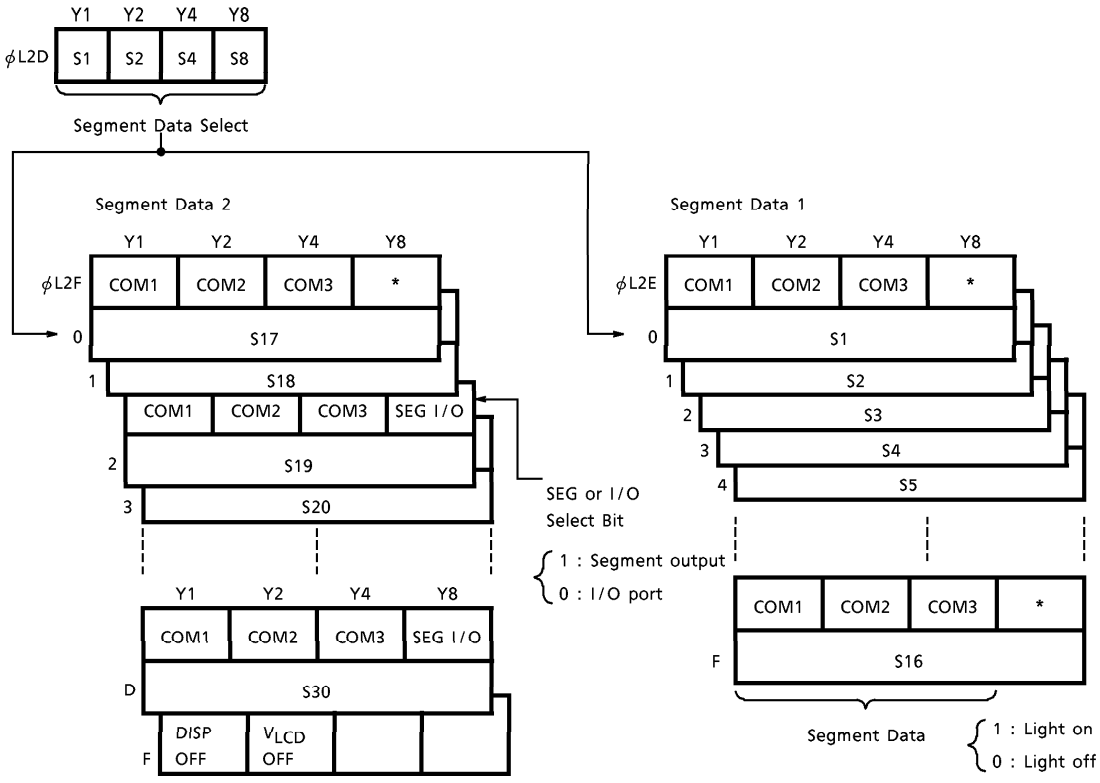


Frequency measuring mode

○ LCD driver

The LCD driver has a 1/3 duty and 1/2 bias drive (frame frequency is 167Hz).
The common outputs are at three voltages : V_{LCD}, $V_{LCD}/2$, and GND. The segment outputs are at two voltages : V_{LCD} and GND.
The combination of three common outputs and 30 segment outputs enables the LCD driver to drive a maximum of 90 segments.
LCD driver segment output pins S23~S30 are also used for the key return timing signals for loading key matrix data.
The LCD driver incorporates a constant voltage circuit (V_{LCD} = 3.0V) for the display. This maintains an even LCD contrast regardless of fluctuations in the supply voltage.
Segment output pins S19~S30 can be individually set as I/O ports by software to suit particular system requirements.

1. LCD driver port



(Note) The segment data control whether or not the segments corresponding to the common and segment outputs are lit.

(Note) The DISP OFF bit is set to "1" at a system reset and at release of clock stop mode.

(Note) The V_{LCD} OFF bit is reset to "0" at a system reset. The SEG I/O bits are all set to "1" at a system reset.

The LCD driver control ports consist of a segment data selection port and segment data ports. Use the OUT2 instruction with the operand [C_N = DH~FH] to access these ports. The LCD driver can operate as an I/O port under the control of the SEG I/O control bit (ϕL2F). Setting the bit to "1" sets segment output. Setting the bit to "0" sets the port as an I/O port.

Set the LCD driver segment data using the segment data ports (ϕL2E, ϕL2F). Set the segment data port to "0" to turn the LCD display off and set "1" to turn the LCD display on. When FH is specified for the segment data select port, the DISP OFF and V_{LCD} OFF bits are selected as segment-2 data (ϕL2FF). The DISP OFF bit can turn the whole LCD display off without setting segment data.

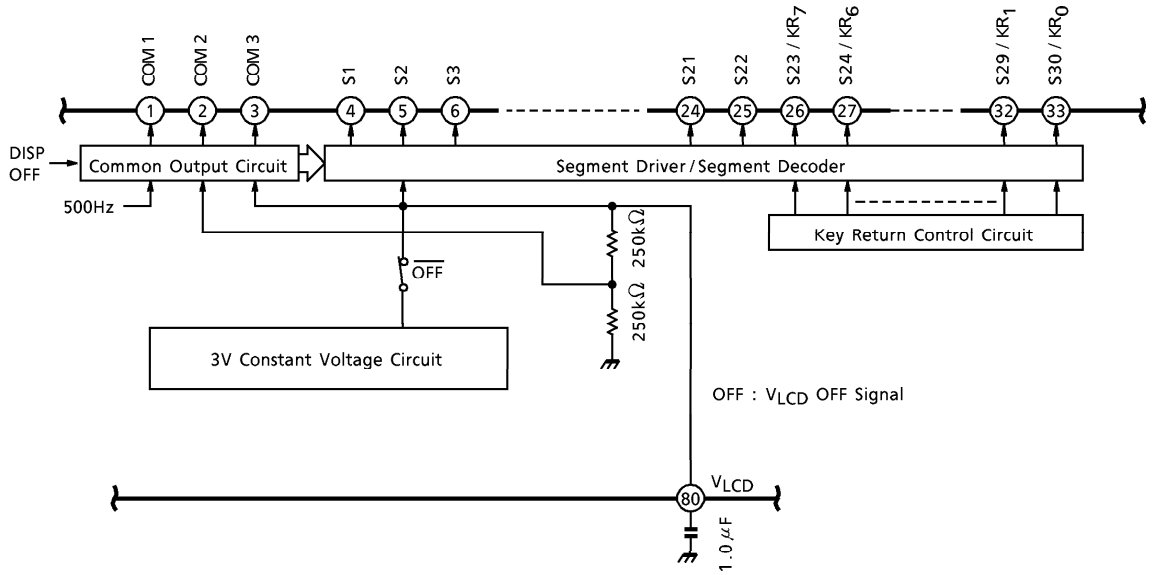
Setting this bit to "1" outputs the de-selected waveform from the common outputs and turns off the entire LCD display. The segment contents are preserved. Setting the DISP OFF bit back to "0" displays the previous LCD screen.

Segment data can be rewritten during DISP OFF. After a reset, and after CKSTP execution, the DISP OFF bit is set to "1".

The V_{LCD} OFF bit allows an external power supply to be used. This is useful for changing the LCD drive voltage.

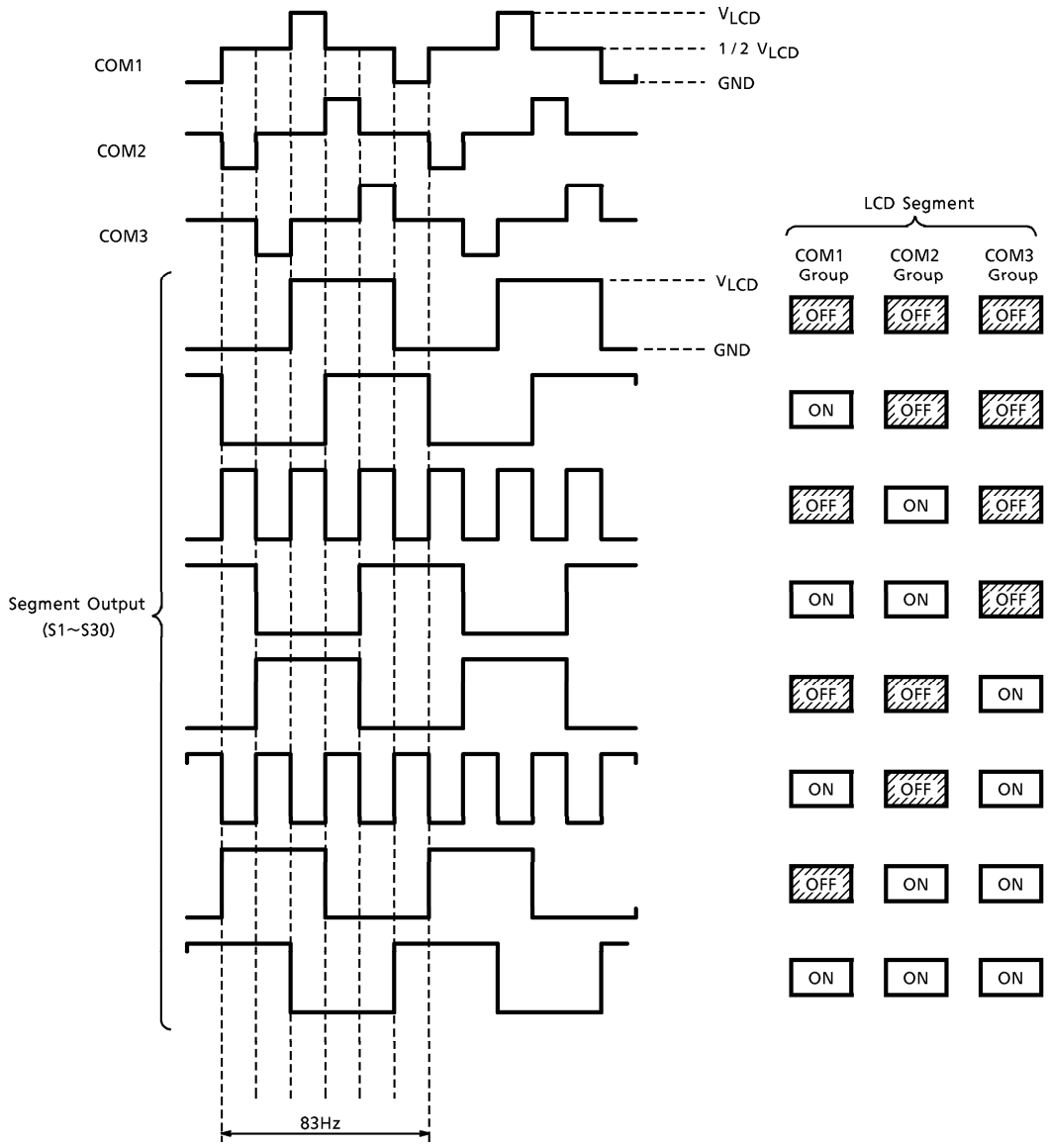
The data are set according to the segment data select port (ϕL2D). Segment output pins S23~S30 are also used for the key return timing signals for loading key matrix data. At the timing for loading the key matrix data, the segment output is set to the V_{LCD} level.

2. LCD driver circuit structure

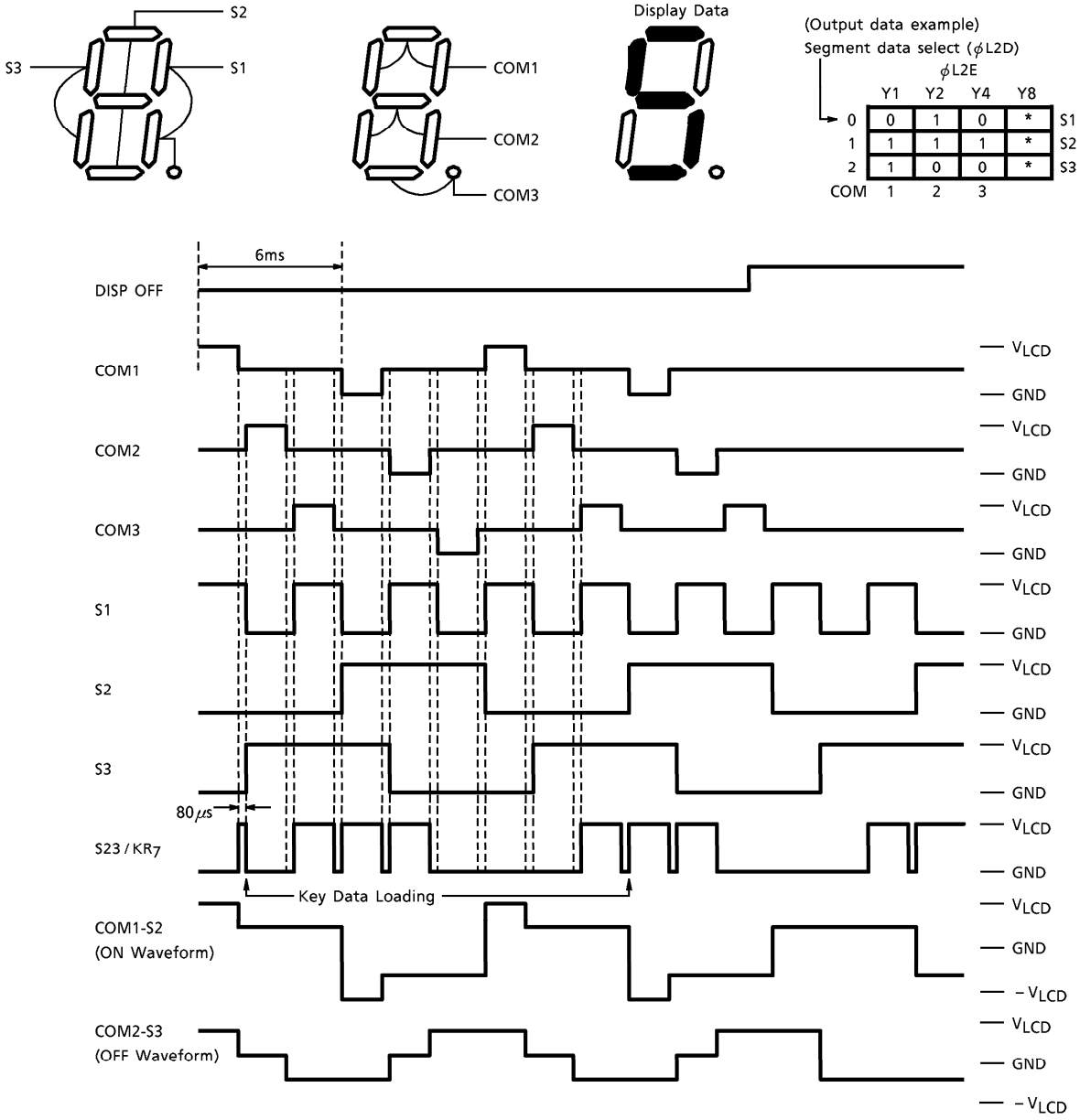


3. LCD driver timing chart

The following chart shows the timing for the COM1~COM3 output waveforms and the eight types of segment output waveform.



4. Example of timing chart for LCD driver output data and loading key data
   The following chart shows the output waveform timing and key return data loading timing when the common and segment outputs are allocated as shown.



The voltages output in the LCD driver waveform are V_{LCD}, GND, and an intermediate voltage halfway between the two. Pins S23~S30 output the key return signals at the timing for switching between these levels. During key return data loading, the segment outputs are at the V_{LCD} level for 80μs.

(Note) At CKSTP instruction execution or at a system reset, the common and segment pins go to the low level.

○ Key input, Key scan timing

The following are the two basic methods of loading key data.

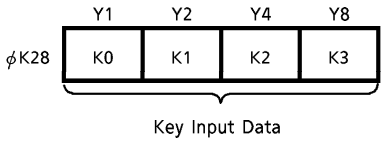
① Use software to set the key timing output port (port pins T0~T7) as the key source.

② Use hardware to set the LCD segment outputs (S30 / KR_0~S23 / KR_7) as the key source.

Select the appropriate method for the system.

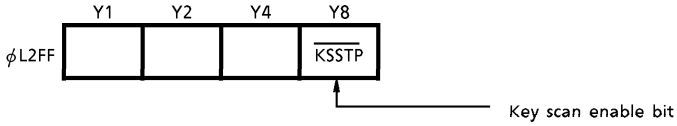
1. Key input port

This is a 4bit, input-only port mainly used when loading key data by software scanning. To read the key input pin data into data memory, execute the IN2 instruction with the operand [$C_N = 8$].



2. Key scan enable bit

This bit sets the key scan method.



0 : Halts key scanning from the LCD segment outputs. In this case, the input pins (K0~K3) are all pulled down.

1 : Performs key scanning from the LCD segment outputs. In this case, the input pins (K0~K3) are pulled down at the key return signal output timing.

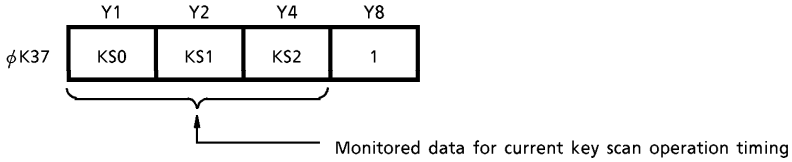
This bit sets the key loading method.

0 : Uses software to set the key timing output port (port pins T0~T7) as the key source.

1 : Uses hardware to set the LCD segment outputs (S30 / KR_0~S23 / KR_7) as the key source.

3. Key scan digit No. port

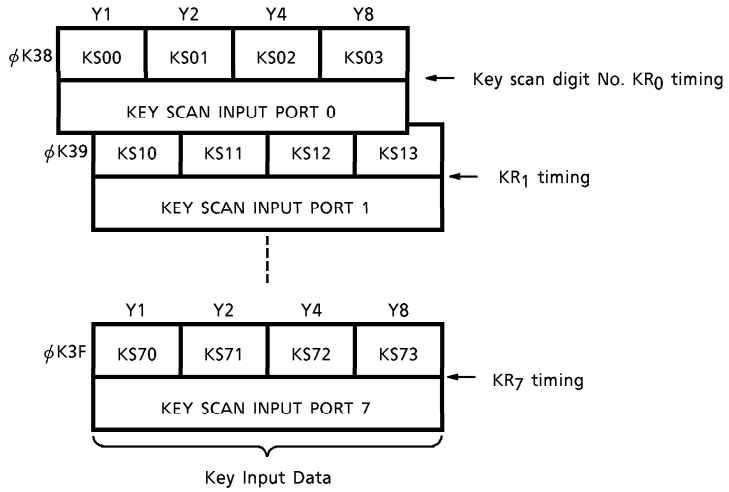
This port monitors the key scan operating state when loading key data using the key return signals from the LCD segment outputs (S30 / KR_0~S23 / KR_7).



	KS2	KS1	KS0	KEY SCAN DIGIT No.
0	0	0	0	KR_0
1	0	0	1	KR_1
2	0	1	0	KR_2
3	0	1	1	KR_3
4	1	0	0	KR_4
5	1	0	1	KR_5
6	1	1	0	KR_6
7	1	1	1	KR_7

4. Key scan data input port

This port saves the result of loading the key data using the key scan from the LCD segment outputs (S30 / KR_0~S23 / KR_7).



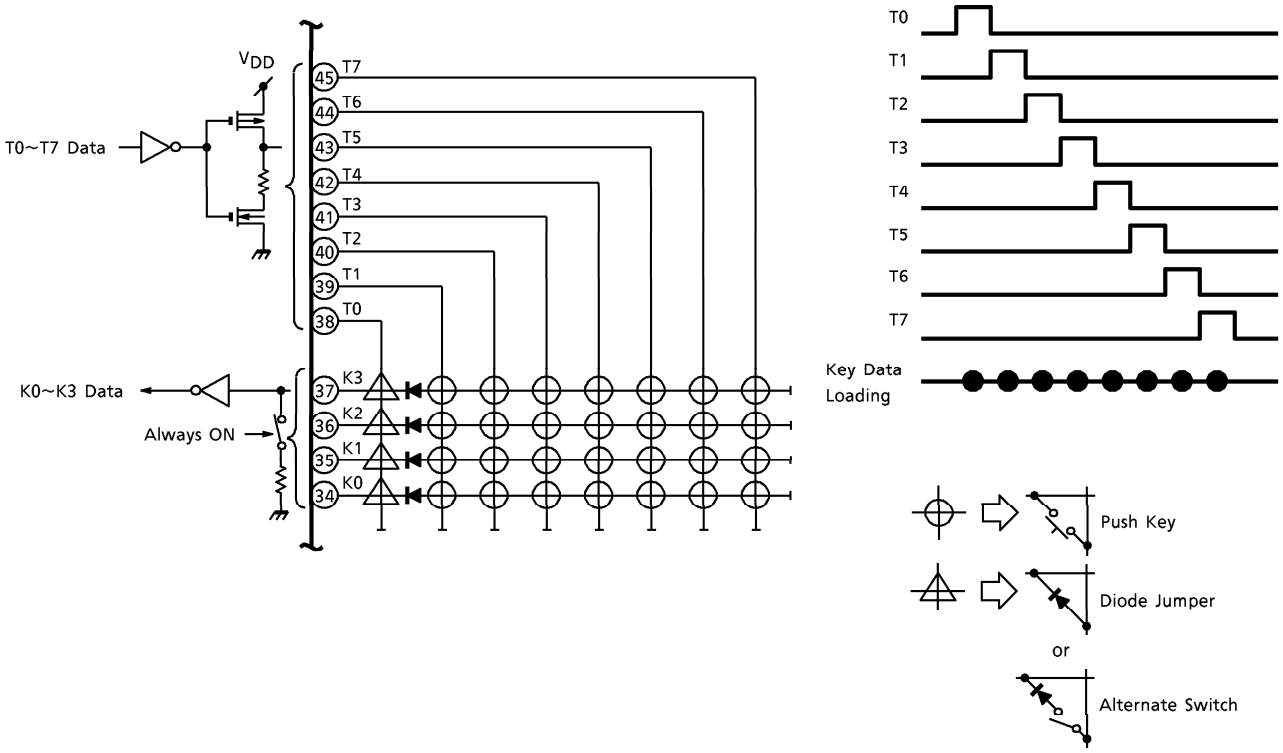
The key scan data input port (ϕK38~ϕK3F) bits are "1" when the corresponding key is pressed, and "0" when not pressed.

(Note) The CPU stop function shuts down the CPU when the supply voltage falls below 1.5V. The key scan data immediately after the CPU restarts are undefined. Therefore, use the STOP flip-flop to check that at least one key scan has completed before loading key scan data into data memory.

5. Key matrix structure

The key matrix can have one of the following two structures.

(1) Key data loading by software (software scan)

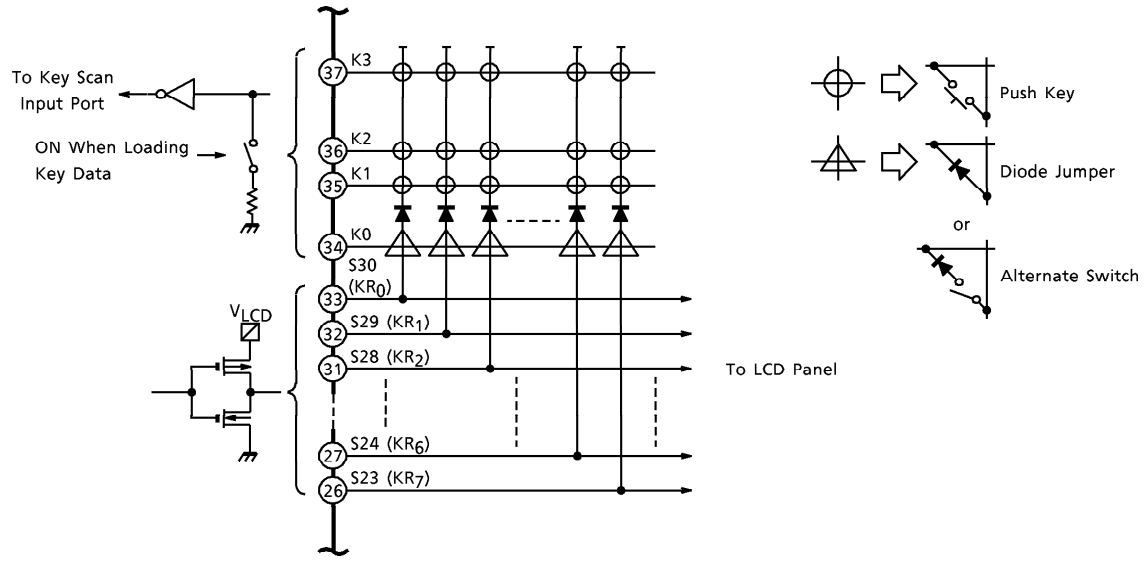


When loading key data by software, use a key matrix with the above structure. This structure allows up to 32 (4×8) keys to be used. The key data can be loaded at high speed. Also, as the structure has a high resistance in the N channel FETs of pins T0~T7, there is no need to use a diode to prevent reverse current flow caused by, for example, multiple keys being pressed.

For this method, set to high the key timing output port data (ϕL37, ϕL38) for the key line to be loaded. Then to determine which keys are pressed, load the key input port (ϕK28) data to memory. At this timing, set the other key timing output ports to low. If the corresponding key is pressed, the key input port data are "1" ; if not pressed, "0".

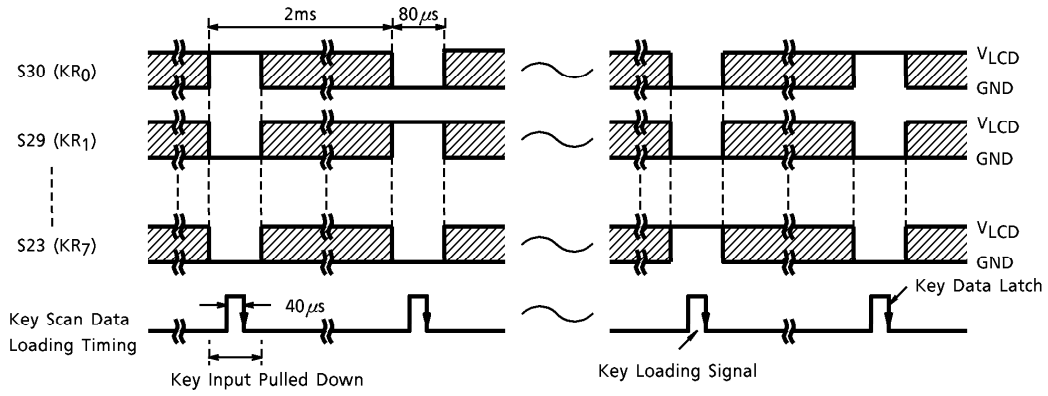
(Note) When executing a wait instruction (in WAIT mode), applying a high level to a key input pin releases WAIT mode and restarts the CPU.

(2) Key data loading by LCD segment output (hardware scan)



(Note) A key matrix to 4×8=32 can be created.

(Note) The same key line cannot contain both push keys and diode jumpers or alternate switches. Place diode jumpers or alternate switches on the key return signal output side.



When loading key data using the LCD segment outputs, form a key matrix as shown in the previous diagram. This key matrix requires a diode to prevent reverse current flow. Note the direction of this diode and the diode jumper.

At the LCD output change timing, the segment pins output the V_{LCD} (3V) or GND voltage. When loading key data, the segment signal being loaded goes to the V_{LCD} voltage at the LCD output change timing, and the key input pin is pulled down to the GND voltage. If the key is not pressed at this timing (or there is no jumper diode), the key input pin inputs the GND level. If the key is pressed (or there is a jumper diode), a voltage equal to the V_{LCD} voltage less the drop across one diode ($\underline{\sim}$0.6V) is input.

The input data are latched to the key scan data input port (ϕK38~ϕK3F) corresponding to the active LCD segment output line.

If the corresponding key is pressed, the key data are "1" ; if not pressed, "0".

Setting the key scan enable bit (ϕL2FF) to "1" starts the key scan and begins repeated key data loading.

The time required to load one line of key data is 2ms. Therefore, load the key scan data (ϕK38~ϕK3F) to data memory while referencing the key scan operating monitor (ϕK37).

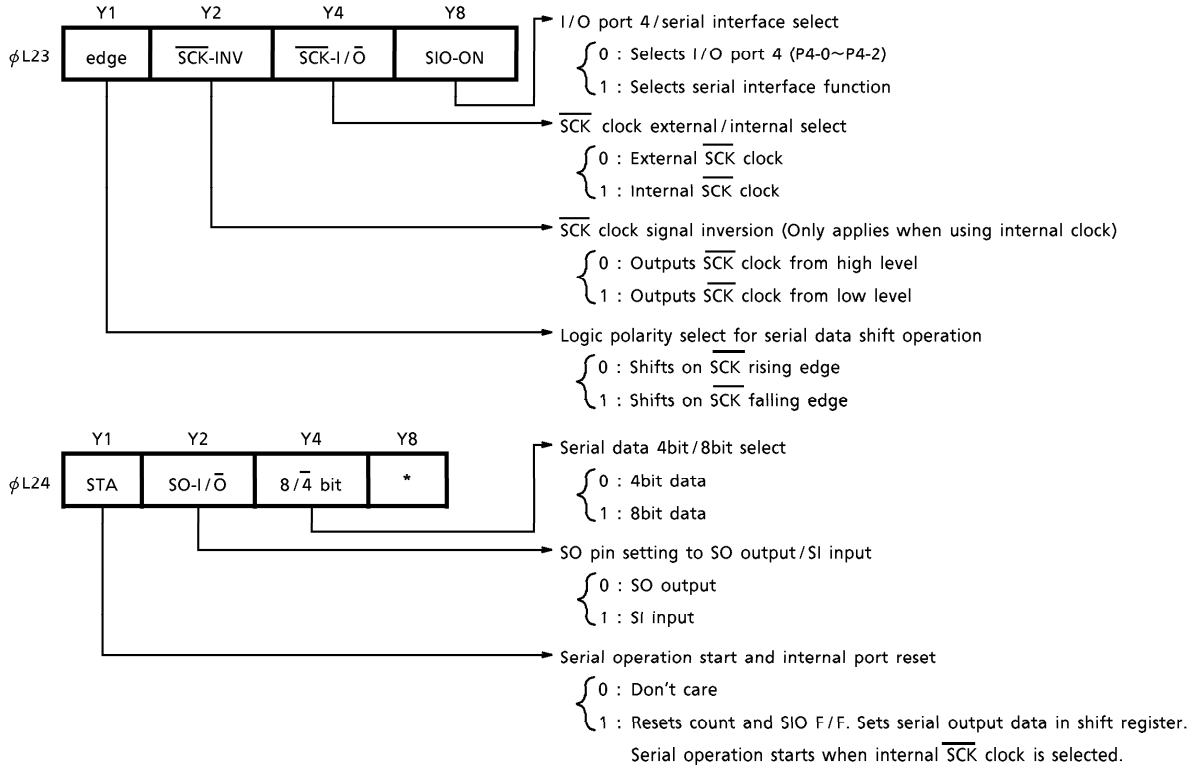
(Note) The diode jumper data are stored in the latch. Therefore, for efficient use of the data memory area, you can reference the contents of the latch as required rather than storing the data in data memory. The contents of the latches are undefined immediately after the CPU restarts after a CPU stop function shutdown.
Accordingly, check that at least one scan data cycle has completed before using the latch contents.

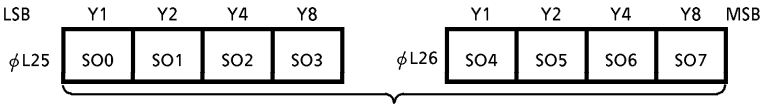
(Note) The key scan range is KR_0~KR_7.

○ Serial interface

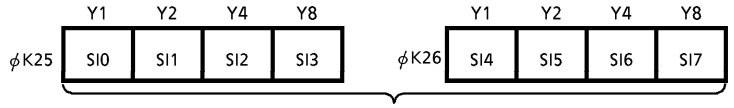
The serial interface is a serial I/O port for receiving and sending 4bit or 8bit data in sync with either an internal or external serial clock. The interface uses the SI, SO, and $\overline{SCK}$ pins. The interface can be used to communicate with devices such as microcontrollers or other LSIs.

1. Serial interface control port, Data port





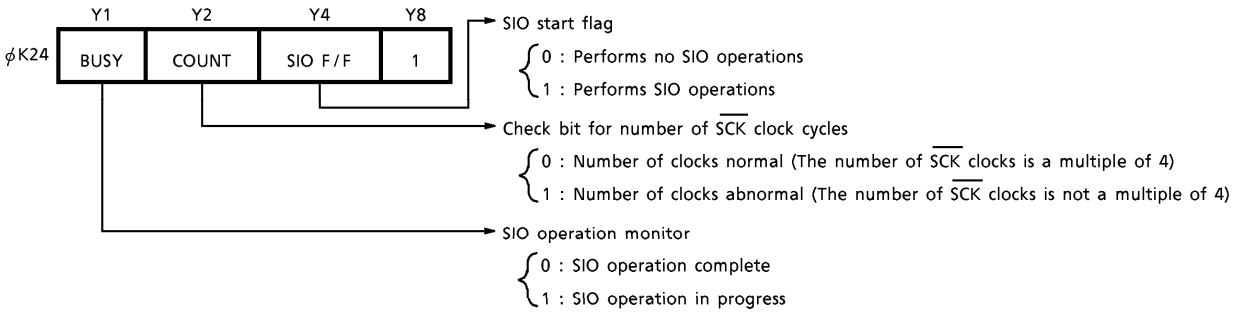
Serial output data ··· The data set in this port are output serially.



Serial input data ··· The serially input data can be loaded to data memory.

(Note) The serial input data are accessed directly from the shift register. The data in the shift register are accessed as-are as serial input data.

(Note) After a system reset, the contents of the serial interface control ports (φL23, φL24) are reset to "0".



The serial interface control and serial data can be accessed by the IN2 and OUT2 instructions with operands [C_N = 3H~6H].
The serial interface pins can also function as I/O port 4 pins : P4-0, P4-1, and P4-2. Setting the SIO ON bit to "1" sets these I/O port 4 pins as the SI, SO, and $\overline{SCK}$ pins, respectively.

① $\overline{SCK}$-INV, $\overline{SCK}$-I/$\overline{O}$ bits

The $\overline{SCK}$-INV and $\overline{SCK}$-I/$\overline{O}$ bits set the input/output format as follows.

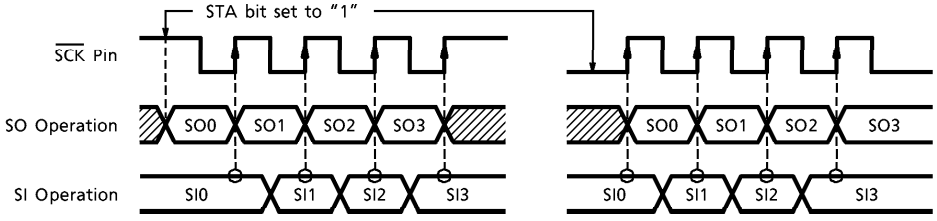
$\overline{SCK}$ pin state

INV	I/$\overline{O}$	INPUT/ OUTPUT	$\overline{SCK}$ CLOCK WAVEFORM
0	0	Output	
1	0	Output	
*	1	Input	—

② edge bit

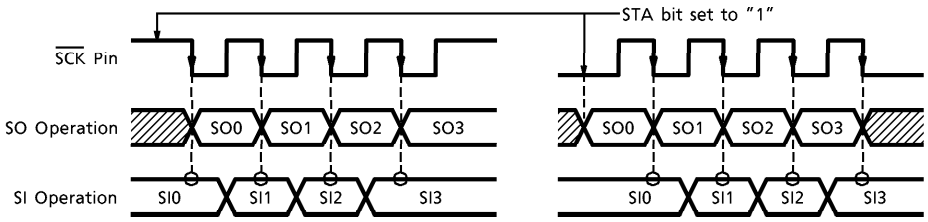
The edge bit sets the serial data shift logic as follows.

- When edge = "0"



When the edge bit is set to "0", the data are output from SO on the rising edge of the $\overline{SCK}$ clock. The SI input is also input to the shift register on the rising edge of the $\overline{SCK}$ clock.

- When edge = "1"

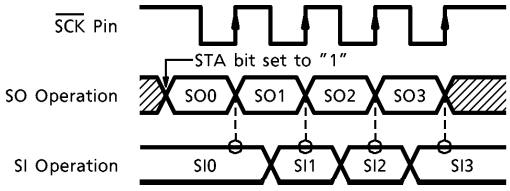


When the edge bit is set to "1", the data are output from SO on the falling edge of the $\overline{SCK}$ clock. The SI input is also input to the shift register on the falling edge of the $\overline{SCK}$ clock.

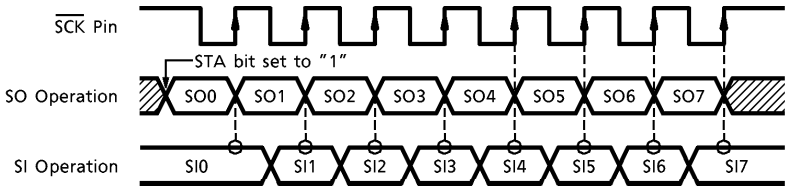
③ 8/$\overline{4}$ bit

The 8/$\overline{4}$ bit selects the length of the serial data. Setting this bit to "0" selects 4bit data ; setting the bit to "1" selects 8bit data. When the internal clock is selected, setting 4bit data outputs four $\overline{SCK}$ clock cycles, while setting 8bit data outputs eight $\overline{SCK}$ clock cycles.

- When 8/$\overline{4}$ bit = "0" (With edge = "0" and $\overline{SCK}$-INV = "0")

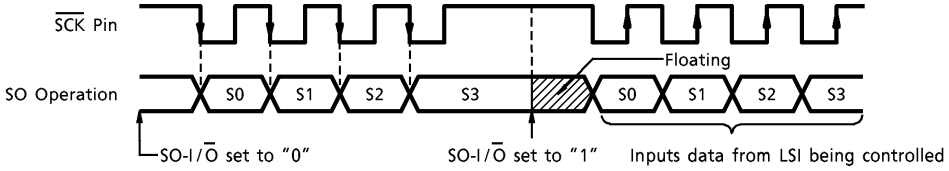


- When 8/$\overline{4}$ bit (With edge = "0" and $\overline{SCK}$-INV = "0")



④ SO-I/$\overline{O}$ bit

The SO-I/$\overline{O}$ bit sets the SO pin to either serial input or serial output.
Setting the SO-I/$\overline{O}$ bit to "0" sets the SO pin to serial data output. Setting "1" sets the pin to serial data input. By using this bit to control the pin operation, the input and output of data with LSIs supporting a serial bus, such as T-BUS, can be easily controlled with a single pin.



(Note) In this case, as there is a period when the pin is floating, the SO pin must be pulled-up.

This method works as follows. To transmit data, the data are set in the serial output data port and SIO is performed. To receive data, the SO pin is set to input and SIO is performed. Then, the data can be loaded to data memory from the serial input data port. Even when the serial interface is selected, the SI pin can be controlled as an I/O port (P4-0). The I/O output pins (P4-0) can be used, for example, as the strobe pulse pins in T-BUS.

(Note) When set as the SI serial data input pin, set the corresponding I/O control port P4-0 bits in I/O port 4 to "0".

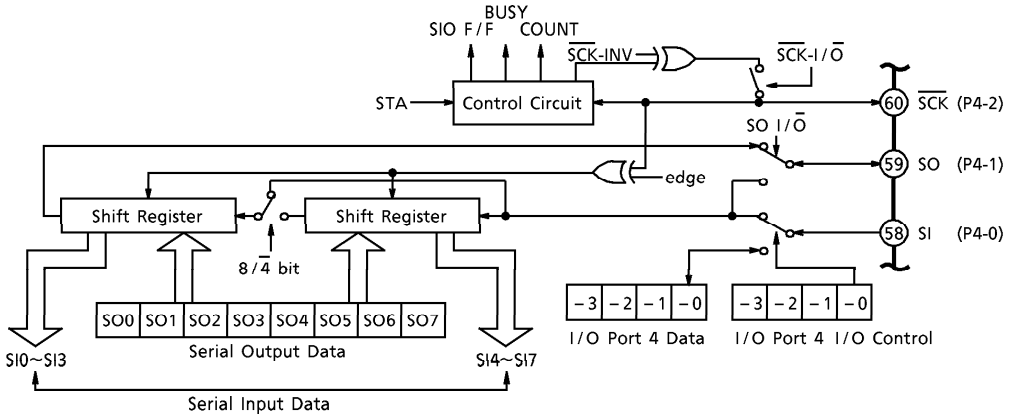
⑤ Monitoring serial interface operation

Use the BUSY, COUNT, and SIO flip-flop bits to check the operating state of the serial interface.
The BUSY bit is set to "1" during SIO operations. Therefore, set the control data and access the serial data when the BUSY bit is "0".
Use the COUNT bit to determine whether data in units of 4 bits have been sent or received. When the number of shift operations is a multiple of 4, the COUNT bit outputs "0". When not a multiple of 4, the bit outputs "1".
The SIO flip-flop bit is set to "1" when the $\overline{SCK}$ pin clock starts.
Setting the STA bit to "1" clears both the COUNT bit and SIO flip-flop bit to "0". These two bits are mainly used when the $\overline{SCK}$ pin is set for the external clock. The bits can be used to test whether the external clock was input, whether serial data were sent or received, or whether operations were normal.

⑥ STA bit

With the $\overline{SCK}$ pin set for the internal clock, each time the STA bit is set to "1", the serial output data are set to the shift register, the clock is output from the $\overline{SCK}$ pin, and shift operations begin. At this time, the COUNT bit and the SIO flip-flop are reset to "0".

2. Serial interface structure



The serial interface consists of a control circuit, a shift register, and I/O ports.

(Note) The SI pin can be used as-is as I/O port 4 (P4-0)

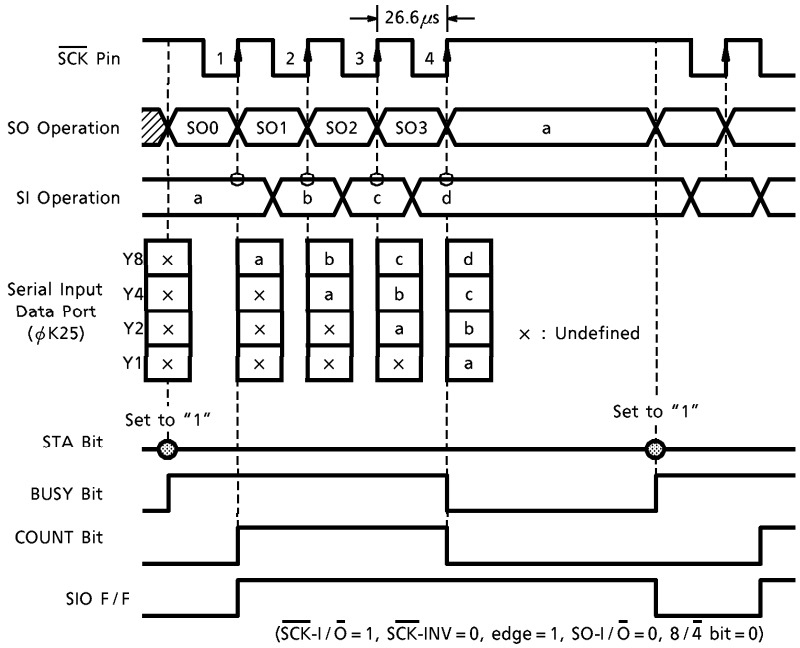
(Note) The data set as the serial output data are different to the serial input data.

(Note) When the SI pin is set to SI input, when the $\overline{SCK}$ pin is set to $\overline{SCK}$ input, and when the SO pin is set to input, the pins are all Schmitt inputs.

3. Serial interface timing

When $\overline{SCK}$ is set for the internal clock, the frequency of the clock output from the $\overline{SCK}$ pin is 37.5kHz (duty : 50%).

The following chart is an example of the serial interface timing.



[Example of serial interface timing]

○ Interrupt function

INTR1 and INTR2 are the input pins for the external interrupts. These pins can also be used for remote control signal input and tape running detection input. The pins can also be set as general-purpose input ports by software.

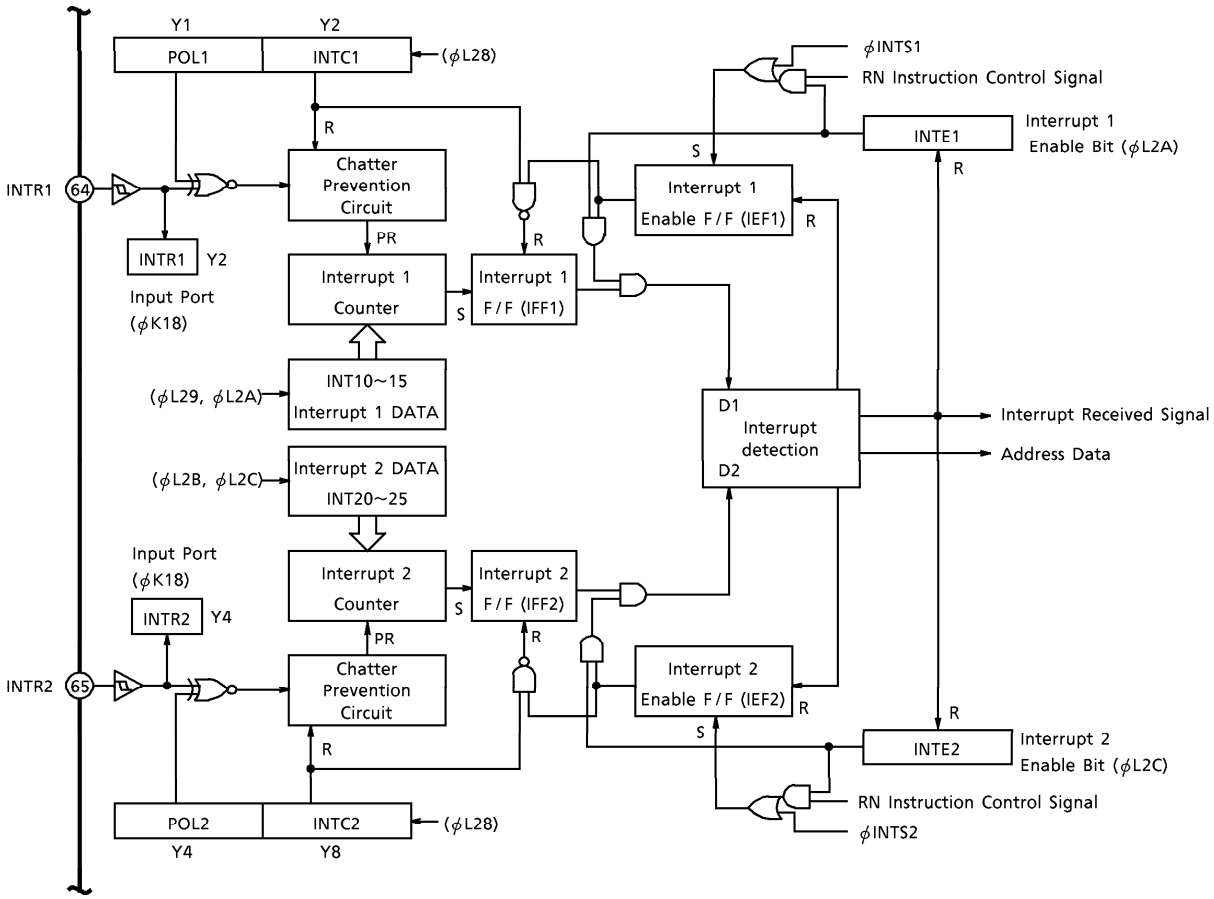
1. Interrupt function

The interrupt function consists of two external interrupt sources : interrupt 1 and interrupt 2. The function supports prioritized multiple interrupts. The interrupt circuit is set using an internal port. Interrupts are received based on the signals input to the corresponding pins (INTR1, INTR2). Interrupt 1 is suitable for use as the remote control interrupt. If the interrupt source input is at high level (with the interrupt signal set for positive logic input) for longer than the time set by the counter circuit (0.3~12.5ms), the signal is recognized as an interrupt. Interrupt 2 is suitable for detecting the end of tape in a cassette deck. The interrupt function begins measuring on a rising edge (with the interrupt signal set for positive logic input). If no other rising edge occurs within the time set by positive logic input). If no other rising edge occurs within the time set by the counter circuit (0.1~6.2s), the signal is recognized as an interrupt.
If the counter setting data are "01H" for either interrupt 1 or interrupt 2, for a pulse of 120μs or longer the interrupt can be received.
The input pins are Schmitt inputs. Moreover, because an internal noise rejection circuit is provided, noise pulses of less than 80~120μs are not detected. The input logic is controlled by an internal port setting to suit various input signals.

EXTERNAL INTERRUPT	INPUT PIN	INTERRUPT SIGNAL DETECTION WIDTH	ENABLE CONDITION	PRIORITY	ENTRY ADDRESS
INTR1 (Interrupt 1)	• Schmitt input • Input logic level control	Minimum detection width 120μs Timer interrupt time 0.3~12.5ms	INTE1 = 1 IEF1 = 1	1	Address 1
INTR2 (Interrupt 2)		Minimum detection width 120μs Timer interrupt time 0.1~6.2s	INTE2 = 1 IEF2 = 1	2	Address 2

2. Interrupt circuit structure

The interrupt circuit consists of the interrupt input circuit, interrupt counter circuit, interrupt flip-flop, interrupt enable flip-flop, interrupt detector circuit, and an interrupt control port located in an internal I/O port used to control these circuits.



(1) Interrupt input circuit (INTR1 pin, INTR2 pin)

The interrupt signal inputs are Schmitt inputs. The inputs have noise rejection circuits that reject input pulses of less than 80~120μs as noise. The POL1/2 bit settings control the input logic. The INTR1 and INTR2 pins can be used as Schmitt input ports. The pin data can be referenced from the INTR1 and INTR2 bits (ϕK18) on the I/O map. In this case, noise rejection and input logic control do not apply.

(2) Counter circuit

Generation of an interrupt is determined by measuring the duration of the interrupt request. If an interrupt request is generated, the interrupt flip-flop is set.
To set the counter circuit, set the measuring time in the interrupt 1 counter setting bits "INT10~INT15", and set the INTC1 bit to "1". Similarly, for interrupt 2, set the counter setting bits "INT20~INT25", and set the INTC2 bit.

(3) Interrupt flip-flops (IEF1, IEF2)

The interrupt flip-flops are set by the output of the counter circuit. When the flip-flop is set to "1", the interrupt enters standby state, and, if the interrupt is enabled, the interrupt is generated.
An INTR1 interrupt request sets the interrupt 1 flip-flop (IFF1) to "1".
An INTR2 interrupt request sets the interrupt 2 flip-flop (IFF2) to "1".
The interrupt flip-flop is reset when the CPU accepts the interrupt. To forcibly reset the flip-flop, set the INTC bit to "0".

(4) Interrupt enable flip-flops (IEF1, IEF2)

The interrupt enable flip-flops 1 and 2 are flags to enable or disable acceptance of interrupts 1 and 2, respectively.
To set interrupt enable 1 flip-flop (IEF1) to "1", set the INTS1 bit to "1", or execute the RN instruction with INTE1 set to "1". The flip-flop is reset to "0" when interrupt 1 is received.
To set interrupt enable 2 flip-flop (IEF2) to "1", set the INTS2 bit to "1", or execute the RN instruction with INTE2 set to "1". The flip-flop is reset to "0" when interrupt 2 is received.

(5) Interrupt detector circuit

When the interrupt flip-flop is set to "1" with interrupt enabled, an interrupt request is issued to the CPU. When the interrupt is accepted, the interrupt enable bit and interrupt enable flip-flop are reset to "0". This disables any concurrent interrupt occurring immediately after the current interrupt is generated. If interrupt 1 and interrupt 2 requests occur simultaneously, the CPU accepts interrupt 1, which has the higher priority.

(6) Interrupt control ports

To set interrupts, use the interrupt control ports (ϕL28~ϕL2C) on the IO map.

	Y1	Y2	Y4	Y8
	Interrupt 1		Interrupt 2	
ϕL28	POL1	INTC1	POL2	INTC2

- POL1, POL2 ..... Interrupt input logic control bits

  1 : Positive logic input
  0 : Negative logic input

- INTC1, INTC2 ..... Interrupt input control bits

  1 : Input on
  0 : Input off

  Setting the INTC bit to "0" resets the corresponding noise rejection circuit, the interrupt counter circuit, and the interrupt flip-flop.

	Y1	Y2	Y4	Y8
	Interrupt 1			
ϕL29	INT10	INT11	INT12	INT13
ϕL2A	INT14	INT15	INTE1	INTS1

- INT10~INT15 ..... Interrupt 1 counter setting bits

  The measuring time can be set in 63 increments (one increment : 200μs) from a minimum time of 120μs to a maximum time of 12.5ms.
  (Note) Data setting "00H" is prohibited.

  Measuring time = $(0.2 \times (N - 1) + 0.12)$ ms * Measuring error = 0.2ms
  N : Setting increments (1~63)

- INTE1 ..... Interrupt 1 enable bit

  This bit is used to enable or disable acceptance of interrupt 1 by software.

  1 : Enables interrupt
  0 : Disables interrupt

  Setting INTE1 to "1" enables acceptance of interrupt 1.
  When interrupt 1 or interrupt 2 is generated, bit INTE1 is reset to "0" to disable acceptance of interrupts. Also, to temporarily disable the interrupt for a section of the program, set INTE1 to "0" by software. However, as the interrupt counter continues to operate, if the interrupt condition is satisfied, the counter sets the interrupt 1 flip-flop to 1. This sets the state to interrupt standby.

- INTS1 ..... Interrupt 1 enable flip-flop setting bit
  Setting the INTS1 bit to "1" sets the interrupt 1 enable flip-flop (IEF1) and enables the acceptance of an interrupt.
  The normal method of setting the interrupt 1 enable flip-flop to "1" to enable the interrupt is to execute the RN instruction with the INTE1 bit set to "1".

	Y1	Y2	Y4	Y8
	Interrupt 2			
ϕL2B	INT20	INT21	INT22	INT23
ϕL2C	INT24	INT25	INTE2	INTS2

- INT20~INT25 ..... Interrupt 2 counter setting bits
  The measuring time can be set in 63 increments (one increment : 100ms) from a minimum time of 120μs to a maximum time of 6.2s.
  (Note) Data setting "00H" is prohibited.

  Measuring time = (100 × (N − 1) + 0.12) ms * Measuring error = 50ms
  N : Setting increments (1~63)

- INTE2 ..... Interrupt 2 enable bit
  This bit is used to enable or disable acceptance of interrupt 2 by software.

  1 : Enables interrupt
  0 : Disables interrupt

  Setting INTE2 to "1" enables acceptance of interrupt 2.
  When interrupt 1 or interrupt 2 is generated, bit INTE2 is reset to "0" to disable acceptance of interrupts. Also, to temporarily disable the interrupt for a section of the program, set INTE2 to "0" by software. However, as the interrupt counter continues to operate, if the interrupt condition is satisfied, the counter sets the interrupt 2 flip-flop to "1". This sets the state to interrupt standby.

- INTS2 ..... Interrupt 2 enable flip-flop setting bit
  Setting the INTS2 bit to "1" sets the interrupt 2 enable flip-flop (IEF2) and enables the acceptance of an interrupt.
  The normal method of setting the interrupt 2 enable flip-flop to "1" to enable the interrupt is to execute the RN instruction with the INTE2 bit set to "1".

	INTERRUPT 1						
	INT 15	INT 14	INT 13	INT 12	INT 11	INT 10	TIMER INTERVAL
00	0	0	0	0	0	0	Prohibited
01	0	0	0	0	0	1	0.12~ [ms]
02	0	0	0	0	1	0	0.3~ [ms]
03	0	0	0	1	0	0	0.5~ [ms]
04	0	0	0	0	1	1	0.7~ [ms]
05	0	0	0	1	0	1	0.9~ [ms]
06	0	0	0	1	1	0	1.1~ [ms]
07	0	0	0	1	1	1	1.3~ [ms]
08	0	0	1	0	0	0	1.5~ [ms]
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
16	0	1	0	0	0	0	3.1~ [ms]
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
32	1	0	0	0	0	0	6.3~ [ms]
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
63	1	1	1	1	1	1	12.5~ [ms]

	INTERRUPT 2						
	INT 25	INT 24	INT 23	INT 22	INT 21	INT 20	TIMER INTERVAL
00	0	0	0	0	0	0	Prohibited
01	0	0	0	0	0	1	0.12~ [ms]
02	0	0	0	0	1	0	0.1~ [s]
03	0	0	0	1	0	0	0.2~ [s]
04	0	0	0	0	1	1	0.3~ [s]
05	0	0	0	1	0	1	0.4~ [s]
06	0	0	0	1	1	0	0.5~ [s]
07	0	0	0	1	1	1	0.6~ [s]
08	0	0	1	0	0	0	0.7~ [s]
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
16	0	1	0	0	0	0	1.5~ [s]
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
32	1	0	0	0	0	0	3.1~ [s]
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
63	1	1	1	1	1	1	6.2~ [s]

3. Interrupt processing

To handle interrupts, set the interrupt control port to enable interrupts, then wait for an interrupt. When an interrupt is received, the interrupt request is held in the interrupt flip-flop. If the interrupt enable bit and request is held in the interrupt flip-flop. If the interrupt enable bit and interrupt enable flip-flop are set to "1", the interrupt request is passed to the CPU. When an interrupt is generated, the interrupt flip-flop and the interrupt enable flip-flop for the interrupt are reset to "0". Then, control branches to the entry address. At the same time, the interrupt 1 and interrupt 2 enable bits are also reset to "0". This temporarily disables any further interrupts. However, the interrupt counter is not reset and continues to measure any further interrupt signals. Therefore, if necessary, use software to set the interrupt input control bits.

To handle multiple interrupts, set the interrupt enable bit to "1" in the interrupt service program.

The entry address specifies the branch destination address for the interrupt service program. During interrupt processing, the contents of the program counter are automatically saved to the stack. However, registers and memory area data are not saved automatically. If required, save such data in the interrupt service program. When handling multiple interrupts, be careful that the memory used to save the data does not overlap.

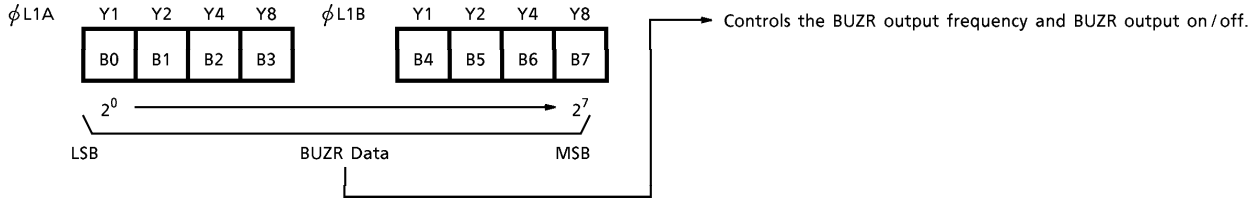
The interrupt service program sets the interrupt enable bit to "1", then terminates by executing the RN instruction.

Setting the interrupt enable bit to "1" and executing the RN instruction resets the interrupt enable flip-flop back to "1". Therefore, the next interrupt can be processed immediately after the instruction is executed.

○ Buzzer output (BUZR)

The buzzer output is used for such purposes as audible alarms or to issue confirmation beeps for key-presses or tuning scan mode. The buzzer frequency can be set as desired. 50% duty waveform is output.

1. BUZR data port



The BUZR output can also be used as the OT1 output port. To switch the OT1 output to BUZR output, set bits B0~B7 to a value of 2 or higher.
The BUZR output has a frequency of 75kHz divided by 2×n (n = B0~B7). The B0~B7 setting range and frequency range is $2 \leqq n \leqq 255$. This can be expressed as a formula as follows.

$$\frac{75\text{kHz}}{2\times 2} = 18.75\text{kHz} \leqq f_{BUZR} \leqq \frac{75\text{kHz}}{2\times 255} = 147\text{Hz}$$

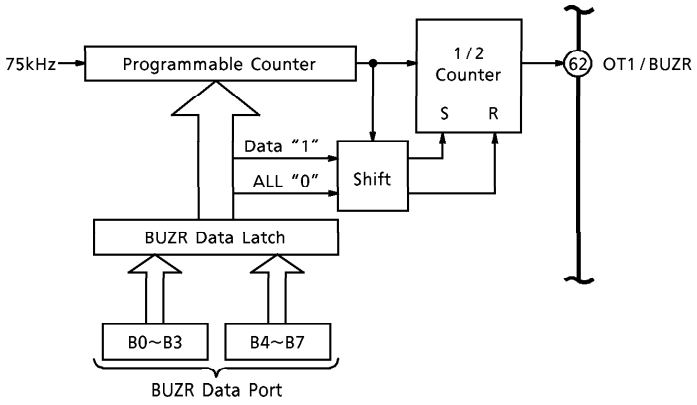
Set B0~B7 to 1 or 0 to use the pin for OT1 output. The output states are as follows.

B7	B6	B5	B4	B3	B2	B1	B0	OT1 OUTPUT
0	0	0	0	0	0	0	0	Low level output
0	0	0	0	0	0	0	1	High level output

To set the above data, use the OUT1 instruction with the operand [C_N = AH~BH].

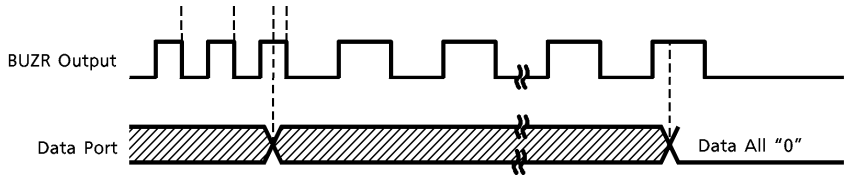
(Note) After a system reset, the BUZR data port is reset to "0".

2. BUZR circuit structure



The buzzer circuit consists of an 8bit programmable counter, a 1 / 2 counter, a buzzer latch, and a buzzer data port.

3. BUZR output timing

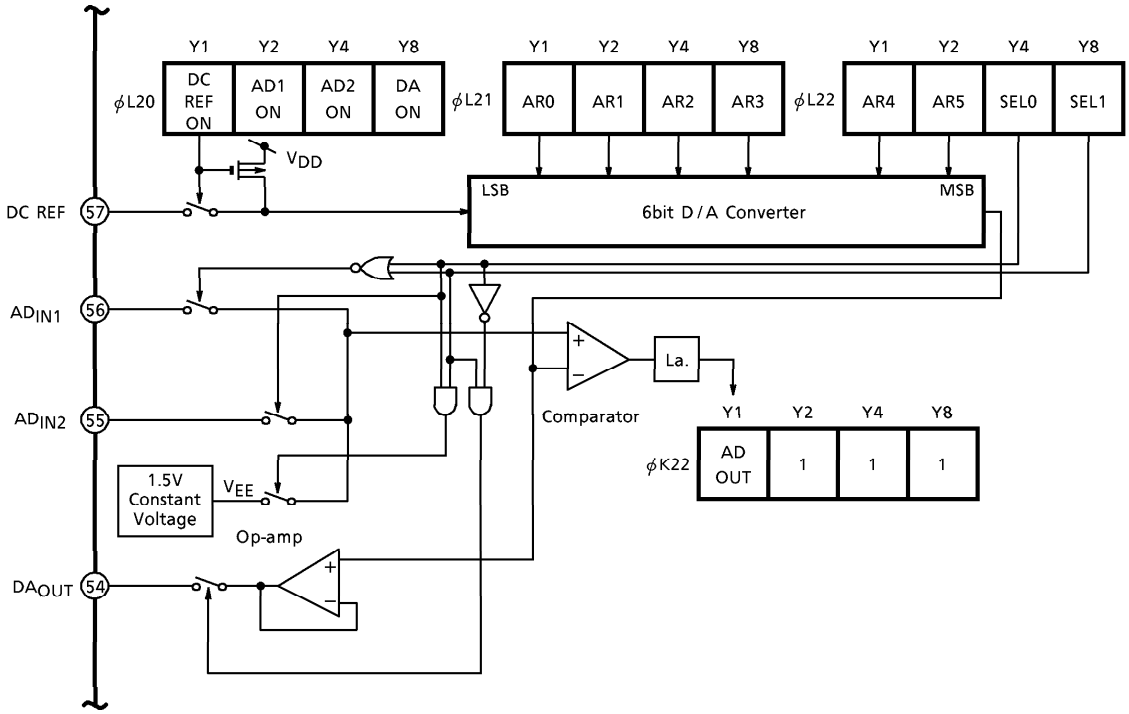


○ A / D and D / A converter

TC9314F incorporates a software-controlled successive approximation 6bit A / D converter and a 6bit D / A converter. The A / D and D / A converters share pins with I / O port 3. Pin operation is set by the DA / AD control port (ϕL20). Setting the DC REF ON bit to "1" sets P3-3 as reference voltage input (DC-REF). Setting the AD1 ON or AD2 ON bit to "1" sets P3-2 and P3-1 to AD analog voltage inputs (AD_{IN1} and AD_{IN2}). Setting the DA ON bit to "1" sets P3-0 to DA analog voltage output (DA_{OUT}).

In this case, the DA REF data 1 port (ϕL21) and DA REF data 2 port (ϕL22) set the A / D and D / A converter control data.

The A / D and D / A converter consists of a 6bit D / A converter, a comparator, an op-amp, and a control circuit.

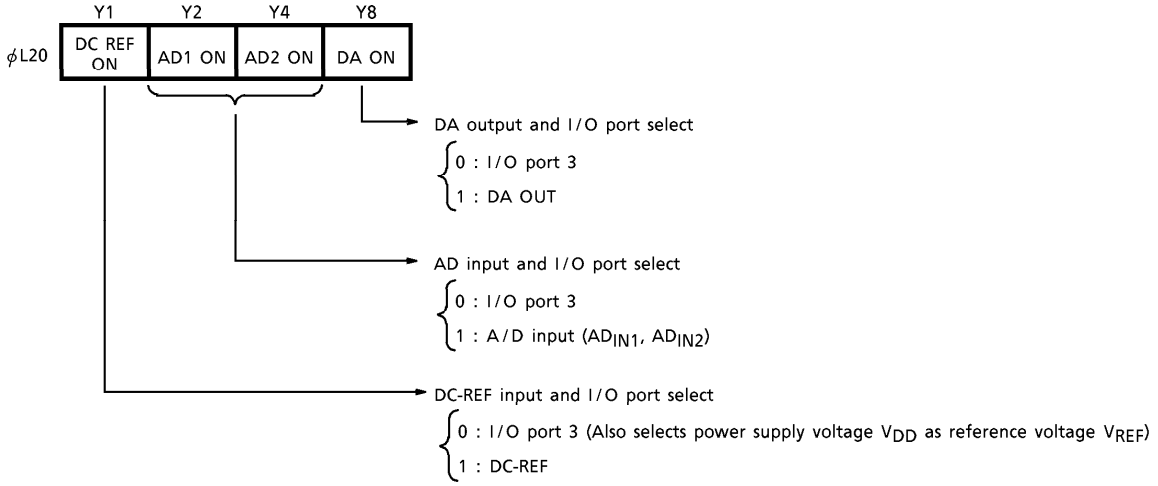


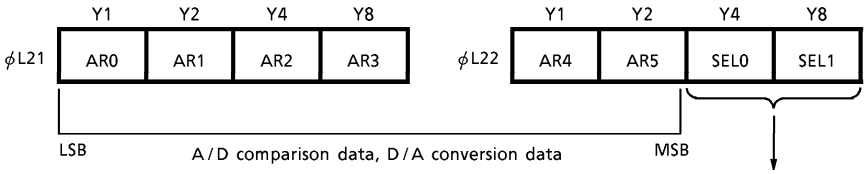
A / D and D / A converter structure

(Note) After a system reset, the DC REF ON bit, the AD1 ON bit, the AD2 ON bit, the DA ON bit, the SEL0 bit, and the SEL1 bit are all reset to "0".

(Note) The 6bit D / A converter used to generate the reference voltage is shared by the A / D and D / A converters.

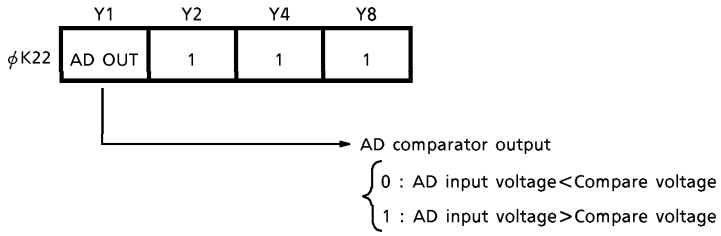
1. A/D, D/A converter control port, data port





A/D, D/A Input/Output Select

SEL1	SEL0	A/D, D/A INPUT/OUTPUT
0	0	AD_{IN1}
0	1	AD_{IN2}
1	0	DA OUT
1	1	1.5V constant voltage (V_{EE})



2. A / D converter

The 6bit resolution A / D converter is used for such purposes as measuring field intensity and battery voltage. The A / D analog input can be multiplexed to the two external A / D analog inputs (pins AD_{IN1} and AD_{IN2}), and can also be switched to the internal 1.5V constant voltage (V_{EE}). Normally, the external voltage (DC-REF) or power supply voltage (V_{DD}) is used as the reference voltage (V_{REF}). The external input voltage (AD input) is compared with the compare voltage corresponding to the AR0~AR5 data, and the result is stored in the comparator output latch. The A / D conversion is performed whenever data are set to the DA REF data 2 port (ϕL22). Therefore, always set the AR4 and AR5 bits of the A / D comparison data (ϕL22) last. The comparison result is output to the AD OUT port (ϕK22). The data can be read to data memory by the IN2 instruction with the operand [$C_N = 2$].

The relation between the input voltage and the compare voltage is :

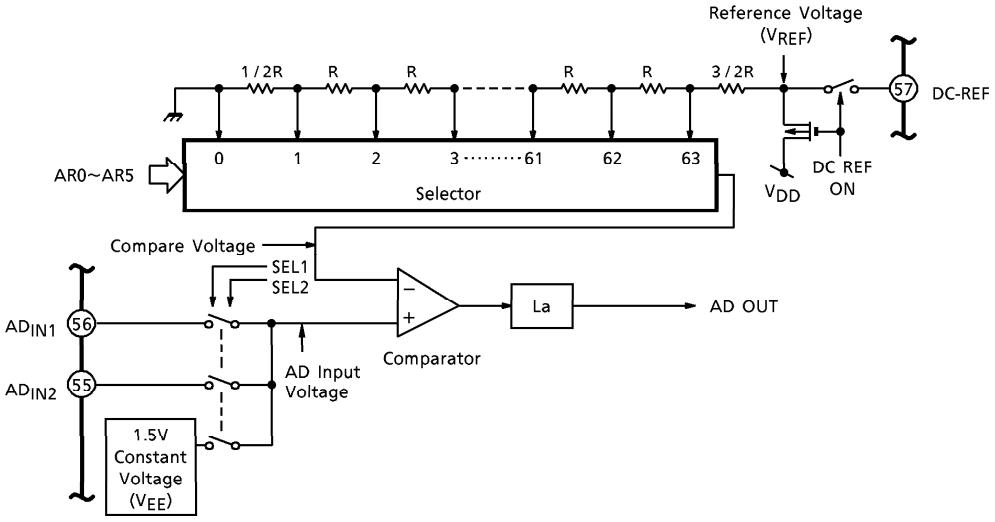
When AD input voltage < compare voltage : AD OUT = "0"

When AD input voltage > compare voltage : AD OUT = "1"

Use the following formula to calculate the compare voltage.

$$\text{Compare voltage} = V_{REF} \times \frac{n - 0.5}{64} \quad (\text{where n is the AR0~AR5 data value [decimal] } 63 \geqq n \geqq 1)$$

The SEL0 and SEL1 bits switch between the AD_{IN1} and AD_{IN2} inputs. When both SEL0 and SEL1 are set to "0", AD_{IN1} is input. When SEL0 is set to "1" and SEL1 is set to "0", AD_{IN2} is input. When both the SEL0 and SEL1 bits are set to "1", the A / D input is switched to the internal 1.5V constant voltage (V_{EE}). In this case, connect a capacitor (Typ. 0.47μF) to the AD_{IN2} pin to stabilize the constant voltage.

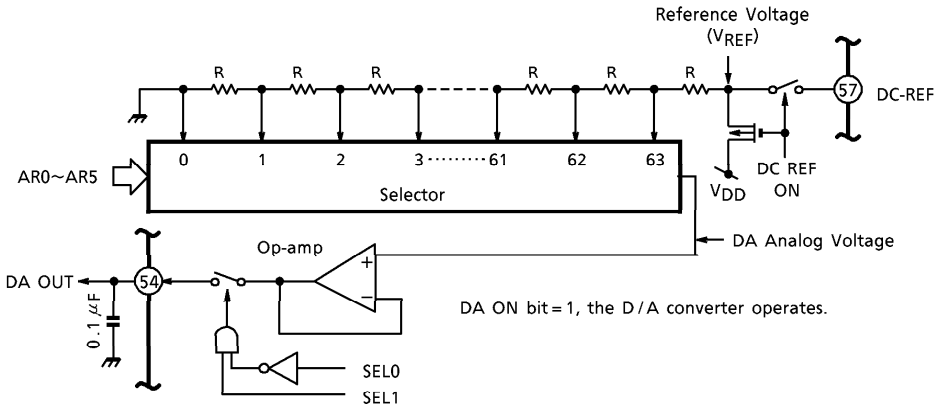


A / D comparator structure

3. D / A converter

The D / A converter can be used for such applications as an electronic volume control that operates using analog voltage control.
When using the D / A converter, set the DA ON bit to "1", set the SEL0 bit to "0", and set the SEL1 bit to "1". This outputs, from the DA OUT pin, the D / A analog voltage corresponding to the AR0~AR5 data. Because setting data to the DA REF data 2 port (ϕL22) simultaneously updates the D / A conversion data AR0~AR5, always set the AR4 and AR5 bits (ϕL22) last. When using the D / A converter and the A / D converter at the same time, control the SEL0 and SEL1 bits by software and operate by time sharing. As the D / A output goes to high impedance when the A / D converter is operating, connect a voltage retention capacitor to the output.
Use the following formula to calculate the D / A output.

$$\text{D / A output voltage} = V_{REF} \times \frac{n}{64} \text{ (where n is the AR0~AR5 data value [decimal] } 63 \geqq n \geqq 1)$$



D / A converter structure

(Note) The D / A output has an internal buffer. If necessary, add an external buffer.

(Note) As the D / A output range is 0V~V_{DD} – 1.0V, be careful when $V_{REF} = V_{DD}$.

(Note) For D / A conversion, the string resistors are the V_{REF} voltage divided into 64 increments.

○ Input / Output ports

1. I / O ports – 1, – 2, – 3, – 4, – 5, – 6, and – 7

I / O ports – 1, – 2, – 3, – 4, – 5, – 6, and – 7 are 4bit ports. Each bit can be set to either input or output by the I / O control internal ports. To set a port to input, set the corresponding bit in the I / O control port to "0". To set the port to output, set the corresponding bit in the I / O control port to "1".

When set to input, executing the IN3 instruction for the corresponding I / O port reads the current I / O port data to data memory. At this time, the contents of the output side latch are not affected by the input data.

When set to output, executing the OUT3 instruction for the corresponding I / O port controls the output state of the port. Executing the IN3 instruction reads the current output port data to data memory.

I / O port 3 is also used for the 6bit A / D, D / A converter analog inputs and output. I / O port 4 is also used for serial interface. When using I / O ports 3 and 4, set the DA / AD control port and SIO ON bit to "0". I / O ports 5~7 are also used for LCD driver output. To use one of these pins as an I / O port, set the SEG I / O bit corresponding to the pin to "0".

After a system reset, the ports that are also used by the serial interface and A / D, D / A converter are set as I / O ports. Also, after a system reset, the I / O ports are set as input ports, and the pins that are used by both the LCD driver and I / O ports are set to LCD driver output. (See the respective sections on the serial interface, the A / D, D / A converter, and the LCD driver.)

A change in the input state of an I / O port 1 port pin set as an input port releases the execution of a WAIT or CKSTP instruction and restarts the CPU. Similarly, when the I / O bit of the MUTE port is set to "1", a change in the input state forcibly sets the MUTE bit of the MUTE port to "1".

(Note) When the pins shared by the LCD driver and I / O ports are set as LCD driver pins, the I / O port input/output setting and the I / O port data are "don't care".

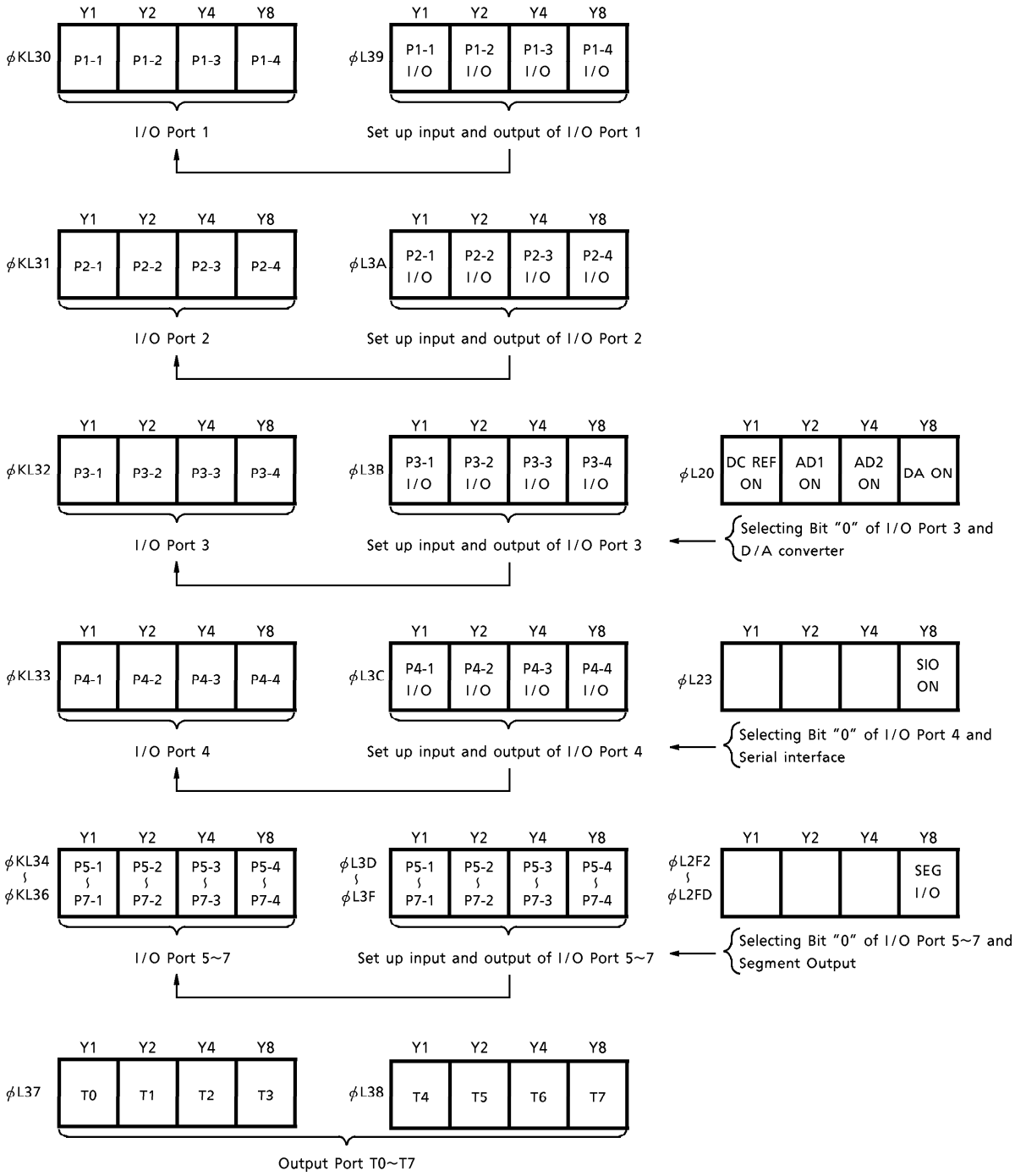
(Note) After a system reset, all the bits of the I / O control ports are reset to "0". This sets all I / O ports as input ports.

(Note) During clock stop mode, all I / O ports set as output ports automatically go to the low level. However, the output latches retain their existing data.

2. Key timing output port

T0~T7 form an 8bit output port. When forming a key matrix by software, this port outputs the key timing signal.

Accordingly, the N channel FET output has a high resistance to minimize the sink current. Therefore, when using these pins as standard output ports, be careful of the type of circuit being driven.


Y1 Y2 Y4 Y8
φKL30 P1-1 P1-2 P1-3 P1-4
I/O Port 1
φL39 P1-1 I/O P1-2 I/O P1-3 I/O P1-4 I/O
Set up input and output of I/O Port 1
φKL31 P2-1 P2-2 P2-3 P2-4
I/O Port 2
φL3A P2-1 I/O P2-2 I/O P2-3 I/O P2-4 I/O
Set up input and output of I/O Port 2
φKL32 P3-1 P3-2 P3-3 P3-4
I/O Port 3
φL3B P3-1 I/O P3-2 I/O P3-3 I/O P3-4 I/O
Set up input and output of I/O Port 3
φL20 DC REF ON AD1 ON AD2 ON DA ON
Selecting Bit "0" of I/O Port 3 and D/A converter
φKL33 P4-1 P4-2 P4-3 P4-4
I/O Port 4
φL3C P4-1 I/O P4-2 I/O P4-3 I/O P4-4 I/O
Set up input and output of I/O Port 4
φL23 SIO ON
Selecting Bit "0" of I/O Port 4 and Serial interface
φKL34 ~ φKL36 P5-1 ~ P7-1 P5-2 ~ P7-2 P5-3 ~ P7-3 P5-4 ~ P7-4
I/O Port 5~7
φL3D ~ φL3F P5-1 ~ P7-1 P5-2 ~ P7-2 P5-3 ~ P7-3 P5-4 ~ P7-4
Set up input and output of I/O Port 5~7
φL2F2 ~ φL2FD SEG I/O
Selecting Bit "0" of I/O Port 5~7 and Segment Output
φL37 T0 T1 T2 T3
φL38 T4 T5 T6 T7
Output Port T0~T7

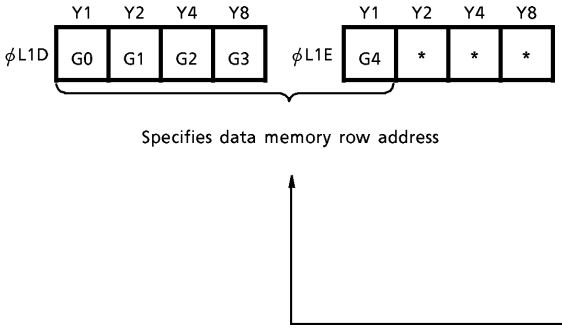
○ Register port

The G register (mentioned in the CPU description) and the data register are treated as internal ports.

1. G register (ϕL1D~ϕL1E)

This register sets the row address (D_R = 04H~17H) in data memory for the MVGD and MVGS instructions. To access this register, execute the OUT1 instruction with the operand [C_N = D~E].

(Note) The register value is only used when the MVGD or MVGS instructions are executed. The register is ignored for other instructions.

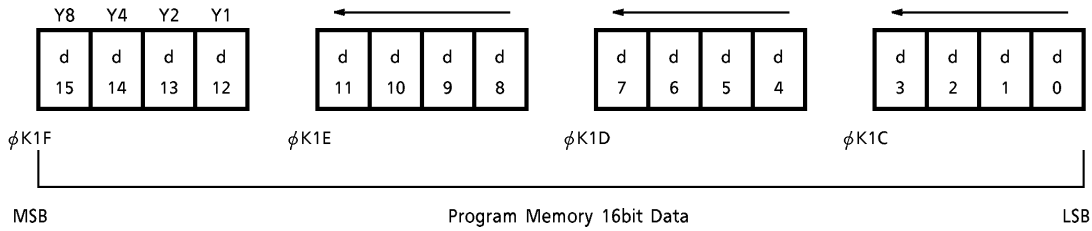


G4	G3	G2	G1	G0	DR
0	0	1	0	0	04H
0	0	1	0	1	05H
0	0	1	1	0	06H
≀	≀	≀	≀	≀	≀
1	0	1	1	0	16H
1	0	1	1	1	17H

(Note) Setting data 00H~17H in the G register allows all the data memory row addresses to be specified indirectly. (D_R = 00H~17H)

2. Data register (ϕK1C~ϕK1F)

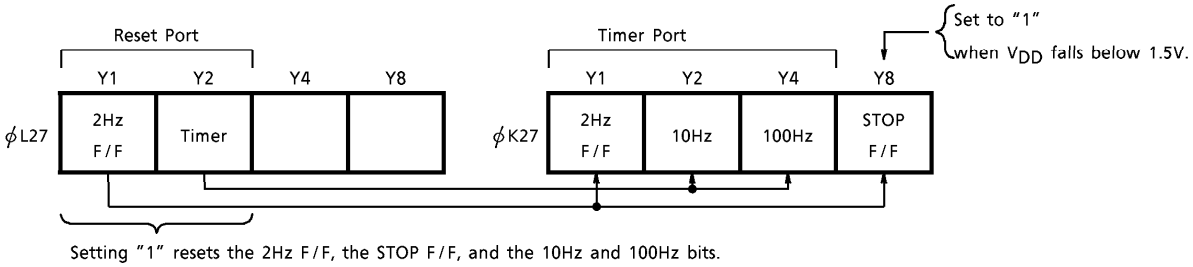
This is a 16bit register to load the program memory data when the DAL instruction is executed. The contents of the register are read to data memory in units of 4 bits by the IN1 instruction with the operands [C_N = CH~FH].
This register can be used for such purposes as LCD segment decoding, radio band edge data, or for coefficient data for binary-to-BCD conversion.



○ Timer and CPU stop function

The timer has 100Hz, 10Hz, and 2Hz flip-flop bits. These are used for counting operations, such as for a clock or tuning scan mode.
The CPU stop function uses a voltage detector circuit to shut down the CPU when the V_{DD} voltage applied to the CPU falls below 1.5V. This prevents CPU malfunction.

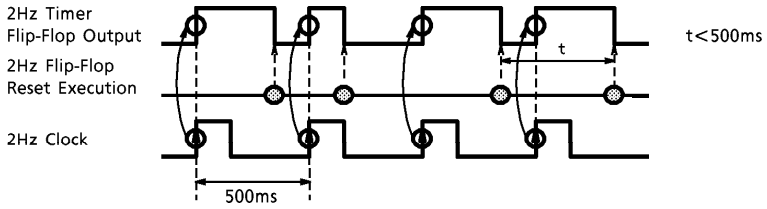
1. Timer port, STOP flip-flop bit



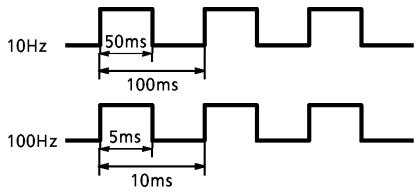
To access the timer port and the STOP flip-flop bit, execute the OUT2 / IN2 instruction with the operand [C_N = 7H].

2. Timer port timing

The 2Hz timer flip-flop is set by the 2Hz (500ms) signal, and reset by setting the RESET port 2Hz flip-flop to "1". This bit can normally be used for the clock count.
The 2Hz timer flip-flop is only reset by the 2Hz flip-flop in the RESET port. Therefore, if the flip-flop is not reset within 500ms, the next count is missed and the correct time is not obtained.



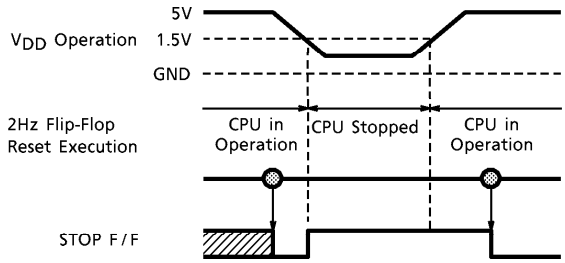
The 10Hz and 100Hz timers are output to the 10Hz and 100Hz bits with a cycle of 100ms and 10ms, respectively, and a pulse duty of 50%. Whenever the RESET port timer bit is set to "1", counters below 1kHz are reset.



3. CPU stop function, STOP flip-flop bit

The STOP flip-flop bit is set to "1" when the V_{DD} voltage applied to the CPU falls below 1.5V. This prevents CPU malfunction by shutting down the CPU. When a voltage of 1.5V or less is applied to the V_{DD} pin, the program counter stops and instruction execution ceases in the CPU. When a voltage higher than 1.5V is again applied to the V_{DD} pin, the CPU starts up again. As the CPU was shut down, the clock and other timings are no longer valid. Use the STOP flip-flop to test whether the CPU stop function operated. Perform initialization or clock correction if required.

The STOP flip-flop bit is reset to "0" whenever the RESET port 2Hz flip-flop is set to "1".



(Note) After a system reset or execution of the CKSTP instruction, the timer port and the STOP flip-flop are reset to "0".

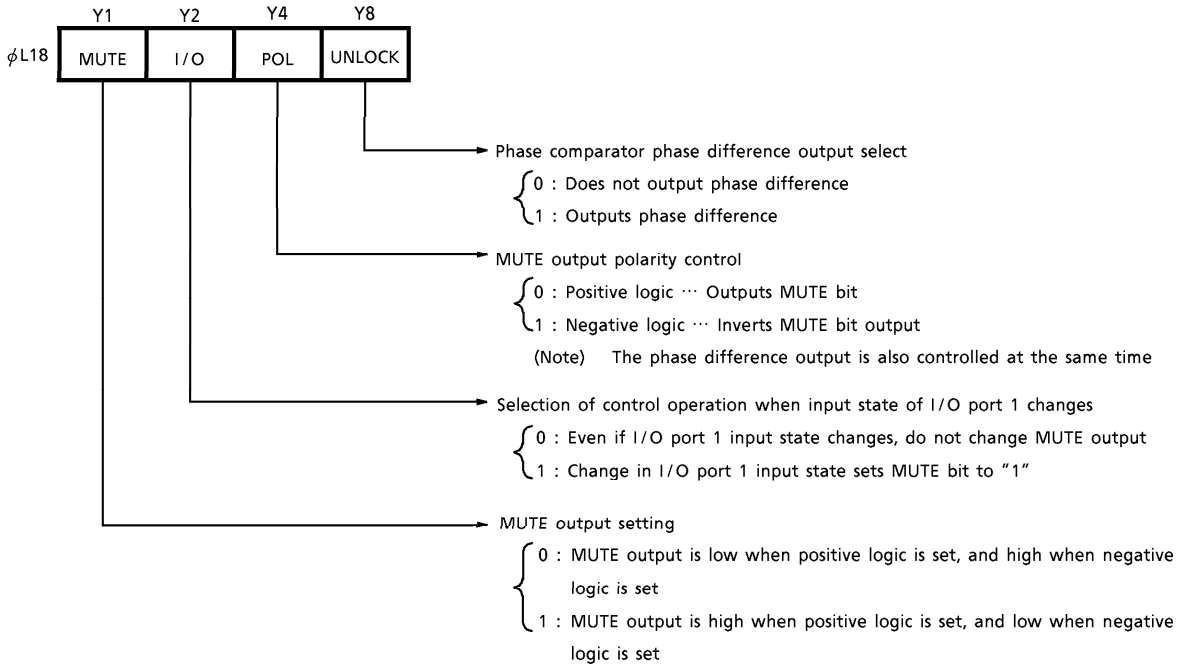
(Note) If the V_{DD} voltage falls below 1.5V when clock-stop mode is set, the CKSTP instruction cannot be executed. Be careful with the supply voltage timing, for example, when the radio is off.

(Note) The key scan data immediately after restarting the CPU are undefined.

○ MUTE output

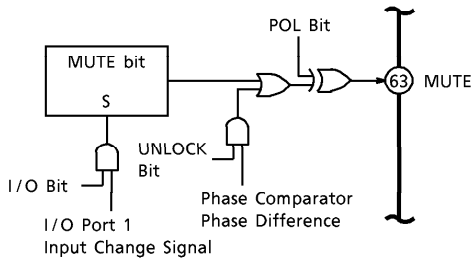
This is a 1bit CMOS-format output-only port for muting control.

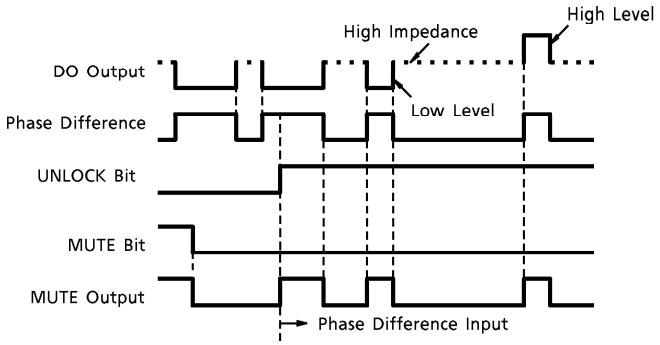
1. MUTE port



Access the MUTE port by executing the OUT1 instruction with the operand [C_N = 8H]. The MUTE output is used for muting control. At such times as switching bands using the I/O port 1 input, the MUTE bit can be set to "1".
When using the I/O port 1 input to switch bands (using a slide switch, for example), this function prevents linear circuit switching noise. This control is based on I/O bit values.
The POL bit sets the MUTE output logic.
The mute output can also control muting using the phase difference output. A pulse is output to indicate when the PLL is not locked. By connecting an external low-pass filter to the MUTE output, the output can be used as a MUTE output. Use the UNLOCK bit to perform selection.

2. MUTE output structure and timing



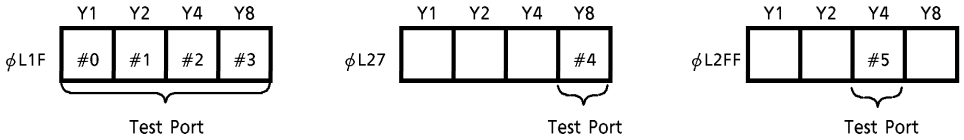


(Note) When POL bit = 0

(Note) When using the phase difference output by the phase comparator, externally connect a low-pass filter to the MUTE output.

○ Test ports

These are internal ports for testing the device's functions. Access the ports by executing the OUT1 instruction with the operand [C_N = FH], or the OUT2 instruction with the operands [C_N = 7H] or [C_N = FFH]. The ports are normally set to "0" by software.



(Note) The ports are reset to "0" after a system reset.

○ Using as an evaluator chip

When a high voltage is supplied to the TEST pin (TEST mode), the device functions as an evaluator chip.
Three test modes are supported. Use three devices to configure a software development tool.
Connecting this software development tool and a tuner IC enables you to check radio operations while developing software.
For the development tool specifications, refer to the TC9314F software development tool specification sheet.

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{DD}	− 0.3~6.0	V
Input Voltage	V_{IN}	− 0.3~V_{DD} + 0.3	V
Power Dissipation	P_D	400	mW
Operating Temperature	T_{opr}	− 10~60	°C
Storage Temperature	T_{stg}	− 55~125	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta = 25°C, V_{DD} = 5.0V)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Operating Power Supply Voltage	V_{DD1}	—	At PLL and DA / AD converter operation, Ta = − 10~60°C		2.7	~	5.5	V
CPU Operating Power Supply Voltage	V_{DD2}	—	When CPU only in operation, Ta = − 10~60°C		1.8	~	5.5	
Memory Retention Voltage	V_{HD}	—	When crystal oscillation stopped (at CKSTP execution), Ta = − 10~60°C		1.2	~	5.5	
Operating Power Supply Current	I_{DD1}	—	In normal operation, at no load output, and when FM_{IN} = 130MHz	At V_{DD} = 5.0V	—	10	20	mA
				At V_{DD} = 3.0V	—	3	6	
	I_{DD2}	—	When CPU only in operation, PLL off and display lit	At V_{DD} = 5.0V	—	70	140	μA
				At V_{DD} = 3.0V	—	50	100	
	I_{DD3}	—	In standby mode, PLL off and only crystal oscillator oscillating	At V_{DD} = 5.0V	—	10	20	
				At V_{DD} = 3.0V	—	10	20	
Memory Retention Current	I_{HD}	—	Crystal oscillation stopped (at CKSTP instruction execution)		—	0.1	1.0	
Crystal Oscillation Frequency	f_{XT}	—	V_{DD} = 1.8~5.5V, Ta = − 10~60°C		—	75	—	kHz
Crystal Oscillation Start Time	t_{ST}	—	Crystal oscillation : 75kHz		—	—	1.0	s

3V constant voltage circuit

Constant Voltage	V_{LCD}	—	GND reference (V_{LCD})	2.7	3.0	3.3	V

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Programmable counter and IF counter operating frequency ranges								
FM_{IN}	FM	—	V_{DD} = 2.7~5.5V V_{IN} = 0.3V_{p-p} input	*	50	~	130	MHz
		—	V_{DD} = 2.7~5.5V V_{IN} = 0.2V_{p-p} input	*	50	~	100	
AM_{IN} (HF Mode)	f_{HF}	—	V_{DD} = 2.7~5.5V V_{IN} = 0.3V_{p-p} input	*	1	~	60	
		—	V_{DD} = 2.7~5.5V V_{IN} = 0.2V_{p-p} input	*	1	~	30	
AM_{IN} (LF Mode)	f_{LF}	—	V_{DD} = 2.7~5.5V V_{IN} = 0.2V_{p-p} input	*	0.5	~	10	
IF_{IN1}, IF_{IN2}	f_{IF}	—	V_{DD} = 2.7~5.5V V_{IN} = 0.2V_{p-p} input	*	0.3	~	12	
Programmable counter and IF counter input amplitude ranges								
FM_{IN}	f_{FM}	—	f_{IN} = 50~130MHz input At V_{DD} = 2.7~5.5V	*	0.3	~	V_{DD} – 0.5	V_{p-p}
		—	f_{IN} = 50~100MHz input At V_{DD} = 2.7~5.5V	*	0.2	~	V_{DD} – 0.5	
AM_{IN} (HF Mode)	f_{HF}	—	f_{IN} = 1~60MHz input At V_{DD} = 2.7~5.5V	*	0.3	~	V_{DD} – 0.5	
		—	f_{IN} = 1~30MHz input At V_{DD} = 2.7~5.5V	*	0.2	~	V_{DD} – 0.5	
AM_{IN} (LF Mode)	f_{LF}	—	f_{IN} = 0.5~10MHz input At V_{DD} = 2.7~5.5V	*	0.2	~	V_{DD} – 0.5	
IF_{IN1}, IF_{IN2}	f_{IF}	—	f_{IN} = 0.3~12MHz input At V_{DD} = 2.7~5.5V	*	0.2	~	V_{DD} – 0.5	

Items with an asterisk (*) are guaranteed at V_{DD} = 3.5~5.5V and Ta = – 10~60°C.

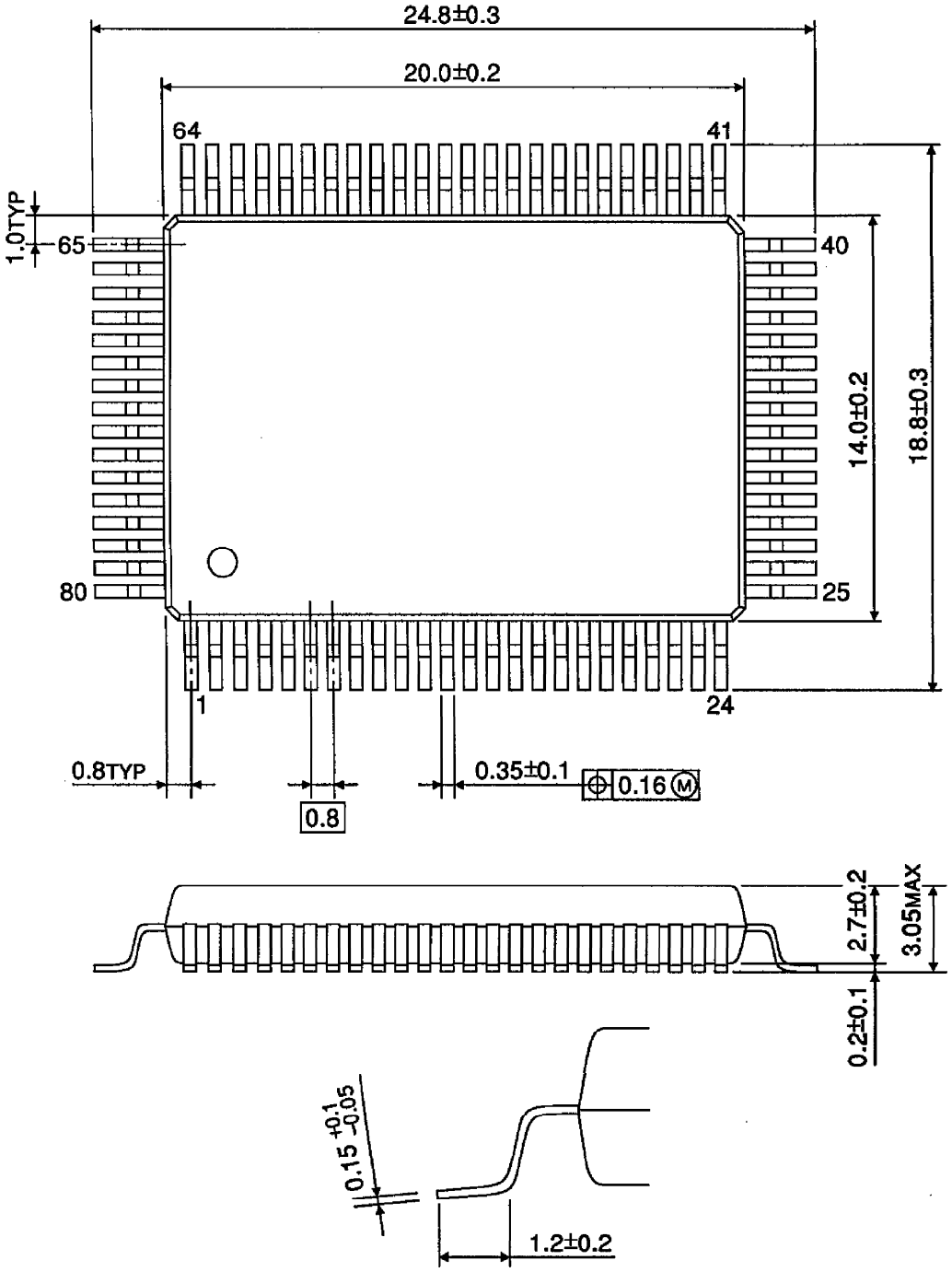
CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
LCD common output / segment output (COM1~COM3, S1~S3)								
Output Current	"H" Level	I_{OH2}	—	V_{LCD} = 3V, V_{OH} = 2.7V	−300	−600	—	μA
	"L" Level	I_{OL2}	—	V_{LCD} = 3V, V_{OL} = 0.3V	300	600	—	μA
Output Voltage 1 / 2 Level		V_{BS}	—	No load	1.3	1.5	1.7	V
Key input ports (K0~K3)								
Input Voltage	"H" Level	V_{IH1}	—	—	2.2	~	V_{DD}	V
	"L" Level	V_{IL1}	—	—	0	~	0.8	
Input Pull-Down Resistance		R_{IN1}	—	—	75	150	300	kΩ
Key return output ports (T0~T7)								
Output Current	"H" Level	I_{OH1}	—	V_{OH} = 4.5V	−1.5	−3.0	—	mA
Load Resistance At N-Channel		R_{ON}	—	V_{OL} = 5.0V	75	150	300	kΩ
$\overline{HOLD}$ input port								
Input Leakage Current		I_{LI}	—	V_{IH} = 5.0V, V_{IL} = 0V	—	—	±1.0	μA
Input Voltage	"H" Level	V_{IH3}	—	—	V_{DD} × 0.8	~	V_{DD}	V
	"L" Level	V_{IL3}	—	—	0	~	V_{DD} × 0.4	
A / D converter								
Analog Input Voltage		V_{AD}	—	AD_{IN1}, AD_{IN2}	0	~	V_{DD}	V
Analog Reference Voltage		V_{REF}	—	DC-REF	2.0	~	V_{DD}	V
Resolution		V_{RES}	—	—	—	6	—	bit
Total Conversion Error		—	—	—	—	±2.0	±3.0	LSB
Analog Input Leakage		I_{LI}	—	V_{IH} = 5.0V, V_{IL} = 0V (AD_{IN1}, AD_{IN2})	—	—	±1.0	μA
Analog Reference Input Current		I_{REF}	—	V_{IH} = 5.0V (DC-REF)	—	0.5	1.0	mA
Analog Output Voltage Range		V_{DAO}	—	DA OUT	0	—	V_{DD} − 1.0	V
Analog Output Voltage Deviation		V_{DA}	—	I_{DA} = ±100μA, V_{DD} = 5V, Ta = 25°C	—	±50	±100	mV

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
DO1, DO2, MUTE, OT1 output								
Output Current	"H" Level	I_{OH1}	—	V_{OH} = 4.5V	− 1.5	− 3.0	—	mA
	"L" Level	I_{OL1}	—	V_{OL} = 0.5V	1.5	3.0	—	
Output Off Leakage Current		I_{TL}	—	V_{TLH} = 5.0V, V_{TLL} = 0V (DO1, DO2)	—	—	± 100	nA
General-purpose I/O ports (P1-0~P4-3)								
Output Current	"H" Level	I_{OH1}	—	V_{OH} = 4.5V	− 1.5	− 3.0	—	mA
	"L" Level	I_{OL1}	—	V_{OL} = 0.5V	1.5	3.0	—	
Input Leakage Current		I_{LI}	—	V_{IH} = 5.0V, V_{IL} = 0V	—	—	± 1.0	μA
Input Voltage	"H" Level	V_{IH2}	—	—	V_{DD} × 0.7	~	V_{DD}	V
	"L" Level	V_{IL2}	—	—	0	~	V_{DD} × 0.3	
General-purpose I/O port (P5-0~P7-3)								
Output Current	"H" Level	I_{OH1}	—	V_{OH} = 4.5V	− 0.5	− 1.0	—	mA
	"L" Level	I_{OL1}	—	V_{OL} = 0.5V	0.5	1.0	—	
Input Leakage Current		I_{LI}	—	V_{IH} = 5.0V, V_{IL} = 0V	—	—	± 1.0	μA
Input Voltage	"H" Level	V_{IH2}	—	—	2.2	~	V_{DD}	V
	"L" Level	V_{IL2}	—	—	0	~	0.8	
INTR1、INTR2								
Input Leakage Current		I_{LI}	—	V_{IH} = 5.0V, V_{IL} = 0V	—	—	± 1.0	μA
Input Voltage	"H" Level	V_{IH3}	—	—	3.8	~	V_{DD}	V
	"L" Level	V_{IL3}	—	—	0	~	1.2	
IN1, IN2, $\overline{\text{RESET}}$ input ports								
Input Leakage Current		I_{LI}	—	V_{IH} = 5.0V, V_{IL} = 0V (Excluding SC_{IN} input)	—	—	± 1.0	μA
Input Voltage	"H" Level	V_{IH2}	—	—	V_{DD} × 0.7	~	V_{DD}	V
	"L" Level	V_{IL2}	—	—	0	~	V_{DD} × 0.3	

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Others							
Input Pull-Down Resistance	R_{IN2}	—	(TEST)	25	50	100	kΩ
X_{IN} Amp Feedback Resistance	R_{fXT}	—	(X_{IN}-X_{OUT})	—	20	—	MΩ
X_{OUT} Output Resistance	R_{OUT}	—	(X_{OUT})	—	3	—	kΩ
Input Amp Feedback Resistance	R_{fIN}	—	(FM_{IN}, AM_{IN}, IF_{IN1}, IF_{IN2})	250	500	1000	kΩ
Low- Voltage Detect Voltage	V_{STP}	—	(V_{DD})	1.3	1.5	1.7	V

PACKAGE DIMENSIONS

QFP80-P-1420-0.80A Unit : mm



Weight : 1.57g (Typ.)

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