The PCI Local Bus Specification, Revision 2.0, should be used as a reference with this document.

- **The TNETE211 Interfaces the ThunderLAN (TNETE100) Media Independent Interface (MII) to a 100VG-AnyLAN IEEE 802.12 Physical Media Dependent (PMD) Interface Device**
- **Single Consistent Driver Interface for 100VG Architectures**
- **Industry-Standard Interface to Multiple IEEE 802.12-Compliant PMD Devices**
- **Supports the Control Signaling Between the Medium Access Control (MAC) or Repeater MAC (RMAC) and the PMD Device**
- **Supports Packet Data Transmission and Reception by Providing a 4-Channel Stream Structure at the MII**
- **Supports Power Management With Microsoft™ Advanced Power Management**
- **IEEE Standard 1149.1† Test-Access Port (JTAG)**
- **Single 5-V Supply**
- **0.8-μm CMOS Technology**
- **PCMCIA-Compatible, Small-Footprint Surface-Mount Package**
- **80-Pin JEDEC Plastic Quad Flatpack (PN Suffix)**
- **Operating Temperature Range: 0°C to 70°C**

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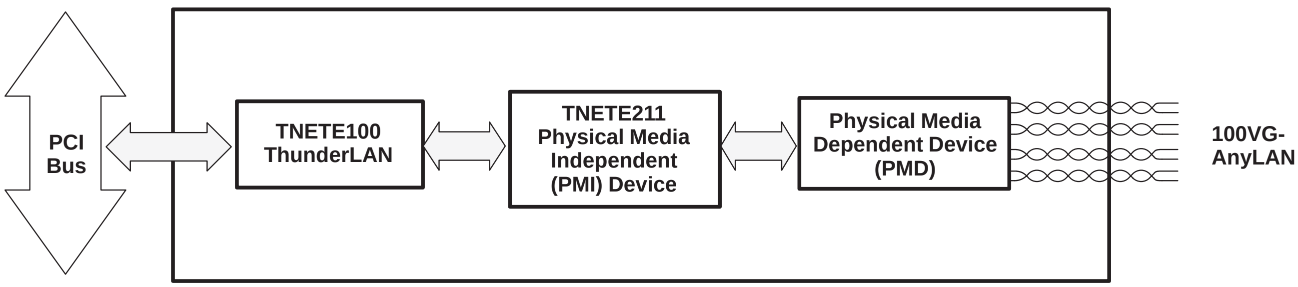

Figure 1. Typical Application

description

The TNETE211 interfaces the ThunderLAN TNETE100’s IEEE 802.3u media independent interface to an IEEE 802.12 physical media-dependent device for 100VG-AnyLAN operation. The TNETE211 is responsible for quartet channeling, scrambling the transmission data into five-bit data quintets, and encoding the resulting quintets into six-bit (5B6B) symbols. The TNETE211 also adds the preamble, start-frame delimiter, and end-frame delimiter to each channel.

Quartet channeling refers to the process of dividing the MAC frame data octets into five-bit data quintets and alloting them sequentially among the four transmission pair channels. The data scrambler alters the five-bit quintet into a randomized bit pattern which is helpful in reducing radio-frequency interference and signal cross talk between channels. The 5B6B symbol encoding transforms the five-bit randomized pattern into predetermined six-bit symbols. This provides a balanced data pattern with an equal number of zeroes and ones for clock transition synchronization for receive circuitry. This symbol encoding also has the added benefit of being an error-checking mechanism.

Compliant with IEEE Standard 1149.1-1990 (JTAG), the TNETE211 provides a five-pin test-access port that is used for boundary-scan testing.

The TNETE211 is available in an 80-pin plastic quad flat package.

† IEEE Standard 1149.1–1990, IEEE Standard Test Access Port and Boundary-Scan Architecture
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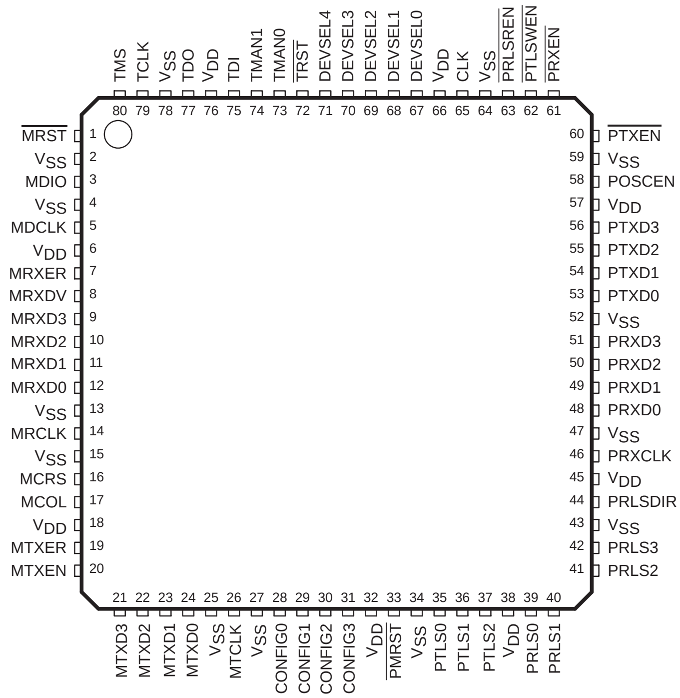
pin assignments



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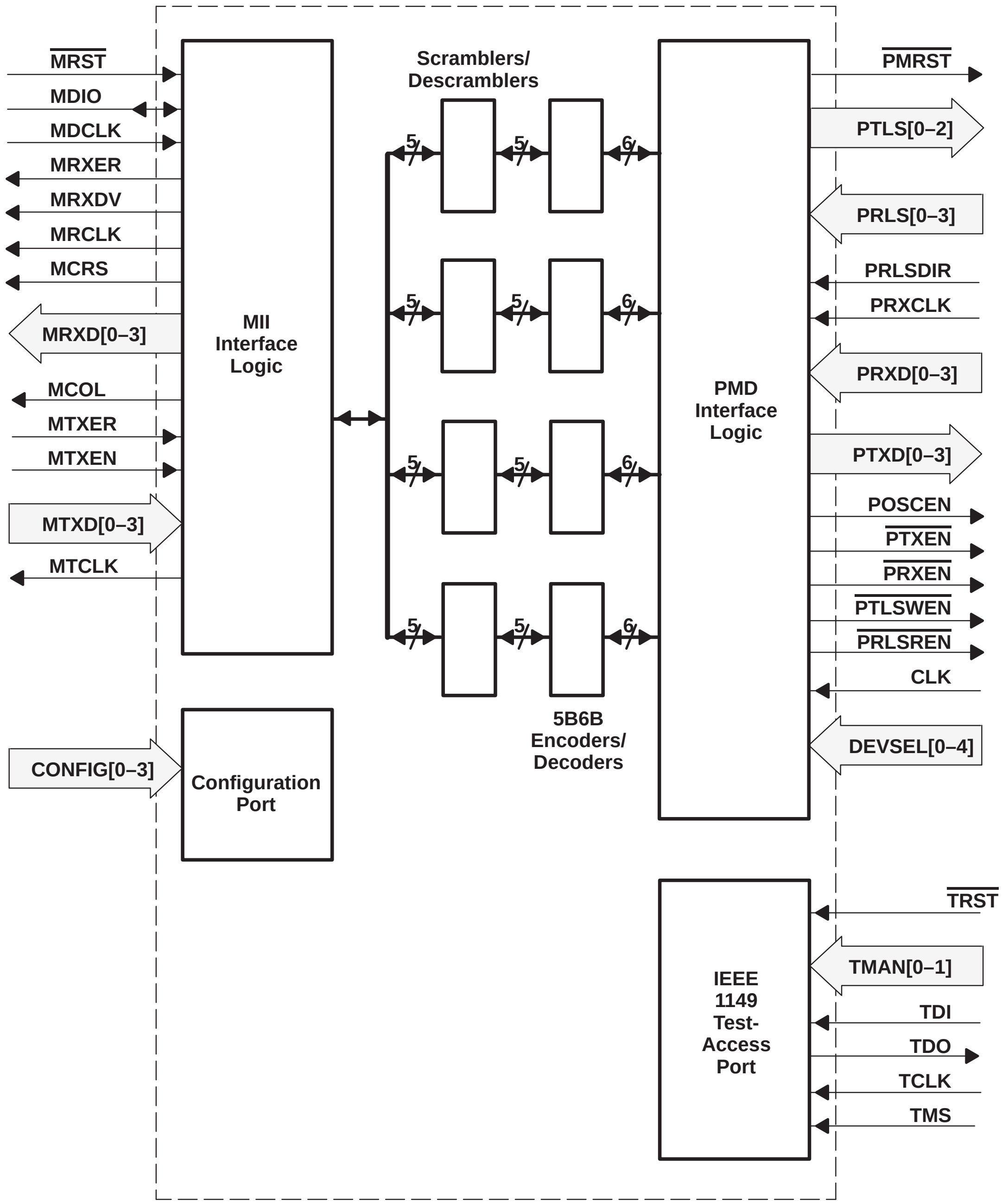
functional block diagram



ADVANCE INFORMATION

Pin Functions

Following is a list of TNETE211 physical media independent (PMI) pins and their functions. Assignment of pin numbers follows the order necessary to allow ThunderLAN and IEEE 802.12-compliant PMD devices to be laid out without any traces crossing. Pin names use the convention of indicating active low signals with an overbar. All ThunderLAN signals begin with an **M** (for MII). All manufacturing test signals begin with a **T** (for Test). All network interface signals begin with a **P** (for Physical Media Dependent).

PIN NAME	PIN NO.	TYPE†	DESCRIPTION
PHYSICAL MEDIA INDEPENDENT INTERFACE PINS (DEMAND-PRIORITY MODE)			
$\overline{MRST}$	1	I	MII reset. $\overline{MRST}$ resets signal to the PMD front end (active low).
MDIO	3	I/O	Management data I/O. MDIO is the serial management interface to PMD chip.
MDCLK	5	I	Management data clock. MDCLK is the serial management interface to PMD chip.
MRXER	7	O	Receive error. MRXER indicates reception of a coding error on received data.
MRXDV	8	O	Receive data valid. MRXDV indicates data on MRXD[0–3] is valid.
MRXD3 MRXD2 MRXD1 MRXD0	9 10 11 12	O	Receive data. MRXD[0–3] represents the nibble receive data from the PMD front end. The PMI indicates the priority of the incoming frames on these pins on the cycle before the assertion of MRXDV (the cycle before frame reception begins). MRXD1 indicates the transmission priority of the received frame. A value of zero indicates normal transmission, a value of one indicates priority transmission. Data on these pins is always synchronous to MRCLK.
MRCLK	14	O	Receive clock. MRCLK is the receive clock source from the PMI front end.
MCRS	16	O	Carrier sense. MCRS is not used in VG operation, but is connected to the TNETE100 MII for completeness.
MCOL	17	O	Collision sense. MCOL indicates that the PMI is transmitting on the physical media. • MCOL (active low) is used to acknowledge a transmission request. TNETE100 must begin frame transmission 50 MTCLK cycles after the assertion (low) of MCOL. MCOL is held asserted low until the PMI has completed all transmission tasks.
MTXER	19	I	Transmit error. MTXER allows coding errors to be propagated across the MII.
MTXEN	20	I	Transmit enable. MTXEN indicates valid transmit data on MTXD[0–3].
MTXD3 MTXD2 MTXD1 MTXD0	21 22 23 24	I	Transmit data. MTXD[0–3] represents the nibble transmit data from TNETE100; when MTXEN is asserted, these pins carry data transmissions. When MTXEN is not asserted (frame transmission not in progress), these pins carry control information. • MTXD0 asserted (high) indicates TNETE100 is requesting frame transmission. • MTXD1 indicates the transmission priority required. A value of zero indicates normal transmission; a value of one indicates priority transmission. Data/control on these pins is always synchronous to MTCLK.
MTCLK	26	O	Transmit clock. MTCLK is the transmit clock source from the PMI front end. Used to clock transmit and control data into the PMI device.

† I = input, O = output, and I/O = 3-state input/output

ADVANCE INFORMATION

Pin Functions (Continued)

PIN NAME	PIN NO.	TYPE†	DESCRIPTION
CONFIGURATION PINS (WIRE TYPE)			
CONFIG0 CONFIG1 CONFIG2 CONFIG3	28 29 30 31	I	Configuration. CONFIG[0–3] indicate the current wire configuration of the PMI.
PHYSICAL MEDIA DEPENDENT (PMD) PINS (PINS CONNECTING TO THE IEEE 802.12-COMPLIANT PMD DEVICE)			
$\overline{\text{PMRST}}$	33	O	PMD reset/detect. $\overline{\text{PMRST}}$, when seen low, resets the PMD.
PTLS0 PTLS1 PTLS2	35 36 37	O	Transmit line status. The PTLS[0–2] pins are used to set the current transmit line state.
PRLS0 PRLS1 PRLS2 PRLS3	39 40 41 42	I	Receive line state. The PRLS[0–3] pins are used to determine the current receive-line state from the PMD.
PRLSDIR	44	I	PMD RLS direct. When the PRLSDIR pin is asserted high, this pin allows the TNETE211 PMD pins to directly connect to the IEEE 802.12 MII interface. When low, this pin allows the TNETE211 PMD pins to directly connect to the AT&T ATT2X01.
PRXCLK	46	I	Receive data clock. PRXCLK is the receive data clock reference.
PRXD0 PRXD1 PRXD2 PRXD3	48 49 50 51	I	Receive data. PRXD[0–3] are used to transfer the data streams received from the PMD.
PTXD0 PTXD1 PTXD2 PTXD3	53 54 55 56	O	Transmit data. PTXD0[0–3] transmit data to the PMD device.
POSCEN	58	O	Oscillator enable. POSCEN is used to enable the TNET211 30-MHz oscillator. When POSCEN is high, the oscillator is driven to the TNETE211. When POSCEN is low, the oscillator is disabled. The POSCEN is mainly used for power-down functions.
$\overline{\text{PTXEN}}$	60	O	Transmit enable. $\overline{\text{PTXEN}}$ indicates valid data on the PTXD[0–3] pins.
$\overline{\text{PRXEN}}$	61	O	Receive enable. $\overline{\text{PRXEN}}$ causes the PMD to drive the received data to the PRXD[0–3] pins.
$\overline{\text{PTLSWEN}}$	62	O	Transmit line state write enable. $\overline{\text{PTLSWEN}}$ indicates when the PTLS[0–2] pins are valid.
$\overline{\text{PRLSREN}}$	63	O	Receive line state read enable. $\overline{\text{PRLSREN}}$ indicates when the PRLS[0–3] pins are valid.
CLK	65	I	Main clock. CLK is the 30-MHz clock pin used to drive all internal transmit and line state control functions.
DEVSEL0 DEVSEL1 DEVSEL2 DEVSEL3 DEVSEL4	67 68 69 70 71	I	Device select. DEVSEL[0–4] are used for PMI device selection. The device number in the MII is compared with these pins for the MII read-and-write operations.

† I = input, O = output, I/O = 3-state input/output

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Pin Functions (Continued)

PIN NAME	PIN NO.	TYPE†	DESCRIPTION
TEST PORT			
$\overline{TRST}$	72	I	Test reset. $\overline{TRST}$ is used for asynchronous reset of the test port controller (optional).
TMAN0 TMAN1	73 74	I	Manufacture test. TMAN[0–1] are used for manufacture test functions. TMAN0 TMAN1 Description 0 0 Unit in place. All internal pullup resistors on all input pins are disabled. 0 1 Reserved 1 0 Reserved 1 1 Normal operation. All input pins' internal pullup resistors are enabled.
TDI	75	I	Test data input. TDI serially shifts test data and test instructions into the device during operation of the test port.
TDO	77	O	Test data output. TDO serially shifts test data and test instructions out of the device during operation of the test port.
TCLK	79	I	Test clock. TCLK clocks state information and test data into and out of the device during operation of the test port.
TMS	80	I	Test mode select. TMS controls the state of the test port controller within the TNETE211.
POWER			
V_{SS}	2, 4, 13, 15, 25, 27, 34, 43, 47, 52, 59, 64, 78	PWR	Ground pins
V_{DD}	6, 18, 32, 38, 45, 57, 66, 76	PWR	Supply voltage

† I = input, O = output, PWR = power

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} (see Note 1) . . . . – 0.5 V to 7 V
Input voltage range (see Note 1) . . . . – 0.5 V to 7 V
Output voltage range . . . . – 0.5 V to 7 V
Maximum operating case temperature, T_C . . . . 95°C
Operating free-air temperature range, T_A . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . – 65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to V_{SS}, and all V_{SS} pins should be routed so as to minimize inductance to system ground.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage (5 V only)		4.75	5	5.25	V
V_{SS}	Ground			0		
V_{IH}	High-level input voltage		2		V_{DD} + 0.3	V
V_{IL}	Low-level input voltage, TTL-level signal (see Note 2)		–0.3		0.8	V
I_{OH}	High-level output current	TTL outputs			–4	mA
I_{OL}	Low-level output current (see Note 3)	TTL outputs			4	mA
T_A	Operating free-air temperature		0		70	°C

NOTES: 2. The algebraic convention, where the more negative (less positive) limit is designated as a minimum, is used for logic-voltage levels only.
3. Output current of 2 mA is sufficient to drive five low-power Schottky TTL loads or ten advanced low-power Schottky TTL loads (worst case).

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS‡		MIN	MAX	UNIT
V_{OH}	High-level output voltage, TTL-level signal	V_{DD} = MIN,	I_{OH} = MAX	2.4		V
V_{OL}	Low-level output voltage, TTL-level signal	V_{DD} = MAX,	I_{OL} = MAX		0.5	V
I_O	High-impedance output current	V_{DD} = MIN,	V_O = V_{DD}		10	µA
		V_{DD} = MIN,	V_O = 0 V		–10	
I_I	Input current	V_I = V_{SS} to V_{DD}			± 1	µA
I_{DD}	Supply current	V_{DD} = MAX			400	mA
C_i	Input capacitance, any input	f = 1 MHz,	Others at 0 V		10	pF
C_o	Output capacitance, any output or input / output	f = 1 MHz,	Others at 0 V		10	pF

‡ For conditions shown as MIN / MAX, use the appropriate value specified under the “recommended operating conditions”.

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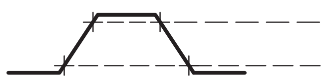
PARAMETER MEASUREMENT INFORMATION

Outputs are driven to a minimum high-logic level of 2.4 V and to a maximum low-logic level of 0.6 V. These levels are compatible with TTL devices.

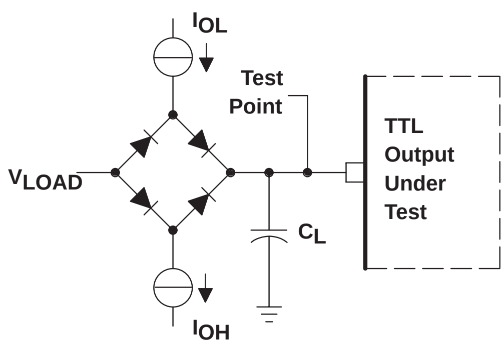
Output transition times are specified as follows: For a high-to-low transition on either an input or output signal, the level at which the signal is said to be no longer high is 2 V and the level at which the signal is said to be low is 0.8 V. For a low-to-high transition, the level at which the signal is said to be no longer low is 0.8 V and the level at which the signal is said to be high is 2 V, as shown below.

The rise and fall times are not specified but are assumed to be those of standard TTL devices, which are typically 1.5 ns.



test measurement

The test-load circuit shown in Figure 2 represents the programmable load of the tester pin electronics that are used to verify timing parameters of TNETE211 output signals.



Where: I_{OL} = Refer to I_{OL} in recommended operating conditions
I_{OH} = Refer to I_{OH} in recommended operating conditions
V_{LOAD} = 1.5 V, typical dc-level verification or 0.7 V, typical timing verification
C_L = 18 pF, typical load-circuit capacitance

Figure 2. Test-Load Circuit

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MII receive timing requirements†

PARAMETER		MIN	MAX	UNIT
$t_{su(MTx\ pins)}$	Setup time of inputs MTXD[0–3], MTXEN, MTXER (see Note 4)	10		ns
$t_{h(MTx\ pins)}$	Hold time of inputs MTXD[0–3], MTXEN, MTXER (see Note 4)	>0		ns

MII transmit switching characteristics†

PARAMETER		MIN	MAX	UNIT
$t_{d(MRx\ pins)}$	MRCLK to output delay for MRXD[0–3], MRXDV, and MRXER (see Note 5)	0	15	ns

† Both MCRS and MCOL are driven asynchronously by the PMI.

NOTES: 4. MTXD[0–3] is driven by the reconciliation sublayer synchronous to the MTCLK. MTXEN is asserted and deasserted by the reconciliation sublayer synchronous to the MTCLK rising edge. MTXER is driven synchronous to the rising edge of MTCLK.

5. MRXD[0–3] is driven by the PMI on the falling edge of MRCLK. It is sampled by the reconciliation sublayer synchronous to the edge of MRCLK. MRXD[0–3] timing must be met during clock periods where MRXDV is asserted. MRXDV is asserted and deasserted by the PMI on the falling edge of MRCLK. It is sampled by the reconciliation sublayer synchronous to the rising edge of MRCLK. MRXER is driven by the PMI on the falling edge of MRCLK. It is sampled by the reconciliation sublayer synchronous to the rising edge of MRCLK. MRXER timing must be met during clock periods when MRXDV is asserted.

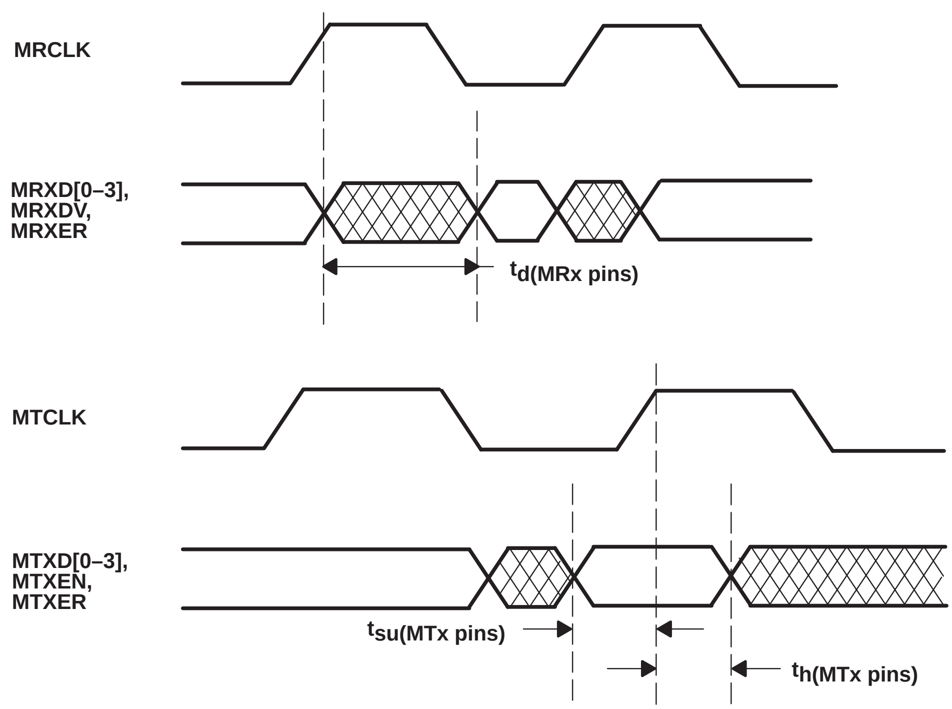

Figure 3. MII Transmit and Receive Timing

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MDIO timing requirements

		MIN	MAX	UNIT
$t_{d(MDCLKH-MDIOV)}$	Delay time, MDIO valid from MDCLK high (see Note 6)	0	25	ns

MDIO switching characteristics

PARAMETER		MIN	MAX	UNIT
$t_{su(MDIOV-MDCLKH)}$	Setup time, MDIO valid to MDCLK high (see Note 7)	15		ns
$t_{h(MDCLKH-MDIOX)}$	Hold time, MDCLK high to MDIO changing (see Note 7)	15		ns

NOTES: 6. When the MDIO signal is sourced by the PMI, it is sampled by TNETE100 synchronous to the rising edge of MDCLK.
7. MDIO is a bidirectional signal that can be sourced by TNETE100 or the PMI.

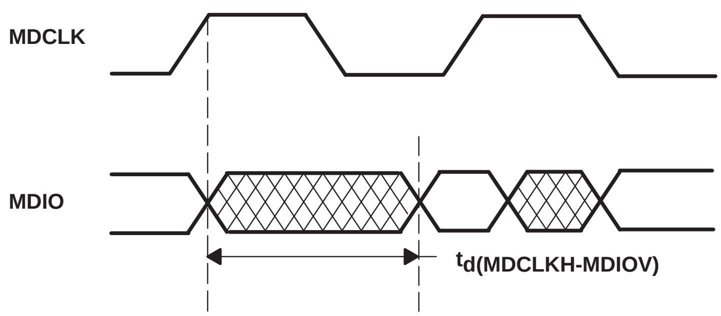

Figure 4. Management Data I/O Timing (Sourced by PMI)

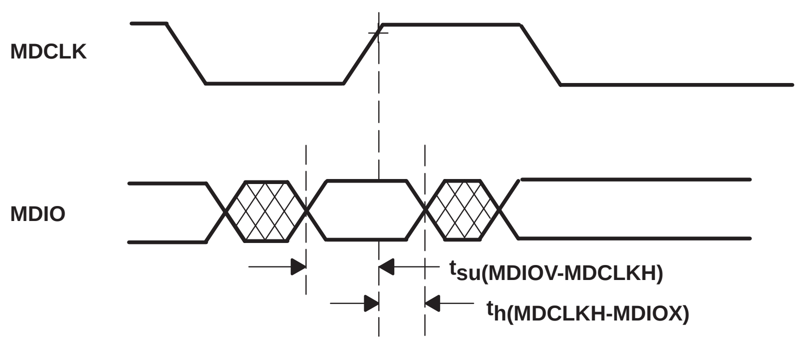

Figure 5. Management Data I/O Timing [Sourced by Station Management Entity (STA)]

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PRXD timing requirements (see Figure 6)

PARAMETER		MIN	MAX	UNIT
$t_{d(CLK\text{-}PRXENL)}$	Delay time, CLK to $\overline{\text{PRXEN}}$ low	>0	15	ns
$t_{d(CLK\text{-}PRXENH)}$	Delay time, CLK to $\overline{\text{PRXEN}}$ high	>0	15	ns
$t_{h(PRXCLK\text{-}PRXD)}$	Hold time, PRXCLK to PRXD changing	>0		ns
$t_{su(PRXD\text{-}PRXCLK)}$	Setup time, PRXD valid to PRXCLK	10		ns

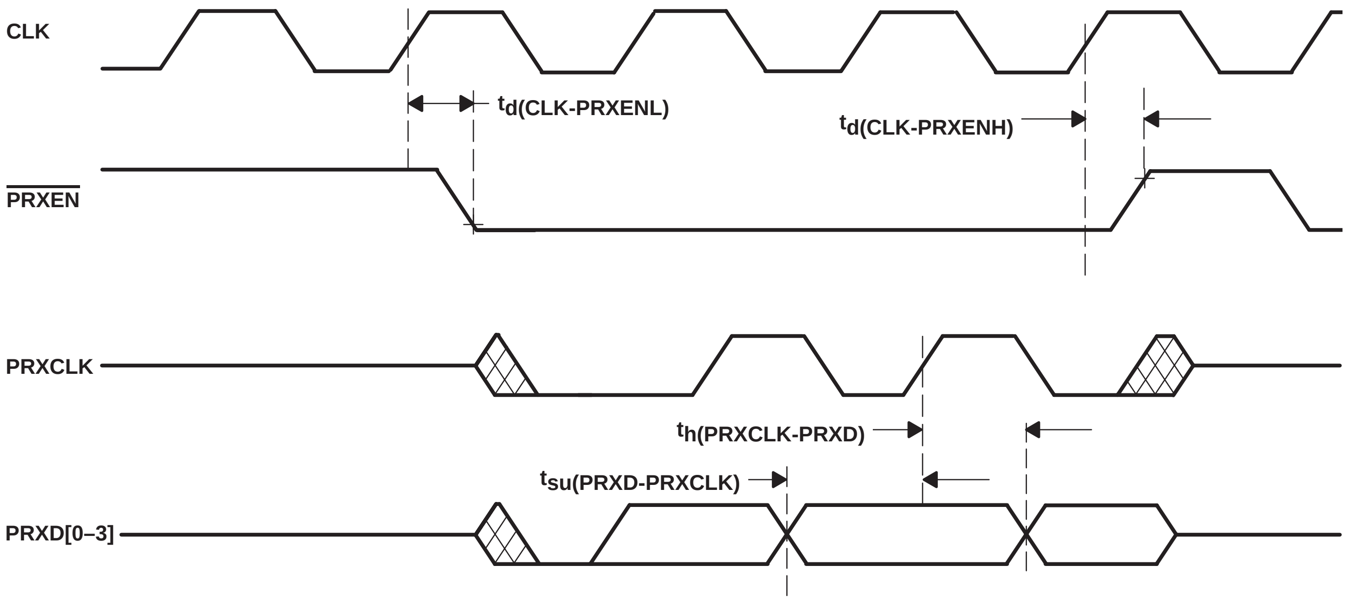

Figure 6. Receive Data Timing

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TDATA timing requirements (see Figure 7)

PARAMETER		MIN	MAX	UNIT
$t_{d(CLK-PTXENL)}$	Delay time, CLK to $\overline{PTXEN}$ low	>0	15	ns
$t_{d(CLK-PTXENH)}$	Delay time, CLK to $\overline{PTXEN}$ high	>0	15	ns
$t_{d(CLK-PTXDV)}$	Delay time, CLK to PTXD valid	>0	15	ns

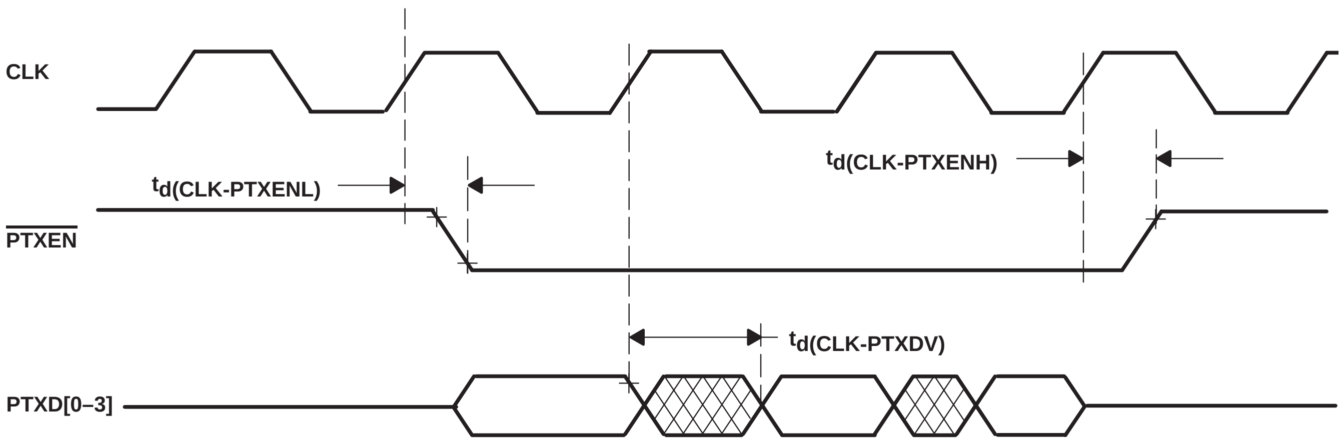

Figure 7. Transmit Data Timing

PRLS timing requirements (see Figure 8)

PARAMETER		MIN	MAX	UNIT
$t_{d(CLK-PRLSRENL)}$	Delay time, CLK to $\overline{PRLSREN}$ low	>0	15	ns
$t_{d(CLK-PRLSRENH)}$	Delay time, CLK to $\overline{PRLSREN}$ high	>0	15	ns
$t_{su(PRLSV-CLK)}$	Setup time, PRLS valid to rising edge of CLK	10		ns
$t_{h(CLK-PRLSX)}$	Hold time, CLK to PRLS changing	>0		ns

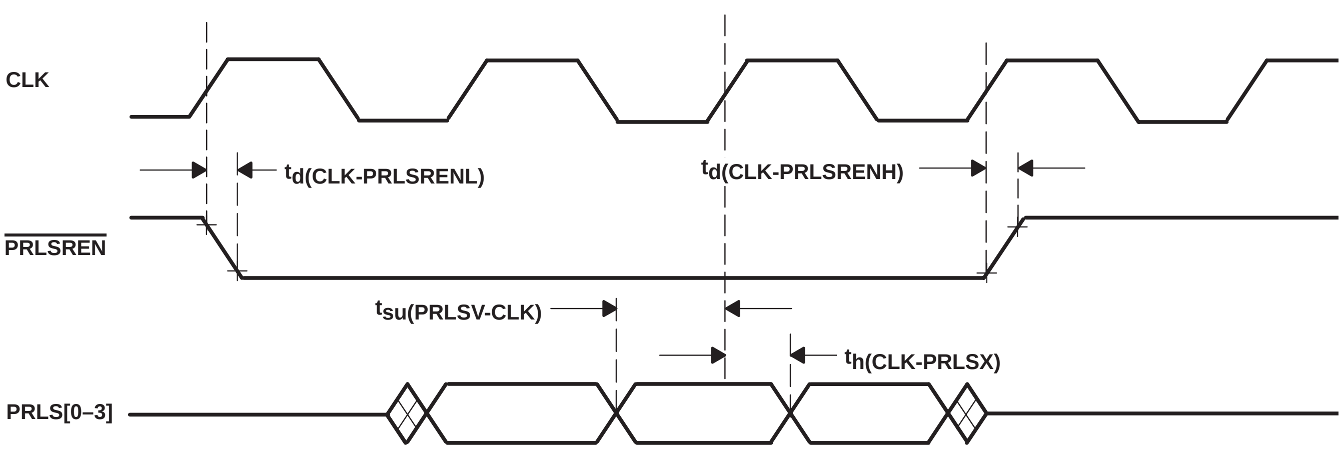

Figure 8. PRLS Timing

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TLS timing requirements (see Figure 9)

PARAMETER		MIN	MAX	UNIT
$t_{d(CLK-PTLSWENL)}$	Delay time, CLK to $\overline{\text{PTLSWEN}}$ low	>0	15	ns
$t_{d(CLK-PTLSV)}$	Delay time, CLK to PTLS[0–2] valid	>0	15	ns

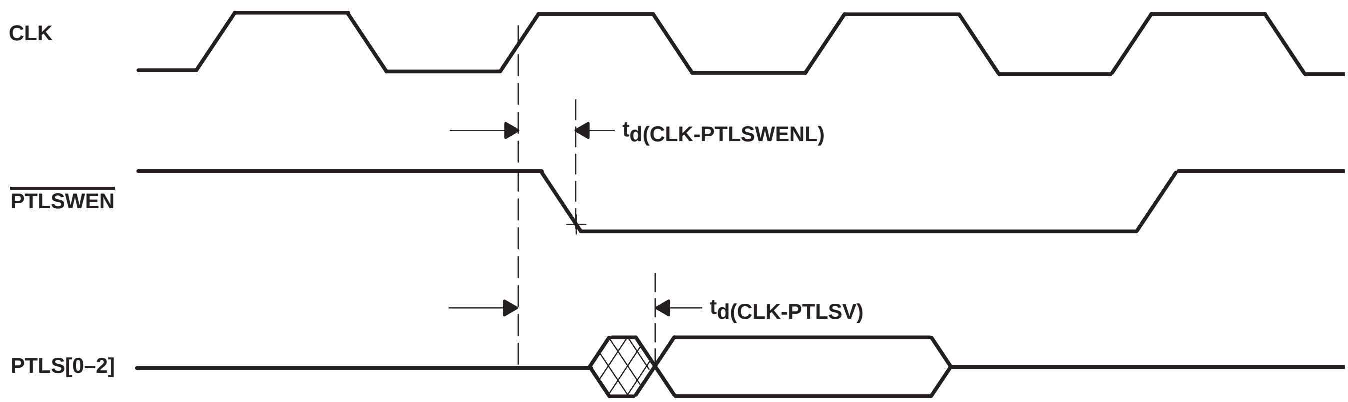

Figure 9. TLS Timing

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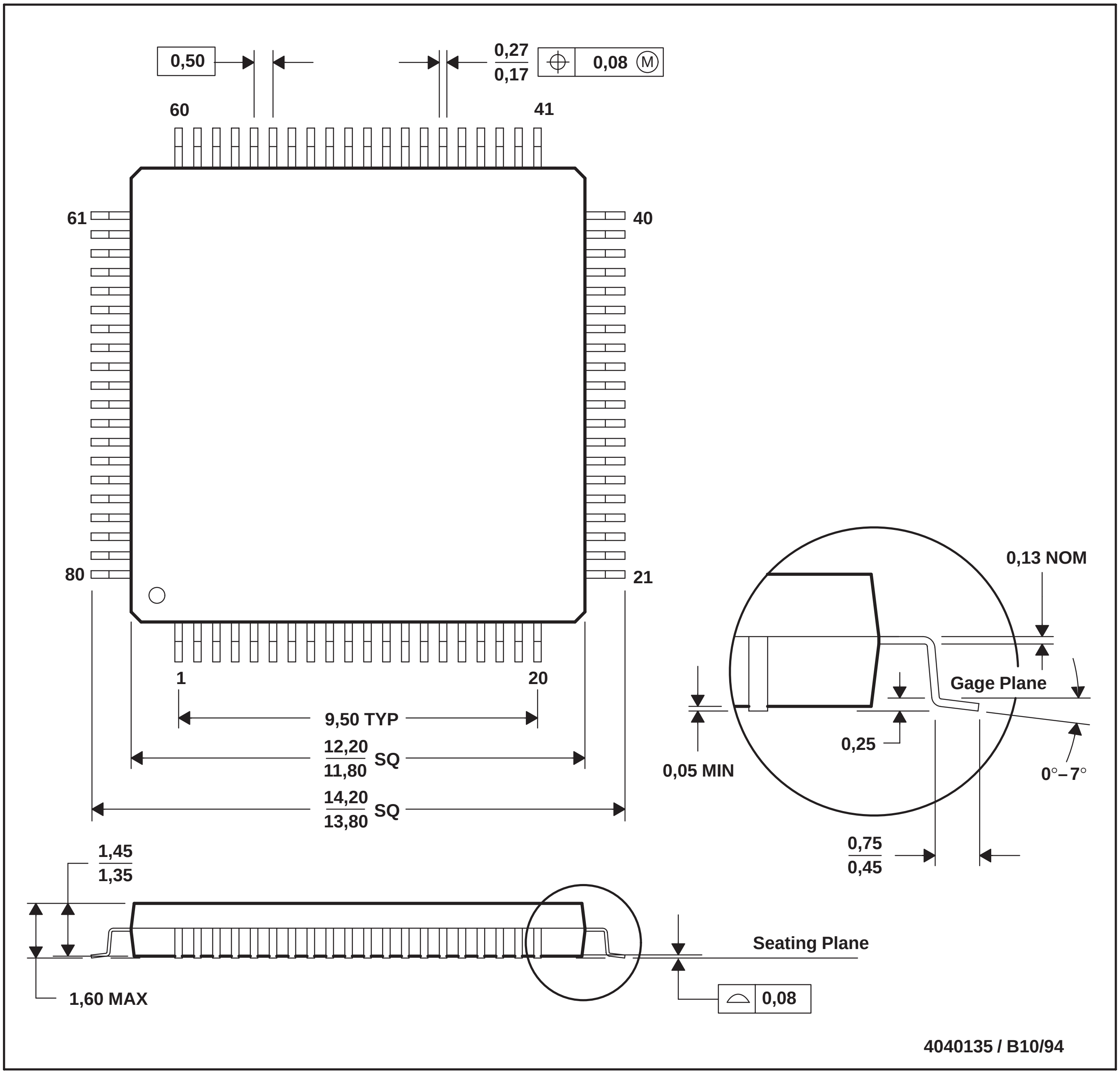
MECHANICAL DATA

PN (S-PQFP-G80) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136

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