CDB Device
Cell Delineation Block
TXC-05150

DATA SHEET
Preliminary

FEATURES

- ATM cell delineation per ITU I.432
- ATM cell rate adaptation
- Selectable cell output: FIFO, SARA, and UTOPIA (Universal Test & Operations Physical Interface for ATM)
- Identifies OAM F4 cells and non-user cells
- Operation from 1.544 Mbit/s to 155.52 Mbit/s
- Programmable interfaces to DS1, DS3, E1, STS-1, STS-3c, and STM-1
- DS3 interface with HEC-based mapping of ATM cells
- Interfaces with TranSwitch SOT-1, SOT-3, DS3F, JT2F and the SARA ATM chipset
- 0.7 µm low power CMOS technology
- 144-pin plastic quad flat pack (PQFP)
- IEEE 1149.1 boundary scan

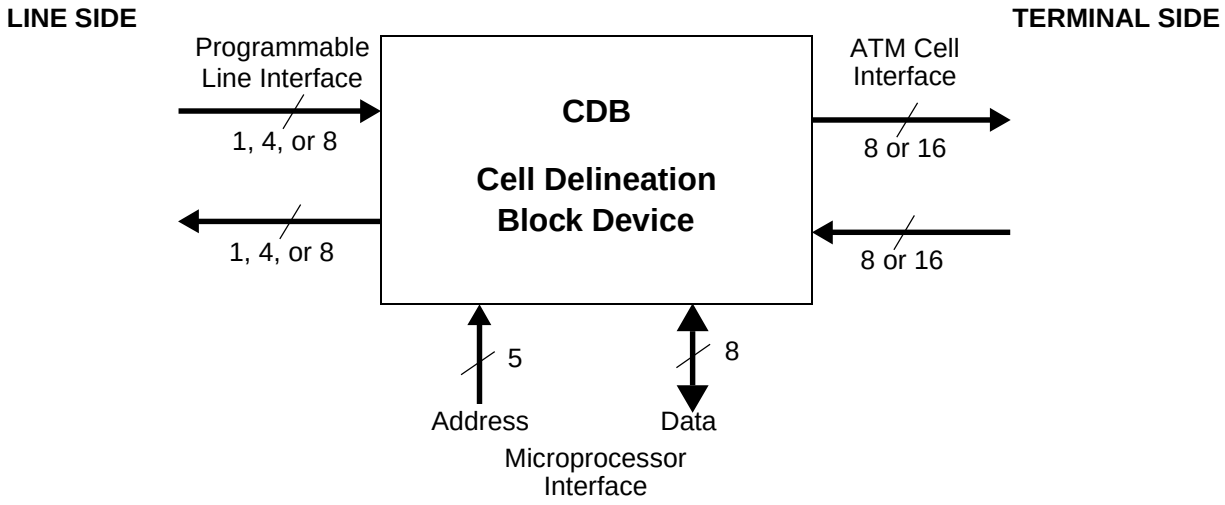
DESCRIPTION

The Cell Delineation Block (CDB) is an ATM cell interface device. The CDB function is to extract ATM cells from, and insert ATM cells into, a line interface signal having one of several possible transmission formats. This function corresponds to portions of the Transmission Convergence (TC) sublayer and the ATM Layer in the BISDN Protocol Reference Model. Specifically, cell delineation is performed by means of a Header Error Control (HEC) byte search. Cell rate adaptation is also performed by generating and terminating unassigned ATM cells of a specified format.

The CDB also supports a limited cell address screening function. A programmable VPI/VCI number register and VPI/VCI mask register are provided. Each incoming cell with address matching in all VPI/VCI bit positions which are not masked will generate an "Address Match" indication.

APPLICATIONS

- ATM switch interfaces
- ATM terminal adapters
- Cell multiplexers
- Routers and bridges



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BLOCK DIAGRAM

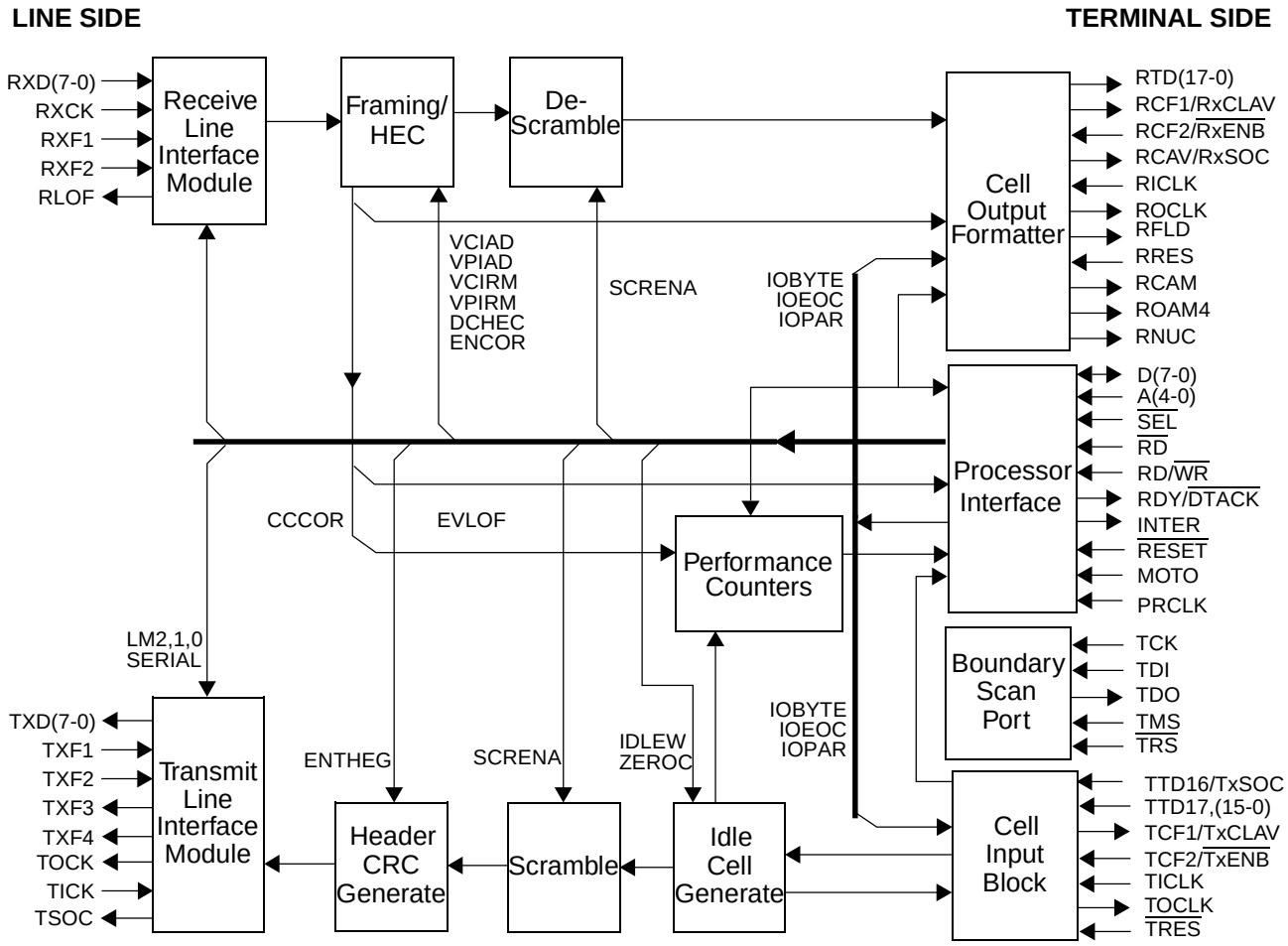


Figure 1. CDB Block Diagram

BLOCK DIAGRAM DESCRIPTION

Receive Path

The Cell Delineation Block (CDB) block diagram is shown in Figure 1. The receive line interface of the CDB accepts data from the line in one of several formats. The device then finds cell framing by searching for a valid Header Error Control (HEC) sequence. The extracted cells are optionally descrambled and passed to the cell output formatter which can interface to an ATM switch, cell bus, or adaptation layer functionality. Performance counters maintain counts of busy cells received. Idle cells are identified and may be dropped. Incoming cell headers are checked for the presence of either an OAM F4 flow cell or a non-user cell (e.g., OAM F5 flow cell). An OAM F4 flow cell is defined by a VCI value equal to either 3 decimal or 4 decimal. An OAM F5 cell is defined as a cell with the MSB of the 3-bit Payload Type Indication (PTI) field set to "1".

The CDB also provides a limited cell address screening function. A 28-bit programmable VPI/VCI number register and VPI/VCI mask register are provided. Each incoming cell with address matching in all VPI and VCI bit positions which are not masked out will generate an address match indication.

Transmit Path

The ATM terminal passes cells to the cell input block to be transmitted through the line interface. The device counts busy cells and generates idle cells to adapt the cell rate to the line interface. The 48-byte cell payload may optionally be scrambled and a HEC byte calculated prior to sending the cell to the transmit line interface.

Line Interface

The CDB supports cell delineation and cell rate adaptation with the following line rates and associated line framing devices:

Transmission Standard	Line Rate	Interface Device
STS-3c, STM-1	155.52 Mbit/s	TXC-03003 (SOT-3)
STS-1	51.840 Mbit/s	TXC-03001 (SOT-1)
DS3	44.736 Mbit/s	TXC-03401 (DS3F, direct mapping only)
DS1	1.544 Mbit/s	Various standard devices
E1	2.048 Mbit/s	Various standard devices

The CDB also supports alternate physical interfaces at different rates, having byte, nibble parallel, or bit serial inputs and byte alignment.

Cell Interface

Cells are transferred between the CDB and a terminal device in one of four modes:

External FIFO	Supports the use of external synchronous FIFO for both the cell output formatter and the cell input.
Internal FIFO	The CDB internally emulates synchronous FIFO, both on the cell output formatter and the cell input.
SARA	Direct connection to the TranSwitch SARA ATM/AAL chipset.
UTOPIA	The CDB supports a fully compliant UTOPIA interface on the cell I/O. This includes timing standards and pin designations.

The cell output formatter includes control signals for cell timing as well as indicators for special cell types. OAM F4 flow cells are output with a ROAM4 indication. Non-user cells are output with a RNUC indication. Cells matching the programmed VPI/VCI value or range of values are output with a RCAM indication. The cell output formatter and cell input data lines can be configured for either 8-bits or 16-bits wide to interface with various ATM/AAL circuitry.

Microprocessor Interface

Access to the CDB registers is provided by the microprocessor interface consisting of an 8-bit data bus, 5-bit address bus, and control signals. The interface can be configured for Intel or Motorola processors, and it uses an independent processor clock for the interface.

PIN DIAGRAM

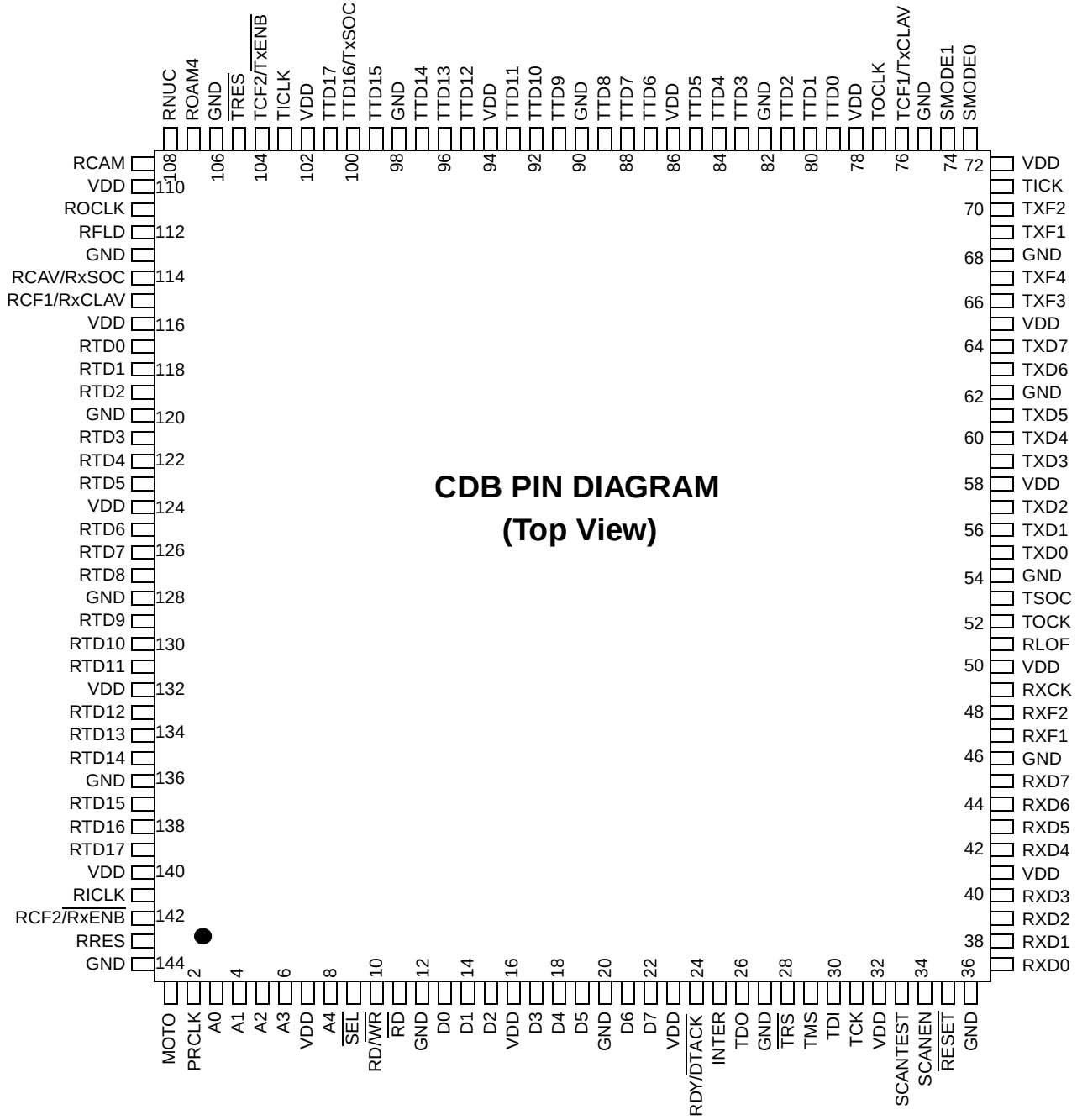


Figure 2. CDB Pin Diagram With Names and Numbers

PIN DESCRIPTIONS

Power Supply and Ground:

Symbol	Pin No.	I/O/P*	Type	Name/Function
VDD	7, 16, 23, 32, 41, 50, 58, 65, 72, 78, 86, 94, 102, 110, 116, 124, 132, 140	P		**VDD:** +5-volt supply, ±5%
GND	12, 20, 27, 36, 46, 54, 62, 68, 75, 82, 90, 98, 106, 113, 120, 128, 136,144	P		**Ground.**

*Note: I = Input; O = Output; P = Power

Microprocessor Interface

Symbol	Pin No.	I/O/P	Type *	Name/Function
MOTO	1	I	TTL	**Motorola/Intel Processor Select:** = 1 selects Motorola mode, = 0 selects Intel mode.
A(3-0) A4	6-3 8	I	TTL	**Address Bus:** Read/write address for microprocessor interface.
$\overline{SEL}$	9	I	TTL	**Select:** A low enables data transfers between the microprocessor and the CDB RAM during a read/write cycle.
RD/$\overline{WR}$	10	I	TTL	**Read/Write (Motorola Mode) or Write (Intel mode):** Motorola Mode - An active high signal generated by the microprocessor for reading the RAM locations. An active low signal is used to write to RAM locations. Intel Mode - An active low signal generated by the microprocessor for writing to the CDB RAM locations.
$\overline{RD}$	11	I	TTL	**Read (Intel mode):** An active low signal generated by the microprocessor for reading the RAM locations.
D(2-0) D(5-3) D(7-6)	15-13 19-17 22-21	I/O	TTL	**Data Bus:** Data in or out. These bidirectional data lines are used to transfer data between the CDB and the microprocessor.

*See Input, Output and I/O Parameters section below for Type definitions.

Symbol	Pin No.	I/O/P	Type	Name/Function
RDY/ DTACK	24	O	CMOS Open drain	**Ready (Intel mode) or Data Transfer Acknowledgment (Motorola mode):** Intel Mode - A high is an acknowledgment from the addressed RAM location that the transfer can be completed. A low indicates that the CDB cannot complete the transfer cycle, and microprocessor wait states must be generated. Motorola Mode - During a read bus cycle, a low signal indicates the information on the data bus is valid. During a write bus cycle, a low signal acknowledges the acceptance of data.
INTER	25	O	CMOS4mA	**Interrupt:** Interrupt output. Intel Mode - active high. Motorola Mode - active low. This output sends an interrupt to the microprocessor.
RESET	35	I	TTL	**Reset:** A 100 nanosecond (minimum) low on this pin resets the processor interface and clears the performance counters to zero. Reset provides a complete power-up reset of the CDB, except for the boundary scan (see TRS pin below).
PRCLK	2	I	TTL	**Processor Clock:** Local clock for microprocessor bus interface. The maximum clock speed is 20 MHz.
SMODE0	73	I	TTL	**Synchronous Mode:** The connection of these pins to VDD or Ground (1 or 0) sets the operating mode of the CDB as shown in the following table:
SMODE1	74	I	TTL	

SMODE 1	SMODE 0	Interface Mode
0	0	External FIFO mode. CDB writes (RX side) and reads (TX side) cells to external synchronous FIFO.
0	1	Internal FIFO mode. CDB RX FIFO is read (RX) or written (TX) as a synchronous FIFO.
1	0	UTOPIA mode.
1	1	Direct SARA interface mode.

Line Input

Symbol	Pin No.	I/O/P	Type	Name/Function
RXD(3-0) RXD(7-4)	40-37 45-42	I	TTL	**Receive Line Data Input:** Line input bit serial data (DS1/E1, RXD0), nibble data (DS3, RXD(3-0)), byte data (STS-1 or STS-3c/STM-1, RXD(7-0)).

Symbol	Pin No.	I/O/P	Type	Name/Function
RXF1*	47	I	TTL	**Receive Line Frame Indication 1:** RSPE if SOT-3 or SOT-1 Frame sync if DS3 Frame sync if DS1/E1.
RXF2*	48	I	TTL	**Receive Line Frame Indication 2:** RPOH if SOT-3 RSYN if SOT-1.
RXCK	49	I	TTL	**Receive Line Clock in:** Line input clock.
RLOF	51	O	CMOS4mA	**Receive Line Loss of Frame:** High if loss of cell synchronization.

* Note: Tie to ground or VDD if not used.

Line Output

Symbol	Pin No.	I/O/P	Type	Name/Function
TOCK	52	O	CMOS4mA	**Transmit Line Output Clock:** Transmit output clock for SOT-1.
TSOC	53	O	CMOS4mA	**Transmit Start of Cell Indication:** High during first byte of a transmitted cell.
TXD(2-0) TXD(5-3) TXD(7-6)	57-55 61-59 64-63	O	CMOS4mA	**Transmit Line Data Out:** Line output bit serial data (DS1/E1, TXD0), nibble data (DS3, TXD(3-0)), byte data (STS-1 or STS-3c/STM-1, TXD(7-0)).
TXF3	66	O	CMOS4mA	**Transmit Line SPE Indication:** TSPE for SOT-1.
TXF4	67	O	CMOS4mA	**Transmit Line SYN Indication:** TSYN (C1J1) for SOT-1.
TXF1*	69	I	TTL	**Transmit Line Frame Indication:** Transmit TSPE if SOT-3 Transmit frame if DS3 Transmit frame if DS1/E1.
TXF2*	70	I	TTL	**Transmit Line POH Indication:** Transmit TPOH if SOT-3.
TICK	71	I	TTL	**Transmit Line REF Clock:** Input clock for transmit side data output.

* Note: Tie to ground or VDD if not used.

Cell Output

Symbol	Pin No.	I/O/P	Type	Name/Function
ROAM4	107	O	CMOS4mA	**Receive Terminal OAM F4 Indication:** High during entire cell if OAM F4 flow cell.
RNUC	108	O	CMOS4mA	**Receive Terminal Non-user Indication:** High during entire cell if non-user type cell.

Symbol	Pin No.	I/O/P	Type	Name/Function
RCAM	109	O	CMOS4mA	**Receive Cell Address Match Indication:** High during entire cell, if both VPI and VCI values are declared matched.
ROCLK	111	O	CMOS4mA	**Receive Terminal Clock Output:** Output clock in external FIFO mode.
RFLD	112	O	CMOS4mA	**Receive Terminal Flush Indication:** Flush done to SARA-R.
RCAV/ RxSOC	114	O	CMOS4mA	**Receive Terminal Cell Available Indication:** Cell available in SARA mode, Receive Start of Cell in UTOPIA mode.
RCF1/ RxCLAV	115	O	CMOS4mA	**Receive Terminal Control Line 1:** Write enable if external FIFO mode (RCF1 active low) FIFO empty if internal FIFO mode (RCF1 active low) FIFO empty if SARA mode (RCF1 active high) Complete cell available for transfer in UTOPIA mode (RxCLAV active high).
RTD(2-0) RTD(5-3) RTD(8-6) RTD(11-9) RTD(14-12) RTD(17-15)	119-117 123-121 127-125 131-129 135-133 139-137	O	CMOS4mA	**Receive Terminal Data Out:** Received data and parity. In the byte mode, RTD (7-0) are data and RTD (8) is an even parity / start of cell indicator. In the word mode, RTD (15-0) are data and RTD (17,16) are even parity / start of cell indicators. If the UTOPIA mode is active, odd parity is provided, but start of cell is on pin 114, RCAV/RxSOC.
RICLK	141	I	TTL	**Receive Input Clock:** Read FIFO input clock. Its maximum frequency is 20 MHz.
$\overline{\text{RCF2}}$/ $\overline{\text{RxENB}}$	142	I	TTL	**Receive Terminal Control Line 2:** FIFO almost full input if external FIFO mode (RCF2 active low) Read enable input if internal FIFO mode (RCF2 active low) Read enable from SARA-R if SARA mode (RCF2 active high) Read enable in UTOPIA mode ($\overline{\text{RxENB}}$ active low).
RRES	143	I	TTL	**Receive Terminal Reset:** Receive side cell reset clears the output FIFO. It must be high for at least 100 nanoseconds.

Cell Input

Symbol	Pin No.	I/O/P	Type	Name/Function
TCF1/ TxCLAV	76	O	CMOS4mA	**Transmit Terminal Control Line 1:** Read enable output, external FIFO mode (TCF1 active low) FIFO full output, internal FIFO mode (TCF1 active low) RDEN to SARA-S in SARA mode (TCF1 active high) Transmit Cell Available in UTOPIA mode (TxCLAV active high).
TOCLK	77	O	CMOS4mA	**Transmit Terminal Clock Output:** Read clock for external FIFO and SARA modes. Maximum frequency is 20 MHz.

Symbol	Pin No.	I/O/P	Type	Name/Function
TTD(2-0) TTD(5-3) TTD(8-6) TTD(11-9) TTD(14-12) TTD(17,15)	81-79 85-83 89-87 93-91 97-95 101,99	I	TTL	**Transmit Terminal Data In:** Transmit data and parity. In the byte mode, TTD (7-0) are data and TTD (8) is an even parity / start of cell indicator. In the word mode, TTD (15-0) are data and TTD (17,16) are even parity / start of cell indicators. If the UTOPIA mode is active, there is no parity on the CDB cell input and start of cell is provided on pin 100, TTD16/TxSOC.
TTD16/ TxSOC	100	I	TTL	**Transmit Terminal Data In**: Parity bit or start of cell in UTOPIA mode (TxSOC).
TICLK	103	I	TTL	**Transmit Input Clock:** Write clock internal FIFO mode. Maximum frequency is 20 MHz.
TCF2/ $\overline{\text{TxENB}}$	104	I	TTL	**Transmit Terminal Control Line 2:** FIFO almost empty input in external FIFO mode (TCF2 active low) Write enable in internal FIFO mode (TCF2 active low) CELAVL from SARA-S in SARA mode (TCF2 active low) Transmit Enable in UTOPIA mode ($\overline{\text{TxENB}}$ active low).
$\overline{\text{TRES}}$	105	I	TTL	**Transmit Terminal Reset:** Clears the input FIFOs. This signal must be low for at least 100 nanoseconds.

Boundary Scan and Test

Symbol	Pin No.	I/O/P	Type	Name/Function
TDO	26	O	CMOS4mA	**Test Data Output:** Data and test instructions from internal test registers output.
$\overline{\text{TRS}}$	28	I	TTLp	**Test Mode Reset:** A 100 nanosecond (minimum) low on this pin resets the boundary scan; recommended for power-up initialization as well.
TMS	29	I	TTLp	**Test Mode Select:** Mode select.
TDI	30	I	TTLp	**Test Data Input:** Data and test instruction input.
TCK	31	I	TTLp	**Test Clock:** Clock in signals on rising edge.
SCANTEST	33	I	TTLp	**Scan Test Select:** Scan test, tie low for normal operating conditions.
SCANEN	34	I	TTLp	**Scan Test Enable:** Scan enable, tie low for normal operating conditions.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	-0.3	7.0	V
DC input voltage	V_{IN}	-0.5	V_{DD} + 0.5	V
Continuous Power Dissipation	P_C			mW
Ambient operating temperature	T_A	-40	85	^oC
Operating junction temperature	T_J		150	^oC
Storage temperature range	T_S	-55	150	^oC

*Note: Operating conditions exceeding those listed in Absolute Maximum Ratings may cause permanent failure. Exposure to absolute maximum ratings for extended periods may impair device reliability.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal resistance - junction to ambient		43		$^oC/W$	

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	4.75	5.0	5.25	V	
I_{DD}		98		mA	
P_{DD}		490		mW	Inputs switching at 20 MHz

INPUT, OUTPUT AND I/O PARAMETERS

Input Parameters For TTL and TTLp*

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current		-1		µA	
Input capacitance		2.95		pF	

* The TTLp pins have internal 10KΩ pull-ups.

Output Parameters For CMOS4mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4			V	$V_{DD} = 4.75$; $I_{OH} = 4.0$
V_{OL}			0.5	V	$V_{DD} = 4.75$; $I_{OL} = -4.0$
I_{OL}			-4.0	mA	
I_{OH}			4.0	mA	
t_{RISE}		2.3		ns	$C_{LOAD} = 15pF$
t_{FALL}		3.3		ns	$C_{LOAD} = 15pF$

Output Parameters For CMOS Open Drain (4mA)

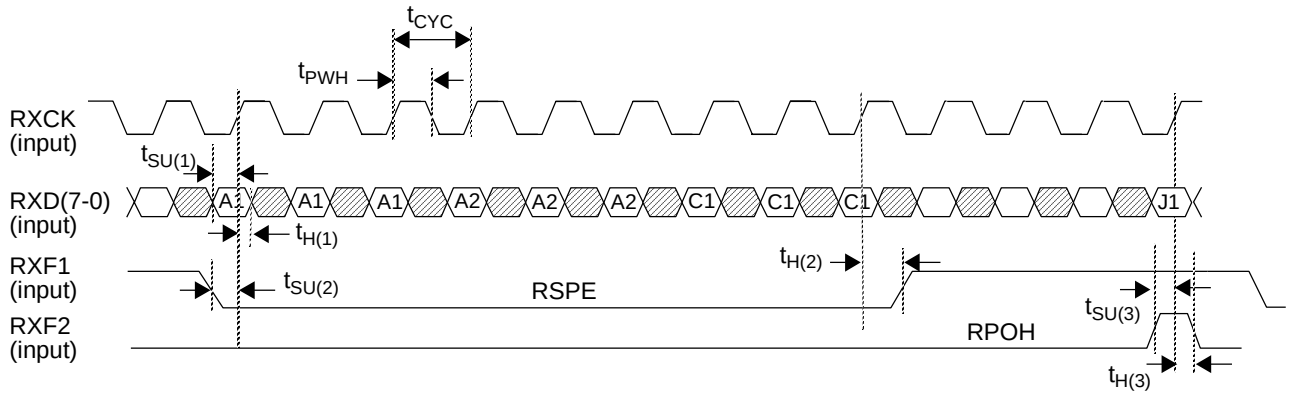
Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OL}			0.5	V	$V_{DD} = 4.75$; $I_{OL} = 4.0$
I_{OL}			4.0	mA	
t_{RISE}		0.8		ns	$C_{LOAD} = 15pF$
t_{FALL}		3.3		ns	$C_{LOAD} = 15pF$

Note: Open Drain requires use of 4.7 KOhm external pull-up resistor. If this resistor is not provided the output behaves as tristate, as shown in Figures 20-23.

TIMING CHARACTERISTICS

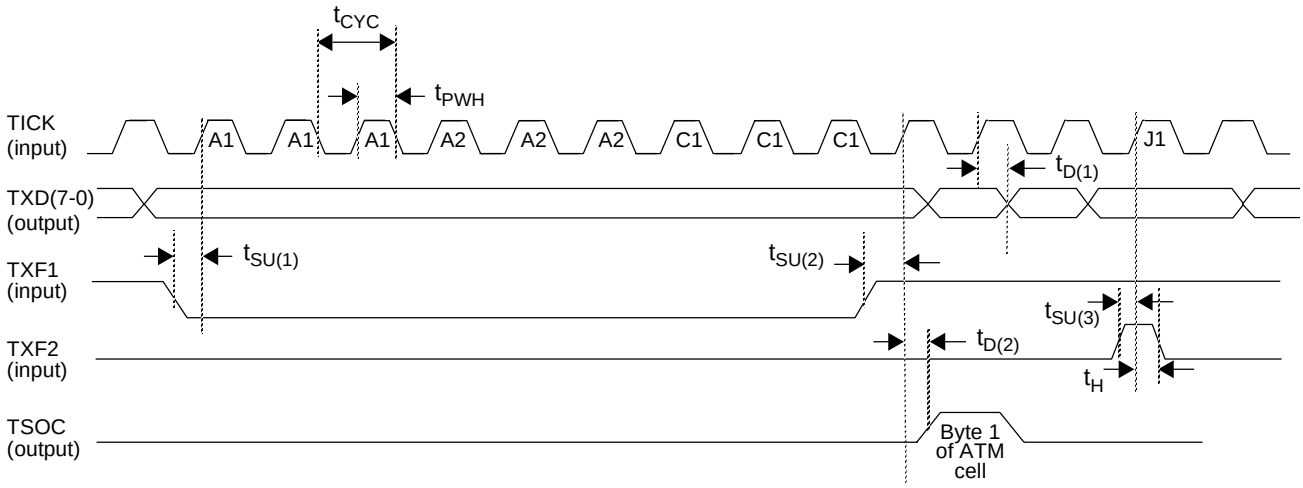
Detailed timing diagrams for the CDB are illustrated in Figures 3 through 23, with values of the timing intervals following each figure. All output times are measured with a maximum 25 pF load capacitance. Timing parameters are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

Figure 3. Receive Line Interface Timing, STS-3c/STM-1 Mode



Parameter	Symbol	Min	Typ	Max	Unit
RXCK clock period	t_{CYC}		51.4		ns
RXCK duty cycle, t_{PWH}/t_{CYC}	---	40		60	%
RXD(7-0) set-up time to RXCK↑	$t_{SU(1)}$	10			ns
RXD(7-0) hold time after RXCK↑	$t_{H(1)}$	4			ns
RXF1 set-up time to RXCK↑	$t_{SU(2)}$	10			ns
RXF1 hold time after RXCK↑	$t_{H(2)}$	4			ns
RXF2 set-up time to RXCK↑	$t_{SU(3)}$	10			ns
RXF2 hold time after RXCK↑	$t_{H(3)}$	4			ns

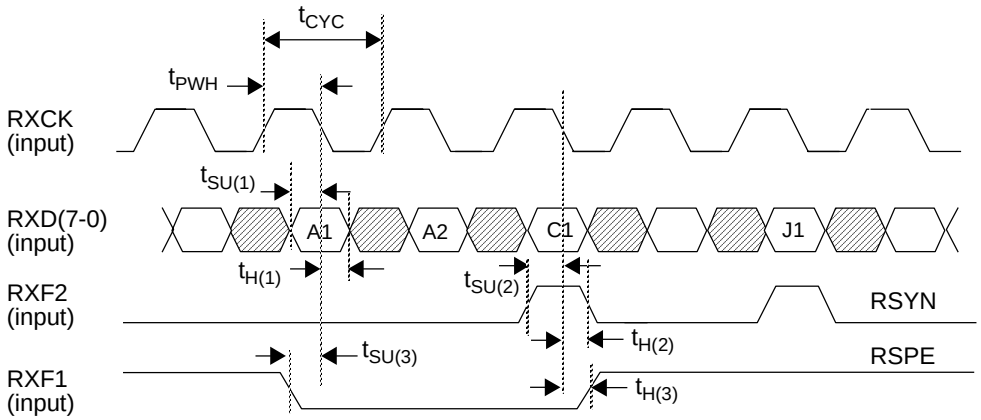
Figure 4. Transmit Line Interface Timing, STS-3c/STM-1 Mode



Parameter	Symbol	Min	Typ	Max	Unit
TICK clock period	t_{CYC}		51.4		ns
TICK duty cycle, t_{PWH}/t_{CYC}	---	40		60	%
TXF1 low set-up time to TICK↑	$t_{SU(1)}$	10			ns
TXF1 high set-up time to TICK↑	$t_{SU(2)}$	10			ns
TXD(7-0) delay after TICK↑	$t_{D(1)}$	4		20	ns
TXF2 set-up time to TICK↑	$t_{SU(3)}$	10			ns
TXF2 hold time after TICK↑	t_H	4			ns
TSOC delay after TICK↑	$t_{D(2)}$	4		20	ns

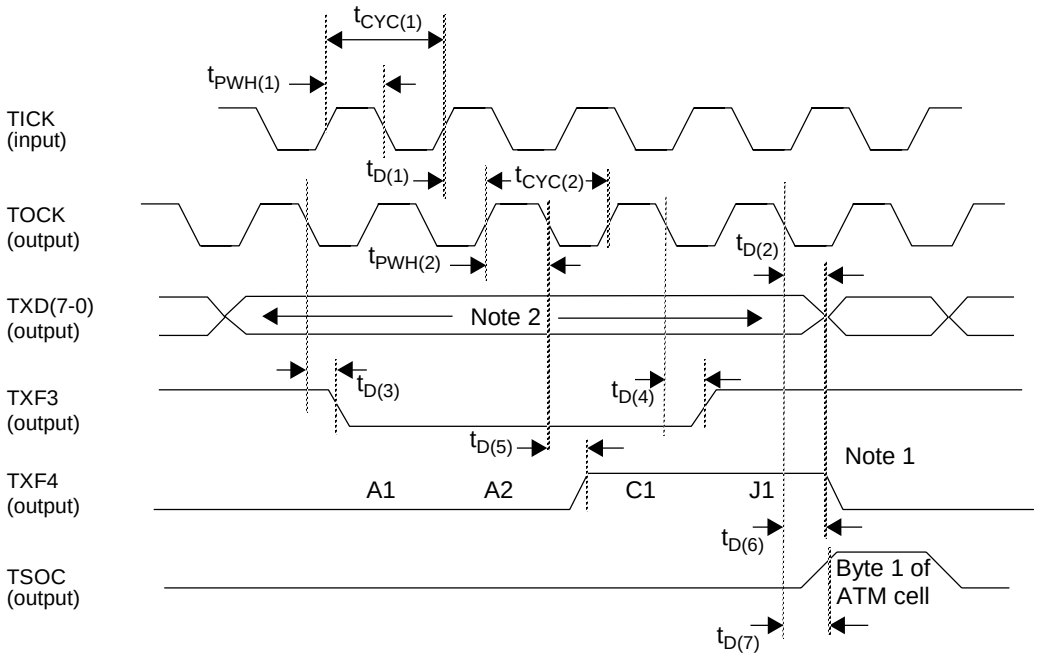
Note that TSOC (Transmit Start Of Cell) can occur anywhere in the output data with respect to the STS-3c /STM-1 frame. It is exactly one byte long and it is synchronous with the first byte of the output cell.

Figure 5. Receive Line Interface Timing, STS-1 Mode



Parameter	Symbol	Min	Typ	Max	Unit
RXCK clock period	t_{CYC}		154		ns
RXCK duty cycle, t_{PWH}/t_{CYC}	---	40		60	%
RXD(7-0) set-up time to RXCK↓	$t_{SU(1)}$	10			ns
RXD(7-0) hold time after RXCK↓	$t_{H(1)}$	4			ns
RXF2 set-up time to RXCK↓	$t_{SU(2)}$	10			ns
RXF2 hold time after RXCK↓	$t_{H(2)}$	4			ns
RXF1 set-up time to RXCK↓	$t_{SU(3)}$	10			ns
RXF1 hold time after RXCK↓	$t_{H(3)}$	4			ns

Figure 6. Transmit Line Interface Timing, STS-1 Mode

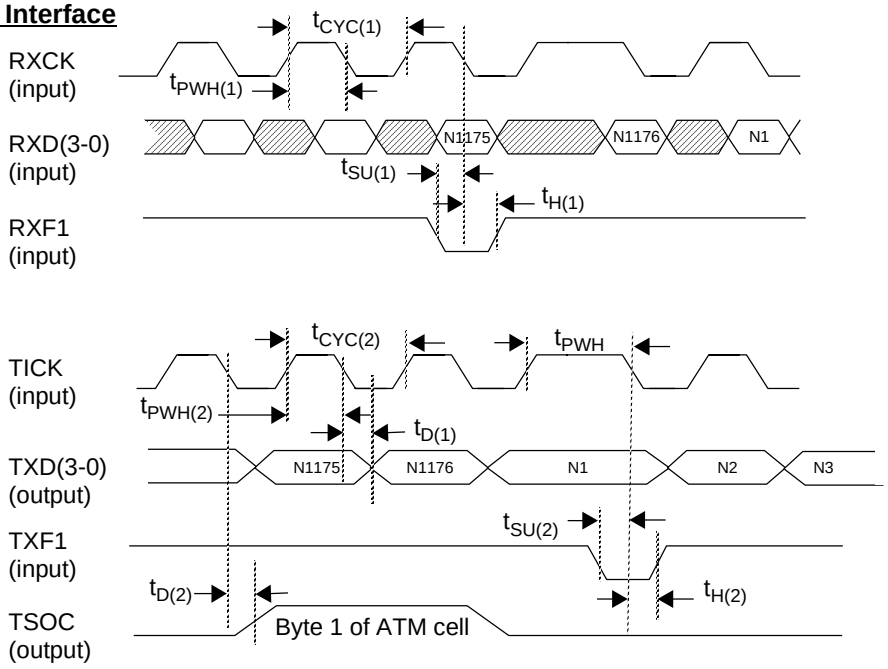


Parameter	Symbol	Min	Typ	Max	Unit
TICK clock period	$t_{CYC(1)}$		154		ns
TICK duty cycle, $t_{PWH(1)}/t_{CYC(1)}$	---	40		60	%
TOCK clock period	$t_{CYC(2)}$		154		ns
TOCK duty cycle, $t_{PWH(2)}/t_{CYC(2)}$	---	40		60	%
TOCK↑ delay after TICK↑	$t_{D(1)}$	3.0		12	ns
TXD(7-0) delay after TOCK↓	$t_{D(2)}$	0.5		6	ns
TXF3↓ delay after TOCK↓	$t_{D(3)}$	0.5		5	ns
TXF3↑ delay after TOCK↓	$t_{D(4)}$	0.5		5	ns
TXF4↑ delay after TOCK↓	$t_{D(5)}$	0.5		5	ns
TXF4↓ delay after TOCK↓	$t_{D(6)}$	0.5		5	ns
TSOC delay after TOCK↓	$t_{D(7)}$	1.5		7	ns

Note 1: TXF4 is only active high for C1 and J1.
Note 2: Regardless of TXF4, TXD(7-0) are held for 5 clock pulses.
Note 3: TSOC (Transmit Start of Cell) can occur anywhere in the output data with respect to the STS-1 frame. It is exactly one byte long and it is synchronous with the first byte of the output cell.

Figure 7. Receive/Transmit Line Interface Timing for DS3

DS3 Framer Interface

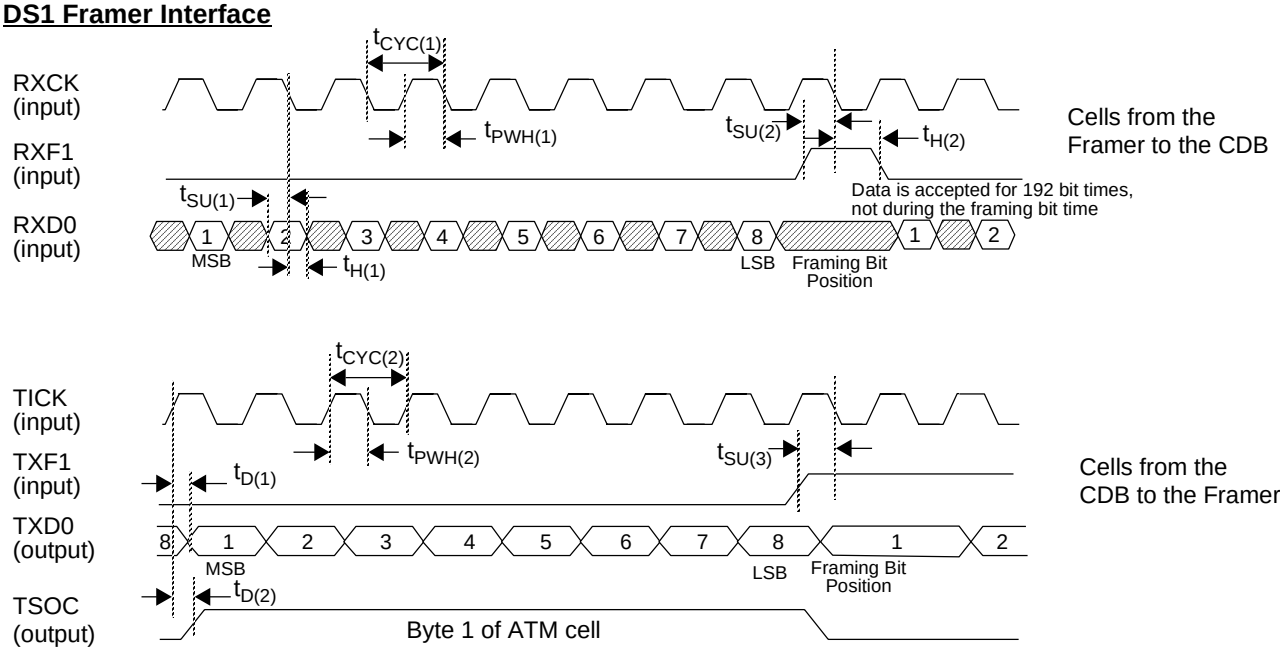


Parameter	Symbol	Min	Typ	Max	Unit
RXCK clock period	$t_{CYC(1)}$		89.4		ns
RXCK duty cycle, $t_{PWH(1)}/t_{CYC(1)}$	---	40		60	%
RXF1 set-up time to RXCK↓	$t_{SU(1)}$	10			ns
RXF1 hold time after RXCK↓	$t_{H(1)}$	4			ns
TICK clock period	$t_{CYC(2)}$		89.4		ns
TICK duty cycle, $t_{PWH(2)}/t_{CYC(2)}$	---	40		60	%
TICK long high time	t_{PWH}		67		ns
TXD(3-0) delay after TICK↓	$t_{D(1)}$	4		21	ns
TXF1 set-up time to TICK↓	$t_{SU(2)}$	10			ns
TXF1 hold time after TICK↓	$t_{H(2)}$	4			ns
TSOC delay after TICK↓	$t_{D(2)}$	4		21	ns

Note: The TSOC output is two nibbles (one byte) long. It indicates the first byte of the cell in the DS3 output. Should the first byte in the cell occur with a stretched clock (to account for DS3 overhead insertion), the TSOC will also be stretched. The TSOC output is synchronous with the output DS3 nibbles.

Figure 8a. Receive/Transmit Line Interface Timing for DS1

DS1 Framer Interface

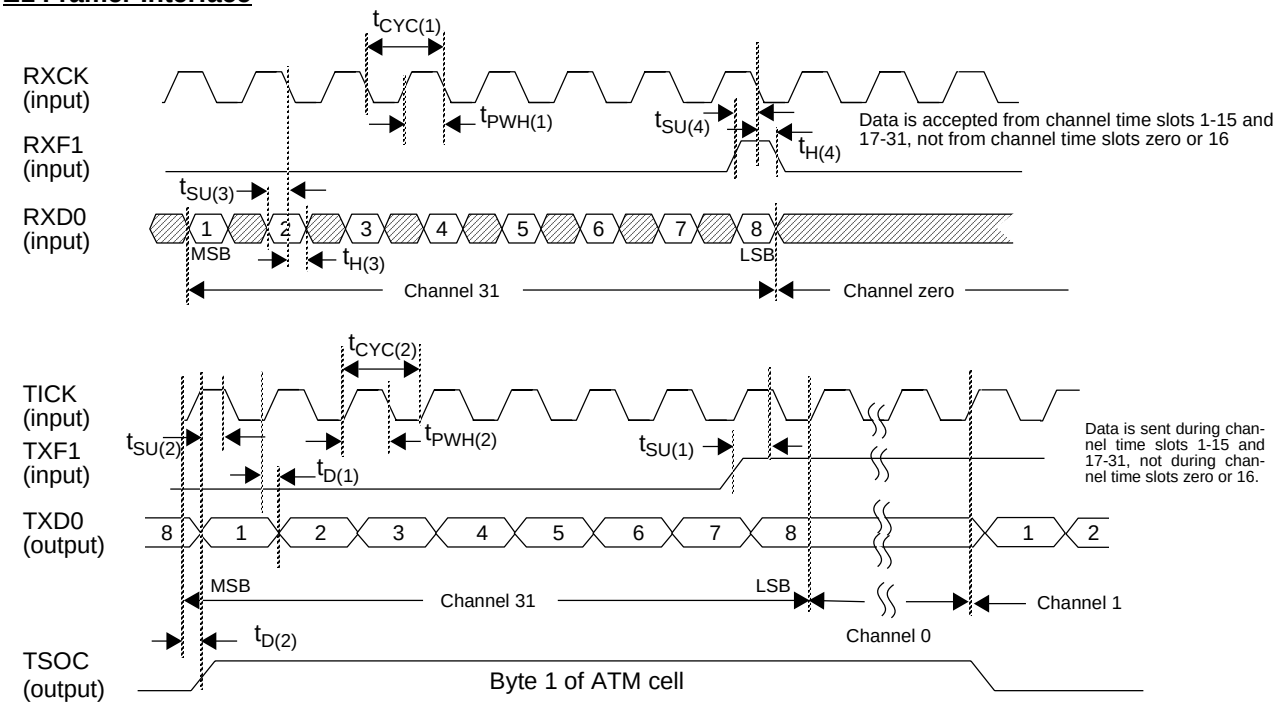


Parameter	Symbol	Min	Typ	Max	Unit
RXCK clock period	$t_{CYC(1)}$		648		ns
RXCK duty cycle, $t_{PWH(1)}/t_{CYC(1)}$	---	40		60	%
RXD0 set-up time to RXCK↓	$t_{SU(1)}$	10			ns
RXD0 hold time after RXCK↓	$t_{H(1)}$	4			ns
RXF1 set-up time to RXCK↓	$t_{SU(2)}$	10			ns
RXF1 hold time after RXCK↓	$t_{H(2)}$	4			ns
TICK clock period	$t_{CYC(2)}$		648		ns
TICK duty cycle, $t_{PWH(2)}/t_{CYC(2)}$	---	40		60	%
TXD0 delay after TICK↑	$t_{D(1)}$	4		20	ns
TXF1 set-up time to TICK↓	$t_{SU(3)}$	10			ns
TSOC delay after TICK↑	$t_{D(2)}$	4		20	ns

Note: The TSOC output is 8 bits (one byte) long. It indicates the first byte of the cell in the DS1 output, and it is synchronous with the DS1 bits.

Figure 8b. Receive/Transmit Line Interface Timing for E1

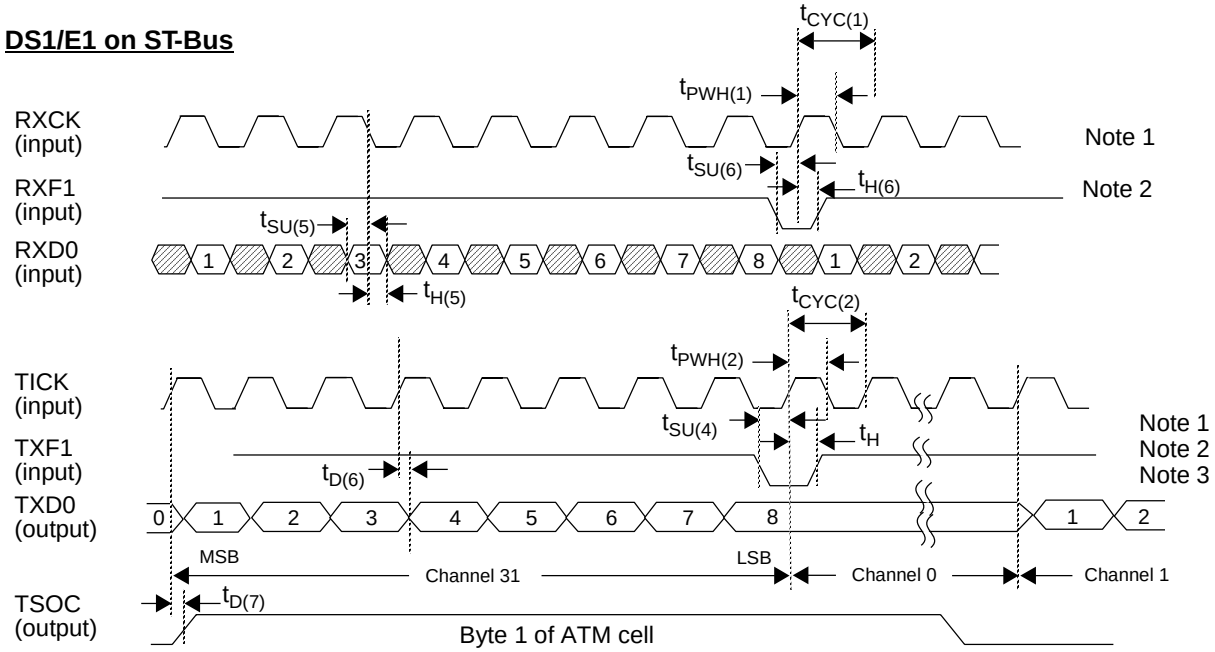
E1 Framer Interface



Parameter	Symbol	Min	Typ	Max	Unit
RXCK clock period	$t_{CYC(1)}$		488		ns
RXCK duty cycle, $t_{PWH(1)}/t_{CYC(1)}$	---	40		60	%
RXD0 set-up time to RXCK↓	$t_{SU(3)}$	10			ns
RXD0 hold time after RXCK↓	$t_{H(3)}$	4			ns
RXF1 set-up time to RXCK↓	$t_{SU(4)}$	10			ns
RXF1 hold time after RXCK↓	$t_{H(4)}$	4			ns
TICK clock period	$t_{CYC(2)}$		488		ns
TICK duty cycle, $t_{PWH(2)}/t_{CYC(2)}$	---	40		60	%
TXD0 delay after TICK↑	$t_{D(1)}$	4		20	ns
TXD0 set-up time to TICK↓	$t_{SU(2)}$	10			ns
TXF1 set-up time to TICK↓	$t_{SU(1)}$	10			ns
TSOC delay after TICK↑	$t_{D(2)}$	4		20	ns

Note: The TSOC output is 8 bits (one byte) long. It indicates the first byte of the cell in the E1 output, and it is synchronous with the E1 bits. Since the first byte of the cell in Figure 9 is in channel 31 of the E1 frame, the TSOC signal is extended over the channel 0 byte of the frame (the framing byte) to the beginning of the second byte of the cell in channel 1. It would also be extended over channel 16 should the first byte of the cell occur in channel 15. Otherwise, the TSOC signal is one byte long.

Figure 9. Receive/Transmit Timing for ST-Bus DS1/E1



E1 Channels on 2048 Kbit/s ST-Bus PCM Highway

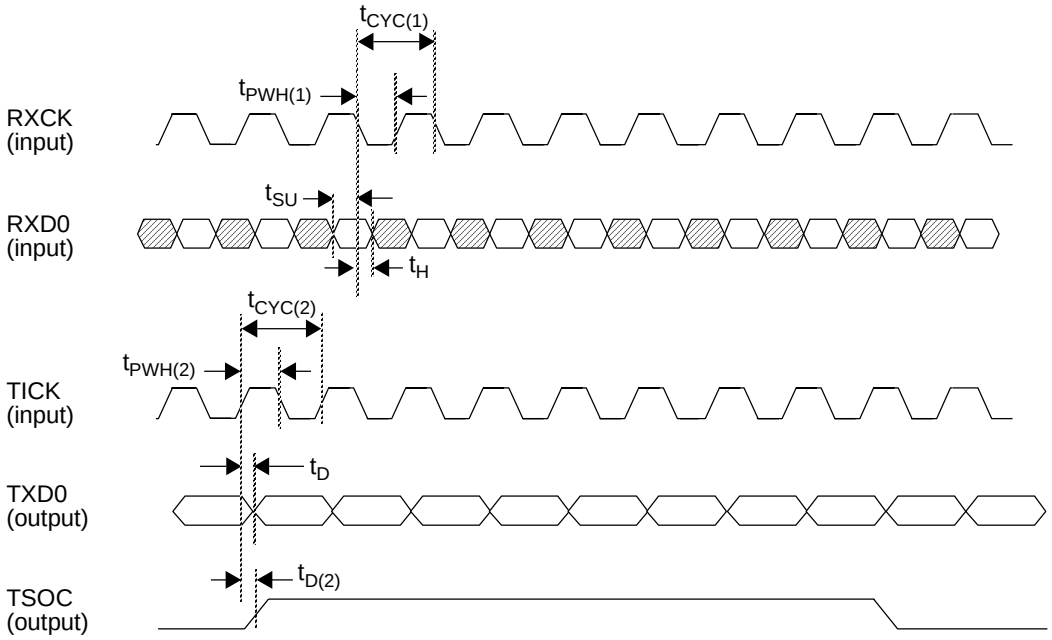
DX	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DS1		1	2	3		4	5	6		7	8	9		10	11	12		13	14	15		16	17	18		19	20	21		22	23	24

DS1 Channels on ST-Bus PCM Highway

Note 1: For DS1 data the CDB neither accepts nor sends for channel time slots 0, 4, 8, 12, 16, 20, 24 and 28.
Note 2: For E1 data the CDB neither accepts nor sends for channel time slots 0 and 16.
Note 3: The TSOC (Transmit Start Of Cell) signal on pin 53 is high during the first byte of an output cell for either DS1 or E1. The TSOC signal is synchronous with the first bit of the output byte and is held for 8 bits unless the first byte of the cell is just before an empty slot for DS1 or channel 0 or 15 of E1. In these cases, TSOC is held for 16 bits or 2 bytes to the start of the second byte of the output ATM cell.

Parameter	Symbol	Min	Typ	Max	Unit
RXCK clock period	$t_{CYC(1)}$		488		ns
RXCK duty cycle, $t_{PWH(1)}/t_{CYC(1)}$	---	40		60	%
RXD0 set-up time to RXCK↓	$t_{SU(5)}$	10			ns
RXD0 hold time after RXCK↓	$t_{H(5)}$	4			ns
RXF1 set-up time to RXCK↑	$t_{SU(6)}$	10			ns
RXF1 hold time after RXCK↑	$t_{H(6)}$	4			ns
TICK clock period	$t_{CYC(2)}$		488		ns
TICK duty cycle, $t_{PWH(2)}/t_{CYC(2)}$	---	40		60	%
TXD0 delay after TICK↑	$t_{D(6)}$	4		20	ns
TXF1 set-up time to TICK↑	$t_{SU(4)}$	10			ns
TXF1 hold time after TICK↑	t_{H}	4			ns
TSOC delay after TICK↑	$t_{D(7)}$	4		20	ns

Figure 10. Receive / Transmit Timing for Serial Mode Operation

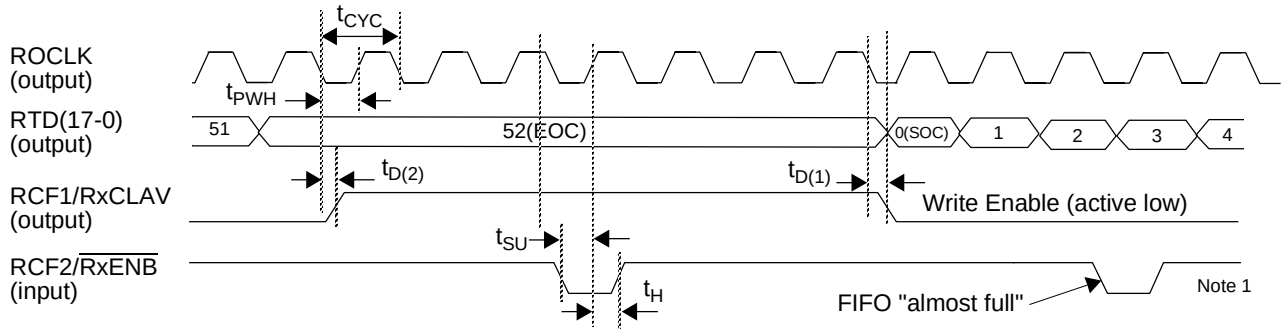


The maximum frequency of the two input clocks (RXCK and TICK) is 20 MHz.

All unused inputs (RXF1, RXF2, TXF1 and TXF2) must not be left open. It is preferred that they be taken to ground, though they can be taken to VDD. The CDB is unaffected by their state when it is operated in the serial mode.

Parameter	Symbol	Min	Typ	Max	Unit
RXCK clock period	$t_{CYC(1)}$		488		ns
RXCK duty cycle, $t_{PWH(1)}/t_{CYC(1)}$	---	40		60	%
RXD0 set-up time to RXCK↓	t_{SU}	10			ns
RXD0 hold time after RXCK↓	t_H	4			ns
TICK clock period	$t_{CYC(2)}$		488		ns
TICK duty cycle, $t_{PWH(2)}/t_{CYC(2)}$	---	40		60	%
TXD0 data change after TICK↑	t_D	4		20	ns
TSOC delay after TICK↑	$t_{D(2)}$	4		20	ns

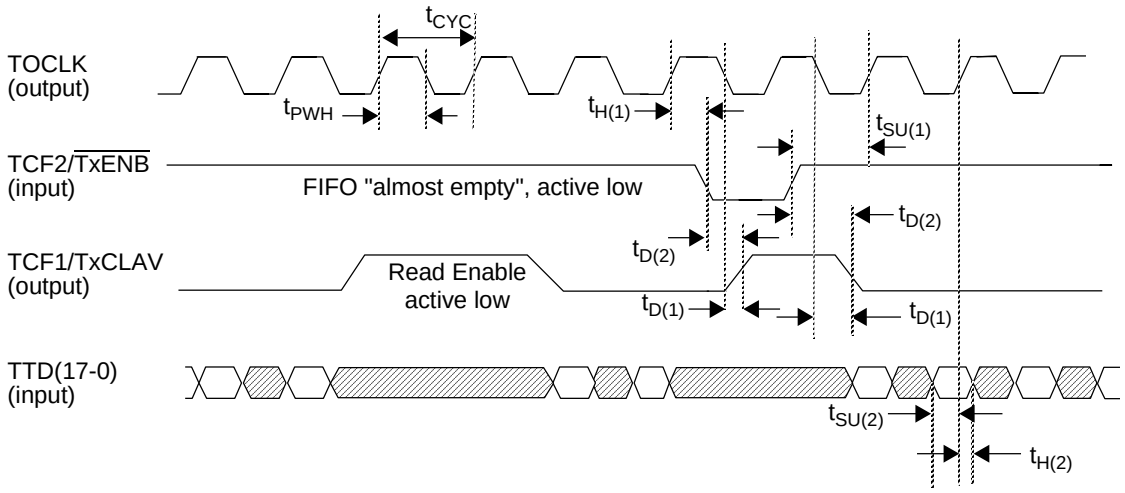
Figure 11. Cell Output Formatter Timing, External FIFO Mode



Parameter	Symbol	Min	Typ	Max	Unit
ROCLK clock period (DS1) ROCLK clock period (E1) ROCLK clock period (DS3) ROCLK clock period (STS-1) ROCLK clock period (STS-3c/STM-1)	t_{CYC}		648 488 89.4 154 51.4		ns
ROCLK duty cycle, t_{PWH}/t_{CYC}	---	40		60	%
RCF1/RxCLAV low delay after ROCLK↓	$t_{D(1)}$	-5		10	ns
RCF1/RxCLAV high delay after ROCLK↓	$t_{D(2)}$	-5		10	ns
RCF2/$\overline{\text{RxENB}}$ set-up time to ROCLK↑	t_{SU}	15			ns
RCF2/$\overline{\text{RxENB}}$ hold time after ROCLK↑	t_H	4			ns

Note 1: The CDB evaluates the status of RCF2/$\overline{\text{RxENB}}$ at the last byte of the current cell. Changes in RCF2/$\overline{\text{RxENB}}$ will not be detected during other byte times of a cell. CDB will only start writing a new cell when RCF2/$\overline{\text{RxENB}}$ is not active (low).

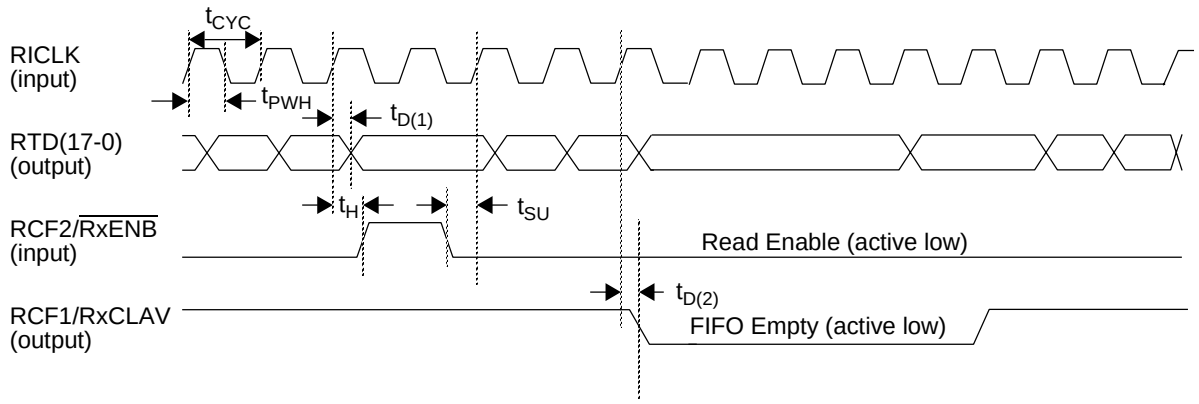
Figure 12. Cell Input Timing, External FIFO Mode



Parameter	Symbol	Min	Typ	Max	Unit
TOCLK clock period (DS1) TOCLK clock period (E1) TOCLK clock period (DS3) TOCLK clock period (STS-1) TOCLK clock period (STS-3c/STM-1)	t_{CYC}		648 488 89.4 154 51.4		ns
TOCLK duty cycle, t_{PWH}/t_{CYC}	---	40		60	%
TCF1/TxCLAV delay after TOCLK↓	$t_{D(1)}$	1		6*	ns
TCF1/TxCLAV delay after TCF2/$\overline{\text{TxENB}}$ valid	$t_{D(2)}$	5		17.5*	ns
TCF2/$\overline{\text{TxENB}}$ set-up time to TOCLK↑	$t_{SU(1)}$	25			ns
TCF2/$\overline{\text{TxENB}}$ hold time after TOCLK↑	$t_{H(1)}$	4			ns
TTD(17-0) set-up time to TOCLK↑	$t_{SU(2)}$	10			ns
TTD(17-0) hold time after TOCLK↑	$t_{H(2)}$	4			ns

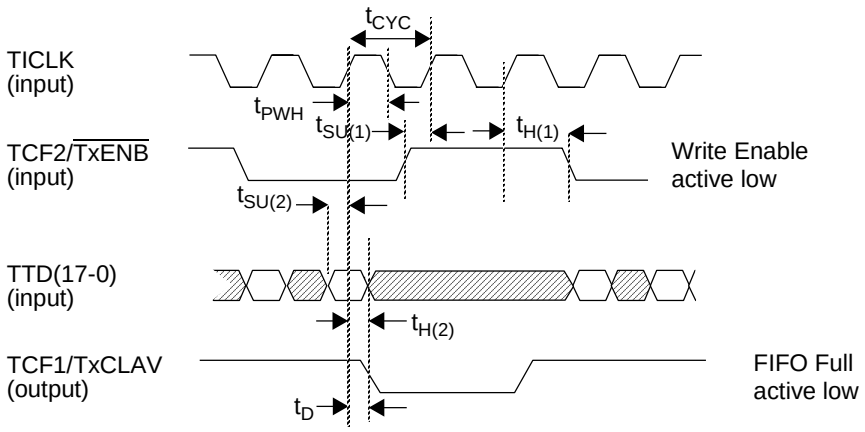
*Note: TCF1/TxCLAV is a combinatorial output of TCF2/$\overline{\text{TxENB}}$ and CDB internal logic. The delays mentioned above are based on how fast TCF2/$\overline{\text{TxENB}}$ changes state with reference to TOCLK edge. Hence, the maximum delay for TCF1/TxCLAV is either $t_{D(2)}$ max. after TCF2/$\overline{\text{TxENB}}$ changes state or $t_{D(1)}$ max. after falling edge of clock, whichever comes later.

Figure 13. Cell Output Formatter Timing, Internal FIFO Mode



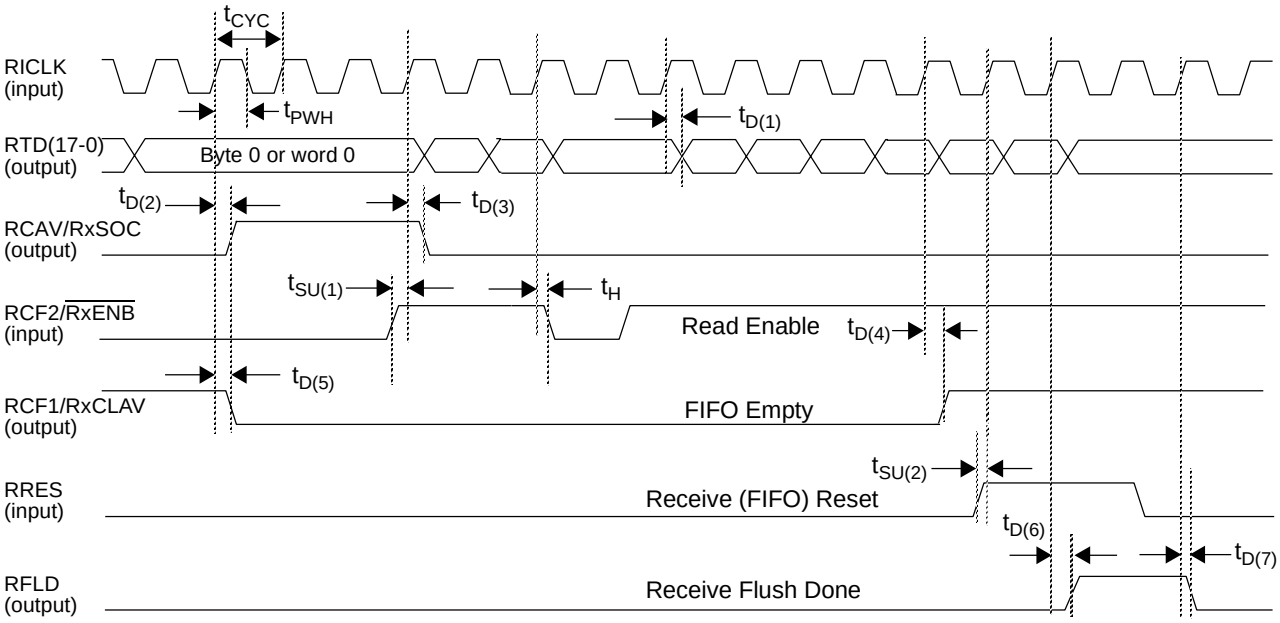
Parameter	Symbol	Min	Typ	Max	Unit
RICLK clock period (DS1) RICLK clock period (E1) RICLK clock period (DS3) RICLK clock period (STS-1) RICLK clock period (STS-3c/STM-1)	t_{CYC}		648 488 89.4 154 51.4		ns
RICLK duty cycle, t_{PWH}/t_{CYC}	---	40		60	%
RTD(17-0) delay after RICLK↑	$t_{D(1)}$	4		22	ns
RCF2/$\overline{\text{RxENB}}$ low set-up time to RICLK↑	t_{SU}	15			ns
RCF2/$\overline{\text{RxENB}}$ low hold time after RICLK↑	t_H	4			ns
RCF1/RxCLAV delay after RICLK↑	$t_{D(2)}$	4		23	ns

Figure 14. Cell Input Timing, Internal FIFO Mode



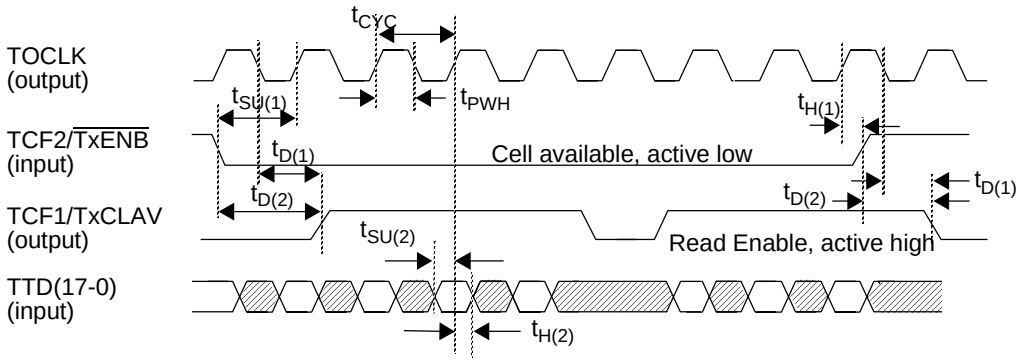
Parameter	Symbol	Min	Typ	Max	Unit
TICLK clock period (DS1) TICLK clock period (E1) TICLK clock period (DS3) TICLK clock period (STS-1) TICLK clock period (STS-3c/STM-1)	t_{CYC}		648 488 89.4 154 51.4		ns
TICLK duty cycle, t_{PWH}/t_{CYC}	---	40		60	%
TCF2/$\overline{\text{TxENB}}$ set-up time to TICLK↑	$t_{SU(1)}$	11			ns
TCF2/$\overline{\text{TxENB}}$ hold time after TICLK↑	$t_{H(1)}$	4			ns
TTD(17-0) set-up time to TICLK↑	$t_{SU(2)}$	10			ns
TTD(17-0) hold time after TICLK↑	$t_{H(2)}$	4			ns
TCF1/TxCLAV delay after TICLK↑	t_D	4		22	ns

Figure 15. Cell Output Formatter Timing, SARA Mode



Parameter	Symbol	Min	Typ	Max	Unit
RICLK clock period	t_{CYC}	51.4		648	ns
RICLK duty cycle, t_{PWH}/t_{CYC}	---	40		60	%
RTD(17-0) delay after RICLK↑	$t_{D(1)}$	5		22	ns
RCAV/RxSOC high delay after RICLK↑	$t_{D(2)}$	5		22	ns
RCAV/RxSOC low delay after RICLK↑	$t_{D(3)}$	5		22	ns
RCF2/$\overline{\text{RxENB}}$ set-up time to RICLK↑	$t_{SU(1)}$	15			ns
RCF2/$\overline{\text{RxENB}}$ hold time after RICLK↑	t_H	4			ns
RCF1/RxCLAV high delay after RICLK↑	$t_{D(4)}$	5		23	ns
RCF1/RxCLAV low delay after RICLK↑	$t_{D(5)}$	5		23	ns
RRES set-up time to RICLK↑	$t_{SU(2)}$	10			ns
RFLD high delay after RICLK↑	$t_{D(6)}$	5		21	ns
RFLD low delay after RICLK↑	$t_{D(7)}$	5		21	ns

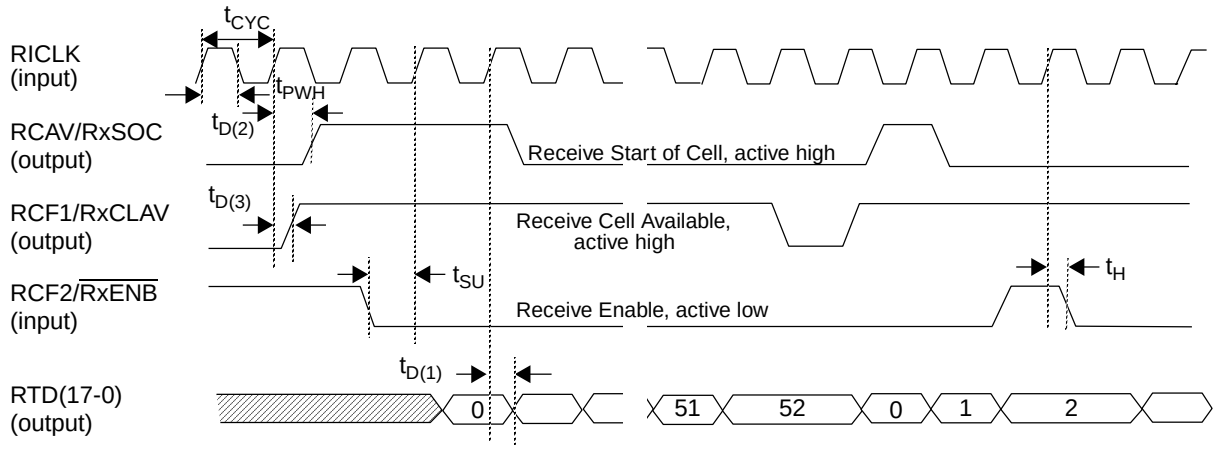
Figure 16. Cell Input Timing, SARA Mode



Parameter	Symbol	Min	Typ	Max	Unit
TOCLK clock period (DS1) TOCLK clock period (E1) TOCLK clock period (DS3) TOCLK clock period (STS-1) TOCLK clock period (STS-3c/STM-1)	t_{CYC}		648 488 89.4 154 51.4		ns
TOCLK duty cycle, t_{PWH}/t_{CYC}	---	40		60	%
TCF1/TxCLAV delay after TOCLK↓	$t_{D(1)}$	1		6*	ns
TCF1/TxCLAV delay after TCF2/$\overline{\text{TxENB}}$ valid	$t_{D(2)}$	5		17.5*	ns
TCF2/$\overline{\text{TxENB}}$ set-up time to TOCLK↑	$t_{SU(1)}$	25			ns
TCF2/$\overline{\text{TxENB}}$ hold time after TOCLK↑	$t_{H(1)}$	4			ns
TTD(17-0) set-up time to TOCLK↑	$t_{SU(2)}$	25			ns
TTD(17-0) hold time after TOCLK↑	$t_{H(2)}$	4			ns

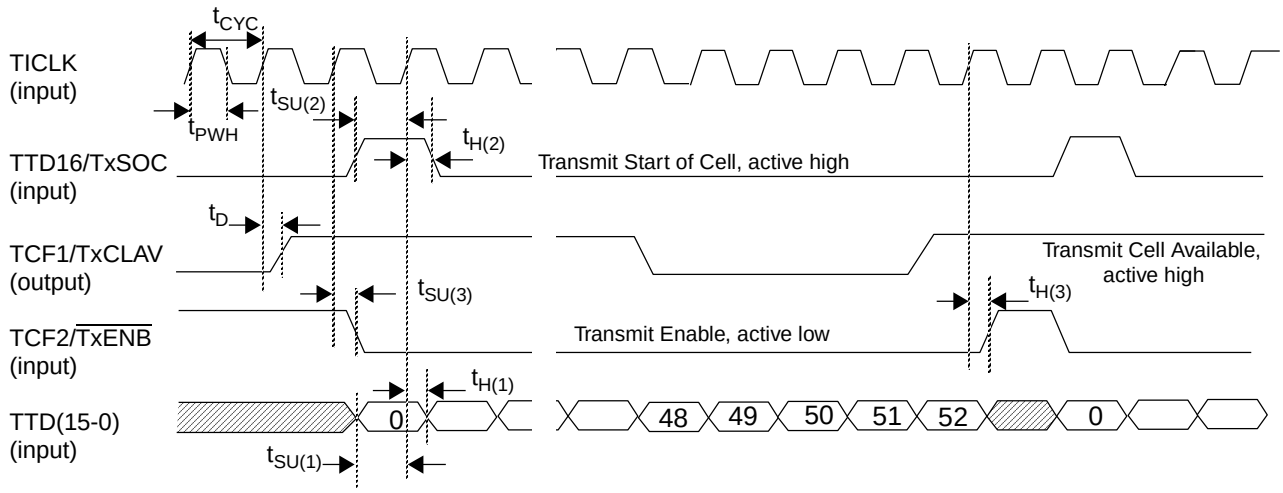
*Note: TCF1/TxCLAV is a combinatorial output of TCF2/$\overline{\text{TxENB}}$ and CDB internal logic. The delays mentioned above are based on how fast TCF2/$\overline{\text{TxENB}}$ changes state with reference to TOCLK edge. Hence, the maximum delay for TCF1/TxCLAV is either $t_{D(2)}$ max. after TCF2/$\overline{\text{TxENB}}$ changes state or $t_{D(1)}$ max. after falling edge of clock, whichever comes later.

Figure 17. Cell Output Timing, UTOPIA Mode



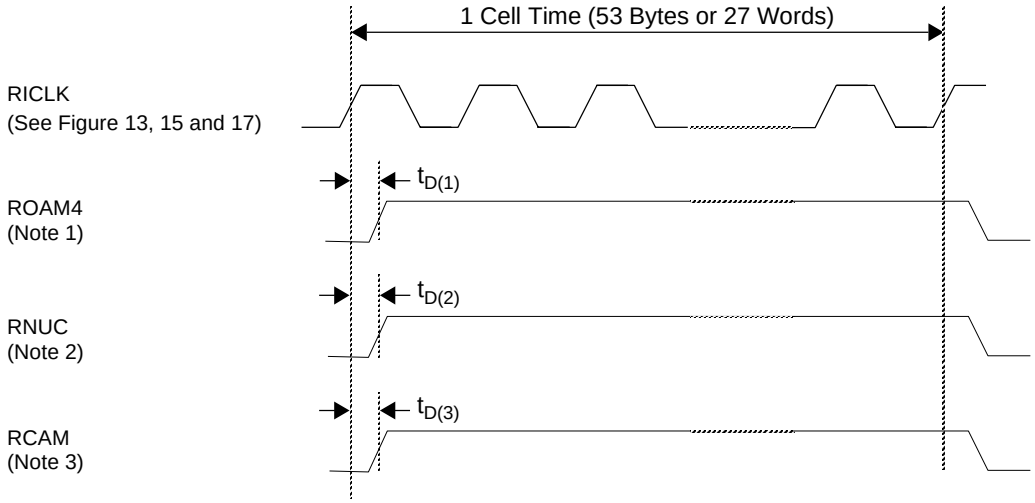
Parameter	Symbol	Min	Typ	Max	Unit
RICLK clock period (DS1) RICLK clock period (E1) RICLK clock period (DS3) RICLK clock period (STS-1) RICLK clock period (STS-3c/STM-1)	t_{CYC}		648 488 89.4 154 51.4		ns
RICLK duty cycle, t_{PWH}/t_{CYC}	---	40		60	%
RTD(17-0) delay after RICLK↑	$t_{D(1)}$	4		22	ns
RCAV/RxSOC delay after RICLK↑	$t_{D(2)}$	4		22	ns
RCF1/RxCLAV delay after RICLK↑	$t_{D(3)}$	4		23	ns
RCF2/$\overline{\text{RxENB}}$ set-up time to RICLK↑	t_{SU}	10			ns
RCF2/$\overline{\text{RxENB}}$ hold time after RICLK↑	t_H	4			ns

Figure 18. Cell Input Timing, UTOPIA Mode



Parameter	Symbol	Min	Typ	Max	Unit
TICLK clock period (DS1) TICLK clock period (E1) TICLK clock period (DS3) TICLK clock period (STS-1) TICLK clock period (STS-3c/STM-1)	t_{CYC}		648 488 89.4 154 51.4		ns
TICLK duty cycle, t_{PWH}/t_{CYC}	---	40		60	%
TTD(15-0) set-up time to TICLK↑	$t_{SU(1)}$	10			ns
TTD(15-0) hold time after TICLK↑	$t_{H(1)}$	1			ns
TTD16/TxSOC set-up time to TICLK↑	$t_{SU(2)}$	10			ns
TTD16/TxSOC hold time after TICLK↑	$t_{H(2)}$	1			ns
TCF2/$\overline{\text{TxENB}}$ set-up time to TICLK↑	$t_{SU(3)}$	10			ns
TCF2/$\overline{\text{TxENB}}$ hold time after TICLK↑	$t_{H(3)}$	1			ns
TCF1/TxCLAV delay from TICLK↑	t_D	4		22	ns

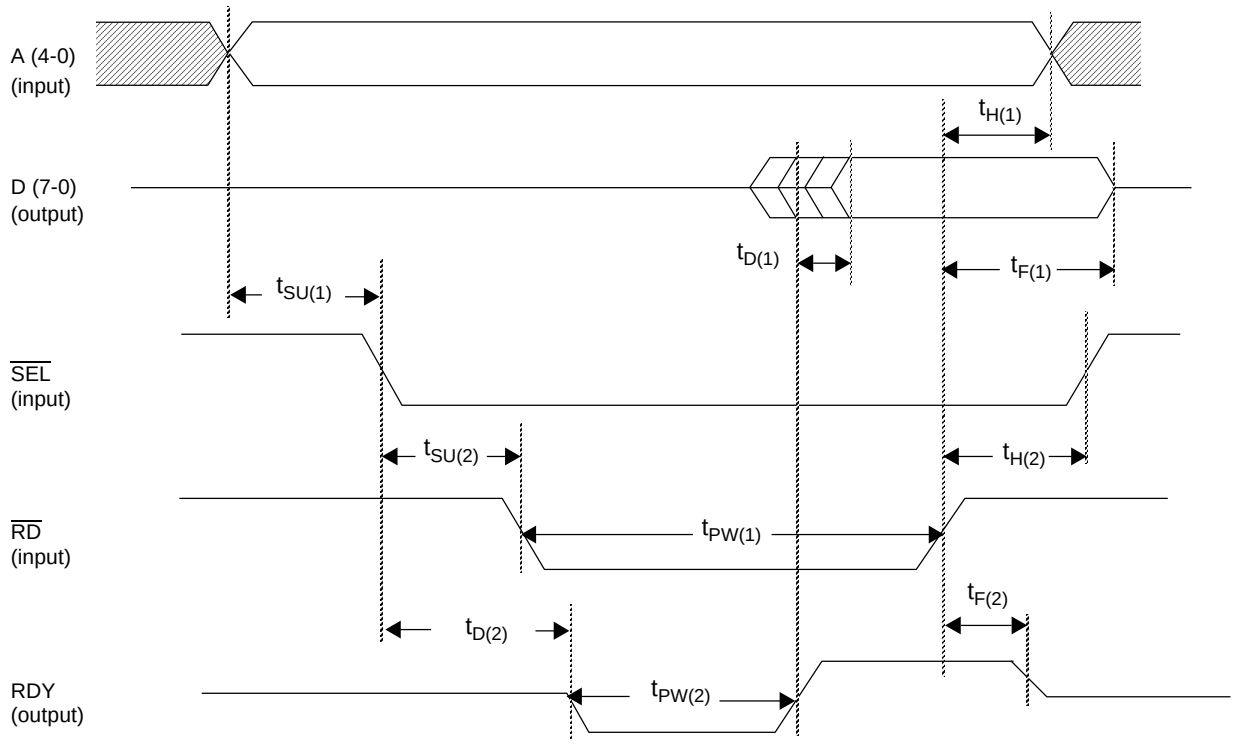
Figure 19. Cell Output Indicator Signal Timing



Parameter	Symbol	Cell Interface Mode	Min	Typ	Max	Unit
ROAM4 delay after RICLK↑	$t_{D(1)}$	External FIFO (Note 4)	-5		10	ns
		Internal FIFO	4		22	ns
		SARA	5		22	ns
		UTOPIA	4		22	ns
RNUC delay after RICLK↑	$t_{D(2)}$	External FIFO (Note 4)	-5		10	ns
		Internal FIFO	4		22	ns
		SARA	5		22	ns
		UTOPIA	4		22	ns
RCAM delay after RICLK↑	$t_{D(3)}$	External FIFO (Note 4)	-5		10	ns
		Internal FIFO	4		22	ns
		SARA	5		22	ns
		UTOPIA	4		22	ns

Note 1: High during entire cell if OAM F4 flow cell.
Note 2: High during entire cell if non-user type cell.
Note 3: High during entire cell if both VPI and VCI values are declared matched.
Note 4: For the External FIFO mode the time delay is relative to ROCLK↑ (Figure 11) instead of RICLK↑.

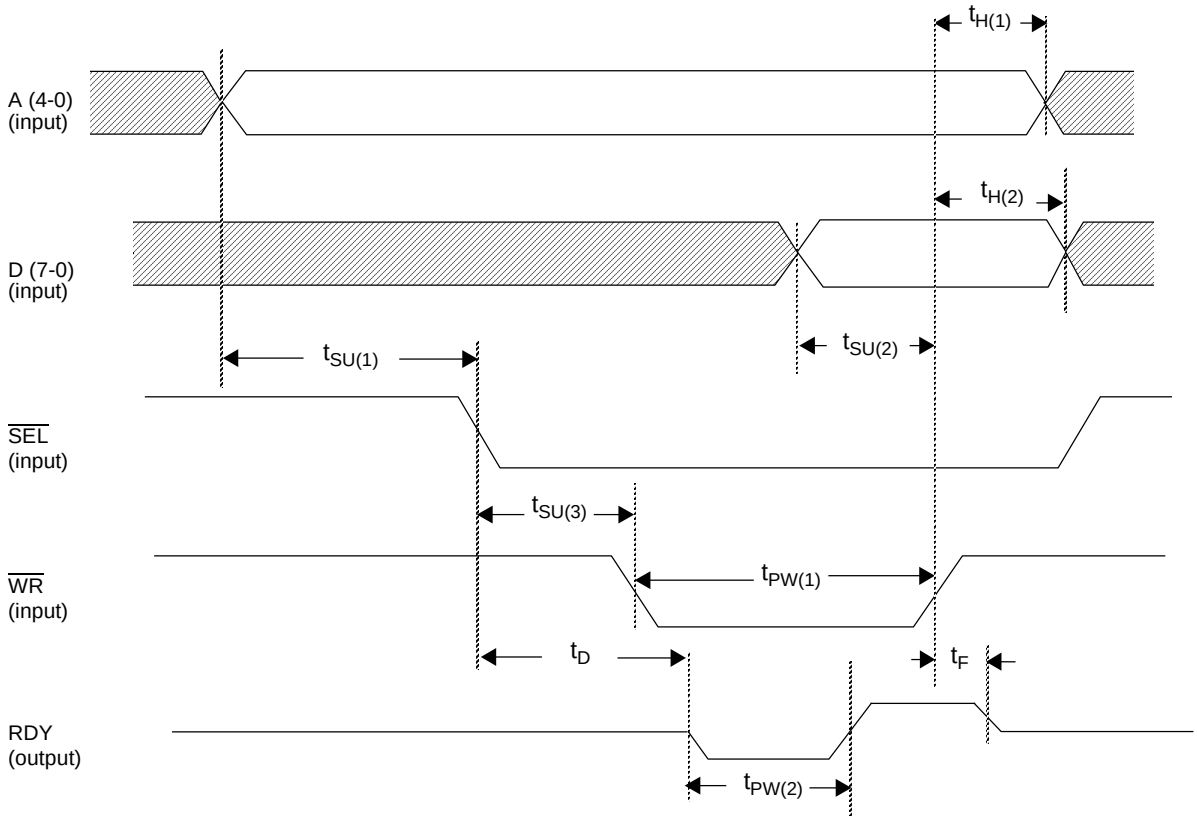
Figure 20. Microprocessor Read, Intel Mode



Parameter	Symbol	Min	Typ	Max	Unit
A(4-0) hold time after $\overline{RD}\uparrow$	$t_{H(1)}$	0.0			ns
A(4-0) set-up time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	15.0			ns
D(7-0) valid delay after RDY$\uparrow$	$t_{D(1)}$	0.0			ns
D(7-0) float time after $\overline{RD}\uparrow$	$t_{F(1)}$	1.0	3.0	5.0	ns
$\overline{RD}$ pulse width	$t_{PW(1)}$	3∗CP *			ns
$\overline{SEL}\downarrow$ set-up time to $\overline{RD}\downarrow$	$t_{SU(2)}$	0.0			ns
$\overline{SEL}\downarrow$ hold time after $\overline{RD}\uparrow$	$t_{H(2)}$	0.0			ns
RDY$\downarrow$ delay after $\overline{SEL}\downarrow$	$t_{D(2)}$			20.0	ns
RDY pulse width	$t_{PW(2)}$			3∗CP+21 *	ns
RDY float time after $\overline{RD}\uparrow$	$t_{F(2)}$			3.0	ns

*Note: CP means the PRCLK clock period, minimum = 50 nanoseconds.

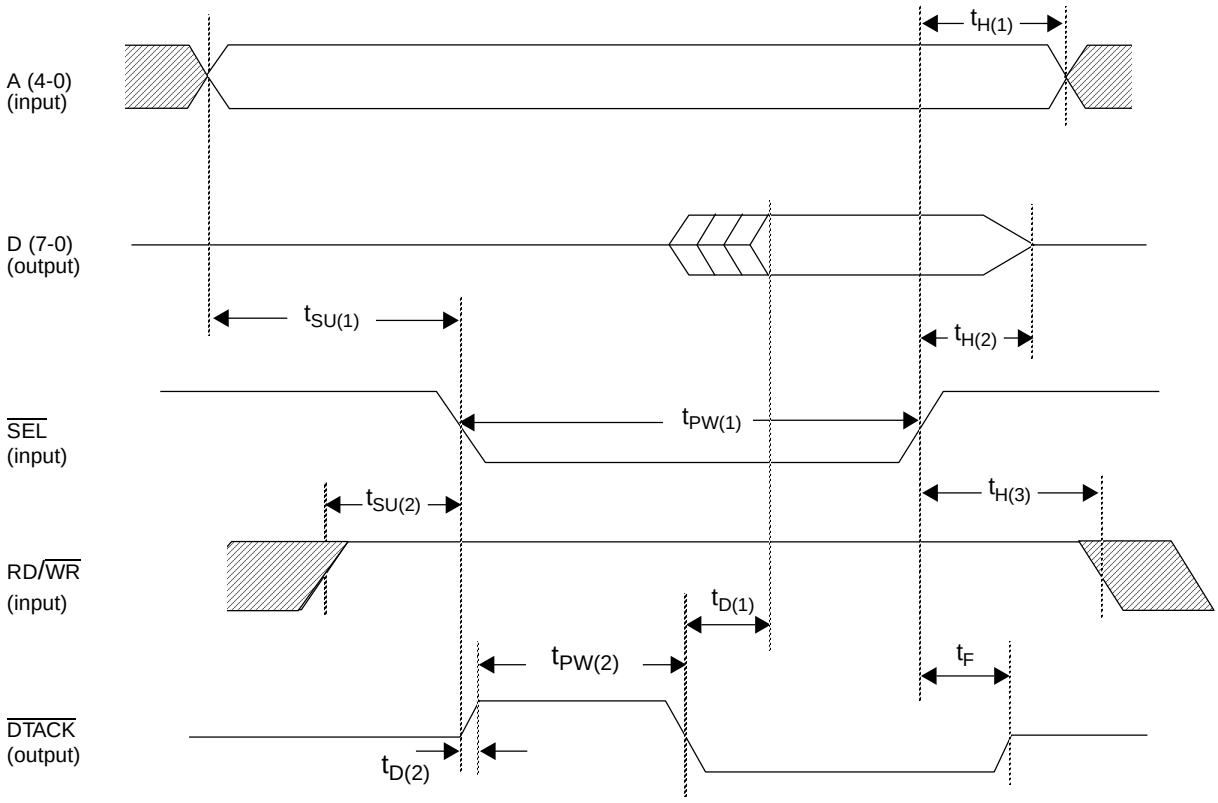
Figure 21. Microprocessor Write, Intel Mode



Parameter	Symbol	Min	Typ	Max	Unit
A(4-0) hold time after $\overline{WR}\uparrow$	$t_{H(1)}$	0.0			ns
A(4-0) set-up time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	15.0			ns
D(7-0) valid set-up time to $\overline{WR}\uparrow$	$t_{SU(2)}$	15.0			ns
D(7-0) hold time after $\overline{WR}\uparrow$	$t_{H(2)}$	10.0			ns
$\overline{SEL}\downarrow$ set-up time to $\overline{WR}\downarrow$	$t_{SU(3)}$	0.0			ns
$\overline{WR}$ pulse width	$t_{PW(1)}$	3∗CP *			ns
RDY$\downarrow$ delay after $\overline{SEL}\downarrow$	t_D			20.0	ns
RDY pulse width	$t_{PW(2)}$			3∗CP+21 *	ns
RDY float time after $\overline{WR}\uparrow$	t_F			3.0	ns

*Note: CP means the PRCLK clock period, minimum = 50 nanoseconds.

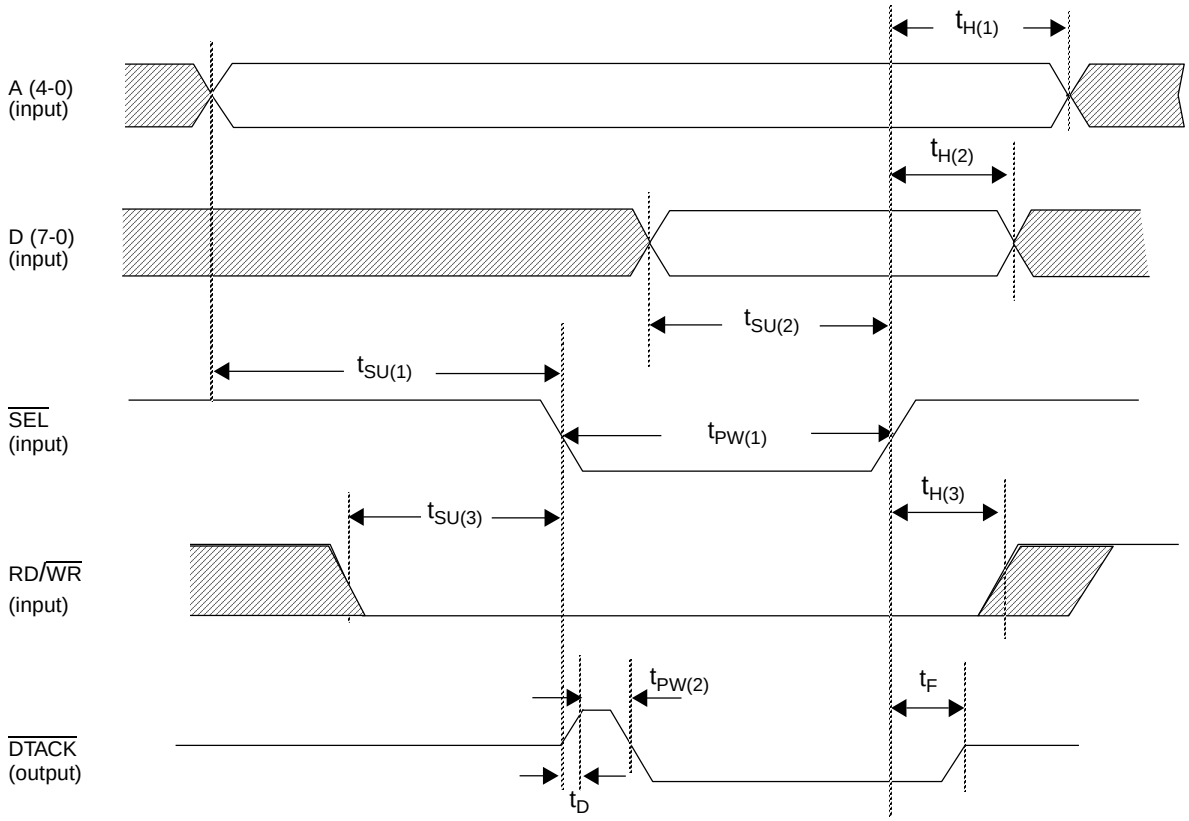
Figure 22. Microprocessor Read, Motorola Mode



Parameter	Symbol	Min	Typ	Max	Unit
A(4-0) hold time after $\overline{SEL}\uparrow$	$t_{H(1)}$	0.0			ns
A(4-0) valid set-up time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	15.0			ns
D(7-0) valid delay after $\overline{DTACK}\downarrow$	$t_{D(1)}$			0.0	ns
D(7-0) hold time after $\overline{SEL}\uparrow$	$t_{H(2)}$	5.0			ns
$\overline{SEL}$ pulse width	$t_{PW(1)}$	3∗CP + 21 *			ns
RD/$\overline{WR}\uparrow$ set-up time to $\overline{SEL}\downarrow$	$t_{SU(2)}$	0.0			ns
RD/$\overline{WR}\uparrow$ hold time after $\overline{SEL}\uparrow$	$t_{H(3)}$	0.0			ns
$\overline{DTACK}\uparrow$ delay after $\overline{SEL}\downarrow$	$t_{D(2)}$			3∗CP + 21 *	ns
$\overline{DTACK}$ pulse width	$t_{PW(2)}$				ns
$\overline{DTACK}$ float time after $\overline{SEL}\uparrow$	t_F			5.0	ns

*Note: CP means the PRCLK clock period, minimum = 50 nanoseconds.

Figure 23. Microprocessor Write, Motorola Mode



Parameter	Symbol	Min	Typ	Max	Unit
A(4-0) hold time after $\overline{SEL}\uparrow$	$t_{H(1)}$	0.0			ns
A(4-0) valid set-up time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	15.0			ns
D(7-0) valid set-up time to $\overline{SEL}\uparrow$	$t_{SU(2)}$	15.0			ns
D(7-0) hold time after $\overline{SEL}\uparrow$	$t_{H(2)}$	0.0			ns
$\overline{SEL}$ pulse width	$t_{PW(1)}$	3∗CP+21 *			ns
RD/$\overline{WR}\downarrow$ set-up time to $\overline{SEL}\downarrow$	$t_{SU(3)}$	0.0			ns
RD/$\overline{WR}\downarrow$ hold time after $\overline{SEL}\uparrow$	$t_{H(3)}$	0.0			ns
$\overline{DTACK}\uparrow$ delay after $\overline{SEL}\downarrow$	t_D			3∗CP+21 *	ns
$\overline{DTACK}$ pulse width	$t_{PW(2)}$	3∗CP+21 *			ns
$\overline{DTACK}$ float time after $\overline{SEL}\uparrow$	t_F			5.0	ns

*Note: CP means the PRCLK clock period, minimum = 50 nanoseconds.

OPERATION

The OPERATION section of this data sheet is divided into two major sections: Internal Device Operations and Line and Terminal External Operations. There are also supporting sections on Control, Testing and Initialization. Reference to the block diagram shown in Figure 1 helps in reading the following text.

INTERNAL DEVICE OPERATIONS

RECEIVE

Line Interface

The line interface will support several operating modes selected by control bits LM2, LM1, LM0 and SERIAL, as shown in the following table.

LM2	LM1	LM0	SERIAL	Mode
0	0	0	0	STS-3c/STM-1
0	0	1	0	STS-1
0	1	0	0	DS3
1	0	0	0	DS1 CS2180 Framer
1	0	1	0	ST-BUS DS1 Mode
1	1	0	0	E1 DS2181 Framer
1	1	1	0	ST-BUS E1 Mode
X	X	X	1	Bit-serial

Note: X = Don't Care

Cell Delineation

All of the standard input formats provide either a byte-aligned input (STS-3c/STM-1, STS-1, DS3) or bit-serial input (all other modes).

Byte-Parallel HEC Search

While searching for the first indication of a valid HEC, the frame search circuit is in the "HUNT" state. This continues until the HEC is valid for some phase. Upon finding the first valid HEC, the frame search circuit enters "PRESYNC" state. This candidate phase is then validated by looking at the HEC every cell time (53 bytes later) for six consecutive cells. If an invalid HEC is seen within the next six cells, the frame search machine reenters the "HUNT" state and search resumes. Six consecutive HEC valid indications takes the frame search circuit into the "SYNC" state and clears the loss of frame indication (EVLOF = 0). After entering the SYNC state, the checking continues. If seven consecutive HEC valid indications are missing while in SYNC state, the frame search circuit falls back into the HUNT state, and the loss of frame indication is set (EVLOF = 1).

Figure 24 illustrates the HEC Search done by the CDB device.

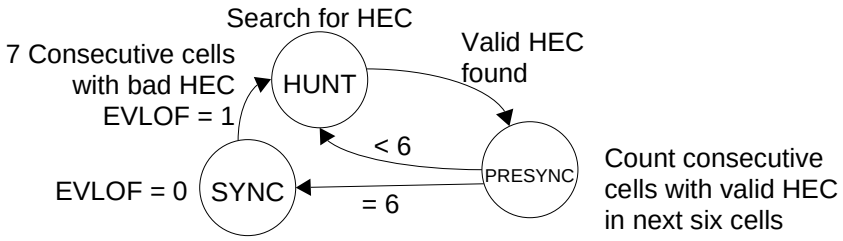


Figure 24. CDB HEC Search Algorithm

While in the HUNT and PRESYNC states (EVLOF = 1), the failed header error check counter CEHEC is not indexed.

If the control bit EVLOF = 1, output pin RLOF is driven high to indicate LOF to external devices.

Bit-Serial HEC Search

If control bit SERIAL or control bit LM2 is set to 1, a bit-serial cell framing is performed. All other operation is as described in the Byte-Parallel HEC Search section above. At input frequencies up to 20 Mbit/s, the CDB will be able to receive and frame to an unformatted, bit-serial input signal.

Cell Header Error Checking, Correction, and Cell Discard

Following acquisition of the HEC phase with the HEC search (in SYNC state), the header CRC of each received cell is checked for correctness. This is achieved by calculating a CRC-8 over the first four bytes of each cell and comparing the value to the received HEC value in the cell. If the header error check fails, and bit ENRHEC = 1, the 8-bit counter CEHEC is indexed by one each time such an error occurs. If ENRHEC = 0, the error counter is disabled.

If bit ENCOR is set, header error correction is enabled. The CDB performs single-bit error correction and multiple-bit error detection. If a correctable error pattern is detected, that error is corrected, and counter CCCOR is indexed. If an uncorrectable error pattern is seen, no correction is made and, if DCHEC is set, the cell will be discarded. If a header error correction is made for one cell, or if an uncorrectable error is observed, a correction cannot be made again until at least one good cell (no errors) has been received. This is per ITU I.432. CCCOR counts cells with single-bit HEC errors that were corrected and CEHEC counts single-bit and multiple-bit errored cells.

Descrambling

Descrambling over the 48 payload bytes of a cell is performed by the CDB if SCRENA = 1. Scrambling and descrambling permits the randomization of cell payload data, which improves cell delineation efficiency and helps avoid continuous non-variable data patterns. Descrambling consists of adding, modulo-2, the scrambler output to the received data. At the end of one cell, the descrambler is stopped and the state saved. At the start of the next cell payload, the descrambler is re-started where it left off. The CDB implements the self synchronizing scrambler $X^{43} + 1$, as defined in ITU I.432. After descrambling, the ATM cell is passed to the cell output FIFO.

Idle Cell Discard

Incoming cells are identified as "idle" cells and are discarded according to the rules selected by control bits IMODE2, IMODE1, and IMODE0. The UNI/NNI operating mode is selected by the UNIMODE control bit. Both physical layer idle cells and ATM layer unassigned cells can be discarded. The different modes provide ANSI, ITU, and ATM Forum compliance. The following table details the meaning of the control bits that influence the handling of idle cells.

Bit Name	Function
UNIMODE	**UNI Mode**: If UNI =1, the application of the CDB is at a User-Network Interface, and the GFC nibble has use. If UNI = 0, the application of the CDB is at a Network Node Interface (NNI), and the GFC nibble is part of the VPI. If UNIMODE = 0 then Mode C in the following table is not used, and the GFC nibble MUST be zero for modes A and B.
IMODE2,1,0	**Idle Mode**: Setting of these bits (together with UNIMODE) determines which cells will be discarded by the CDB according to this table and the following diagram ("x" means "don't care". Cells are not discarded for undefined combinations of IMODE2, 1, 0): IMODE2 IMODE1 IMODE0 MODE 0 0 0 A 1 0 0 B 1 1 0 A or C 0 1 1 D

GFC	VPI	VCI	PTI	CLP	MODE
x x x x	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	x x x	1	A
x x x x	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	x x x	x	B
0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	x x x	0	C
0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0	1	D

Bit Values of Discarded Cells in the ATM Cell Header for the CDB Device

OAM F4 Flow Cell Detection

When cells having VCI address 0000 0000 0000 0011 or 0000 0000 0000 0100 (F4 flow) are detected, a high level will be output on pin ROAM4 for the entire duration of the cell (all 53 bytes).

Non-User Type Cell Detection

When cells having Payload Type Indicator (PTI) MSB = 1 (non-user type) are detected, a high level will be output on pin RNUC for the entire duration of the cell (all 53 bytes). Cells with VPI,VCI = 0,0, but not defined as "idle" as per idle cell discard mode (according to IMODE2, IMODE1, IMODE0) are also output as non-user type cells.

Cell Address Detection

The CDB enables the detection of cells having a VPI/VCI number matching a programmable value or range of

values. Whenever a cell having such an address match is observed, a high level will be output on pin RCAM during the time that the cell (all 53 bytes) is clocked out of the output formatter. An address match is declared if VPI match and VCI match, as described below, are active. Note that VPI match and VCI match are internal signals only.

VPI Number, VPI Mask

Two 12-bit registers, VPIAD and VPIRM, are provided. A bit-by-bit comparison of the received VPI number and the contents of VPIAD and VPIRM is made. If the received VPI number matched VPIAD in a bit position, or if VPIRM is set for that position, a match is declared for that bit position. If match is declared for all 12 bit positions, then VPI match is declared. When operating in UNI mode, the first nibble of VPIAD must be set to zero and the first nibble of VPIRM must be set to F(H) in order to mask out the generic flow control bits.

VCI Number, VCI Mask

Two 16-bit registers, VCIAD and VCIRM are provided. A bit-by-bit comparison of the received VCI number and the contents of VCIAD and VCIRM is made. If the received VCI number matched VCIAD in a bit position, or if VCIRM is set for that position, a match is declared for that bit position. If match is declared for all 16 bit positions, then VCI match is declared. If there is a match for both the VPI and the VCI then RCAM is high during the cell output.

Busy Cell Count

The total number of busy cells received is recorded. A busy cell is defined as any cell not discarded, not non-user type, and not OAM F4 flow type. A 16-bit non-saturating counter, RBUSYC, is indexed for each busy cell.

Cell Output Formatter

External FIFO / Internal FIFO / SARA Modes (SMODE1, SMODE0 $\neq$ 1,0)

Inside the CDB is a FIFO cell buffer having storage capability for three full ATM cells. This allows for rate decoupling between the receive line interface and the cell output formatter. Four interface modes are supported by external control pins as shown in the following table:

SMODE1	SMODE0	Interface Mode
0	0	External FIFO mode. CDB writes (RX side) and reads (TX side) cells to external synchronous FIFO.
0	1	Internal FIFO mode. CDB RX FIFO is read (RX) or written (TX) as a synchronous FIFO.
1	0	UTOPIA mode.
1	1	Direct SARA interface mode.

Two data widths are supported in all modes: 9 bits and 18 bits. Control bit IOBYTE selects between 9-bit and 18-bit data widths. In all modes, the entire 53-byte ATM cell is sent and received on the terminal side of the CDB device.

In 9-bit mode (IOBYTE = 1), the cell is sent out as 53 bytes. This output format is illustrated in Figures 25(a,c) below. The ninth bit functions either as a parity bit, or as a start of cell delineation bit, as described below.

In 18-bit mode (IOBYTE=0), the cell is sent out as 27 words. This output format is illustrated in Figures 25(b,d). Bits 16 and 17 function either as parity bits, or as start of cell delineation bits, as described below.

(a) External FIFO Byte Mode

Bit 8	Bits 7-0	Row
x	hdr0	1
p	hdr1	
p	hdr2	
p	hdr3	
p	hec	
p	pld0	
p	pld1	
p	pld2	
p	pld3	
	*	27
	*	
	*	
p	pld45	
p	pld46	
y	pld47	53

(b) External FIFO Word Mode

Bit 17	Bit 16	Bits 15-8	Bits 7-0
x	x	hrd0	hdr1
p	p	hdr2	hdr3
p	p	hec	00
p	p	pld0	pld1
p	p	pld2	pld3
		* * *	* * *
p	p	pld44	pld45
y	y	pld46	pld47

(c) Internal FIFO or SARA * Byte Mode

Bit 8	Bits 7-0
x	hdr0
p	hdr1
p	hdr2
p	hdr3
p	hec
p	pld0
p	pld1
p	pld2
p	pld3
	*
	*
	*
p	pld45
p	pld46
y	pld47

(d) Internal FIFO or SARA * Word Mode

Bit 17	Bit 16	Bits 15-8	Bits 7-0
x	x	hrd0	hdr1
p	p	hdr2	hdr3
p	p	hec	pld0
p	p	pld1	pld2
p	p	pld3	pld4
		* * *	* * *
p	p	pld45	pld46
y	y	pld47	xx

* SARA mode does not use parity bits for a start of cell indication at the cell input interface. SARA mode uses control line TCF1/ TxCLAV to indicate the start of a cell.

Figure 25. Cell Input / Output Formats for Internal / External FIFO or SARA Operation

The contents of the p, x, and y bits depend on the state of control bits IOPAR and IOEOC as shown in the following table. Control bit IOPAR enables parity. Start of cell indication can be associated with the first byte/word in the cell (IOEOC = 0) or the last byte/word in the cell (IOEOC = 1). When parity is enabled (IOPAR = 1), if IOEOC = 0, the start of cell is indicated by inverted parity on the first byte/word.

IOPAR	IOEOC	p, x, y Bit Meanings in Byte or Word Modes
0	0	p = 0, x = 1, y = 0
0	1	p = 0, x = 0, y = 1
1	0	p = parity over bits 7-0, x = not-p, y = p
1	1	p = parity over bits 7-0, x = p, y = not-p

The CDB accepts and sends even parity when it is enabled in one of these three non-UTOPIA modes.

UTOPIA Mode (SMODE1, SMODE0 = 1,0)

The UTOPIA mode supports both the 9- and 18-bit interface, but in this mode, the IOPAR and IOEOC bits are not used and their value has no effect. In the 9-bit mode (control bit IOBYTE = 1), the cell is sent out as 53 bytes. The output is illustrated in Figure 26 (a) below. The ninth bit functions as a parity bit only, not as a start of cell indicator. For the UTOPIA mode, **odd** parity is on the output of the CDB. In the 18-bit mode (control bit IOBYTE = 0), the cell is sent out as 27 words. This output format is illustrated in Figure 26 (b). On the terminal input of the CDB, there is no parity bit included. Therefore, the terminal input is either 8 bits (IOBYTYE = 1) or 16 bits (IOBYTE = 0). The terminal inputs are illustrated in Figures 26 (c) and (d).

(a) UTOPIA Byte Mode, Receive Terminal Output

Bit 8	Bits 7-0	Row
p	hdr0	1
p	hdr1	
p	hdr2	
p	hdr3	
p	hec	
p	pld0	
p	pld1	
p	pld2	
p	pld3	
	*	
	*	27
	*	
p	pld45	
p	pld46	
p	pld47	53

(b) UTOPIA Word Mode, Receive Terminal Output

Bit 17	Bit 16	Bits 15-8	Bits 7-0
p	p	hrd0	hdr1
p	p	hdr2	hdr3
p	p	hec	00
p	p	pld0	pld1
p	p	pld2	pld3
		* * *	* * *
p	p	pld44	pld45
p	p	pld46	pld47

Note 1: The "00" following the HEC output is a user byte in the UTOPIA mode. The CDB inserts zeros for this byte value.

(c) UTOPIA Byte Mode, Transmit Terminal Input

Bits 7-0
hdr0
hdr1
hdr2
hdr3
hec
pld0
pld1
pld2
pld3
*
*
*
pld45
pld46
pld47

(d) UTOPIA Word Mode, Transmit Terminal Input

Bits 15-8	Bits 7-0
hrd0	hdr1
hdr2	hdr3
hec	00
pld0	pld1
pld2	pld3
* * *	* * *
pld44	pld45
pld46	pld47

Note 1: The "00" following the HEC input is a user byte in the UTOPIA mode, and it is assigned by the input data.

Figure 26. UTOPIA Mode Input and Output Formats

In the UTOPIA mode, the CDB sends odd parity (in other modes, it sends even parity).

TRANSMIT

A three-cell internal buffer is implemented in the CDB transmit path. When one buffer is full with a cell, it is passed to the second buffer. When the second buffer is full it is passed to the transmit line interface at the next cell time. Meanwhile, the input buffer can be written to by the cell input block to be ready to send after the first is empty, and so on. This provides for the pipelining required so that the cell rate adaptation function does not limit the data throughput.

Cell Input Block

Just as for the Receive Terminal output, the Transmit Terminal input interfaces to an external FIFO, an external ATM source that can use the internal FIFO of the CDB, the SARA-S, or the UTOPIA mode interface.

The CDB cell input has exactly the same formats illustrated in Figures 25 and 26. The CDB, however, does not calculate the parity of the input signal and does not check for parity errors.

All interfaces, both terminal and line, are discussed below in the Line and Terminal External Operations section.

Idle Cell Generation

Regardless of the cell input mode or transmit line interface modes, the output cell stream which is passed through the transmit line interface is continuous, with the time between busy cells filled with whole, unassigned (idle) cells. Idle cells will have a header value of all-zeros, except for the LSB of the fourth byte (the CLP bit) which will be set equal to control bit ZEROC. All of the bytes of the payload information field will be filled with the value of control byte IDLEW. This mechanism allows both ITU and ANSI compatibility.

It is possible for a cell to be transmitted into the CDB having a combination of zero VPI/VCI and having those bits in the GFC and PTI positions set to some values for control purposes. These cells will be accepted and transmitted normally, and they will be counted as busy cells in the transmitted busy cells counter.

Busy Cell Counter

The total number of busy cells transmitted is recorded. An internal 16-bit non-saturating counter, TBUSYC, is indexed for each busy cell.

Cell Scrambling

The 48 bytes of the cell payload in each cell are scrambled on the outgoing signal if SCRENA = 1. The scrambler operates on all cells whether sourced from the cell input or generated by the CDB. The data bytes of the payload are scrambled using a self-synchronizing polynomial of $X^{43} + 1$ in order to improve the efficiency of cell delineation. The scrambler runs for the duration of the 48 bytes of the cell payload and then is held until the next cell. At the start of the next cell payload, the scrambler continues from the same point at which it left off. The 5-byte ATM header is not scrambled.

Header CRC Generation

The CDB can optionally calculate and overwrite the HEC byte of a cell received in the 53-byte format. If ENTHEG = 1, the CDB will ignore the last eight bits of the cell header, calculate a proper header CRC, and insert it into the header in the last byte position.

In order to improve the performance of the HEC framing circuitry, the HEC is modified before transmission by the addition, modulo-2, of a 01010101 sequence (the COSET polynomial). The leading "0" bit is added to the first outgoing HEC bit, and the trailing "1" bit is added to the final outgoing HEC bit. On reception, the same 01010101 sequence is added to the received HEC bits before checking.

The double addition of the 01010101 pattern, first at the generator, then at the decoder, has no net effect on the HEC process. The purpose of the pattern addition is to improve the statistics of the HEC byte, particularly with idle cells.

Line Output

The transmit line interface supports the same modes as the receive line interface.

LINE AND TERMINAL EXTERNAL OPERATIONS

Line Side Interfaces

SONET STS-3c/SDH STM-1/Byte-Parallel Mode

The CDB will be connected to the TXC-03003 SOT-3 device operating in the datacom mode. Connections are shown in Figure 27 and timing is shown in Figures 3 and 4. Data bytes are accepted from the SOT-3 on the rising edge of RXCK. This mode may also be used as a general purpose byte parallel I/O mode. Pin RXF1 should be tied high and RXF2 should be tied low to allow all bytes to be data (i.e., to enable a pure cell format with no overhead gaps).

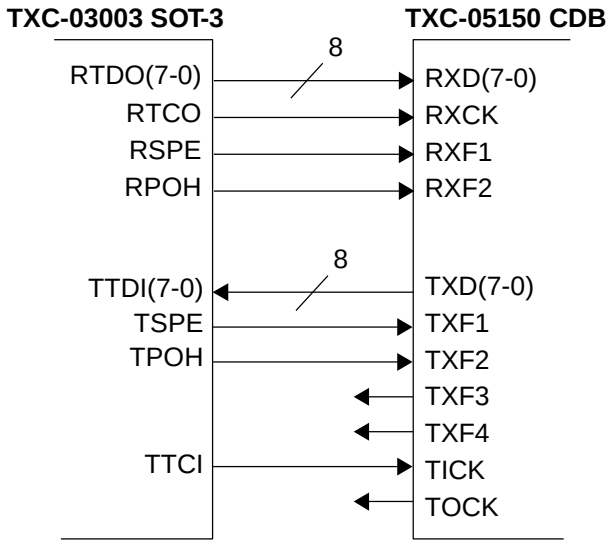


Figure 27. CDB Connections to the SOT-3

For the transmit data from the CDB to the SOT-3, the SOT-3 acts as the master. As illustrated in the timing diagram of Figure 4, the TSPE and TPOH signals block the sending of data from the CDB. The transmit clock is provided by the SOT-3 on the TICK input to the CDB, and data is transmitted on the rising edges of this clock.

If TXF1 is tied high and TXF2 is tied low, this interface will support an unformatted byte-parallel interface from the CDB. Clock and timing inputs will be accepted on the rising edge, and data will be output on the rising edge.

SONET STS-1

When working with the SOT-1 (TXC-03001) for STS-1 interface, the SOT-1 is operated in the parallel, STS-1 pass through mode. Data bytes are accepted from the SOT-1 output on the falling edge of RXCK, if RXF1 (RSPE) = 1, and RXF2 (RSYN) = 0. The cell mapping is in all payload bytes, except for columns 1 (the POH), 30, and 59. SOT-1/CDB connections are shown in Figure 28a and timing is shown in Figures 5 and 6.

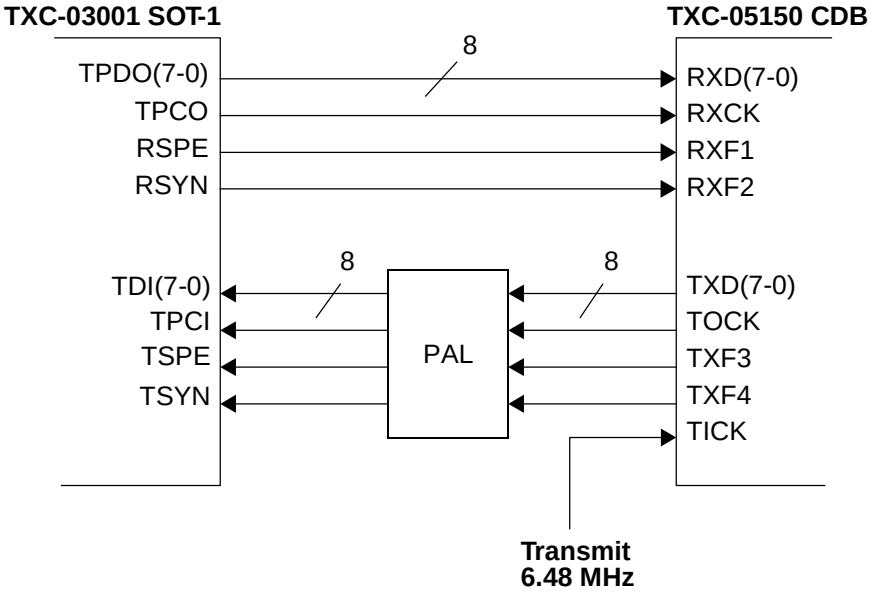


Figure 28a. CDB Connections to the SOT-1

A 6.48 MHz clock enters the CDB on pin TICK, and drives an internal counter chain which forms an STS-1 frame. The CDB outputs an SPE indication (TSPE) on pin TXF3, and a J1 time pulse (TSYN) on pin TXF4. The CDB will not output data bytes during payload bytes 1, 30 or 59 since these are fixed stuff columns. Data bytes are output on the falling edge of TOCK during the times that the SPE indication TXF3 is high, except that data is not sent out during those times of the POH byte positions. This configuration requires the use of an external PAL to add bytes A1, A2, H1 and H2 at the proper times.

A flowchart for the PAL in Figure 28a is illustrated in Figure 28b:

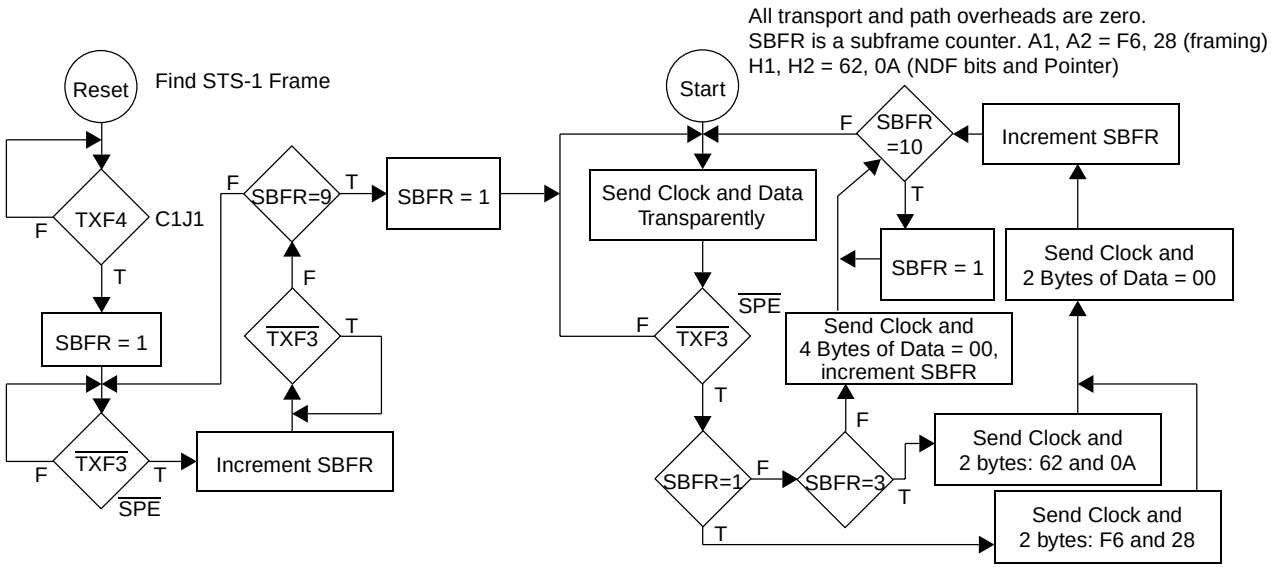


Figure 28b. PAL Flowchart for STS-1

DS3 Line

On the falling edge of RXCK data nibbles are accepted from the TXC-03401 (DS3F)framer device. An active indication on the RXF1(RFN if DS3) serves to delineate nibble boundaries. For DS3F, RXF1 is active during the first nibble of a byte. Connections are shown in Figure 29 and timing is shown in Figure 7. Note that ATM cells are mapped into DS3 in the direct mapping mode as described in T1S1/94-243 under HEC-based mapping of ATM into 44,736 Kbit/s.

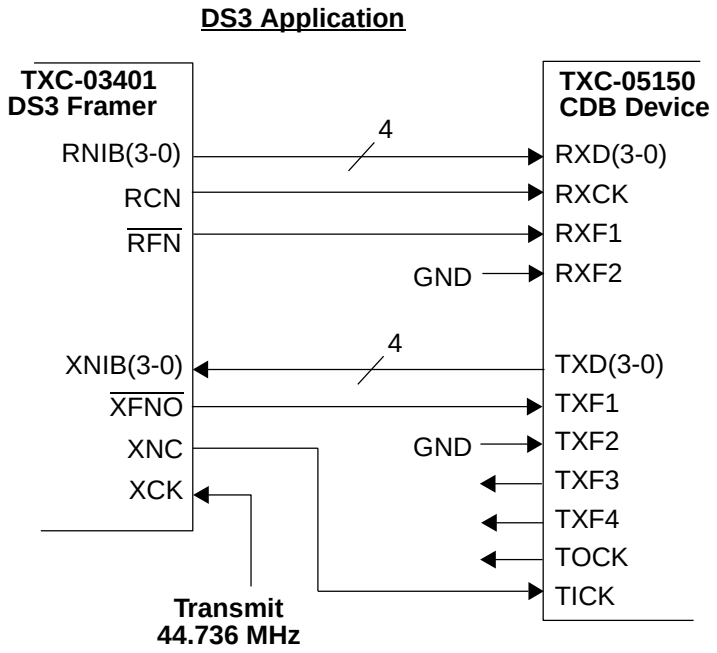


Figure 29. DS3 Connections to the CDB

DS1/E1 Lines

Bit-serial data is accepted on the falling edge of RXCK. For the CS2180 interface, DS1 data bits are accepted except during the framing bit position, designated as a high level on RXF1. RXF1 occurs every superframe or extended superframe (the CDB contains a counter to accommodate the framing times for DS1), and during the LSB of frame 31 for E1 signals. For E1 operation with the DS2181, bit-serial data will be accepted on the falling edge of RXCK, except during channel times 0 and 16.

For the Mitel 7230 devices, the connection is to a 32-channel, 2048 Kbit/s highway. Frame timing is given by a frame pulse on RXF1. For DS1 operation, data is accepted in channel positions other than 0,4,8,12,16,20,24, and 28. For E1 operation, data is accepted in channel positions other than 0 and 16.

Connections are shown in Figure 30 and timing is shown in Figures 8a, 8b and 9.

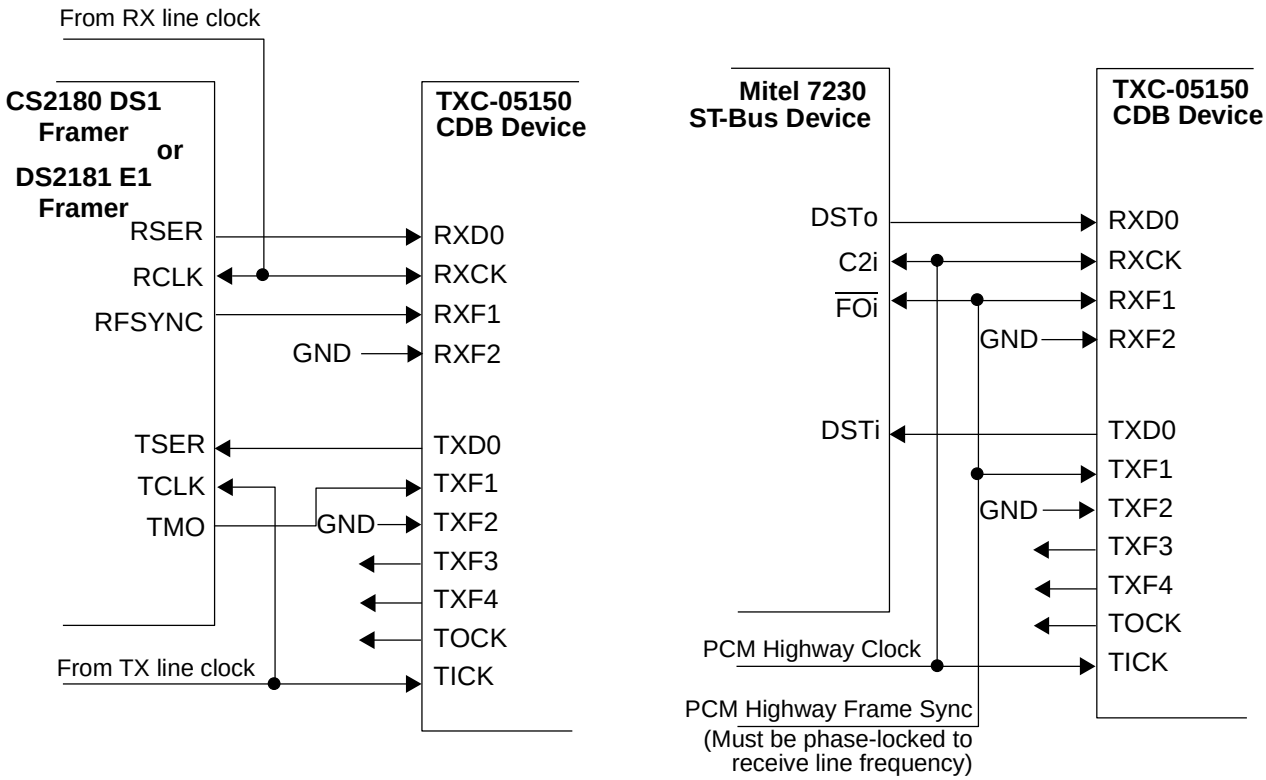


Figure 30. DS1/E1 Connections to the CDB

The CDB outputs bit-serial data on the rising edge of TICK. DS1/E1 and ST-bus type modes are controlled by LM2, LM1, LM0, and SERIAL bits.

For the CS2180, data is output during 192 bits of every frame, except the framing bit position. For the DS2181, data is output except during the eight bits of channels 0 and 16. In both the CS2180 and DS2181 cases, an internal counter tracks the frame position.

For the Mitel 7230 ST-BUS in DS1 and E1 mode, connection is to a 32-channel 2048 Kbit/s highway. In the DS1 case, channels 0, 4, 8, 12, 16, 20, 24, and 28 are unused. In the E1 case, channels 0 and 16 are not used.

Unframed Bit-Serial Mode Input

At input frequencies up to 20 Mbit/s, the CDB will be able to receive and frame to an unformatted, bit-serial input signal. This will be done if control bit SERIAL = 1. HEC framing is found as illustrated in Figure 24 and the following text. In this mode, data will enter on pin RXD0 on the falling edge of clock RXCK. The other input pins are unused, and they must be grounded. Timing is shown in Figure 10.

Serial Output

If SERIAL = 1, the output is unformatted bit-serial as follows. TICK is an input. One data bit is returned on every rising edge of TICK. No other signals are active.

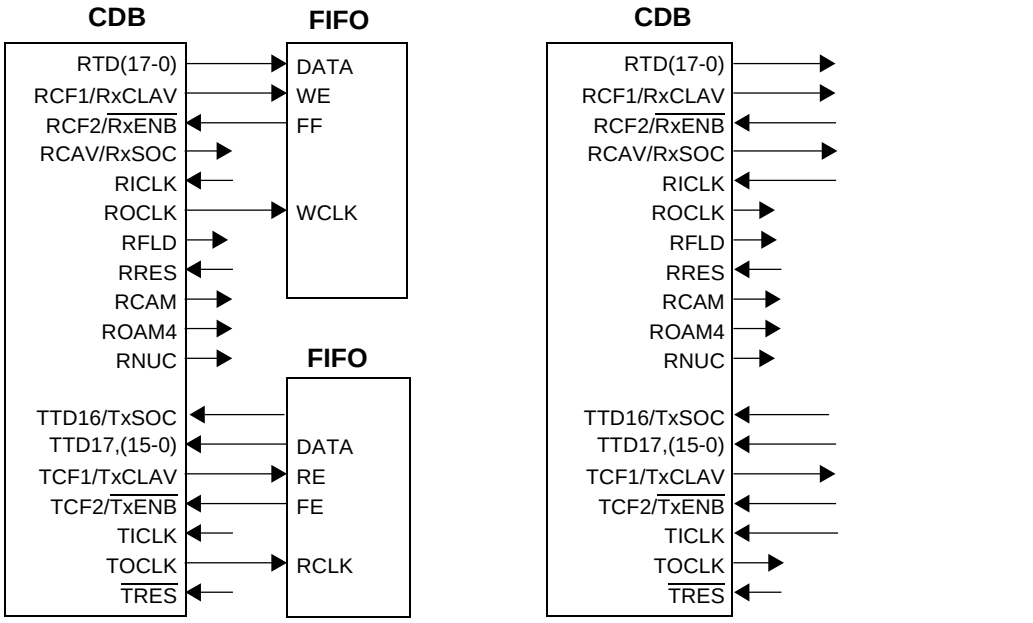
Terminal Side Interfaces

External Synchronous FIFO Write Output

In this mode (SMODE1,SMODE0 = 0,0), the CDB cell output formatter is configured to be connected to the write port of a synchronous FIFO. The CDB cell output formatter assumes a master role to the synchronous FIFO.

Before any cell is sent out, a complete cell is captured in an internal RAM. Once a cell is ready to be sent out, it is transmitted to the FIFO on 53 (or 27) consecutive write pulses. The CDB signal pin ROCLK is connected to the external FIFO write clock as shown in Figure 31(a) for the upper FIFO. CDB signal pin RCF1 provides write enable in this mode. The transfer rate is derived from the receive line frequency as shown in the following table. Note that the word mode is not supported in DS1 and E1 modes. Timing for this mode is shown in Figure 11.

The meaning of the incoming FIFO full signal will actually be an almost-full indication. Incoming RCF2 (FIFO full) will be inactive if there is space for at least 53 bytes available in the external FIFO, and active if, in the external FIFO, the available space is less than 53 bytes. If the external FIFO indicates full, cells are buffered in the CDB internal buffer. If this internal buffer is full, incoming cells are discarded. The counter of cells discarded for FIFO full (CDRFF) is indexed on each discard.



(a) External FIFO Mode (b) Internal FIFO and UTOPIA Mode

Figure 31. Synchronous FIFO Connections

Required FIFO widths and clock rates are given in the following table for different control bit settings.

Line Rate	LM2,1,0	IOBYTE	FIFO Width	FIFO Write Clock
STS-3c/STM-1	000	0	18 bit	19.44 MHz
		1	9 bit	
STS-1	001	0	18 bit	6.48 MHz
		1	9 bit	
DS3	010	0	18 bit	11.182 MHz
		1	9 bit	
DS1	100	1	9 bit	1.544 MHz
E1	11X	1	9 bit	2.048 MHz

External Synchronous FIFO Mode Cell Input

All of the I/O modes described previously with respect to widths, HEC byte output, and the use of the p, x, and y bits for parity and cell delineation are supported in the synchronous mode on the transmit side.

If SMODE1,SMODE0 = 0,0, then cells are assumed to come from an external synchronous FIFO (Figure 31a, lower FIFO). In this case, the cell input block assumes a master role to the FIFO. When the CDB has an available buffer internally, and the TCF2 indicates that the external FIFO is not empty, it will fetch a cell from the FIFO by asserting a read enable output on TCF1. There is no restriction on the TCF2 pin going active and inactive (and TCF1 also, as a consequence) during the course of reading a cell. When the CDB detects FIFO almost empty from the external FIFO (TCF2 = 0), it will simply wait until FIFO empty clears, and then read the rest of the cell. The CDB will accumulate bytes of the cell until a full cell is in the internal buffer, and then send it out at the next available cell time. Connections are shown in Figure 31 (a) and timing in Figure 12.

The roles of IOBYTE (enable byte-parallel), and IOPAR are the same as on the receive output side.

The CDB will check the cell delineation bit (explicit bit or parity reversal). If it detects a new cell delineation indication, it will resynchronize immediately on that indication.

Internal FIFO Mode Read Output

In this mode (SMODE1, SMODE0 = 0,1), the CDB's internal 3-cell FIFO is directly readable by external circuitry. Connections are shown in Figure 31(b) and timing in Figure 13. Operation is the same as for the read port of a synchronous FIFO. RCF2 is a read enable input, and RCF1 is a FIFO empty output.

If the internal FIFO fills due to the external system not keeping up with the line speed, cells are discarded. The counter of cells discarded for internal FIFO full (CDRFF) is indexed on each discard.

Internal Synchronous FIFO Mode Cell Input

If SMODE1, SMODE0 = 0,1, then the CDB is treated as a FIFO. Write operations into the CDB cell input are initiated by external circuitry. Pin TCF2 is the write enable input, and TCF1 is the FIFO full output. Connections are shown in Figure 31(b) and timing in Figure 14.

If none of the three cell buffers in the CDB transmit path is available, the device will deliver a FIFO full signal on pin TCF1.

Direct SARA-R / SARA-S Device Interface

SARA-R

This mode (SMODE1, SMODE0 = 1,1) specifically supports interconnection to an external synchronous FIFO and the TXC-05501 SARA-R reassembly chip. Connections are shown in Figure 32 and timing in Figure 15. RCAV is a cell available output signal; RCF2 is a read enable input; RCF1 is the FIFO empty output; RRES is the input for the FIFO flush signal from the SARA-R; and RFLD is the flush done output signal returned.

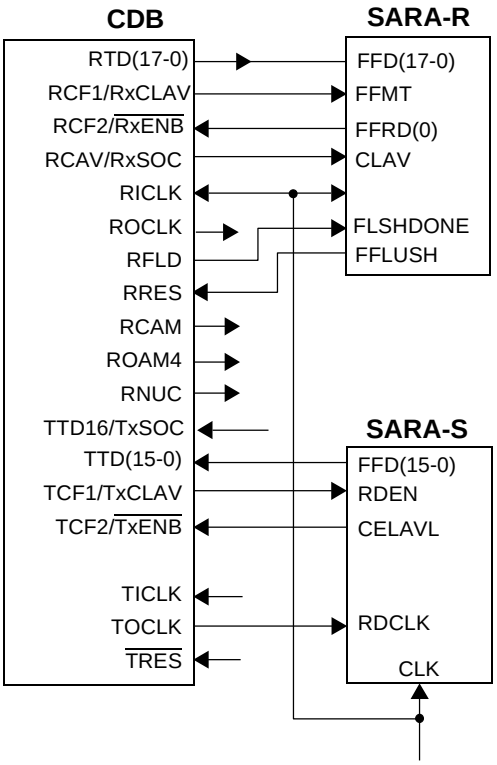


Figure 32. SARA Device Connections

The CDB stores incoming cells (if not discarded) first into its 3-cell internal FIFO. Whenever the CDB has at least one complete cell in RAM, it will assert its RCAV (received cell available) line. Some time later, the SARA-R will respond by asserting RCF2 (FFRD(0) from the SARA-R), enabling an output read on the clock RICLK. Either 53 bytes (IOBYTE = 1) or 27 words (IOBYTE = 0) will be read out. After the first byte or word has been output, RCAV is deasserted. Following this transaction, the CDB determines if it has at least one complete cell in RAM again. If so, it asserts RCAV again and the cycle proceeds. Whenever the CDB does not have a full cell in RAM, it will not assert RCAV, but will do so as soon as the next cell is completely received.

If RRES is made high, it is a global reset command for the CDB receive path from the SARA-R chip (FFLUSH). The CDB will reset the cell framing circuit, and clear any contents of the receive side FIFOs. The performance counters will not be reset in this case. FIFO writing will restart on the first new cell following RRES = 0. RFLD (FLSHDONE) will be returned to SARA-R one cycle of RICLK after RRES is seen as high.

In this mode, the counter for cells discarded for FIFO full (CDRFF) is indexed if there is no room in the internal FIFO to store incoming cells.

SARA-S

The CDB depends upon the SARA-S to indicate the availability of a full cell. When TCF2 (CELAVL from the SARA-S) is asserted, the CDB will assert TCF1 (RDEN to the SARA-S) and enable a read operation from the SARA-S. After reading in the cell, the CDB will send it out during the next cell time. At the end of the cell, the SARA-S will deassert the TCF2 (CELAVL). In this mode, the falling edge of TCF2 is the Start-of-Cell indication. The CDB will ignore any start-of-cell indication (TCF2 going high) while reading a cell from SARA-S, and will re-establish cell delineation on the next instance of TCF2 going active. Timing is shown in Figure 16.

UTOPIA Mode Read Output

In this mode (SMODE1, SMODE0 = 1, 0), the CDB's internal 3-cell FIFO is directly readable by external circuitry. Data formats are shown in Figure 25(a and b) and timing in Figure 17. Operation is the same as for the read port of a synchronous FIFO. RCF2/$\overline{\text{RxENB}}$ is a read enable input, and RCF1/RxCLAV is a cell available output indicating CDB has a complete cell available for transfer.

If the internal FIFO fills due to the external system not keeping up with the line speed, cells are discarded. The counter of cells discarded for internal FIFO full (CDRFF) is indexed on each discard.

UTOPIA Mode Cell Input

If SMODE1, SMODE0=1,0, then the CDB is treated as FIFO. Write operations into the CDB cell input are initiated by external circuitry. Pin TCF2/$\overline{\text{TxENB}}$ is the write enable input, and TCF1/TxCLAV is the output signal indicating CDB can accept the transfer of a complete cell. Data formats are shown in Figure 25(c and d) and timing in Figure 18. Connections are shown in Figure 31(b). There are no parity bits for the UTOPIA word and byte modes at the cell input interface.

If none of the three cell buffers in the CDB transmit path is available, the device will deliver a FIFO full signal on pin TCF1/TxCLAV.

Cell Output Indications

The CDB provides receive terminal OAM F4 and non-user, and receive cell address match, indicator outputs. The timing of these signals is shown in Figure 19.

CONTROL

Microprocessor Interface

The microprocessor interface consists of a simple pair of data (D7-D0) and address (A4-A0) buses, and control signals to accomplish all functions. Control leads are: chip select ($\overline{\text{SEL}}$), read ($\overline{\text{RD}}$), write ($\overline{\text{WR}}$), ready (RDY) and interrupt (INTER) lines. Input MOTO makes certain operating changes to allow simpler interfacing to Motorola microprocessors when MOTO = 1, and to Intel microprocessors when MOTO = 0. Timing is shown in Figures 20 through 23.

Processor Clock (PRCLK) Line

PRCLK is the local clock input to synchronize microprocessor operation. Its maximum frequency is 20 MHz.

Performance Counters

All performance counters (CDHEC, CCCOR, CDRFF, RBUSYC, and TBUSYC) are non-saturating, and "roll-over" to zero from maximum count. To read a 16-bit counter, first read it at its lower byte address. This will cause the lower byte to be read properly, and the upper byte to be latched. The upper byte is then read at the next higher address location. The read mechanism is such that no pending count is lost due to the read procedure.

TESTING

Boundary Scan

Exterior boundary scan is implemented on the CDB, as defined in IEEE standard 1149.1-1990. I/O pins used are defined in the table below.

Pin Name	Function
TCK	Test Clock
TDI	Test Data Input
TDO	Test Data Output
TMS	Test Mode Select
$\overline{\text{TRS}}$	Test Mode Reset

Pins TCK, TDI, TMS, and $\overline{\text{TRS}}$ all have internal pull-ups.Note that SCANTEST and SCANEN must be high to enable the scan test.

The TAP controller is included, as specified in 1149.1. The BYPASS, SAMPLE/PRELOAD, and EXTEST commands are also implemented. The binary code for SAMPLE/PRELOAD is 1010, BYPASS is 1111, and EXTEST is 0000.

INITIALIZATION

On power-up, the following hardware resets should be issued to the device:

$\overline{\text{RESET}}$, pin 35, low;
RRES, pin 143, high;
$\overline{\text{TRES}}$, pin 105, low;
$\overline{\text{TRS}}$, pin 28, low.

There are no software resets.

CONTROL BIT AND REGISTER MEMORY MAP

Address (Hex)	Mode*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00 - 03	R	DEVID (4 bytes)							
04 - 07	NA	Unused (4 bytes)							
08	R	Unused (7 bits)							EVLOF
09	R/W	LM2	LM1	LM0	SERIAL	Unused (2 bits)		EIOOF	EIINF
0A	R/W	IMODE2	IMODE1	IMODE0	UNIMODE	IOPAR	IOEOC	Unused	IOBYTE
0B	R/W	ZEROC	Unused (2 bits)		ENRHEC	SCRENA	ENTHEG	ENCOR	DCHEC
0C - 0F	NA	Unused (4 bytes)							
10	R/W	IDLEW	IDLEW	IDLEW	IDLEW	IDLEW	IDLEW	IDLEW	IDLEW
11	R/W	VCIAD	VCIAD	VCIAD	VCIAD	VCIAD	VCIAD	VCIAD	VCIAD
12	R/W	VCIAD	VCIAD	VCIAD	VCIAD	VCIAD	VCIAD	VCIAD	VCIAD
13	R/W	VCIRM	VCIRM	VCIRM	VCIRM	VCIRM	VCIRM	VCIRM	VCIRM
14	R/W	VCIRM	VCIRM	VCIRM	VCIRM	VCIRM	VCIRM	VCIRM	VCIRM
15	R/W	Unused (4 bits)				VPIAD	VPIAD	VPIAD	VPIAD
16	R/W	VPIAD	VPIAD	VPIAD	VPIAD	VPIAD	VPIAD	VPIAD	VPIAD
17	R/W	Unused (4 bits)				VPIRM	VPIRM	VPIRM	VPIRM
18	R/W	VPIRM	VPIRM	VPIRM	VPIRM	VPIRM	VPIRM	VPIRM	VPIRM
19	R	CEHEC	CEHEC	CEHEC	CEHEC	CEHEC	CEHEC	CEHEC	CEHEC
1A	R	CCCOR	CCCOR	CCCOR	CCCOR	CCCOR	CCCOR	CCCOR	CCCOR
1B	R	CDRFF	CDRFF	CDRFF	CDRFF	CDRFF	CDRFF	CDRFF	CDRFF
1C	R	RBUSYC	RBUSYC	RBUSYC	RBUSYC	RBUSYC	RBUSYC	RBUSYC	RBUSYC
1D	R	RBUSYC	RBUSYC	RBUSYC	RBUSYC	RBUSYC	RBUSYC	RBUSYC	RBUSYC
1E	R	TBUSYC	TBUSYC	TBUSYC	TBUSYC	TBUSYC	TBUSYC	TBUSYC	TBUSYC
1F	R	TBUSYC	TBUSYC	TBUSYC	TBUSYC	TBUSYC	TBUSYC	TBUSYC	TBUSYC

* Note: R = Read; R/W = Read / Write; NA = Not Applicable. Unused bytes and bits should not be addressed.

CONTROL BIT AND REGISTER DESCRIPTIONS

Device ID, Reset, Loss of Frame Alarm

Address (Hex)	Bit	Symbol	Description
00 - 03	4 bytes	DEVID	**Device Identification**: This field contains information on the device type and revision level.
08	0	EVLOF	**Event Loss Of Frame**: This bit is set during the time that the CDB is searching for the HEC byte of the incoming ATM cell. If framing is lost for 7 consecutive cells, EVLOF is also set. EVLOF is zero when the CDB is synchronized with the incoming cells. (See Figure 24.)

Line Side Control Bits

Address (Hex)	Bit	Symbol	Description
09	7	LM2	**Line Mode Bits (2-0)**: The following table lists the line interfaces as a function of the Line Mode bits:
09	6	LM1	
09	5	LM0	
09	4	SERIAL	**Serial**: If this bit is set, the line side of the CDB is set for a serial data I/O with a pure ATM cell format with no "framing bits". The CDB can operate in this mode at data rates up to 20 Mbit/s. This bit over-rides the setting of the Line Mode bits, LM2,1,0, and they become "don't care".

LM2	LM1	LM0	Mode
0	0	0	STS-3c/STM-1
0	0	1	STS-1
0	1	0	DS3
1	0	0	DS1 CS2180 Framer
1	0	1	ST-BUS DS1 Mode
1	1	0	E1 DS2181 Framer
1	1	1	ST-BUS E1 Mode

Interrupt Mask Bits

Address (Hex)	Bit	Symbol	Description
09	1	EIOOF*	**Enable Interrupt on Out Of Frame**: If this bit is set, the microprocessor will be interrupted when the CDB goes out of frame (loses the HEC framing). If the bit is zero, the event is masked, and no interrupt is passed to the microprocessor.
09	0	EIINF*	**Enable Interrupt on In Frame**: If this bit is set, the microprocessor will be interrupted when the CDB goes into frame (first finds the HEC framing). If the bit is zero, the event is masked, and no interrupt is passed to the microprocessor.

* The interrupt stays high for the length of the condition.

Receive Idle Cell Discard Control and UNIMODE

<table>
<tr><th>Address (Hex)</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td>0A</td><td>7</td><td>IMODE2</td><td rowspan="3">Idle Mode (2-0): These three bits determine which of four formats of idle cells are to be dropped (cells are not dropped for other values of the IMODE bits). The following table and diagram give the formats of the received cells that can be discarded by the CDB:
<table>
<tr><th>IMODE2</th><th>IMODE1</th><th>IMODE0</th><th>MODE</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>A</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>B</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>A or C</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>D</td></tr>
</table>
<table>
<tr><th>GFC</th><th>VPI</th><th>VCI</th><th>PTI</th><th>CLP</th><th>MODE</th></tr>
<tr><td>x x x x</td><td>0 0 0 0 0 0 0 0</td><td>0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td><td>x x x</td><td>1</td><td>A</td></tr>
<tr><td>x x x x</td><td>0 0 0 0 0 0 0 0</td><td>0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td><td>x x x</td><td>x</td><td>B</td></tr>
<tr><td>0 0 0 0</td><td>0 0 0 0 0 0 0 0</td><td>0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td><td>x x x</td><td>0</td><td>C</td></tr>
<tr><td>0 0 0 0</td><td>0 0 0 0 0 0 0 0</td><td>0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td><td>0 0 0</td><td>1</td><td>D</td></tr>
</table></td></tr>
<tr><td>0A</td><td>6</td><td>IMODE1</td></tr>
<tr><td>0A</td><td>5</td><td>IMODE0</td></tr>
<tr><td>0A</td><td>4</td><td>UNIMODE</td><td>User to Network Interface Mode: This bit is normally set when the CDB device is located at a cell termination / source at the user's location. It enables the use of the GFC nibble and limits the VPI to 8 bits. When it is set, only modes A and B in the above table can be used since the GFC nibble may not be zero. This bit is normally zero when the CDB is located at a Network to Network interface (NNI), and the GFC nibble is not used. The VPI is then 12 bits in length.</td></tr>
</table>

Terminal Output Control Bits

Address (Hex)	Bit	Symbol	Description
0A	3	IOPAR	**Input / Output Parity**: If IOPAR = 1, the CDB calculates even parity for the receive terminal output data and includes it as the ninth bit of a byte output, or the 17th and 18th bits of a word output. If IOPAR = 0, the corresponding bit positions are always zero (except when there is a start or end of cell indication). See Note1.
0A	2	IOEOC	**Input / Output End Of Cell**: The value of this bit determines where the start of cell indicator occurs. If it is one, the start of cell indicator is at the last byte of the cell (the byte preceding the start of cell). If it is zero, the start of cell indication is at the first byte of the cell. If IOPAR = 0, the start of cell indication is a one (1). If IOPAR = 1, the start of cell indicator is a reversal of parity. See Figure 25 and Note 1 below.
0A	0	IOBYTE	**Input / Output Byte**: If IOBYTE = 1, the terminal I/O of the CDB is in the byte (9-bit) mode. If IOBYTE = 0, the terminal I/O of the CDB is in the word (18-bit) mode.

Internal Control Bits

Address (Hex)	Bit	Symbol	Description
0B	7	ZEROC	**Zero the CLP bit**: If this bit is one, the Cell Loss Priority (CLP) bit is one for idle cells produced by the CDB. If ZEROC = 0, then the CLP bit is zero for idle cells.
0B	4	ENRHEC	**Enable Receive side HEC error Counter**: If ENRHEC = 1, then the HEC error counter will be incremented for each HEC value found to be in error by the CDB. If ENRHEC = 0, the HEC error counter is disabled.
0B	3	SCRENA	**Scramble Enable**: If SCRENA = 1, then the scrambler / descrambler circuits in the CDB are enabled, and the payload of each cell is scrambled on transmission and descrambled on reception. If SCRENA = 0, the scrambler / descrambler circuits are disabled.
0B	2	ENTHEG	**Enable Transmit HEC Generation**: If ENTHEG = 1, the CDB ignores the HEC (Header Error Check) value in the transmit cell overhead and calculates a proper HEC with the COSET polynomial (01010101) being added mod2. If ENTHEG = 0, the HEC value that is received at the terminal transmit input of the CDB will be preserved.
0B	1	ENCOR	**Enable data Correction**: If ENCOR = 1 and there is a single bit error in the header as determined by the HEC value, then the bit error will be corrected and the CCCOR counter (byte address 1A Hex) is incremented. If there are multiple bit errors in the cell header, then no correction is made. If ENCOR = 0, then no corrections are made even if it were possible.
0B	0	DCHEC	**Discard Cell on HEC error**: If DCHEC = 1 and if the CDB detects an HEC error, the errant cell will be discarded. If DCHEC = 0, an HEC error does not cause the cell to be dropped.

Note 1: This bit is not used in UTOPIA mode.

Idle Cell and Cell VPI, VCI Presets

Address (Hex)	Bit	Symbol	Description
10	7 - 0	IDLEW	**Idle Word**: This byte value is sent as data payload when the CDB transmits an idle cell. If SCRENA = 1, then the contents of the data are scrambled before transmission. Idle cells will have a header value of all-zeros, except for the LSB of the fourth byte (the CLP bit) which will be set equal to control bit ZEROC, bit 7 of register 0B Hex.
11 - 12	2 bytes	VCIAD	**Virtual Circuit Identifier (VCI) Address**: The VCI is two bytes long in the cell header. These two bytes in the bit map are used in conjunction with VCIRM bytes to test the value of the VCI in the received cell.
13 - 14	2 bytes	VCIRM	**VCI Range Mask**: These two bytes are used with the two bytes of VCIAD to find a VCI match. In words, if a bit of the VCI is the same as the corresponding bit of VCIAD or if the corresponding bit of VCIRM is set then there is a match for that bit. This is done over the 16 bits of the VCI. If all 16 bits show a match, then there is a VCI match. The RCAM (Receive Cell Address Match) lead is forced high for the duration of the cell if both VCI and VPI values are matched.
15 - 16	2 bytes	VPIAD	**Virtual Path Identifier (VPI) Address**: The first four bits of address 15 are not used. This allows 12 bits for the VPI address register, and this is the maximum number of bits used for the VPI in an ATM cell. These 12 bits are used with 12 bits of the VPIRM register to test the value of the VPI in the received cell.
17 - 18	2 bytes	VPIRM	**VPI Range Mask**: These two bytes (12 bits, the first four bits of address 17 are not used) are used with the 12 bits of VPIAD to find a VPI match. In words, if a bit of the VPI is the same as the corresponding bit of VPIAD or if the corresponding bit of VPIRM is set then there is a match for that bit. This is done over the 12 bits of the VPI. If all 12 bits show a match, then there is a VPI match. The RCAM (Receive Cell Address Match) lead is forced high for the duration of the cell if both VCI and VPI values are matched. If UNIMODE =1, then the leading nibble of VPIAD must be set to 0000, and leading nibble of VPIRM must be set to 1111. This causes any value of the GFC nibble to be matched.

Counters (All counters are non-saturating; they roll from maximum value to zero. They are not cleared when read, so that event counts for a time period may be found by subtracting the start-of-period value from the end-of-period value, allowing for rollovers.)

Address (Hex)	Bit	Symbol	Description
19	7 - 0	CEHEC	**Cell Error Header Error Check (HEC)**: This counter is incremented when there is an error in the HEC value indicating either single or multiple errors in the ATM cell header. This counter is enabled by the ENRHEC bit in register 0B Hex.
1A	7 - 0	CCCOR	**Counter, Cells Corrected**: This counter is incremented for every ATM cell header that is corrected for a single bit error. This counter is enabled by the ENCOR bit in register 0B Hex.
1B	7 - 0	CDRFF	**Cells Discarded Receive FIFO Full**: This counter is incremented when the 3-cell output FIFO of the CDB is forced to overflow.
1C - 1D	2 bytes	RBUSYC	**Receive Busy Cell Counter**: This 16-bit counter is incremented for each complete received busy cell. A busy cell is one that is not discarded, not a non-user type, and not an OAM F4 flow type.
1E - 1F	2 bytes	TBUSYC	**Transmit Busy Cell Counter**: This 16-bit counter is incremented for each complete transmitted busy cell, as defined above for RBUSYC.

PACKAGING

The CDB device is packaged in a 144-pin plastic quad flat pack suitable for socket or surface mounting. All dimensions shown are in millimeters and are nominal unless otherwise noted.

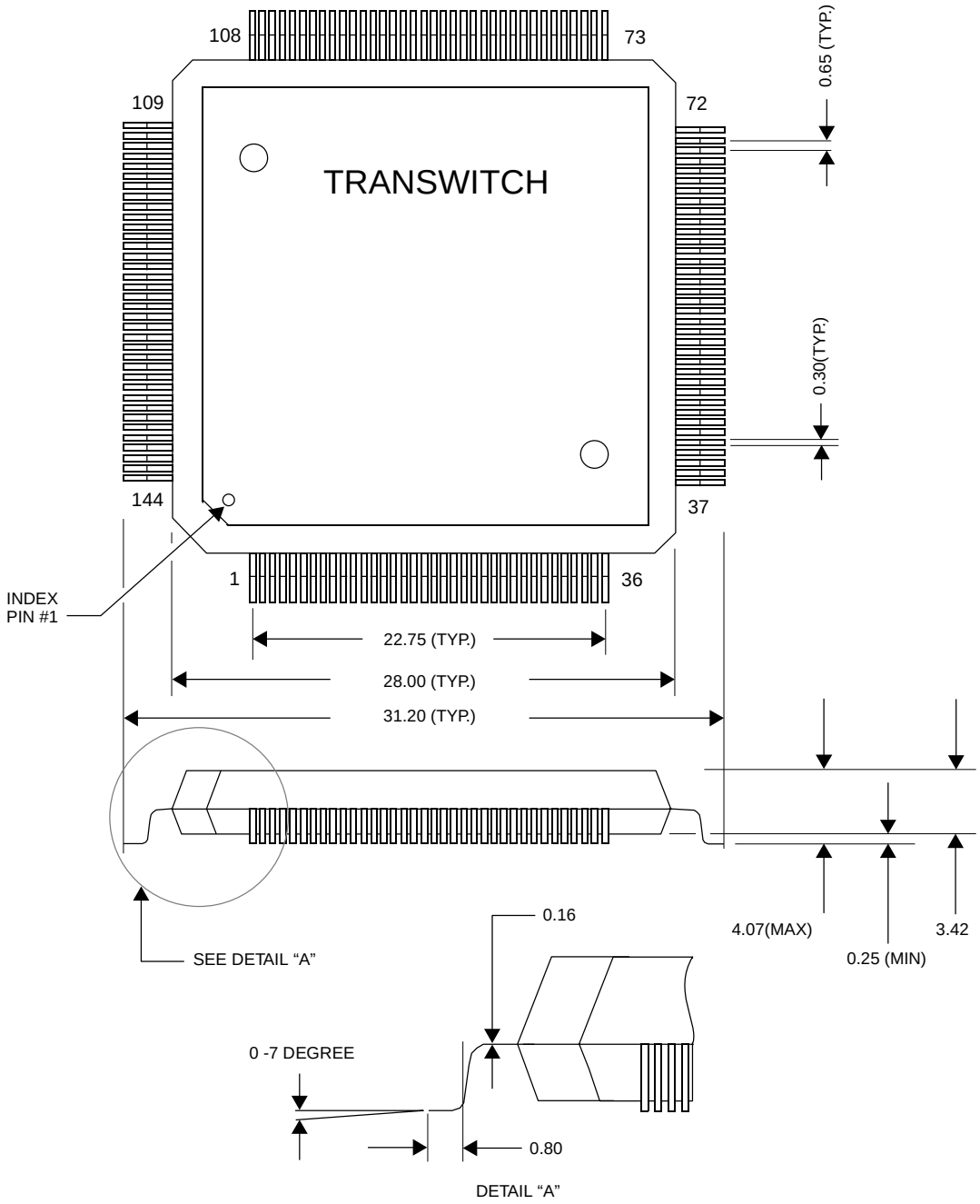


Figure 33. CDB 144-Pin Plastic Quad Flat Pack

ORDERING INFORMATION

Part Number:	TXC-05150-BIPQ	144-Pin Plastic Quad Flat Pack

RELATED PRODUCTS

TXC-02301, SYN155 VLSI Device (155-Mbit/s Synchronizer, Data Output). Provides complete STS-3/STM-1 frame synchronization function on incoming 155 Mbit/s signals in a single low power CMOS unit.

TXC-02302, SYN155C VLSI Device (155-Mbit/s Synchronizer, Clock and Data Output). This device is similar to the SYN155. It has both clock and data outputs on the line side.

TXC-03001, SOT-1 VLSI Device (SONET STS-1 Overhead Terminator). Provides the SONET interface to any payload and access to all of the transport and path overhead defined for an STS-1 SONET signal.

TXC-03003, SOT-3 VLSI Device (STM-1/STS-3/STS-3c Overhead Terminator). This programmable SONET/SDH overhead terminator performs section, line and path overhead processing for STM-1/STS-3/STS-3c signals.

TXC-03401, DS3F VLSI Device (DS3 Framer). Maps broadband payloads into the DS3 frame format. Operates in either the C-bit parity or M13 operating modes.

TXC-05501, SARA-S VLSI Device (ATM/SMDS Segmentation Controller). Simultaneously segments up to 8000 packets into ATM/SMDS cells.

TXC-05601, SARA-R VLSI Device (ATM/SMDS Reassembly Controller). Simultaneously reassembles ATM/SMDS cells back into up to 8000 packets.

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute (ANSI)
11 West 42nd Street
New York, New York 10036

Tel: 212-642-4900
Fax: 212-302-1286

Bellcore (U.S.A.):

Bellcore
Attention - Customer Service
8 Corporate Place
Piscataway, NJ 08854

Tel: 800-521-CORE (In U.S.A.)
Tel: 908-699-5800
Fax: 908-336-2559

ITU:

Publication Services of ITU
Place des Nations
CH 1211
Geneve 20, Switzerland

Tel: 41-22-730-5285
Fax: 41-22-730-5991

TTC (Japan):

TTC Standard Publishing Group of the
Telecommunications Technology Committee
2nd Floor, Hamamatsucho - Suzuki Building,
1 2-11, Hamamatsu-cho, Minato-ku, Tokyo

Tel: 81-3-3432-1551
Fax: 81-3-3432-1553

LIST OF DATA SHEET CHANGES

This change list identifies those areas within this updated CDB Data Sheet that have technical differences relative to the superseded CDB Data Sheet:

Updated CDB Data Sheet:	Edition 4, October 1994
Superseded CDB Data Sheet:	Edition 3, February 1994

The page numbers indicated below of this updated data sheet include changes relative to the superseded data sheet.

Page Number of Updated Data Sheet	Summary of the Change
All	Changed edition number and date.
1	Added item 3 to Feature List.
1	Changed items 1, 6, 8 and 9 of Feature List.
1	Made minor clarification to the figure.
2	Added Table of Contents.
3	Made minor change to Figure 1.
3	Changed Receive Path section on the third sentence from header error check to Header Error Control (HEC).
4	Deleted E3 row from the first table and modified Interface Device column on DS3.
4	Added UTOPIA to the second table.
4	Modified the last sentence on Microprocessor Interface section
5	Modified pins 2, 76, 100, 104, 114, 115 and 142 on Figure 2.
6	Deleted pin no. 2 from GND.
6	Made minor clarification to Name/Function column on RD/$\overline{WR}$ (pin 10) and $\overline{RD}$ (pin 11).
6	Added a note to the bottom to explain Type column heading.
7	Made minor clarification to the title on Name/Function column of RDY/$\overline{DTACK}$ (pin 24).

Page Number of Updated Data Sheet	Summary of the Change
7	Changed Type column from CMOS to CMOS4mA on INTER (pin 25).
7	Added PRCLK.
7	Changed Name/Function column on $\overline{\text{RESET}}$, SMODE0, SMODE1 and RXD(7-0).
8	Made change to Name/Function column on RXF1 (pin 47), TSOC (pin 53), TXD(7-0), TXF4 (pin 67), TXF1 (pin 69) and TICK (pin 71).
8	Added note to Line Input and Line Output sections.
8-10	Changed all Type column from CMOS to CMOS4mA.
9-10	Changed Name/Function column on RCAM (pin 109), RFLD (pin 112), RCAV/RxSOC (pin 114), RCF1/RxCLAV (pin 115), RTD(17-0), RICLK (pin 141), RCF2/$\overline{\text{RxENB}}$ (pin 142), RRES (pin 143), TCF1/TxCLAV (pin 76), TOCLK (pin 77), TTD(17, 15-0), $\overline{\text{TTD16}}$/TxSOC (pin 100), TICLK (pin 103), TCF2/$\overline{\text{TxENB}}$ (pin 104), $\overline{\text{TRES}}$ (pin 105), TDO (pin 26), $\overline{\text{TRS}}$ (pin 28), TMS (pin 29), TDI (pin 30), TCK (pin 31), SCANTEST (pin 33) and SCANEN (pin 34).
9-10	Changed Symbol column on pins 114, 115, 142, 76, 100 and 104.
10	Changed all Type column from TTL to TTLp.
11	Changed Max column on T_J and added Continuous Power Dissipation row to Absolute Maximum Ratings section.
11	Added Type column to I_{DD}; added Type and Test Conditions columns to P_{DD}.
12	Changed heading from Input and Output Parameters to Input, Output and I/O Parameters.
12	Changed first table title from Input Parameters For TTL to Input Parameters For TTLp* and added note to the table.
12	Changed Test Conditions column on V_{OL} of Output Parameters For CMOS4mA section.
12	Added a note to the bottom.
13	Made change to Figure 3 and the table.
14	Made change to Figure 4 and the table; added Note.
15	Made change to Figure 5 and the table.
16	Made change to Figure 6 and the table; added Note 3.
17	Made change to Figure 7 and the table; added Note.
18-19	Made change to Figure 8 and the table; added Note.
20	Made change to Figure 9, the table and the notes; added Note 3.
21	Added Figure 10.

Page Number of Updated Data Sheet	Summary of the Change
22-57	Re-ordered all the Figures from Figure 11 to Figure 33.
22	Made change to Figure 11, the table and the note.
23	Made change to Figure 12, the table and the note.
24	Made change to Figure 13 and the table.
25	Made change to Figure 14 and the table.
26	Made change to Figure 15 and the table.
27	Made change to Figure 16 and the table.
28	Added Figure 17.
29	Added Figure 18.
30	Added Figure 19.
31	Made minor change to Figure 20, the table and the note.
32	Made minor change to Figure 21, the table and the note.
33	Made minor change to Figure 22 and the note; added Min to $t_{PW(1)}$.
34	Made minor change to Figure 23, the table and the note.
35-56	Changed Operation section.
57	Made changes in Figure 33.
58	Deleted item 6 from Related Products section.
59	Changed Standards Documentation Sources from CCITT to ITU.

- NOTES -

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