



## Wireless Components

ASK/FSK Transmitter 868/433 MHz

TDA 5100 Version 2.1

Addendum for the extended temperature range -40 to +105°C

Specification June 2001

<b>Revision History</b>		
Current Version: 2.1 as of 12.06..2001		
Previous Version: 2.0, November 2000		
Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)
2-7	2-7	Limits tightened for: Supply Current, Saturation Voltage of Clock Driver Output and Output Power
4,7	4,7	Supply-voltage dependency of Output Power added as footnote
4,7	4,7	Limits corrected for Input current CSEL

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## 1. Extended Absolute Maximum Ratings

*The AC/DC characteristic limits are not guaranteed. The maximum ratings must not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC may result.*

Table 1-1					
Parameter	Symbol	Limit Values		Unit	Remarks
		Min	Max		
Junction Temperature	$T_J$	-40	150	°C	
Storage Temperature	$T_s$	-40	125	°C	
Thermal Resistance	$R_{thSA}$		230	K/W	
ESD integrity, all pins	$V_{ESD}$	-1	+1	kV	100pF, 1500 $\Omega$

Ambient Temperature under bias:  $T_A = -40$  to  $+105^\circ\text{C}$

## 2. Extended Operating Range

Within the operational range the IC operates as described in the circuit description. The AC / DC characteristic limits are not guaranteed

Table 2-1					
Parameter	Symbol	Limit Values		Unit	Test Conditions
		Min	Max		
Supply voltage	$V_S$	2.1	4.0	V	$-40^\circ\text{C}$ to $+85^\circ\text{C}$
Supply voltage	$V_S$	2.2	4.0	V	$+85^\circ\text{C}$ to $+105^\circ\text{C}$
Ambient temperature	$T_A$	-40	105	°C	

### 3. Extended AC/DC Characteristics

#### 3.1. AC/DC Characteristics at 3 V, -40°C ... +105°C

**Table 3-1 Supply Voltage  $V_S = 3\text{ V}$ , Ambient temperature  $T_{\text{amb}} = -40^\circ\text{C} \dots +105^\circ\text{C}$** 

Parameter	Symbol	Limit Values			Unit	Test Conditions
		Min	Typ	Max		
<b>Current consumption</b>						
Stand-by mode	$I_{S\text{ PDWN}}$			1000	nA	$V$ (Pins 1, 6 and 7) < 0.2 V
PLL enable mode	$I_{S\text{ PLL\_EN}}$		3.3	4.6	mA	
Transmit mode	$I_{S\text{ TRANSM}}$		7	8.7	mA	Load tank see Specification TDA5100V2.1 Figures 4-1 and 4-2
<b>Power Down Mode Control (Pin 1)</b>						
Stand-by mode	$V_{\text{PDWN}}$	0		0.5	V	$V_{\text{ASKDTA}} < 0.2\text{ V}$ $V_{\text{FSKDTA}} < 0.2\text{ V}$
PLL enable mode	$V_{\text{PDWN}}$	1.5		$V_S$	V	$V_{\text{ASKDTA}} < 0.5\text{ V}$
Transmit mode	$V_{\text{PDWN}}$	1.5		$V_S$	V	$V_{\text{ASKDTA}} > 1.5\text{ V}$
Input bias current PDWN	$I_{\text{PDWN}}$			30	$\mu\text{A}$	$V_{\text{PDWN}} = V_S$
<b>Low Power Detect Output (Pin 2)</b>						
Internal pull up current	$I_{\text{LPD1}}$	30			$\mu\text{A}$	$V_S = 2.3\text{ V} \dots V_S$
Input current low voltage	$I_{\text{LPD2}}$	0.7			mA	$V_S = 1.9\text{ V} \dots 2.05\text{ V}$
<b>Loop Filter (Pin 4)</b>						
VCO tuning voltage	$V_{\text{LF}}$	$V_S - 1.91$		$V_S - 0.45$	V	$f_{\text{VCO}} = 869\text{ MHz}$
Output frequency range 868 MHz-band	$f_{\text{OUT, 868}}$	865	869	874	MHz	$V_S - V_{\text{LF}} = 0.38 \dots 2.01\text{ V}$ $V_{\text{FSEL}} = V_S$
Output frequency range 433 MHz-band	$f_{\text{OUT, 433}}$	432.5	434.5	437.5	MHz	$V_S - V_{\text{LF}} = 0.38 \dots 2.01\text{ V}$ $V_{\text{FSEL}} = 0\text{ V}$
<b>ASK Modulation Data Input (Pin 6)</b>						
ASK Transmit disabled	$V_{\text{ASKDTA}}$	0		0.5	V	
ASK Transmit enabled	$V_{\text{ASKDTA}}$	1.5		$V_S$	V	
Input bias current ASKDTA	$I_{\text{ASKDTA}}$			30	$\mu\text{A}$	$V_{\text{ASKDTA}} = V_S$
Input bias current ASKDTA	$I_{\text{ASKDTA}}$	-20			$\mu\text{A}$	$V_{\text{ASKDTA}} = 0\text{ V}$
ASK data rate	$f_{\text{ASKDTA}}$			20	kHz	

**Table 3-1 Supply Voltage  $V_S = 3\text{ V}$ , Ambient temperature  $T_{\text{amb}} = -40^\circ\text{C} \dots +105^\circ\text{C}$** 

Parameter	Symbol	Limit Values			Unit	Test Conditions
		Min	Typ	Max		
<b>FSK Modulation Data Input (Pin 7)</b>						
FSK Switch on	$V_{\text{FSKDTA}}$	0		0.5	V	
FSK Switch off	$V_{\text{FSKDTA}}$	1.5		$V_S$	V	
Input bias current FSKDTA	$I_{\text{FSKDTA}}$			30	$\mu\text{A}$	$V_{\text{FSKDTA}} = V_S$
Input bias current FSKDTA	$I_{\text{FSKDTA}}$	-20			$\mu\text{A}$	$V_{\text{FSKDTA}} = 0\text{ V}$
FSK data rate	$f_{\text{FSKDTA}}$			20	kHz	
<b>Clock Driver Output (Pin 8)</b>						
Output current (Low)	$I_{\text{CLKOUT}}$	0.95			mA	$V_{\text{CLKOUT}} = V_S$
Output current (High)	$I_{\text{CLKOUT}}$			5	$\mu\text{A}$	$V_{\text{CLKOUT}} = V_S$
Saturation Voltage (Low) <sup>1)</sup>	$V_{\text{SATL}}$			0.49	V	$I_{\text{CLKOUT}} = 0.75\text{ mA}$
<b>Clock Divider Control (Pin 9)</b>						
Setting Clock Driver output frequency $f_{\text{CLKOUT}}=3.39\text{ MHz}$	$V_{\text{CLKDIV}}$	0		0.2	V	
Setting Clock Driver output frequency $f_{\text{CLKOUT}}=847.5\text{ kHz}$	$V_{\text{CLKDIV}}$				V	pin open
Input bias current CLKDIV	$I_{\text{CLKDIV}}$			30	$\mu\text{A}$	$V_{\text{CLKDIV}} = V_S$
Input bias current CLKDIV	$I_{\text{CLKDIV}}$	-20			$\mu\text{A}$	$V_{\text{CLKDIV}} = 0\text{ V}$
<b>Crystal Oscillator Input (Pin 10)</b>						
Load capacitance	$C_{\text{COSCmax}}$			5	pF	
Serial Resistance of the crystal				100	$\Omega$	$f = 6.78\text{ MHz}$
Input inductance of the COSC pin			12		$\mu\text{H}$	$f = 6.78\text{ MHz}$
Serial Resistance of the crystal				100	$\Omega$	$f = 13.56\text{ MHz}$
Input inductance of the COSC pin			11		$\mu\text{H}$	$f = 13.56\text{ MHz}$
<b>FSK Switch Output (Pin 11)</b>						
On resistance	$R_{\text{FSKOUT}}$			220	$\Omega$	$V_{\text{FSKDTA}} = 0\text{ V}$
On capacitance	$C_{\text{FSKOUT}}$			6	pF	$V_{\text{FSKDTA}} = 0\text{ V}$
Off resistance	$R_{\text{FSKOUT}}$	10			k $\Omega$	$V_{\text{FSKDTA}} = V_S$
Off capacitance	$C_{\text{FSKOUT}}$			1.5	pF	$V_{\text{FSKDTA}} = V_S$

**Table 3-1 Supply Voltage  $V_S = 3\text{ V}$ , Ambient temperature  $T_{\text{amb}} = -40^\circ\text{C} \dots +105^\circ\text{C}$** 

Parameter	Symbol	Limit Values			Unit	Test Conditions
		Min	Typ	Max		
<b>Power Amplifier Output (Pin 14)</b>						
Output Power <sup>2)</sup> at 434 MHz transformed to 50 Ohm	$P_{\text{OUT}434}$	2.3	5	6.5	dBm	$f_{\text{OUT}} = 434\text{ MHz}$ $V_{\text{FSEL}} = 0\text{ V}$
Output Power <sup>3)</sup> at 868 MHz transformed to 50 Ohm.	$P_{\text{OUT}868}$	-2.8	2	5.1	dBm	$f_{\text{OUT}} = 868\text{ MHz}$ $V_{\text{FSEL}} = V_S$
<b>Frequency Range Selection (Pin 15)</b>						
Transmit frequency 434 MHz	$V_{\text{FSEL}}$	0		0.5	V	
Transmit frequency 868 MHz	$V_{\text{FSEL}}$				V	pin open
Input bias current FSEL	$I_{\text{FSEL}}$			30	$\mu\text{A}$	$V_{\text{FSEL}} = V_S$
Input bias current FSEL	$I_{\text{FSEL}}$	-20			$\mu\text{A}$	$V_{\text{FSEL}} = 0\text{ V}$
<b>Crystal Frequency Selection (Pin 16)</b>						
Crystal frequency 6.78 MHz	$V_{\text{CSEL}}$	0		0.2	V	
Crystal frequency 13.56 MHz	$V_{\text{CSEL}}$				V	pin open
Input bias current CSEL	$I_{\text{CSEL}}$			50	$\mu\text{A}$	$V_{\text{CSEL}} = V_S$
Input bias current CSEL	$I_{\text{CSEL}}$	-25			$\mu\text{A}$	$V_{\text{CSEL}} = 0\text{ V}$

- 1) Derating linearly to a saturation voltage of max. 150 mV at  $I_{\text{CLKOUT}} = 0\text{ mA}$
- 2) Matching circuitry as used in the 50 Ohm-Output Testboard for 434 MHz operation.  
Range @ 3.0 V, +25°C: 5.0 dBm +/- 1.0 dBm  
Temperature dependency at 3.0 V: +0.5 dBm@-40°C and -1.7 dBm@+105°C, reference +25°C
- 3) Matching circuitry as used in the 50 Ohm-Output Testboard for 868 MHz operation.  
Range @ 3.0 V, +25°C: 2.0 dBm +/- 2.0 dBm  
Temperature dependency at 3.0 V: +1.1 dBm@-40°C and -2.8 dBm@+105°C, reference +25°C

A higher load impedance reduces the temperature dependency.

### 3.2. AC/DC Characteristics at 2.1 V ... 4.0 V, -40°C ... +105°C

**Table 3-2 Supply Voltage  $V_S = 2.1\text{ V} \dots 4.0\text{ V}$ , Ambient temperature  $T_{\text{amb}} = -40^\circ\text{C} \dots +105^\circ\text{C}$** 

Parameter	Symbol	Limit Values			Unit	Test Conditions
		Min	Typ	Max		
<b>Current consumption</b>						
Stand-by mode	$I_{S\text{ PDWN}}$			1000	nA	V (Pins 1, 6 and 7) < 0.2 V
PLL enable mode	$I_{S\text{ PLL\_EN}}$		3.3	4.8	mA	
Transmit mode	$I_{S\text{ TRANSM}}$		7	9.2	mA	Load tank see Specification TDA5100V2.1 Figures 4-1 and 4-2
<b>Power Down Mode Control (Pin 1)</b>						
Stand-by mode	$V_{\text{PDWN}}$	0		0.5	V	$V_{\text{ASKDTA}} < 0.2\text{ V}$ $V_{\text{FSKDTA}} < 0.2\text{ V}$
PLL enable mode	$V_{\text{PDWN}}$	1.5		$V_S$	V	$V_{\text{ASKDTA}} < 0.5\text{ V}$
Transmit mode	$V_{\text{PDWN}}$	1.5		$V_S$	V	$V_{\text{ASKDTA}} > 1.5\text{ V}$
Input bias current PDWN	$I_{\text{PDWN}}$			30	$\mu\text{A}$	$V_{\text{PDWN}} = V_S$
<b>Low Power Detect Output (Pin 2)</b>						
Internal pull up current	$I_{\text{LPD1}}$	30			$\mu\text{A}$	$V_S = 2.3\text{ V} \dots V_S$
Input current low voltage	$I_{\text{LPD2}}$	0.7			mA	$V_S = 1.9\text{ V} \dots 2.1\text{ V}$
<b>Loop Filter (Pin 4)</b>						
VCO tuning voltage	$V_{\text{LF}}$	$V_S - 1.91$		$V_S - 0.45$	V	$f_{\text{VCO}} = 869\text{ MHz}$
Output frequency range 868 MHz-band	$f_{\text{OUT, 868}}$	865	869	874	MHz	$V_S - V_{\text{LF}} = 0.38 \dots 2.01\text{ V}$ $V_{\text{FSEL}} = V_S$
Output frequency range 433 MHz-band	$f_{\text{OUT, 433}}$	432.5	434.5	437	MHz	$V_S - V_{\text{LF}} = 0.38 \dots 2.01\text{ V}$ $V_{\text{FSEL}} = 0\text{ V}$
<b>ASK Modulation Data Input (Pin 6)</b>						
ASK Transmit disabled	$V_{\text{ASKDTA}}$	0		0.5	V	
ASK Transmit enabled	$V_{\text{ASKDTA}}$	1.5		$V_S$	V	
Input bias current ASKDTA	$I_{\text{ASKDTA}}$			30	$\mu\text{A}$	$V_{\text{ASKDTA}} = V_S$
Input bias current ASKDTA	$I_{\text{ASKDTA}}$	-20			$\mu\text{A}$	$V_{\text{ASKDTA}} = 0\text{ V}$
ASK data rate	$f_{\text{ASKDTA}}$			20	kHz	

**Table 3-2 Supply Voltage  $V_S = 2.1\text{ V} \dots 4.0\text{ V}$ , Ambient temperature  $T_{\text{amb}} = -40^\circ\text{C} \dots +105^\circ\text{C}$** 

Parameter	Symbol	Limit Values			Unit	Test Conditions
		Min	Typ	Max		
<b>FSK Modulation Data Input (Pin 7)</b>						
FSK Switch on	$V_{\text{FSKDTA}}$	0		0.5	V	
FSK Switch off	$V_{\text{FSKDTA}}$	1.5		$V_S$	V	
Input bias current FSKDTA	$I_{\text{FSKDTA}}$			30	$\mu\text{A}$	$V_{\text{FSKDTA}} = V_S$
Input bias current FSKDTA	$I_{\text{FSKDTA}}$	-20			$\mu\text{A}$	$V_{\text{FSKDTA}} = 0\text{ V}$
FSK data rate	$f_{\text{FSKDTA}}$			20	kHz	
<b>Clock Driver Output (Pin 8)</b>						
Output current (Low)	$I_{\text{CLKOUT}}$	0.9			mA	$V_{\text{CLKOUT}} = V_S$
Output current (High)	$I_{\text{CLKOUT}}$			5	$\mu\text{A}$	$V_{\text{CLKOUT}} = V_S$
Saturation Voltage (Low) <sup>1)</sup>	$V_{\text{SATL}}$			0.47	V	$I_{\text{CLKOUT}} = 0.7\text{ mA}$
<b>Clock Divider Control (Pin 9)</b>						
Setting Clock Driver output frequency $f_{\text{CLKOUT}}=3.39\text{ MHz}$	$V_{\text{CLKDIV}}$	0		0.2	V	
Setting Clock Driver output frequency $f_{\text{CLKOUT}}=847.5\text{ kHz}$	$V_{\text{CLKDIV}}$				V	pin open
Input bias current CLKDIV	$I_{\text{CLKDIV}}$			30	$\mu\text{A}$	$V_{\text{CLKDIV}} = V_S$
Input bias current CLKDIV	$I_{\text{CLKDIV}}$	-20			$\mu\text{A}$	$V_{\text{CLKDIV}} = 0\text{ V}$
<b>Crystal Oscillator Input (Pin 10)</b>						
Load capacitance	$C_{\text{COSCmax}}$			5	pF	
Serial Resistance of the crystal				100	$\Omega$	$f = 6.78\text{ MHz}$
Input inductance of the COSC pin			12		$\mu\text{H}$	$f = 6.78\text{ MHz}$
Serial Resistance of the crystal				100	$\Omega$	$f = 13.56\text{ MHz}$
Input inductance of the COSC pin			11		$\mu\text{H}$	$f = 13.56\text{ MHz}$
<b>FSK Switch Output (Pin 11)</b>						
On resistance	$R_{\text{FSKOUT}}$			220	$\Omega$	$V_{\text{FSKDTA}} = 0\text{ V}$
On capacitance	$C_{\text{FSKOUT}}$			6	pF	$V_{\text{FSKDTA}} = 0\text{ V}$
Off resistance	$R_{\text{FSKOUT}}$	10			k $\Omega$	$V_{\text{FSKDTA}} = V_S$
Off capacitance	$C_{\text{FSKOUT}}$			1.5	pF	$V_{\text{FSKDTA}} = V_S$

**Table 3-2 Supply Voltage  $V_S = 2.1\text{ V} \dots 4.0\text{ V}$ , Ambient temperature  $T_{\text{amb}} = -40^\circ\text{C} \dots +105^\circ\text{C}$** 

Parameter	Symbol	Limit Values			Unit	Test Conditions
		Min	Typ	Max		
<b>Power Amplifier Output (Pin 14)</b>						
Output Power <sup>2)</sup> at 434 MHz transformed to 50 Ohm. $V_{\text{FSEL}} = 0\text{ V}$	$P_{\text{OUT}, 434}$	0.6	2.5	3.6	dBm	$V_S = 2.2\text{ V}$
	$P_{\text{OUT}, 434}$	2.3	5	6.5	dBm	$V_S = 3.0\text{ V}$
	$P_{\text{OUT}, 434}$	2.6	6.8	9.4	dBm	$V_S = 4.0\text{ V}$
Output Power <sup>3)</sup> at 868 MHz transformed to 50 Ohm. $V_{\text{FSEL}} = V_S$	$P_{\text{OUT}, 868}$	-2.9	0.5	2.2	dBm	$V_S = 2.2\text{ V}$
	$P_{\text{OUT}, 868}$	-2.8	2	5.1	dBm	$V_S = 3.0\text{ V}$
	$P_{\text{OUT}, 868}$	-2.7	3.2	7.4	dBm	$V_S = 4.0\text{ V}$
<b>Frequency Range Selection (Pin 15)</b>						
Transmit frequency 433 MHz	$V_{\text{FSEL}}$	0		0.5	V	
Transmit frequency 868 MHz	$V_{\text{FSEL}}$				V	pin open
Input bias current FSEL	$I_{\text{FSEL}}$			30	$\mu\text{A}$	$V_{\text{FSEL}} = V_S$
Input bias current FSEL	$I_{\text{FSEL}}$	-20			$\mu\text{A}$	$V_{\text{FSEL}} = 0\text{ V}$
<b>Crystal Frequency Selection (Pin 16)</b>						
Crystal frequency 6.78 MHz	$V_{\text{CSEL}}$	0		0.2	V	
Crystal frequency 13.56 MHz	$V_{\text{CSEL}}$				V	pin open
Input bias current CSEL	$I_{\text{CSEL}}$			50	$\mu\text{A}$	$V_{\text{CSEL}} = V_S$
Input bias current CSEL	$I_{\text{CSEL}}$	-25			$\mu\text{A}$	$V_{\text{CSEL}} = 0\text{ V}$

- 1) Derating linearly to a saturation voltage of max. 150 mV at  $I_{\text{CLKOUT}} = 0\text{ mA}$
- 2) Matching circuitry as used in the 50 Ohm-Output Testboard for 434 MHz operation.  
 Range @ 2.2 V, +25°C: 2.5 dBm +/- 0.7 dBm  
 Temperature dependency at 2.2 V: +0.4 dBm@-40°C and -1.2 dBm@+105°C, reference +25°C  
 Range @ 3.0 V, +25°C: 5.0 dBm +/- 1.0 dBm  
 Temperature dependency at 3.0 V: +0.5 dBm@-40°C and -1.7 dBm@+105°C, reference +25°C  
 Range @ 4.0 V, +25°C: 6.8 dBm +/- 2.0 dBm  
 Temperature dependency at 4.0 V: +0.6 dBm@-40°C and -2.2 dBm@+105°C, reference +25°C
- 3) Matching circuitry as used in the 50 Ohm-Output Testboard for 868 MHz operation.  
 Range @ 2.2 V, +25°C: 0.5 dBm +/- 1.0 dBm  
 Temperature dependency at 2.2 V: +0.7 dBm@-40°C and -2.4 dBm@+105°C, reference +25°C  
 Range @ 3.0 V, +25°C: 2.0 dBm +/- 2.0 dBm  
 Temperature dependency at 3.0 V: +1.1 dBm@-40°C and -2.8 dBm@+105°C, reference +25°C  
 Range @ 4.0 V, +25°C: 3.2 dBm +/- 2.7 dBm  
 Temperature dependency at 4.0 V: +1.5 dBm@-40°C and -3.2 dBm@+105°C, reference +25°C

A smaller load impedance reduces the supply-voltage dependency.  
 A higher load impedance reduces the temperature dependency.