Wireless Components

ASK/FSK Transmitter 868/433 MHz

TDA 5100 Version 2.1

Addendum for the extended temperature range -40 to +105°C

Specification June 2001

Revision History		
Current Version: 2.1 as of 12.06..2001		
Previous Version: 2.0, November 2000		
Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)
2-7	2-7	Limits tightened for: Supply Current, Saturation Voltage of Clock Driver Output and Output Power
4,7	4,7	Supply-voltage dependency of Output Power added as footnote
4,7	4,7	Limits corrected for Input current CSEL

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1. Extended Absolute Maximum Ratings

The AC/DC characteristic limits are not guaranteed. The maximum ratings must not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC may result.

Table 1-1

Parameter	Symbol	Limit Values		Unit	Remarks
		Min	Max		
Junction Temperature	T_J	-40	150	°C	
Storage Temperature	T_s	-40	125	°C	
Thermal Resistance	R_{thSA}		230	K/W	
ESD integrity, all pins	V_{ESD}	-1	+1	kV	100pF, 1500 Ω

Ambient Temperature under bias: T_A=-40 to +105°C

2. Extended Operating Range

Within the operational range the IC operates as described in the circuit description. The AC / DC characteristic limits are not guaranteed

Table 2-1

Parameter	Symbol	Limit Values		Unit	Test Conditions
		Min	Max		
Supply voltage	V_S	2.1	4.0	V	-40°C to +85°C
Supply voltage	V_S	2.2	4.0	V	+85°C to +105°C
Ambient temperature	T_A	-40	105	°C	

3. Extended AC/DC Characteristics

3.1. AC/DC Characteristics at 3 V, -40°C ... +105°C

Table 3-1 Supply Voltage V_S = 3 V, Ambient temperature T_{amb} = -40°C ... +105°C

Parameter	Symbol	Limit Values			Unit	Test Conditions
		Min	Typ	Max		
Current consumption						
Stand-by mode	$I_{S\ PDWN}$			1000	nA	V (Pins 1, 6 and 7) < 0.2 V
PLL enable mode	$I_{S\ PLL\_EN}$		3.3	4.6	mA	
Transmit mode	$I_{S\ TRANSM}$		7	8.7	mA	Load tank see Specification TDA5100V2.1 Figures 4-1 and 4-2
Power Down Mode Control (Pin 1)						
Stand-by mode	V_{PDWN}	0		0.5	V	V_{ASKDTA} < 0.2 V V_{FSKDTA} < 0.2 V
PLL enable mode	V_{PDWN}	1.5		V_S	V	V_{ASKDTA} < 0.5 V
Transmit mode	V_{PDWN}	1.5		V_S	V	V_{ASKDTA} > 1.5 V
Input bias current PDWN	I_{PDWN}			30	µA	$V_{PDWN} = V_S$
Low Power Detect Output (Pin 2)						
Internal pull up current	I_{LPD1}	30			µA	V_S = 2.3 V ... V_S
Input current low voltage	I_{LPD2}	0.7			mA	V_S = 1.9 V ... 2.05 V
Loop Filter (Pin 4)						
VCO tuning voltage	V_{LF}	V_S - 1.91		V_S - 0.45	V	f_{VCO} = 869 MHz
Output frequency range 868 MHz-band	$f_{OUT,\ 868}$	865	869	874	MHz	V_S-V_{LF} = 0.38...2.01V $V_{FSEL} = V_S$
Output frequency range 433 MHz-band	$f_{OUT,\ 433}$	432.5	434.5	437.5	MHz	V_S-V_{LF} = 0.38...2.01V V_{FSEL} = 0 V
ASK Modulation Data Input (Pin 6)						
ASK Transmit disabled	V_{ASKDTA}	0		0.5	V	
ASK Transmit enabled	V_{ASKDTA}	1.5		V_S	V	
Input bias current ASKDTA	I_{ASKDTA}			30	µA	$V_{ASKDTA} = V_S$
Input bias current ASKDTA	I_{ASKDTA}	-20			µA	V_{ASKDTA} = 0 V
ASK data rate	f_{ASKDTA}			20	kHz	

Table 3-1 Supply Voltage V_S = 3 V, Ambient temperature T_{amb} = -40°C ... +105°C						
Parameter	**Symbol**	**Limit Values**			**Unit**	**Test Conditions**
		Min	**Typ**	**Max**		
FSK Modulation Data Input (Pin 7)						
FSK Switch on	V_{FSKDTA}	0		0.5	V	
FSK Switch off	V_{FSKDTA}	1.5		V_S	V	
Input bias current FSKDTA	I_{FSKDTA}			30	µA	$V_{FSKDTA} = V_S$
Input bias current FSKDTA	I_{FSKDTA}	-20			µA	V_{FSKDTA} = 0 V
FSK data rate	f_{FSKDTA}			20	kHz	
Clock Driver Output (Pin 8)						
Output current (Low)	I_{CLKOUT}	0.95			mA	$V_{CLKOUT} = V_S$
Output current (High)	I_{CLKOUT}			5	µA	$V_{CLKOUT} = V_S$
Saturation Voltage (Low)[1)]	V_{SATL}			0.49	V	I_{CLKOUT} = 0.75 mA
Clock Divider Control (Pin 9)						
Setting Clock Driver output frequency f_{CLKOUT}=3.39 MHz	V_{CLKDIV}	0		0.2	V	
Setting Clock Driver output frequency f_{CLKOUT}=847.5kHz	V_{CLKDIV}				V	pin open
Input bias current CLKDIV	I_{CLKDIV}			30	µA	$V_{CLKDIV} = V_S$
Input bias current CLKDIV	I_{CLKDIV}	-20			µA	V_{CLKDIV} = 0 V
Crystal Oscillator Input (Pin 10)						
Load capacitance	$C_{COSCmax}$			5	pF	
Serial Resistance of the crystal				100	Ω	f = 6.78 MHz
Input inductance of the COSC pin			12		µH	f = 6.78 MHz
Serial Resistance of the crystal				100	Ω	f = 13.56 MHz
Input inductance of the COSC pin			11		µH	f = 13.56 MHz
FSK Switch Output (Pin 11)						
On resistance	R_{FSKOUT}			220	Ω	V_{FSKDTA} = 0 V
On capacitance	C_{FSKOUT}			6	pF	V_{FSKDTA} = 0 V
Off resistance	R_{FSKOUT}	10			kΩ	$V_{FSKDTA} = V_S$
Off capacitance	C_{FSKOUT}			1.5	pF	$V_{FSKDTA} = V_S$

Table 3-1 Supply Voltage V_S = 3 V, Ambient temperature T_{amb} = -40°C ... +105°C						
Parameter	**Symbol**	**Limit Values**			**Unit**	**Test Conditions**
		Min	**Typ**	**Max**		
Power Amplifier Output (Pin 14)						
Output Power[2] at 434 MHz transformed to 50 Ohm	P_{OUT434}	2.3	5	6.5	dBm	f_{OUT} = 434 MHz V_{FSEL} = 0 V
Output Power [3] at 868 MHz transformed to 50 Ohm.	P_{OUT868}	-2.8	2	5.1	dBm	f_{OUT} = 868 MHz V_{FSEL} = V_S
Frequency Range Selection (Pin 15)						
Transmit frequency 434 MHz	V_{FSEL}	0		0.5	V	
Transmit frequency 868 MHz	V_{FSEL}				V	pin open
Input bias current FSEL	I_{FSEL}			30	µA	V_{FSEL} = V_S
Input bias current FSEL	I_{FSEL}	-20			µA	V_{FSEL} = 0 V
Crystal Frequency Selection (Pin 16)						
Crystal frequency 6.78 MHz	V_{CSEL}	0		0.2	V	
Crystal frequency 13.56 MHz	V_{CSEL}				V	pin open
Input bias current CSEL	I_{CSEL}			50	µA	V_{CSEL} = V_S
Input bias current CSEL	I_{CSEL}	-25			µA	V_{CSEL} = 0 V

1) Derating linearly to a saturation voltage of max. 150 mV at I_{CLKOUT} = 0 mA

2) Matching circuitry as used in the 50 Ohm-Output Testboard for 434 MHz operation.
Range @ 3.0 V, +25°C: 5.0 dBm +/- 1.0 dBm
Temperature dependency at 3.0 V: +0.5 dBm@-40°C and -1.7 dBm@+105°C, reference +25°C

3) Matching circuitry as used in the 50 Ohm-Output Testboard for 868 MHz operation.
Range @ 3.0 V, +25°C: 2.0 dBm +/- 2.0 dBm
Temperature dependency at 3.0 V: +1.1 dBm@-40°C and -2.8 dBm@+105°C, reference +25°C

A higher load impedance reduces the temperature dependency.

3.2. AC/DC Characteristics at 2.1 V ... 4.0 V, -40°C ... +105°C

Table 3-2 Supply Voltage V_S = 2.1 V ... 4.0 V, Ambient temperature T_{amb} = -40°C ... +105°C

Parameter	Symbol	Limit Values Min	Typ	Max	Unit	Test Conditions
Current consumption						
Stand-by mode	$I_{S\ PDWN}$			1000	nA	V (Pins 1, 6 and 7) < 0.2 V
PLL enable mode	$I_{S\ PLL\_EN}$		3.3	4.8	mA	
Transmit mode	$I_{S\ TRANSM}$		7	9.2	mA	Load tank see Specification TDA5100V2.1 Figures 4-1 and 4-2
Power Down Mode Control (Pin 1)						
Stand-by mode	V_{PDWN}	0		0.5	V	V_{ASKDTA} < 0.2 V V_{FSKDTA} < 0.2 V
PLL enable mode	V_{PDWN}	1.5		V_S	V	V_{ASKDTA} < 0.5 V
Transmit mode	V_{PDWN}	1.5		V_S	V	V_{ASKDTA} > 1.5 V
Input bias current PDWN	I_{PDWN}			30	µA	$V_{PDWN} = V_S$
Low Power Detect Output (Pin 2)						
Internal pull up current	I_{LPD1}	30			µA	V_S = 2.3 V ... V_S
Input current low voltage	I_{LPD2}	0.7			mA	V_S = 1.9 V ... 2.1 V
Loop Filter (Pin 4)						
VCO tuning voltage	V_{LF}	V_S - 1.91		V_S - 0.45	V	f_{VCO} = 869 MHz
Output frequency range 868 MHz-band	$f_{OUT,\ 868}$	865	869	874	MHz	V_S-V_{LF} = 0.38...2.01V $V_{FSEL} = V_S$
Output frequency range 433 MHz-band	$f_{OUT,\ 433}$	432.5	434.5	437	MHz	V_S-V_{LF} = 0.38...2.01V V_{FSEL} = 0 V
ASK Modulation Data Input (Pin 6)						
ASK Transmit disabled	V_{ASKDTA}	0		0.5	V	
ASK Transmit enabled	V_{ASKDTA}	1.5		V_S	V	
Input bias current ASKDTA	I_{ASKDTA}			30	µA	$V_{ASKDTA} = V_S$
Input bias current ASKDTA	I_{ASKDTA}	-20			µA	V_{ASKDTA} = 0 V
ASK data rate	f_{ASKDTA}			20	kHz	

Table 3-2 Supply Voltage V_S = 2.1 V ... 4.0 V, Ambient temperature T_{amb} = -40°C ... +105°C						
Parameter	**Symbol**	**Limit Values**			**Unit**	**Test Conditions**
		Min	**Typ**	**Max**		
FSK Modulation Data Input (Pin 7)						
FSK Switch on	V_{FSKDTA}	0		0.5	V	
FSK Switch off	V_{FSKDTA}	1.5		V_S	V	
Input bias current FSKDTA	I_{FSKDTA}			30	µA	$V_{FSKDTA} = V_S$
Input bias current FSKDTA	I_{FSKDTA}	-20			µA	V_{FSKDTA} = 0 V
FSK data rate	f_{FSKDTA}			20	kHz	
Clock Driver Output (Pin 8)						
Output current (Low)	I_{CLKOUT}	0.9			mA	$V_{CLKOUT} = V_S$
Output current (High)	I_{CLKOUT}			5	µA	$V_{CLKOUT} = V_S$
Saturation Voltage (Low)[1)]	V_{SATL}			0.47	V	I_{CLKOUT} = 0.7 mA
Clock Divider Control (Pin 9)						
Setting Clock Driver output frequency f_{CLKOUT}=3.39 MHz	V_{CLKDIV}	0		0.2	V	
Setting Clock Driver output frequency f_{CLKOUT}=847.5kHz	V_{CLKDIV}				V	pin open
Input bias current CLKDIV	I_{CLKDIV}			30	µA	$V_{CLKDIV} = V_S$
Input bias current CLKDIV	I_{CLKDIV}	-20			µA	V_{CLKDIV} = 0 V
Crystal Oscillator Input (Pin 10)						
Load capacitance	$C_{COSCmax}$			5	pF	
Serial Resistance of the crystal				100	Ω	f = 6.78 MHz
Input inductance of the COSC pin			12		µH	f = 6.78 MHz
Serial Resistance of the crystal				100	Ω	f = 13.56 MHz
Input inductance of the COSC pin			11		µH	f = 13.56 MHz
FSK Switch Output (Pin 11)						
On resistance	R_{FSKOUT}			220	Ω	V_{FSKDTA} = 0 V
On capacitance	C_{FSKOUT}			6	pF	V_{FSKDTA} = 0 V
Off resistance	R_{FSKOUT}	10			kΩ	$V_{FSKDTA} = V_S$
Off capacitance	C_{FSKOUT}			1.5	pF	$V_{FSKDTA} = V_S$

Parameter	Symbol	Limit Values			Unit	Test Conditions
		Min	Typ	Max		
Power Amplifier Output (Pin 14)						
Output Power 2) at 434 MHz transformed to 50 Ohm.	$P_{OUT, 434}$	0.6	2.5	3.6	dBm	V_S = 2.2 V
	$P_{OUT, 434}$	2.3	5	6.5	dBm	V_S = 3.0 V
V_{FSEL} = 0 V	$P_{OUT, 434}$	2.6	6.8	9.4	dBm	V_S = 4.0 V
Output Power 3) at 868 MHz transformed to 50 Ohm.	$P_{OUT, 868}$	-2.9	0.5	2.2	dBm	V_S = 2.2 V
	$P_{OUT, 868}$	-2.8	2	5.1	dBm	V_S = 3.0 V
V_{FSEL} = V_S	$P_{OUT, 868}$	-2.7	3.2	7.4	dBm	V_S = 4.0 V
Frequency Range Selection (Pin 15)						
Transmit frequency 433 MHz	V_{FSEL}	0		0.5	V	
Transmit frequency 868 MHz	V_{FSEL}				V	pin open
Input bias current FSEL	I_{FSEL}			30	µA	V_{FSEL} = V_S
Input bias current FSEL	I_{FSEL}	-20			µA	V_{FSEL} = 0 V
Crystal Frequency Selection (Pin 16)						
Crystal frequency 6.78 MHz	V_{CSEL}	0		0.2	V	
Crystal frequency 13.56 MHz	V_{CSEL}				V	pin open
Input bias current CSEL	I_{CSEL}			50	µA	V_{CSEL} = V_S
Input bias current CSEL	I_{CSEL}	-25			µA	V_{CSEL} = 0 V

Table 3-2 Supply Voltage V_S = 2.1 V ... 4.0 V, Ambient temperature T_{amb} = -40°C ... +105°C

1) Derating linearly to a saturation voltage of max. 150 mV at I_{CLKOUT} = 0 mA

2) Matching circuitry as used in the 50 Ohm-Output Testboard for 434 MHz operation.
Range @ 2.2 V, +25°C: 2.5 dBm +/- 0.7 dBm
Temperature dependency at 2.2 V: +0.4 dBm@-40°C and -1.2 dBm@+105°C, reference +25°C
Range @ 3.0 V, +25°C: 5.0 dBm +/- 1.0 dBm
Temperature dependency at 3.0 V: +0.5 dBm@-40°C and -1.7 dBm@+105°C, reference +25°C
Range @ 4.0 V, +25°C: 6.8 dBm +/- 2.0 dBm
Temperature dependency at 4.0 V: +0.6 dBm@-40°C and -2.2 dBm@+105°C, reference +25°C

3) Matching circuitry as used in the 50 Ohm-Output Testboard for 868 MHz operation.
Range @ 2.2 V, +25°C: 0.5 dBm +/- 1.0 dBm
Temperature dependency at 2.2 V: +0.7 dBm@-40°C and -2.4 dBm@+105°C, reference +25°C
Range @ 3.0 V, +25°C: 2.0 dBm +/- 2.0 dBm
Temperature dependency at 3.0 V: +1.1 dBm@-40°C and -2.8 dBm@+105°C, reference +25°C
Range @ 4.0 V, +25°C: 3.2 dBm +/- 2.7 dBm
Temperature dependency at 4.0 V: +1.5 dBm@-40°C and -3.2 dBm@+105°C, reference +25°C

A smaller load impedance reduces the supply-voltage dependency.
A higher load impedance reduces the temperature dependency.