- **Single-Chip Scheduler for Scheduling Available Bit Rate (ABR) Connections**
- **Used With the TNETA1575 to Provide a Complete Solution for Segmentation and Reassembly of Data on ABR Connections as Specified in the Asynchronous Transfer Mode (ATM) Forum's Traffic Management 4.0 Document (TM4.0) and ITU-TI.371**
- **Supports Scheduling of Variable-Bit-Rate Non-Real Time (VBR-nrt) Using Host-Programmable Peak Cell Rate (PCR), Sustained Cell Rate (SCR), and Maximum Burst Size (MBS)**
- **On-Chip Self-Sorting FIFO-Based Scheduler Used to Schedule the Transmission of Cells for All Connections**
- **Simultaneously Supports Both Virtual Path (VP) and Virtual Channel (VC) Level ABR Traffic Management**
- **Provides Scheduling for up to 2047 ABR Connections Required for Large-Scale LAN Emulation Installations**
- **On-Chip Processors Implement the End-System Behavior as Defined in TM4.0, Providing a High-Performance and Flexible Solution to Track Future Standards**
- **On-Chip Instruction RAMs Hold the Microcode for the Source and Destination Processors, Providing Fast Execution of Code on Chip**
- **Configuration Support for All Primary and Optional TM4.0 Parameters, Providing Maximum Implementation Flexibility**
- **Supports TM4.0-Defined Resource Management (RM)-Cell Formats and Provides the RM-Cell Payload and Information on How to Configure the RM-Cell Header to the Segmentation and Reassembly (SAR) Device**
- **Supports Out-of-Rate Forward and Backward RM-Cell Generation to Prevent Deadlock Situations When the Rates of Sources and Destinations Are Driven to or Below a Minimum Cell Rate of 10 Cells Per Second**
- **Processes Received RM Cells, Maintaining Parameters and Variables in Accordance With TM4.0**
- **Hardware Assistance Is Provided for 1/ACR Calculations That Support Scheduling Operations to Maximize Performance**
- **Hardware Assistance Is Provided for 15-Bit Floating-Point To/From Integer Conversions to Maximize Performance**
- **UTOPIA Level-1 Revision-2.01 Receive (Observe-Only) Cell Interface**
- **Internal 8-Cell Receive FIFO**
- **Receive-Cell Interface Can Be Programmed to Operate as Either a Physical (PHY-Layer) Interface or as a SAR/Switch (ATM-Layer) Interface.**
- **Supports Boundary Scan Through a Five-Wire JTAG Interface in Accordance With IEEE Std 1149.1-1990 (Includes IEEE Std 1149.1a-1993) IEEE Standard Test-Access-Port and Boundary-Scan Architecture**

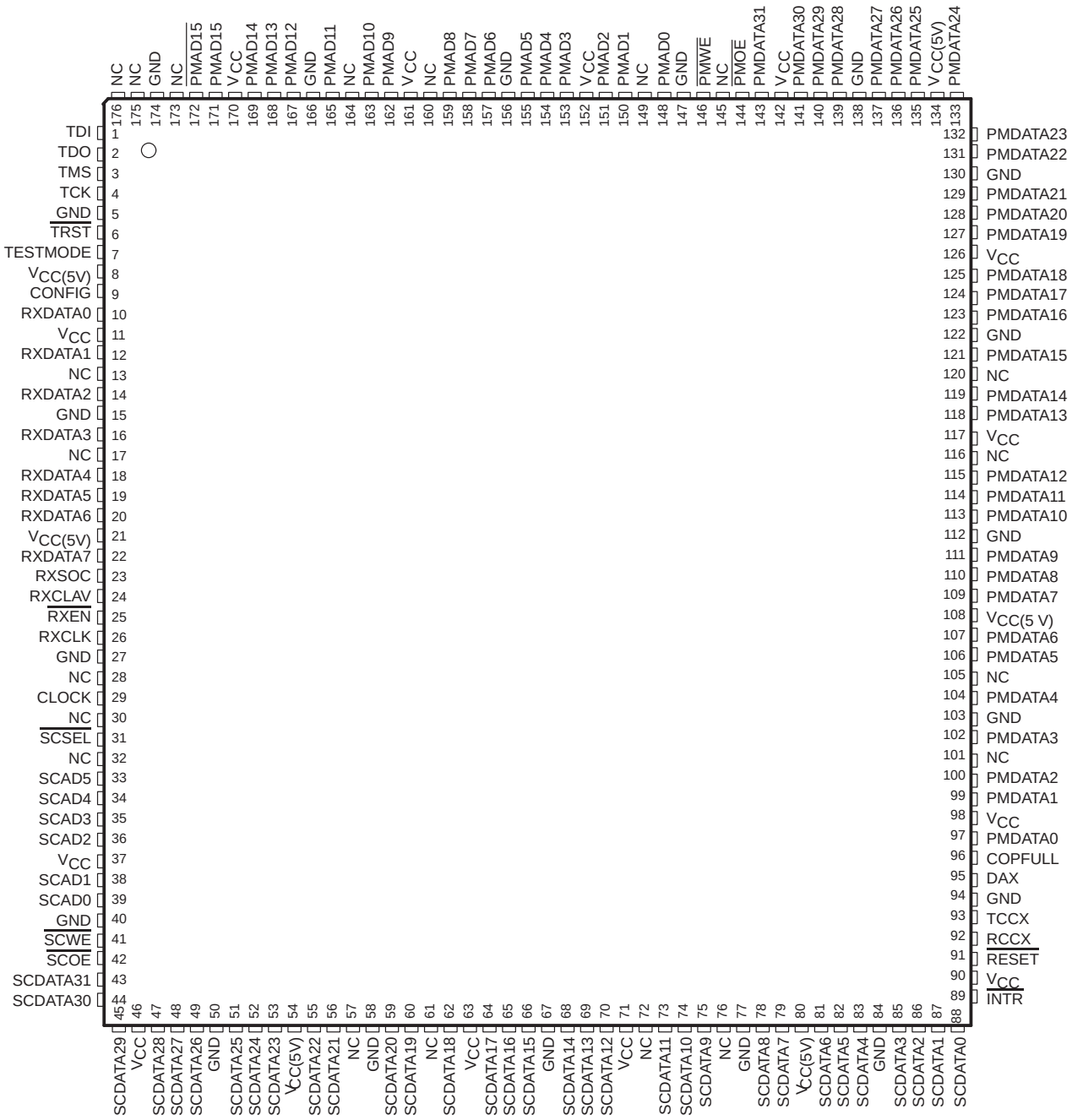
description

The TNETA1585 is an asynchronous transfer mode (ATM) programmable traffic management scheduler device that is used with a segmentation and reassembly (SAR) device to provide a flexible, high-performance solution for the available bit rate (ABR) service category. Its programmability enables it to support other special modes including variable-bit-rate non-real-time (VBR-nrt) service category and virtual-path (VP)-level ABR in addition to and simultaneously with ABR. Combining the TNETA1585 with the TNETA1575 provides a high-performance solution for classical LAN-to-ATM backbone applications, including high-performance networking hubs.

This data sheet provides information on the device hardware specifications that includes device interfaces, timing diagrams, electrical characteristics, terminal and package information, and an overview of device operation. All information on the TNETA1585 data structures, configuration, and features is provided in the *TNETA1585 Programmer's Reference Guide*, literature number SDNU016.

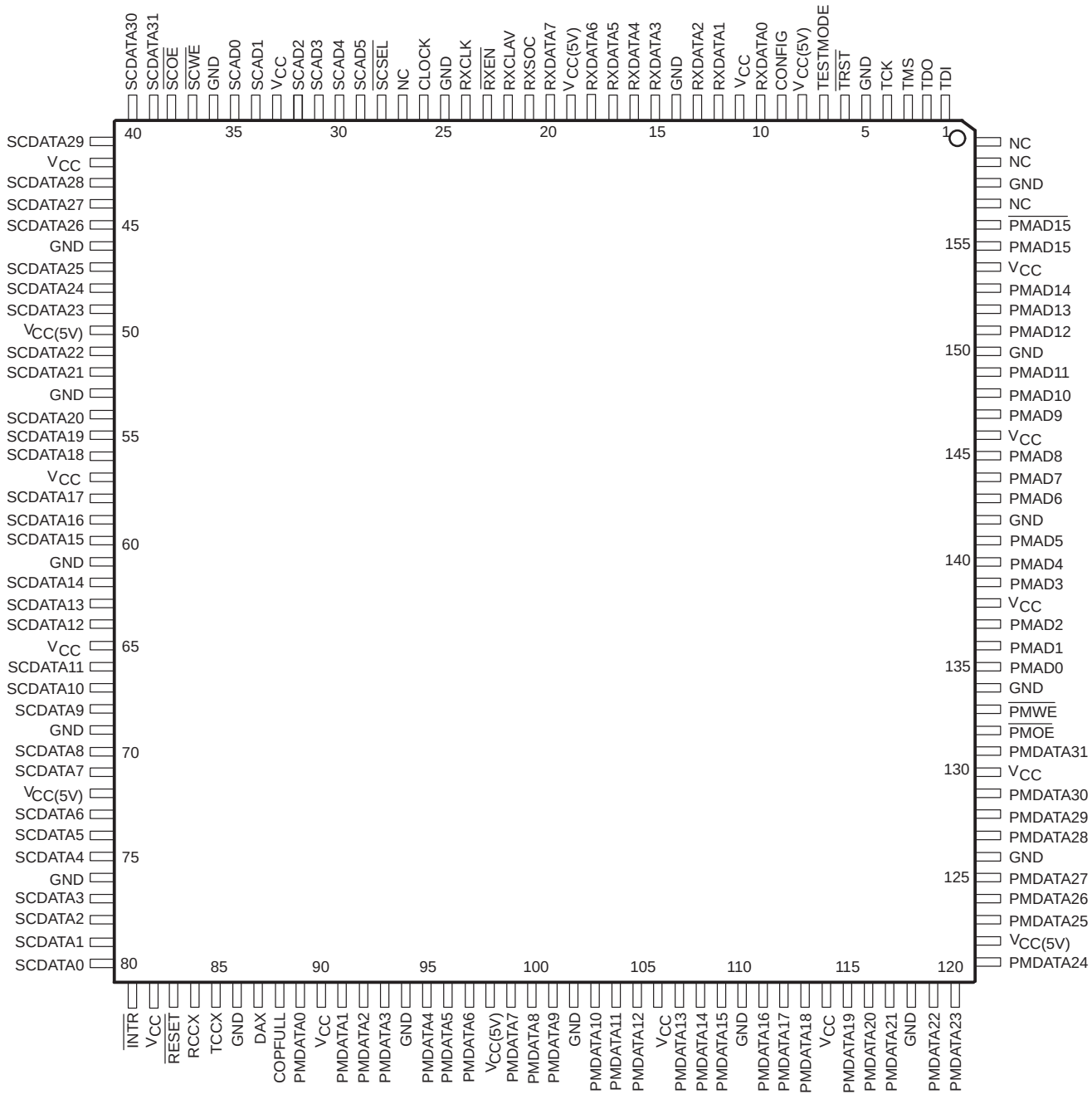
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PGF PACKAGE
(TOP VIEW)



NC – No internal connection

PCM PACKAGE
(TOP VIEW)



NC – No internal connection

Terminal Functions

slave interface

TERMINAL NAME	TERMINAL NO. PGF	TERMINAL NO. PCM	I/O	RESET STATE	DESCRIPTION
SCAD5–SCAD0	33–36 38–39	29–32 34–35	I (TTL)	I	Slave-control address. SCAD5–SCAD0 consists of a 6-bit address.
SCDATA31– SCDATA0	43–45 47–49 51–53 55–56 59–60 62 64–66 68–70 73–75 78–79 81–83 85–88	39–41 43–45 47–49 51–52 54–56 58–60 62–64 66–68 70–71 73–75 77–80	I/O (TTL/ CMOS)	Hi-Z	Slave-control data. SCDATA31–SCDATA0 consists of 32-bit data.
$\overline{\text{SCOE}}$	42	38	I (TTL)	I	Slave-control output enable. $\overline{\text{SCOE}}$ is active low. When $\overline{\text{SCOE}}$ and $\overline{\text{SCSEL}}$ are low, TNETA1585 reads are enabled.
$\overline{\text{SCSEL}}$	31	28	I (TTL)	I	Slave-control select. $\overline{\text{SCSEL}}$ is active low. $\overline{\text{SCSEL}}$ enables the slave-control interface.
$\overline{\text{SCWE}}$	41	37	I (TTL)	I	Slave-control write enable. $\overline{\text{SCWE}}$ is active low. When $\overline{\text{SCWE}}$ and $\overline{\text{SCSEL}}$ are low, TNETA1585 writes are enabled.

coprocessor interface

TERMINAL NAME	TERMINAL NO. PGF	TERMINAL NO. PCM	I/O	RESET STATE	DESCRIPTION
CLOCK	29	26	I (TTL)	I	Clock. The RCCX, TCCX, and DAX inputs are clocked into the device on the rising edge of the clock input. This clock also is used as an operating clock source for the TNETA1585.
COPFULL	96	88	O (CMOS)	Low	Receive-FIFO full indication. COPFULL provides an indication of the status of the receive UTOPIA interface FIFO. When the PHY/$\overline{\text{ATM}}$ input is low, COPFULL goes high when the receive UTOPIA interface FIFO is full. When the PHY/$\overline{\text{ATM}}$ input is high, COPFULL goes high when the FIFO is within 4 bytes of being full.
DAX	95	87	I (TTL)	I	Data-availability indication. DAX provides an indication to the device when data is available on a particular channel or when the SAR has completed segmentation of queued packets.
$\overline{\text{INTR}}$	89	81	O (CMOS)	High	Local interrupt. $\overline{\text{INTR}}$ provides an interrupt indication from the traffic coprocessor to the SAR.
RCCX	92	84	I (TTL)	I	Receive-cell status indication. RCCX provides an indication to the device that a cell has been received on the UTOPIA interface along with the receive channel number assigned to the cell.
$\overline{\text{RESET}}$	91	83	I (TTL)	I	Reset. When low, $\overline{\text{RESET}}$ resets the device.
TCCX	93	85	I (TTL)	I	Transmit-cell status indication. TCCX provides an indication to the device that a cell has been transmitted from the SAR along with the channel number of that cell.

Terminal Functions (Continued)

receive-UTOPIA interface

TERMINAL NAME	TERMINAL NO. PGF	TERMINAL NO. PCM	I/O	RESET STATE	DESCRIPTION
RXCLK	26	24	I (TTL)	I	Receive clock. RXCLK is the data transfer/synchronization clock for synchronizing transfers on RXDATA.
RXDATA7– RXDATA0	22 20–18 16 14 12 10	20 18–15 13–12 10	I (TTL)	I	Receive data. Eight-bit data lines. RXDATA7 is the most significant bit.
RXCLAV	24	22	I (TTL)	I	Receive-cell available. RXCLAV is an indication that a transfer of a complete cell can be accepted.
$\overline{\text{RXEN}}$	25	23	I (TTL)	I	Receive enable. $\overline{\text{RXEN}}$ indicates to the TNETA1585 when RXDATA contains a valid byte.
RXSOC	23	21	I (TTL)	I	Receive start of cell. RXSOC is received by the device when RXDATA contains the first valid byte of the cell.

parameter-memory interface

TERMINAL NAME	TERMINAL NO. PGF	TERMINAL NO. PCM	I/O	RESET STATE	DESCRIPTION
PMAD15– PMAD0	171 169–167 165 163–162 159–157 155–153 151–150 148	155 153–151 149–147 145–143 141–139 137–135	O (CMOS)	Low	Parameter-memory address. PMAD15–PMAD0 provides a 16-bit physical address to the parameter memory.
PMDATA31– PMDATA0	143 141–139 137–135 133–131 129–127 125–123 121 119–118 115–113 111–109 107–106 104 102 100–99 97	131 129–127 125–123 121–119 117–115 113–111 109–107 105–103 101–99 97–95 93–91 89	I/O (TTL/CMOS)	Low	Parameter-memory data. PMDATA31–PMDATA0 provides 32-bit data to/from the parameter memory.
$\overline{\text{PMWE}}$	146	133	O (CMOS)	High	Parameter-memory write enable. The address and data are valid when $\overline{\text{PMWE}}$ is low.
$\overline{\text{PMAD15}}$	172	156	O (CMOS)	High	Inverse of PMAD15. $\overline{\text{PMAD15}}$ can be used with PMAD15 to provide SRAM bank switching.
$\overline{\text{PMOE}}$	144	132	O (CMOS)	High	Parameter-memory output enable. The PMAD15–PMAD0 address is valid when $\overline{\text{PMOE}}$ is low. Data is read into the TNETA1585 on the rising edge of $\overline{\text{PMOE}}$.

Terminal Functions (Continued)

boundary-scan interface

TERMINAL NAME	TERMINAL NO. PGF	TERMINAL NO. PCM	I/O	RESET STATE	DESCRIPTION
TCK	4	4	I (TTL)	I	Test clock. TCK is used to clock the test-access-port (TAP) operation.
TDI	1	1	I (TTL)	I	Test data input. TDI is used to shift serial test data and instruction into the device during TAP operation.
TDO	2	2	O (CMOS)	Hi-Z	Test data output. TDO is used to shift serial test data and instructions out of the device during TAP operation.
TMS	3	3	I (TTL)	I	Test mode select. TMS is used to control the state of the TAP controller.
$\overline{\text{TRST}}$	6	6	I (TTL)	I	Test reset. $\overline{\text{TRST}}$ asynchronously forces the TAP controller to a known state.

miscellaneous signals

TERMINAL NAME	TERMINAL NO. PGF	TERMINAL NO. PCM	I/O	RESET STATE	DESCRIPTION
CONFIG	9	9	I (TTL)	I	This terminal must be tied low during normal operation.
TESTMODE	7	7	I (TTL)	I	Test/normal mode. TESTMODE selects test mode when high and normal operation when low.

power and ground

TERMINAL NAME	TERMINAL NO. PGF	TERMINAL NO. PCM	DESCRIPTION
GND	5, 15, 27, 40, 50, 58, 67, 77, 84, 94, 103, 112, 122, 130, 138, 147, 156, 166, 174	5, 14, 25, 36, 46, 53, 61, 69, 76, 86, 94, 102, 110, 118, 126, 134, 142, 150, 158	Ground. GND is the 0-V reference for the device.
NC	13, 17, 28, 30, 32, 57, 61, 72, 76, 101, 105, 116, 120, 145, 149, 160, 164, 173, 175, 176	27, 157, 159, 160	No internal connection. NC terminals have no internal connections. For potential functionality additions, it is recommended that these terminals not be connected to any signal, power, or ground connection.
V_{CC}	11, 37, 46, 63, 71, 90, 98, 117, 126, 142, 152, 161, 170	11, 33, 42, 57, 65, 82, 90, 106, 114, 130, 138, 146, 154	Supply voltage. V_{CC} is the 3.3-V (with respect to GND) supply for the functional logic gates.
$V_{CC(5V)}$	8, 21, 54, 80, 108, 134	8, 19, 50, 72, 98, 122	Supply voltage. $V_{CC(5\ V)}$ is the 5-V secondary supply voltage for the clamp diodes of 5-V tolerant input and output buffers. The clamp diodes provide protection for the buffers in a 5-V switching environment.

detail description

The TNETA1585 device contains the following interfaces:

- COPI interface:
  - Slave-control interface
  - Coprocessor interface
- Receive-UTOPIA interface
- Parameter-memory interface
- JTAG interface

COPI interface

The traffic-coprocessor interface (COPI) provides the means of communication between the TNETA1585 and the master device. It consists of the slave interface and the coprocessor interface.

slave-control interface

The slave-control (SC) interface consists of a 32-bit data bus, a 6-bit address bus, an output-enable terminal ($\overline{\text{SCOE}}$), a write-enable terminal ($\overline{\text{SCWE}}$), and a select terminal ($\overline{\text{SCSEL}}$). When used with the TNETA1575 SAR device, the TNETA1585 slave-control interface is mapped into the SAR's control-memory space starting at address 10000h and extending to address 1FFFFh. This equates to a total address space of 64K 32-bit words with 64 locations applicable to the TNETA1585. The TNETA1575 uses its select terminal to choose between its control memory and the TNETA1585. The TNETA1585 is a slave to all to-and-from transfers. These are initiated by the master device that is a SAR or switch port controller.

Table 1 lists the slave registers that are directly accessible through the slave interface. A heading specifies the slave-interface addresses as control-memory addresses because of the TNETA1575 mapping of the TNETA1585. Each register is either host associated or SAR associated.

The host accesses the host-associated registers through the SAR and are used by the host to initialize the TNETA1585 and to configure the TNETA1585's other internal-data structures and associated parameter memory. The host has access to the TNETA1585's other internal-data structures and associated parameter memory through the host-associated read address, read data, write address, and write data registers as described in the *TNETA1585 Programmer's Reference Guide*, literature number SDNU016.

The SAR-associated registers are used by the SAR to obtain information related to the scheduling of cells. The next-cell register indicates when one of the TNETA1585 scheduled connections is ready to transmit and what type of cell to transmit. It also provides information on how to build the associated cell's header. In addition, if the SAR is instructed by the TNETA1585 to transmit an RM cell for ABR connections, the SAR obtains the properly formatted RM-cell payload from one of the RM-cell-contents FIFOs of the TNETA1585.

slave-control interface (continued)

Table 1. Slave-Control Interface Register Map

DESCRIPTION	HOST/SAR ASSOCIATED	R/W	CONTROL MEMORY ADDRESS (TNETA1575)	PCI OFFSET ADDRESS (TNETA1575)
Next-cell register	SAR	R	h10000	h40000
RM-cell-contents FIFO A	SAR	R	h10001	h40004
RM-cell-contents FIFO B	SAR	R	h10002	h40008
RM-cell-contents FIFO C	SAR	R	h10003	h4000C
RM-cell-contents FIFO D	SAR	R	h10004	h40010
Reserved	N/A	N/A	h10005–7	h40014–1C
Configuration register	Host	R/W	h10008	h40020
Status register	Host	R	h10009	h40024
Interrupt-mask register	Host	R/W	h1000A	h40028
Schedule-on register	Host	W	h1000B	h4002C
Schedule-off register	Host	W	h1000C	h40030
Read-address register	Host	R/W	h1000D	h40034
Read-data register	Host	R	h1000E	h40038
Write-address register	Host	R/W	h1000F	h4003C
Write-data register	Host	W	h10010	h40040
Clock-frequency register	Host	R/W	h10011	h40044
Revision-number register	Host	R	h10012	h40048
ACR-low register	Host	R	h10013	h4004C
ACR-OK register	Host	R	h10014	h40050
Reserved	N/A	N/A	h10015–19	h40054–64
General-purpose registers	Host	R/W	h1001A–1D	h40068–74
Reserved	N/A	N/A	h100IE–3F	h40078–FC

The following describes the SAR-associated registers with respect to what the TNETA1575 requires of the interface. However, these registers can be used by other COPI-compliant ATM-layer devices to assist in the scheduling of cells and the generation of RM cells.

next-cell register

The TNETA1575 uses the next-cell register to determine if one of the TNETA1585's scheduled connections is ready to transmit and, if so, which channel and what type of cell (i.e., data, forward RM, backward RM). This register is read only.

READY	CELL COUNT	RESERVED	CHANNEL NUMBER	CLP	CELL TYPE
BIT					
31	30–26	25–15	14–4	3	2–0

Bit 31 (ready). The TNETA1585 sets bit 31 to indicate that the contents of the register are valid and ready to read.

Bits 30–26 (cell count). This field indicates the number of cells (minus one) that are to be sent by the SAR for this particular channel. A zero entry tells the SAR to send a single cell and an all-ones entry tells the SAR to send 32 cells.

(next-cell register continued)

Bits 14–4 (channel number). This field contains the channel number that the cell(s) is sent on.

Bit 3 (CLP). This field contains the cell-loss-priority indication that the SAR should insert in the outgoing cell's header.

Bits 2–0 (cell type). This field indicates the source of cell(s) to be sent. Several options are available for outgoing cells, and this field, along with the CLP bit, indicates where the cell should be obtained. If the cell type is an RM cell, then the SAR must obtain the RM-cell payload from one of the RM-cell-contents FIFOs through the slave interface. If the cell type is data, then the SAR must obtain data from its own transmit buffers. Details are provided in Table 2:

Table 2. Next-Cell Register Cell-Type Definition

CLP	CELL TYPE			INDICATION
	BIT 2	BIT 1	BIT 0	
0	0	0	0	In-rate VC-level RM cell from RM-cell-contents FIFO A
0	0	0	1	In-rate VC-level RM cell from RM-cell-contents FIFO B
0	0	1	0	In-rate data cell
0	0	1	1	Reserved
0	1	0	0	In-rate VP-level RM cell from RM-cell-contents FIFO A
0	1	0	1	In-rate VP-level RM cell from RM-cell-contents FIFO B
0	1	1	0	Reserved
0	1	1	1	Reserved
1	0	0	0	Out-of-rate VC-level RM cell from RM-cell-contents FIFO C
1	0	0	1	Out-of-rate VC-level RM cell from RM-cell-contents FIFO D
1	0	1	0	Out-of-rate data cell
1	0	1	1	Reserved
1	1	0	0	Out-of-rate VP-level RM cell from RM-cell-contents FIFO C
1	1	0	1	Out-of-rate VP-level RM cell from RM-cell-contents FIFO D
1	1	1	0	Reserved
1	1	1	1	Reserved

If an RM cell is sent, the TNETA1575 reads the payload portion for the cell from the appropriate FIFO, using 12 sequential accesses to the associated control-memory location.

RM-cell-contents FIFO A

When the TNETA1575 reads the next-cell register and an indication is given that an RM cell should be sent from the RM-cell-contents FIFO A, the TNETA1575 must make 12 accesses to control-memory location 10001h to fetch one entire cell payload. The data that is returned by the TNETA1585 is in big-endian format as follows:

Byte 0 (31–24)	Byte 1 (23–16)	Byte 2 (15–8)	Byte 3 (7–0)

The ordering and formatting of data (as it is sequentially read from this register) is:

Word 0 – Bytes 0, 1, 2, 3
Word 1 – Bytes 0, 1, 2, 3
•
•
•

RM-cell-contents FIFO B

When the TNETA1575 reads the next-cell register and an indication is given that an RM cell should be sent from the RM-cell-contents FIFO B, the TNETA1575 must make 12 accesses to control-memory location 10002h to fetch one entire cell payload. The data that is returned by the TNETA1585 is in big-endian format as follows:

Byte 0 (31–24)	Byte 1 (23–16)	Byte 2 (15–8)	Byte 3 (7–0)

The ordering and formatting of data (as it is sequentially read from this register) is:

Word 0 – Bytes 0, 1, 2, 3
Word 1 – Bytes 0, 1, 2, 3
•
•
•

RM-cell-contents FIFO C

When the TNETA1575 reads the next-cell register and an indication is given that an RM cell should be sent from the RM-cell-contents FIFO C, the TNETA1575 must make 12 accesses to control-memory location 10003h to fetch one entire cell payload. The data that is returned by the TNETA1585 is in big-endian format as follows:

Byte 0 (31–24)	Byte 1 (23–16)	Byte 2 (15–8)	Byte 3 (7–0)

The ordering and formatting of data (as it is sequentially read from this register) is:

Word 0 – Bytes 0, 1, 2, 3
Word 1 – Bytes 0, 1, 2, 3
•
•
•

RM-cell-contents FIFO D

When the TNETA1575 reads the next-cell register and an indication is given that an RM cell should be sent from the RM-cell contents FIFO D, the TNETA1575 must make 12 accesses to control-memory location 10004h to fetch one entire cell payload. The data that is returned by the TNETA1585 is in big-endian format as follows:

Byte 0 (31–24)	Byte 1 (23–16)	Byte 2 (15–8)	Byte 3 (7–0)

The ordering and formatting of data (as it is sequentially read from this register) is:

Word 0 – Bytes 0, 1, 2, 3
Word 1 – Bytes 0, 1, 2, 3
•
•
•

coprocessor interface

The coprocessor interface consists of a group of unidirectional serial channels through which real-time information concerning the transmission and reception of cells by the SAR/switch port is passed between the TNETA1585 and the SAR/switch port. Reset and interrupt capabilities also are provided by the coprocessor interface. The unidirectional serial-interface implementation by the TNETA1575 SAR is described below. Similar requirements apply when interfacing to a different SAR device or a switch port. The coprocessor interface consists of:

Received cell-indication interface (RCCX)
Transmitted cell-indication interface (TCCX)
Data-availability interface (DAX)
COP full-indication interface (COPFULL)

received-cell-indication interface (RCCX)

A serial-bit interface allows the TNETA1575 to signal to the TNETA1585 that a cell has been received on the UTOPIA interface on a particular channel. This interface is necessary to avoid duplicating the hardware that is used to resolve a virtual path identifier (VPI) or virtual channel identifier (VCI) to a channel number. When a cell is received, the VPI/VCI value from the header is extracted by the TNETA1575 and is used as a key in a lookup algorithm to resolve its associated channel number. When the lookup is complete, the TNETA1575 passes relevant information to the TNETA1585 by sending a 13-bit frame formatted as follows:

Channel number (12–2)	Good/bad cell indicator (1)	Framing (0)

Bits 12–2 (channel number). These bits indicate on which of the 2K channels the last cell was received.

Bit 1 (good/bad cell indicator). This bit indicates whether or not the last cell passed the lookup test or if it should be discarded. The bit is encoded as follows:

BIT 1	INDICATION
0	Cell is good (VPI/VCI was found in the lookup)
1	Cell should be discarded

Bit 0 (framing). This bit is set to a 1 to denote the start of a frame.

The frame is transmitted to the TNETA1585 through the RCCX terminal starting with bit 0. When a frame is not actively being transmitted, the RCCX terminal is driven to a 0.

transmitted-cell-indication interface (TCCX)

A single-bit interface allows the TNETA1575 to signal to the TNETA1585 that a cell will be transmitted on a particular channel. This interface can be used to facilitate statistics processing in the TNETA1585 and to aid in ATM Forum ABR scheduling. When the TNETA1575 determines that it has the data to send a cell, it simultaneously sends an 18-bit frame to the TNETA1585 that is formatted as follows. The information reflected by this interface confirms the information reflected in the next-cell register, if the TNETA1575 is transmitting a TNETA1585 scheduled cell.

CHANNEL NUMBER	CLP INDICATOR	CELL TYPE	SCHEDULING SOURCE	SEND ACKNOWLEDGE	FRAMING
BIT					
17–7	6	5–3	2	1	0

Bits 17–7 (channel number). These bits indicate which one of the 2K channels transmitted the last cell.

Bit 6 (CLP). This field contains the cell-loss-priority indication that was inserted in the outgoing cell's header.

Bits 5–3 (cell type). This field indicates what type of cell was sent. This field, along with the CLP bit, indicates the origin of the cell sent. Details are provided in Table 3.

Table 3. TCCX Cell-Type Definition

CLP	CELL TYPE			INDICATION
	BIT 2	BIT 1	BIT 0	
0	0	0	0	In-rate VC-level RM cell from RM-cell-contents FIFO A
0	0	0	1	In-rate VC-level RM cell from RM-cell-contents FIFO B
0	0	1	0	In-rate data cell
0	0	1	1	Reserved
0	1	0	0	In-rate VP-level RM cell from RM-cell-contents FIFO A
0	1	0	1	In-rate VP-level RM cell from RM-cell-contents FIFO B
0	1	1	0	Reserved
0	1	1	1	Reserved
1	0	0	0	Out-of-rate VC-level RM cell from RM-cell-contents FIFO C
1	0	0	1	Out-of-rate VC-level RM cell from RM-cell-contents FIFO D
1	0	1	0	Out-of-rate data cell
1	0	1	1	Reserved
1	1	0	0	Out-of-rate VP-level RM cell from RM-cell-contents FIFO C
1	1	0	1	Out-of-rate VP-level RM cell from RM-cell-contents FIFO D
1	1	1	0	Reserved
1	1	1	1	Reserved

Bit 2 (scheduling source). This bit indicates whether the cell was scheduled directly from the TNETA1575 scheduler table or if it was scheduled by the TNETA1585. This bit is encoded as follows:

BIT 2	INDICATION
0	Scheduler-table scheduled cell
1	TNETA1585 scheduled cell

transmitted-cell-indication interface (TCCX) (continued)

Bit 1 (send acknowledge). This bit indicates whether the SAR will send a cell. The bit is encoded as follows:

BIT 1	INDICATION
0	Cell will not be sent.
1	Cell will be sent.

Bit 0 (framing). This bit is set to a 1 to denote the start of a frame.

The frame is transmitted to the coprocessor through the TCCX terminal starting with bit 0. When a frame is not actively being transmitted, the TCCX terminal is driven to a 0.

data-availability interface (DAX)

A single-bit interface allows the TNETA1575 to signal to the TNETA1585 when data is available or unavailable on a particular channel. A 13-bit frame is sent to the TNETA1585 for a particular channel only when its data-availability status changes (i.e., when the host writes to the transmit-queue register to notify the TNETA1575 that a packet has been queued, or if the TNETA1575 completes segmentation of the last packet on a particular channel). The frame is formatted as follows:

Channel number (12–2)	Data available/unavailable (1)	Framing (0)

Bits 12–2 (channel number). These bits indicate which one of the 2K channels has available or unavailable data.

Bit 1 (data available/unavailable). This field indicates the new status of the segmentation queue for the given channel number. This field is encoded as follows:

BIT 1	INDICATION
0	All data has been segmented (data unavailable).
1	New data has been added (data available).

Bit 0 (framing). This bit is set to a 1 to denote the start of a frame.

The frame is transmitted to the TNETA1585 through the DAX terminal starting with bit 0. When a frame is not actively being transmitted, the DAX terminal is driven to a 0.

COP full-indication interface (COPFULL)

A single-bit interface allows the TNETA1585 to signal to the TNETA1575 the status of the TNETA1585's receive-UTOPIA-interface FIFO. When in ATM mode (CONFIG = 0), this output goes high when the receive-UTOPIA-interface FIFO is full. When in PHY mode (CONFIG = 1), this output goes high when the FIFO is within four bytes of being full.

TNETA1585-to-TNETA1575 interconnection

Figure 1 shows the interconnection of the TNETA1575 SAR and the TNETA1585 traffic management scheduler.

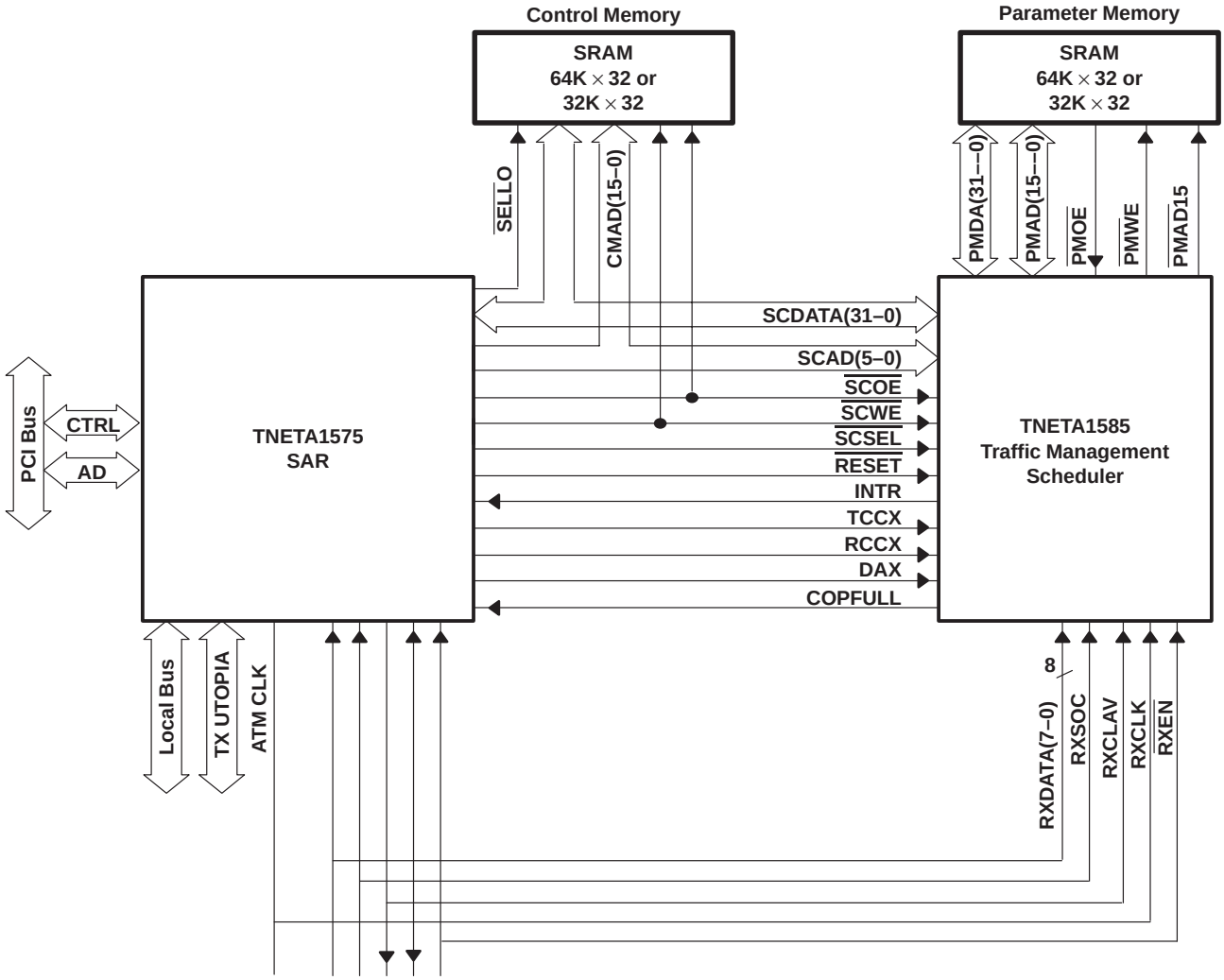


Figure 1. TNETA1585 Interconnection to TNETA1575

receive-UTOPIA interface

The TNETA1585 receives ATM cells through a receive-UTOPIA level-1 interface with cell-level handshake only. This interface is configurable as either an 8-bit PHY or ATM interface. The ATM mode is chosen when the TNETA1585 interfaces with a framer (such as the TNETA1500). The PHY mode is chosen when the TNETA1585 interfaces with a switch port. The operation of this dual PHY/ATM interface requires connection of the UTOPIA signals to the appropriate input terminals of the TNETA1585.

In both modes, the receive UTOPIA interface on the TNETA1585 monitors only, i.e., the device does not actively participate in the UTOPIA protocol. If the system is to work correctly, a fully compliant UTOPIA-peer device is required. This interface is designed so that the TNETA1585 could be connected as a peer to the TNETA1575, which are both then connected to an ATM (e.g., switch port) or PHY device.

receive-UTOPIA interface (continued)

In ATM mode, the TNETA1585 receive-UTOPIA interface behaves as an RX UTOPIA, monitoring incoming cells from a framer such as the TNETA1500 into the reassembly interface of a SAR device such as the TNETA1575. An external clock input provides for data transfers/synchronization between the TNETA1585 receive-UTOPIA and TNETA1500 interfaces.

In PHY mode, the TNETA1585 receive-UTOPIA interface behaves as a TX UTOPIA of a PHY device, monitoring incoming cells from a switching element into the reassembly interface of a SAR device such as the TNETA1575. An external clock input provides for data transfers/synchronization between the TNETA1585 receive-UTOPIA and ATM switching-element TX UTOPIA interfaces.

The receive-UTOPIA interface operates as a synchronous 8-bit (byte-wide) data path. The interface functions with cell-level handshaking. The maximum clock speed supported by this interface is 33 MHz.

receive-UTOPIA interface in PHY mode

The receive-UTOPIA interface on the TNETA1585 operates as the TX UTOPIA interface in a PHY device when the TNETA1585 is operating in PHY mode.

This cell interface works on the low-to-high transition of RXCLK to sample and generate signals.

TNETA1585 SIGNAL NAME	UTOPIA SIGNAL NAME
RXCLK	TXCLK
RXDATA7–RXDATA0	TXDATA7–TXDATA0
RXSOC	TXSOC
$\overline{\text{RXEN}}$	$\overline{\text{TXEnb}}$
RXCLAV	TXClav

connecting the TNETA1585 to the UTOPIA bus in PHY mode (see Figure 2)

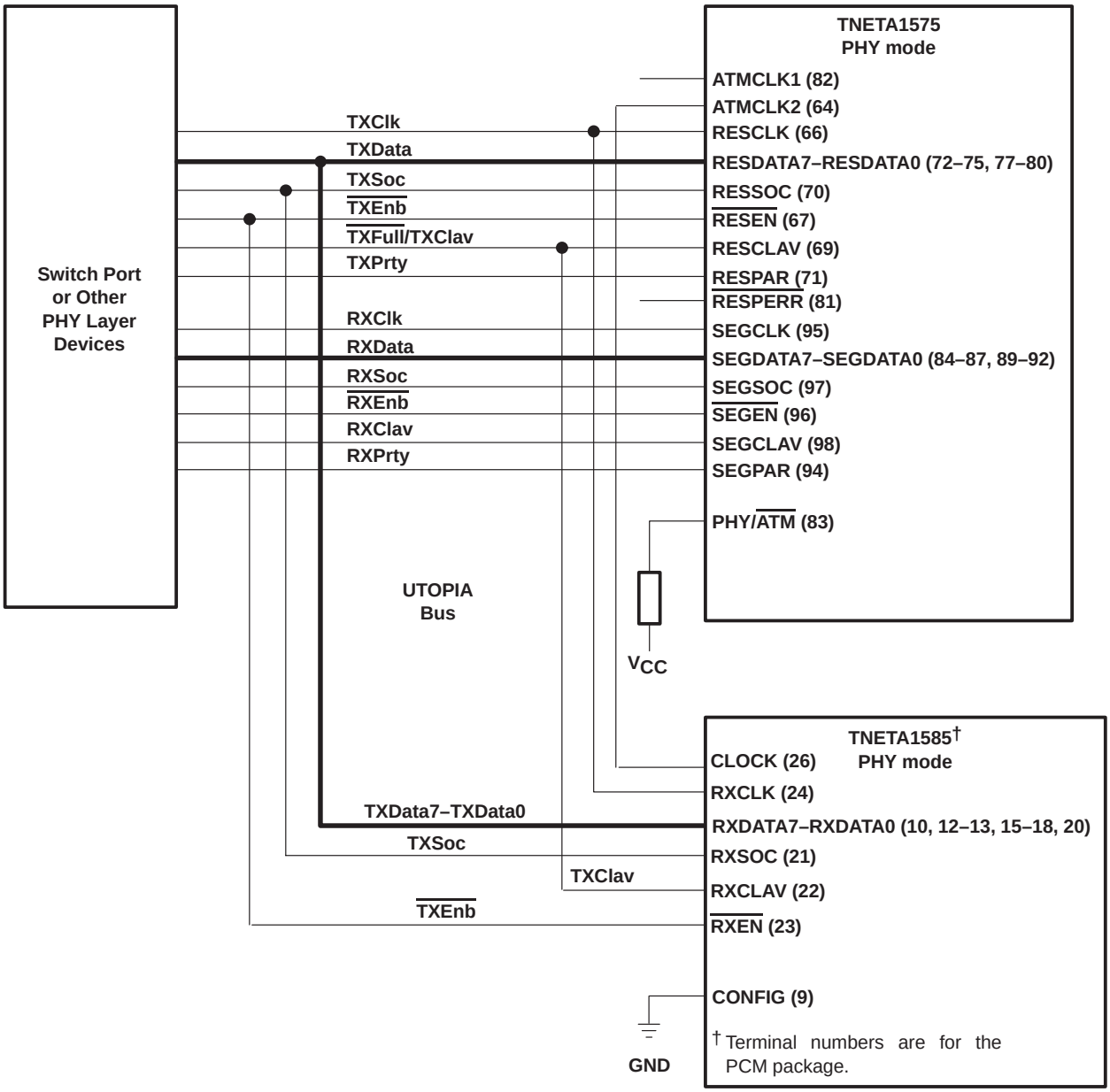


Figure 2. UTOPIA Bus Connections In PHY Mode

receive-UTOPIA interface in ATM mode

The receive-UTOPIA interface on the TNETA1585 functions as the RX UTOPIA interface in an ATM device when the TNETA1585 is operating in ATM mode.

This receive-cell interface works on the low-to-high transition of RXCLK to sample and generate signals.

TNETA1585 SIGNAL NAME	UTOPIA SIGNAL NAME
RXCLK	RXCLK
RXDATA7–RXDATA0	RXDATA7–RXDATA0
RXSOC	RXSOC
RXCLAV	RXClav
$\overline{\text{RXEN}}$	$\overline{\text{RXEnb}}$

connecting the TNETA1585 to the UTOPIA bus in ATM mode (see Figure 3)

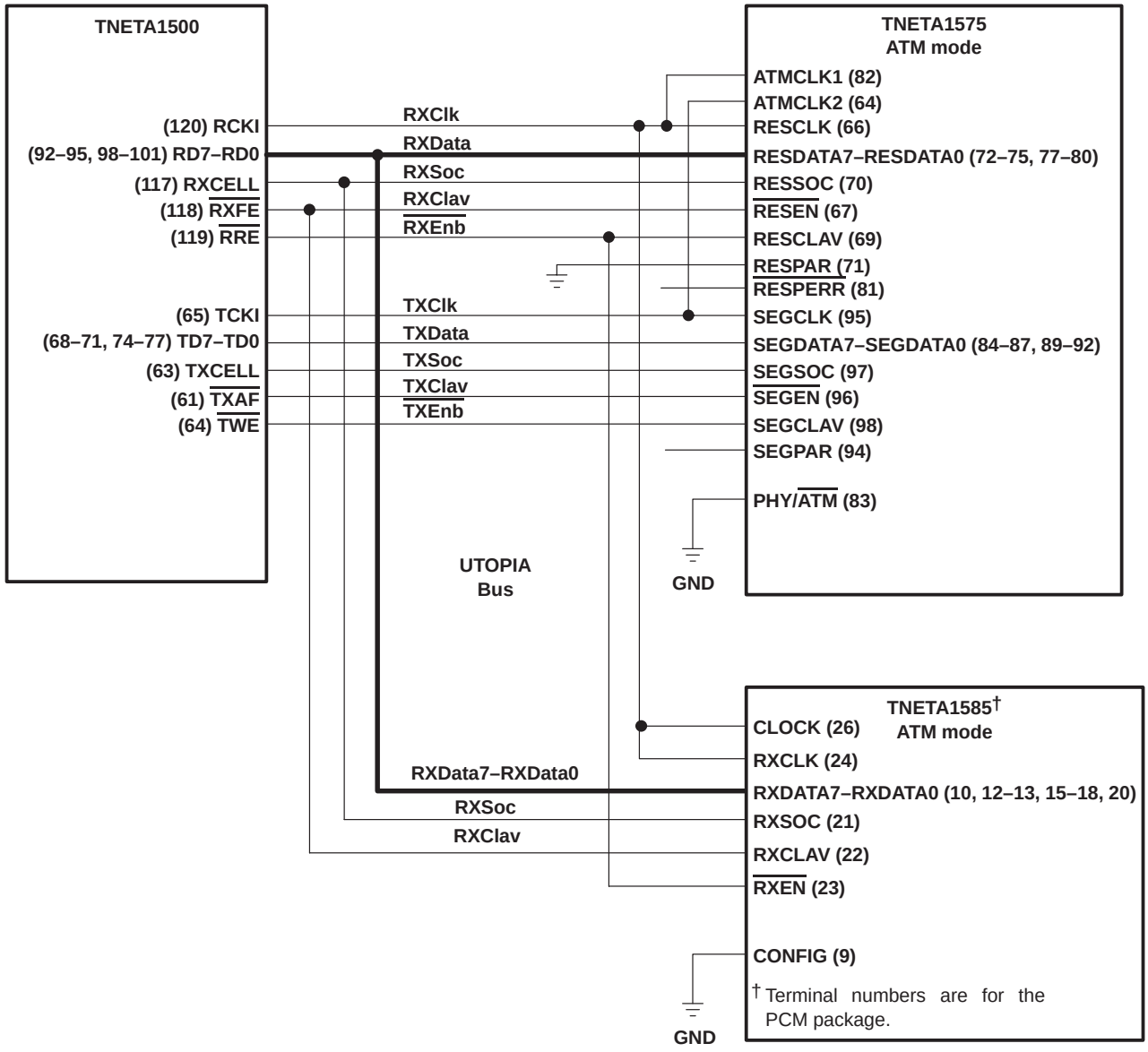


Figure 3. UTOPIA Bus Connections in ATM Mode

parameter-memory interface

The parameter-memory interface on the TNETA1585 is used for interface to the external SRAM containing the connection-state information and parameters required per channel. The interface consists of a 32-bit data bus, a 16-bit address bus, an output-enable terminal, and a write-enable terminal. The interface also provides an additional address terminal ($\overline{\text{PMAD15}}$) that can be used with address terminal (PMAD15) to provide support for SRAM bank switching. This allows the user to use two 32K $\times$ 32 banks of SRAM instead of one 64K $\times$ 32 bank by using PMAD15 and $\overline{\text{PMAD15}}$ as chip selects. The TNETA1585 is designed to operate with a 15 ns or faster asynchronous SRAM. The total SRAM requirement for parameter memory to support 2K connections is 32K $\times$ 32.

The parameter-memory information is accessed by the host via the slave interface. Details of the parameters in parameter memory are found in the *TNETA1585 Programmer's Reference Guide*, literature number SDNU016.

JTAG interface

The TNETA1585 supports boundary scan through a five-wire JTAG interface in accordance with IEEE Std 1149.1-1990 (includes IEEE Std 1149.1a-1993) IEEE Standard Test-Access Port and Boundary-Scan Architecture.

The maximum operating frequency is 10 MHz for the JTAG interface.

JTAG instruction set

The TNETA1585 supports the following instructions:

INSTRUCTION	OP CODE (BINARY FORMAT)
EXTEST	000
IDCODE	100
SAMPLE/PRELOAD	001
BYPASS	111
INTERNAL SCAN	010
HIGH Z	101

idcode

	VARIANT	PART NUMBER	MANUFACTURER	LSB
Bit number	31–28	27–12	11–1	0
Binary code	0000	TBD	00000010111	1

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.5 V to 4 V
Supply voltage range, $V_{CC(5V)}$ (see Note 1) . . . . . –0.5 V to 5.5 V
Input voltage range, standard TTL, V_I . . . . . –0.5 V to V_{CC} + 0.5 V
Input voltage range, 5-V tolerant TTL, V_I . . . . . $V_{CC(5V)}$ + 0.5 V
Output voltage range, standard TTL, V_O . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, 5-V tolerant TTL, V_O . . . . . 5 V to V_{CC} + 0.5 V
Input clamp current, TTL, I_{IK} (V_I < 0 or V_I > V_{CC}) (see Note 2) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) (see Note 3) . . . . . ±20 mA
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the GND terminals.
2. Applies for external input and bidirectional buffers without hysteresis. $V_I > V_{CC}$ does not apply to fail-safe terminals. Use $V > V_{CC(5V)}$ for 5-V tolerant terminals.
3. Applies for external output and bidirectional buffers. $V_O > V_{CC}$ does not apply to fail-safe terminals. Use $V_O > V_{CC(5V)}$ for 5-V tolerant terminals.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	Commercial	3	3.3	3.6	V
$V_{CC(5V)}$	Supply voltage, 5-V tolerant TTL	Commercial	4.5	5	5.5	V
V_I	Input voltage	TTL	0		V_{CC}	V
		5-V tolerant TTL	0		$V_{CC(5V)}$	
V_O	Output voltage	TTL	0		V_{CC}	V
		5-V tolerant TTL‡	0		V_{CC}	
V_{IH}	High-level input voltage	TTL	2		V_{CC}	V
		5-V tolerant TTL	2		$V_{CC(5V)}$	
V_{IL}	Low-level input voltage	TTL	0		0.8	V
		5-V tolerant TTL	0		0.8	
T_A	Operating free-air temperature		0		70	°C

‡ V_{CC} must be applied to drive the output to a high-impedance state (Z) for 5-V tolerant operation.

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	TTL	I_{OH} = 8 mA		$V_{CC}-0.6$		V
			I_{OH} = 4 mA				
		5-V tolerant TTL	I_{OH} = 8 mA		$V_{CC}-0.6$		
			I_{OH} = 4 mA				
V_{OL}	Low-level output voltage	TTL	I_{OL} = 8 mA			0.4	V
			I_{OL} = 4 mA			0.4	
		5-V tolerant TTL	I_{OL} = 8 mA			0.4	
			I_{OL} = 4 mA			0.4	
I_{IH}	High-level input current	TTL	$V_I = V_{IH\ (max)}$,	See Note 4		±1	µA
		5-V tolerant TTL	$V_I = V_{IH\ (min)}$			–760	
I_{IL}	Low-level input current	TTL	$V_I = V_{IL\ (min)}$,	See Note 5		±1	µA
		5-V tolerant TTL				±1	
I_{OZ}	High-impedance-state output current	TTL				±20	µA
		5-V tolerant TTL				±20	

NOTES: 4. These specifications apply only when the pulldown terminator is turned off.
5. These specifications apply only when the pullup terminator is turned off.

recommended power-supply sequencing for mixed-voltage devices

The recommended power-supply sequencing in a mixed-voltage system is as follows:

- When the power supply is being turned on, all 3.3-V and 5-V supplies should start ramping from 0 V and reach 95 percent of their end-point values within a 25-ms time window. All bus contention between the TNETA1585 and external devices is eliminated by the end of the 25-ms time window. The preferred order of supply ramping is to ramp the 3.3-V supply followed by the 5-V supply. This order is not mandatory, but it allows a larger cumulative number of power-supply on events than the reverse order.
- When the power supply is being turned off, all 3.3-V and 5-V supplies should start ramping from steady state values and reach 5 percent of these values within a 25-ms time window. All bus contention between the TNETA1585 and external devices is eliminated by the end of the 25-ms time window. The preferred order of supply ramping is to ramp down the 5-V supply followed by the 3.3-V supply. This order is not mandatory, but it allows a larger cumulative number of power-supply off events than the reverse order.

If these precautions and guidelines are not followed, the TNETA1585 device may experience failures.

operating characteristics over recommended operating conditions (see Figure 4)
parameter-memory interface – write operation

NO.	PARAMETER		MIN	MAX	UNIT
1	$t_{d(PMAD)}$	Delay time, from CLOCK↑ to PMAD15–PMAD0 valid	5	12	ns
2	$t_{d(PMDATA)}$	Delay time, from CLOCK↑ to PMDATA31–PMDATA0 valid	5	12	ns
3	$t_{d(PMOE)}$	Delay time, from CLOCK↑ to $\overline{\text{PMOE}}$↑	5	13	ns
4	$t_{d(PMWE)1}$	Delay time, from CLOCK↓ to $\overline{\text{PMWE}}$↓	7	15	ns
5	$t_{d(PMWE)2}$	Delay time, from CLOCK↓ to $\overline{\text{PMWE}}$↑	7	15	ns

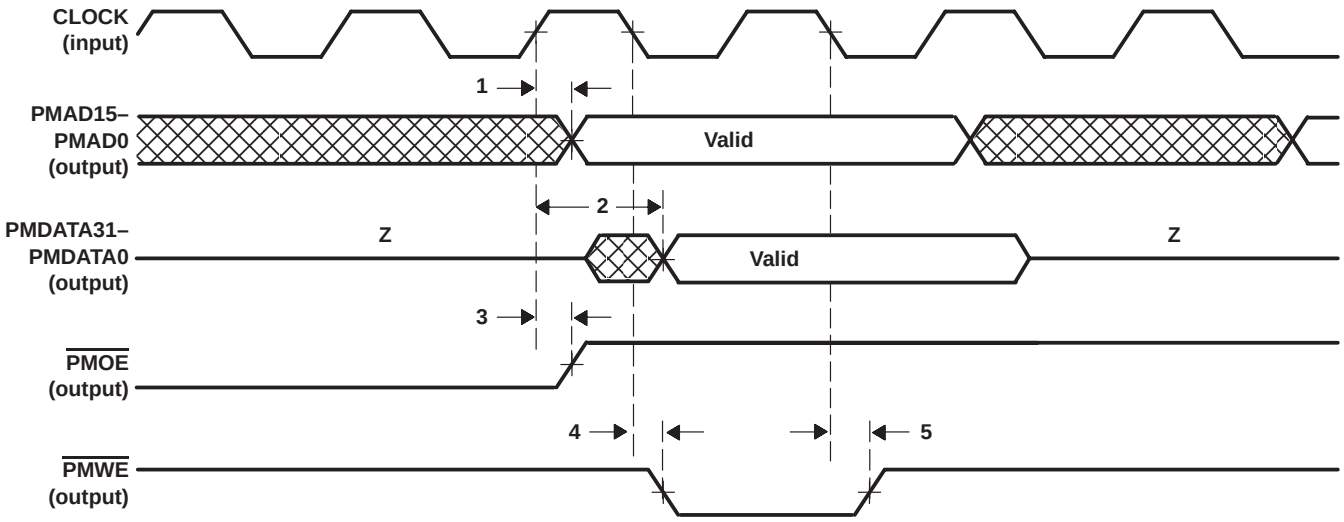


Figure 4. Parameter-Memory Interface – Write Operation

operating characteristics over recommended operating conditions (see Figure 5)
parameter-memory interface (write operation)
data bus enable and disable times

NO.	PARAMETER		MIN	MAX	UNIT
1	$t_{en(CH-PE)}$	Enable time, from CLOCK↑ to PMDATA31–PMDATA0 enabled	8	20	ns
1	$t_{dis(CH-PZ)}$	Disable time, from CLOCK↑ to PMDATA31–PMDATA0 disabled (Z state)	3	9	ns

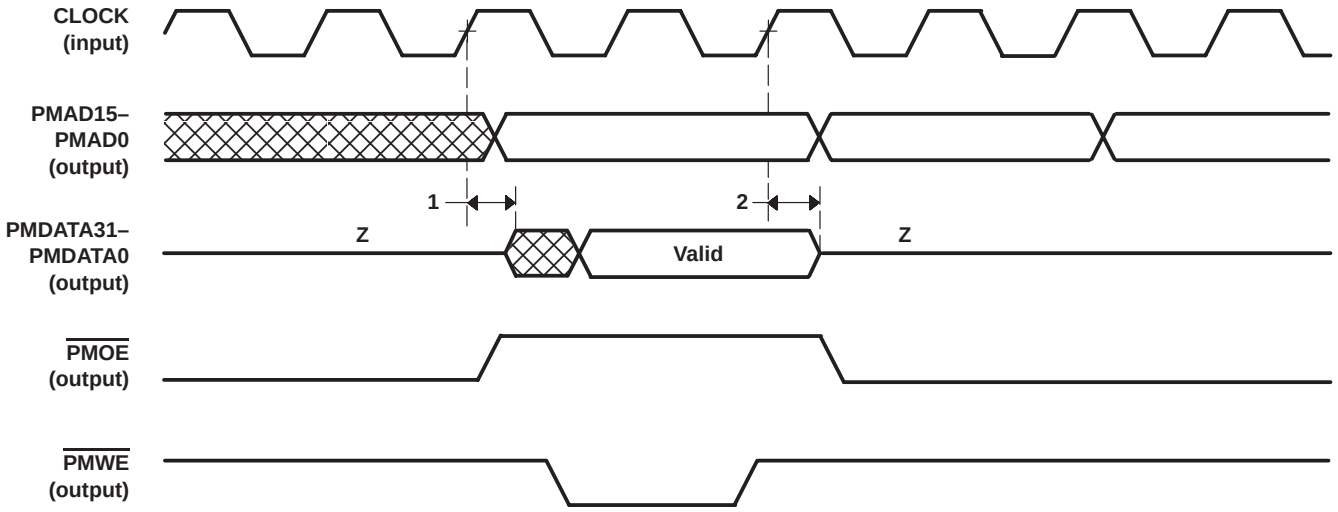


Figure 5. Parameter-Memory Interface (Write Operation) – Data Bus Enable and Disable Times

timing requirements (see Figure 6)
parameter-memory interface – read operation

NO.			MIN	MAX	UNIT
1	$t_{su(PMDATA)}$	Setup time, PMDATA31–PMDATA0 valid before CLOCK↑	3		ns
2	$t_{h(PMDATA)}$	Hold time, PMDATA31–PMDATA0 valid after CLOCK↑	2		ns

operating characteristics over recommended operating conditions (see Figure 6)
parameter-memory interface – read operation

NO.	PARAMETER		MIN	MAX	UNIT
3	$t_{d(PMAD)}$	Delay time, from CLOCK↑ to PMAD15–PMAD0 valid	5	12	ns
4	$t_{d(PMOE)}$	Delay time, from CLOCK↑ to $\overline{PMOE}$↓	5	13	ns

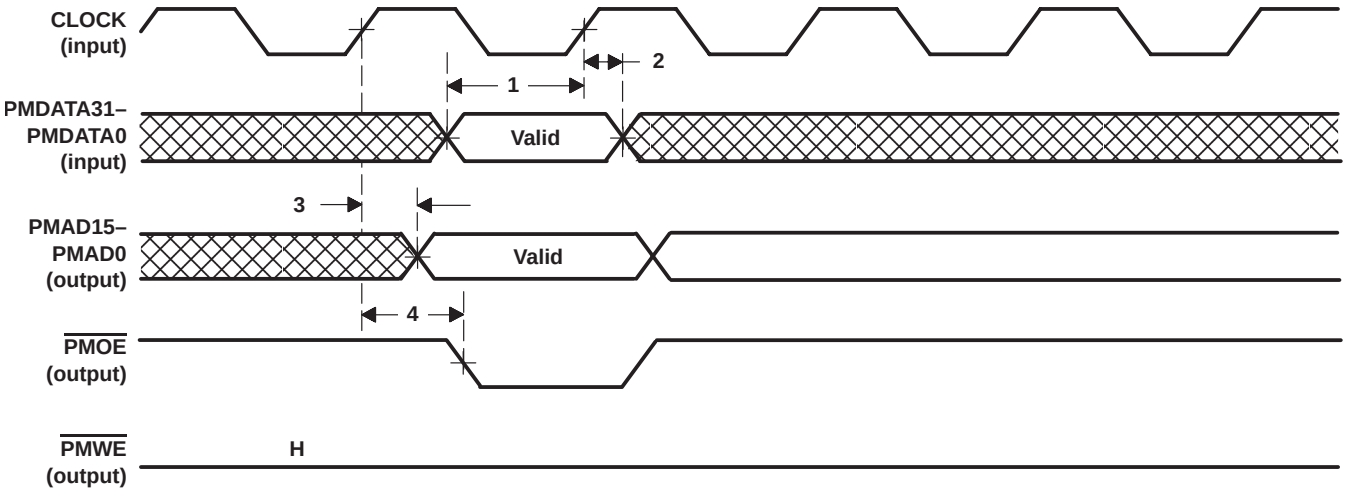


Figure 6. Parameter-Memory Interface – Read Operation

timing requirements (see Figure 7)
receive-UTOPIA interface

NO.			MIN	MAX	UNIT
1	$t_{su(RXCLAV)}$	Setup time, RXCLAV low before RXCLK↑	10		ns
2	$t_{su(RXSOC)}$	Setup time, RXSOC high before RXCLK↑	10		ns
3†	$t_{su(RXDATA)}$	Setup time, RXDATA7–RXDATA0 valid before RXCLK↑	11		ns
4‡	$t_{h(RXCLAV)}$	Hold time, RXCLAV low after RXCLK↑	2		ns
5	$t_{h(RXSOC)}$	Hold time, RXSOC high after RXCLK↑	1		ns
6	$t_{h(RXDATA)}$	Hold time, RXDATA7–RXDATA0 valid after RXCLK↑	1		ns

† This 11-ns minimum setup time deviates from the 10-ns minimum setup time specified in the UTOPIA level-1 revision1-2.01 specification.
‡ This 2-ns minimum hold time deviates from the 1-ns minimum hold time specified in the UTOPIA level-1 revision1-2.01 specification.

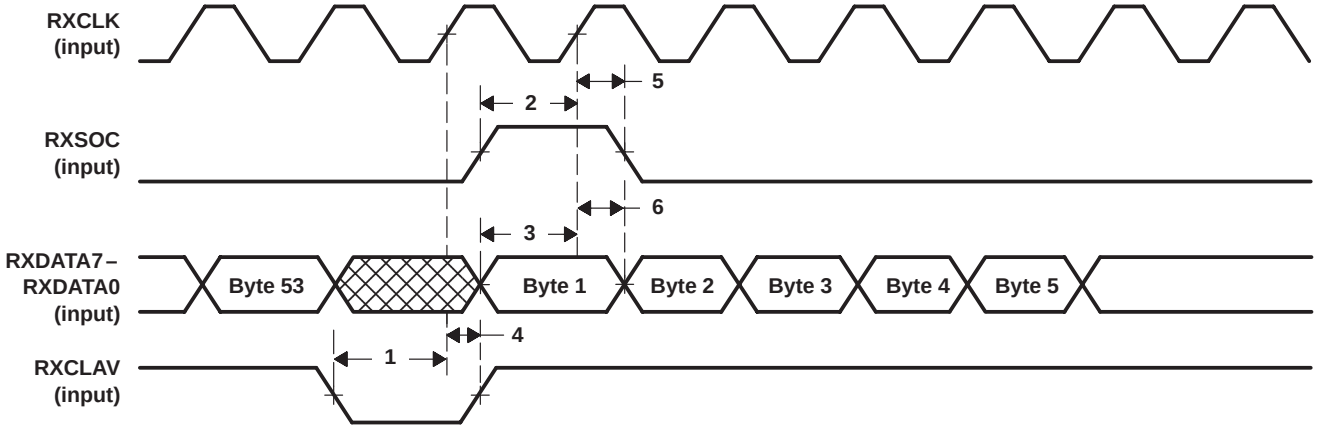


Figure 7. Receive-UTOPIA Interface

timing requirements (see Figure 8)
slave interface – read operation

NO.			MIN	MAX	UNIT
1	$t_{su(SCAD)}$	Setup time, SCAD5–SCAD0 valid before CLOCK↑	17		ns
2†	$t_{su(SCSEL)}$	Setup time, $\overline{\text{SCSEL}}$ low before CLOCK↑	13		ns
3	$t_{su(SCWE)}$	Setup time, $\overline{\text{SCWE}}$ high before CLOCK↑	6		ns
4†	$t_{su(SCOE)}$	Setup time, $\overline{\text{SCOE}}$ low before CLOCK↑	13		ns
5	$t_{h(SCAD)}$	Hold time, SCAD5–SCAD0 valid after CLOCK↑	1		ns
6‡	$t_{h(SCSEL)}$	Hold time, $\overline{\text{SCSEL}}$ low after CLOCK↑	3		ns
7	$t_{h(SCWE)}$	Hold time, $\overline{\text{SCWE}}$ high after CLOCK↑	1		ns
8‡	$t_{h(SCOE)}$	Hold time, $\overline{\text{SCOE}}$ low after CLOCK↑	2		ns

† These measurements are taken with the data enabled 4 ns before the rising edge of the clock.
‡ These measurements are taken with the data disabled at the time of the rising edge of the clock.

operating characteristics over recommended operating conditions (see Figure 8)
slave interface – read operation

NO.	PARAMETER		MIN	MAX	UNIT
9	$t_{d(SCDATA)1}$	Delay time, from SCAD5–SCAD0 to SCDATA31–SCDATA0 valid	5	13	ns
10	$t_{d(SCDATA)2}$	Delay time, from $\overline{\text{SCSEL}}$↓ to SCDATA31–SCDATA0 enabled	3	10	ns
11	$t_{d(SCDATA)3}$	Delay time, from $\overline{\text{SCOE}}$↓ to SCDATA31–SCDATA0 enabled	4	11	ns
12	$t_{d(SCDATA)4}$	Delay time, from $\overline{\text{SCSEL}}$↑ to SCDATA31–SCDATA0 disabled	4	9	ns
13	$t_{d(SCDATA)5}$	Delay time, from $\overline{\text{SCOE}}$↑ to SCDATA31–SCDATA0 disabled	4	9	ns

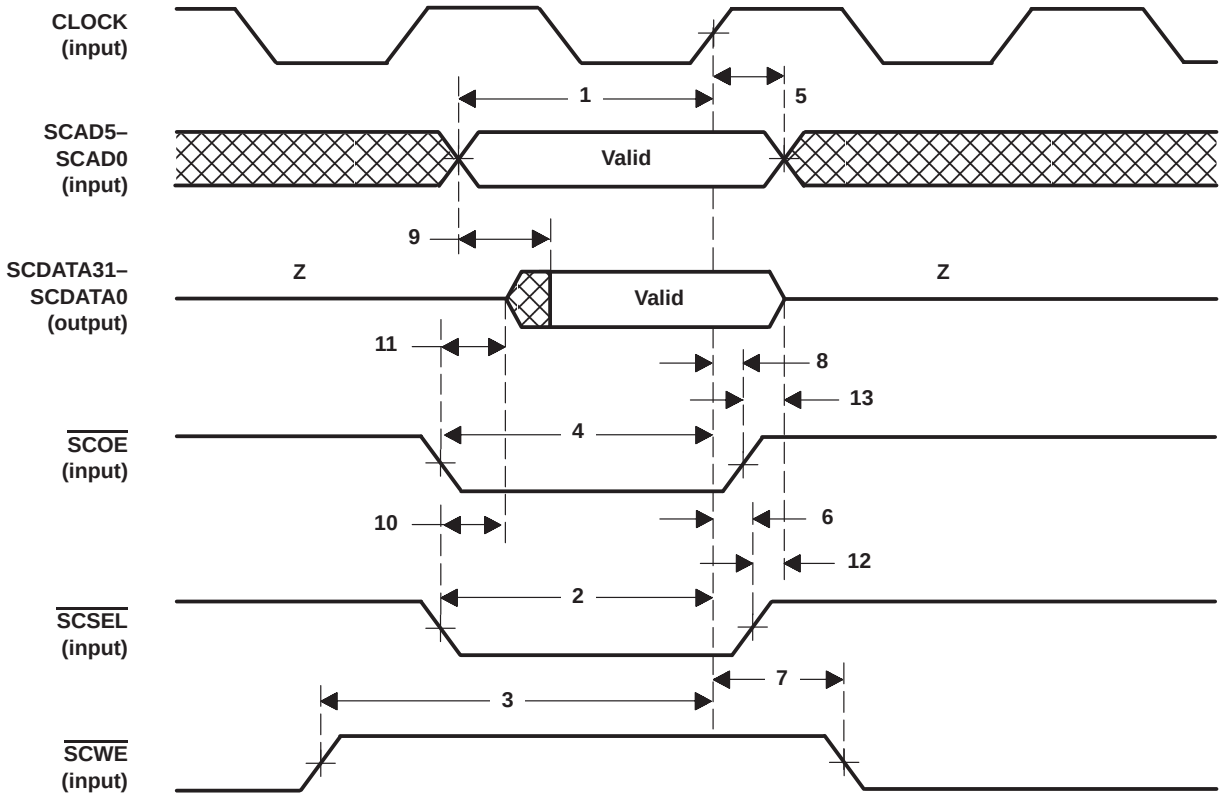


Figure 8. Slave Interface – Read Operation

timing requirements (see Figure 9)
slave interface – write operation

NO.			MIN	MAX	UNIT
1	$t_{su(SCAD)}$	Setup time, SCAD5–SCAD0 valid before CLOCK↑	7		ns
2	$t_{su(SCDATA)}$	Setup time, SCDATA31–SCDATA0 valid before CLOCK↓	0		ns
3	$t_{su(SCWE)}$	Setup time, $\overline{\text{SCWE}}$ low before CLOCK↑	5		ns
4	$t_{su(SCSEL)}$	Setup time, $\overline{\text{SCSEL}}$ low before CLOCK↑	5		ns
5	$t_{su(SCOE)}$	Setup time, $\overline{\text{SCOE}}$ high before CLOCK↓	5		ns
6	$t_{h(SCAD)}$	Hold time, SCAD5–SCAD0 valid after CLOCK↑	0		ns
7	$t_{h(SCDATA)}$	Hold time, SCDATA31–SCDATA0 valid after CLOCK↓	7		ns
8	$t_{h(SCWE)}$	Hold time, $\overline{\text{SCWE}}$ low after CLOCK↑	4		ns
9	$t_{h(SCSEL)}$	Hold time, $\overline{\text{SCSEL}}$ low after CLOCK↑	0		ns
10	$t_{h(SCOE)}$	Hold time, $\overline{\text{SCOE}}$ high after CLOCK↓	2		ns

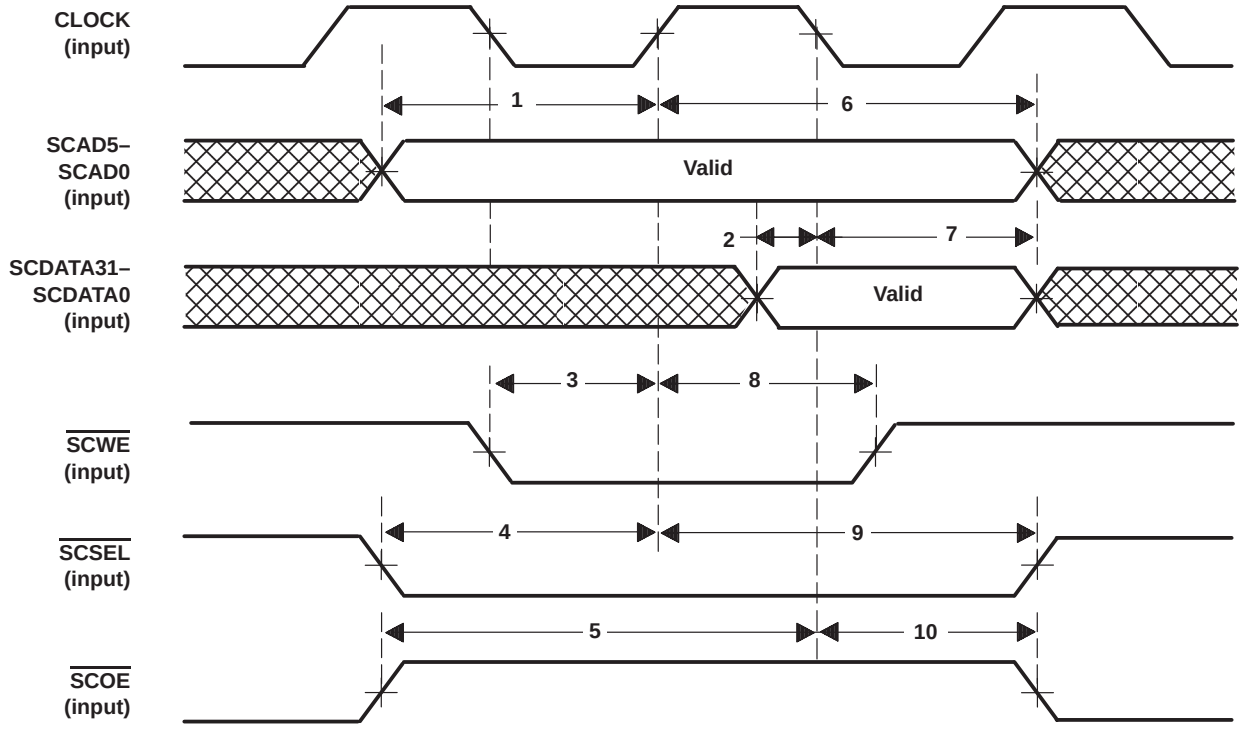


Figure 9. Slave Interface – Write Operation

timing requirements (see Figure 10)
coprocessor interface (TCCX)

NO.			MIN	MAX	UNIT
1	$t_{su(TCCX)}$	Setup time, TCCX high before CLOCK↑	10		ns
2	$t_{h(TCCX)}$	Hold time, TCCX valid after CLOCK↑	1		ns

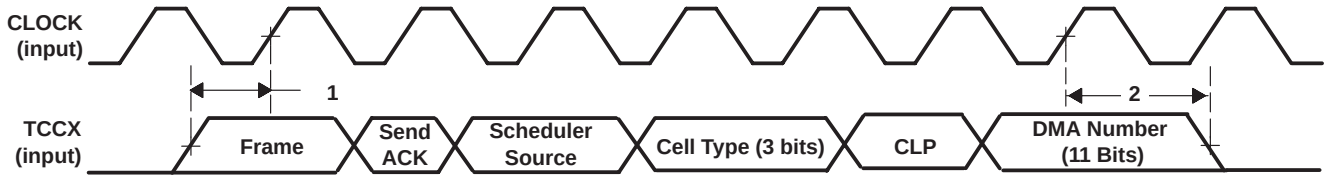


Figure 10. TCCX Interface

timing requirements (see Figure 11)
coprocessor interface (RCCX)

NO.			MIN	MAX	UNIT
1	$t_{su(RCCX)}$	Setup time, RCCX high before CLOCK↑	10		ns
2	$t_{h(RCCX)}$	Hold time, RCCX valid after CLOCK↑	1		ns

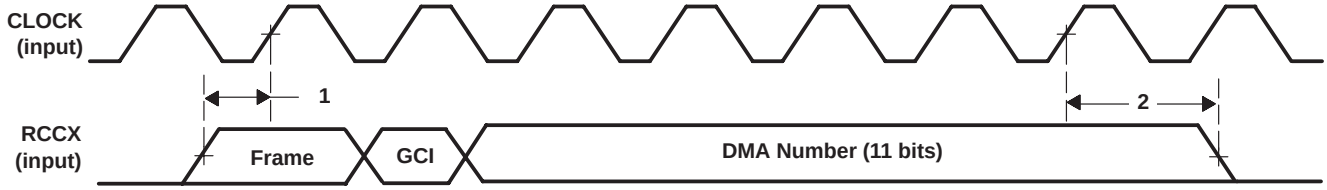


Figure 11. RCCX Interface

timing requirements (see Figure 12)
coprocessor interface (DAX)

NO.			MIN	MAX	UNIT
1	$t_{su(DAX)}$	Setup time, DAX high before CLOCK↑	10		ns
2	$t_{h(DAX)}$	Hold time, DAX valid after CLOCK↑	1		ns

Figure 12. DAX Interface

operating characteristics (see Note 6 and Figure 13)
coprocessor interface

NO.	PARAMETER		MIN	MAX	UNIT
1	$t_{d(COPFULL)}$	Delay time, from CLOCK↑ to COPFULL↑	5	15	ns

NOTE 6: The COPFULL signal is asserted high after the last byte of the seventh cell in the UTOPIA FIFO is received by the TNETA1585, or if a new RXSOC is received by the TNETA1585 for the cell that fills the FIFO. It remains high until a cell location is available in the FIFO.

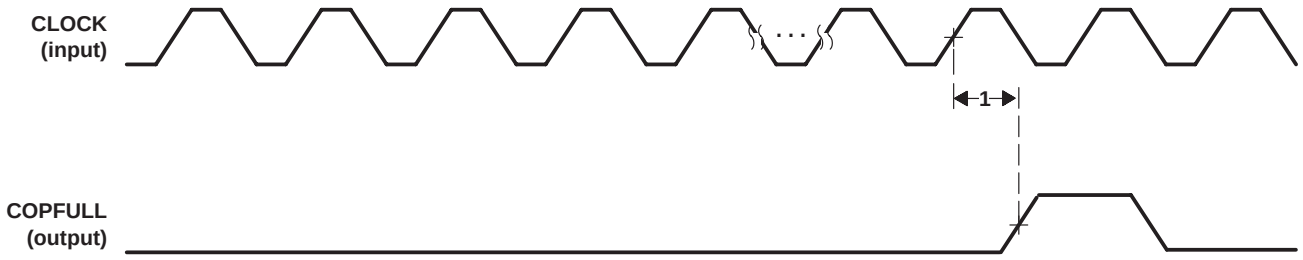
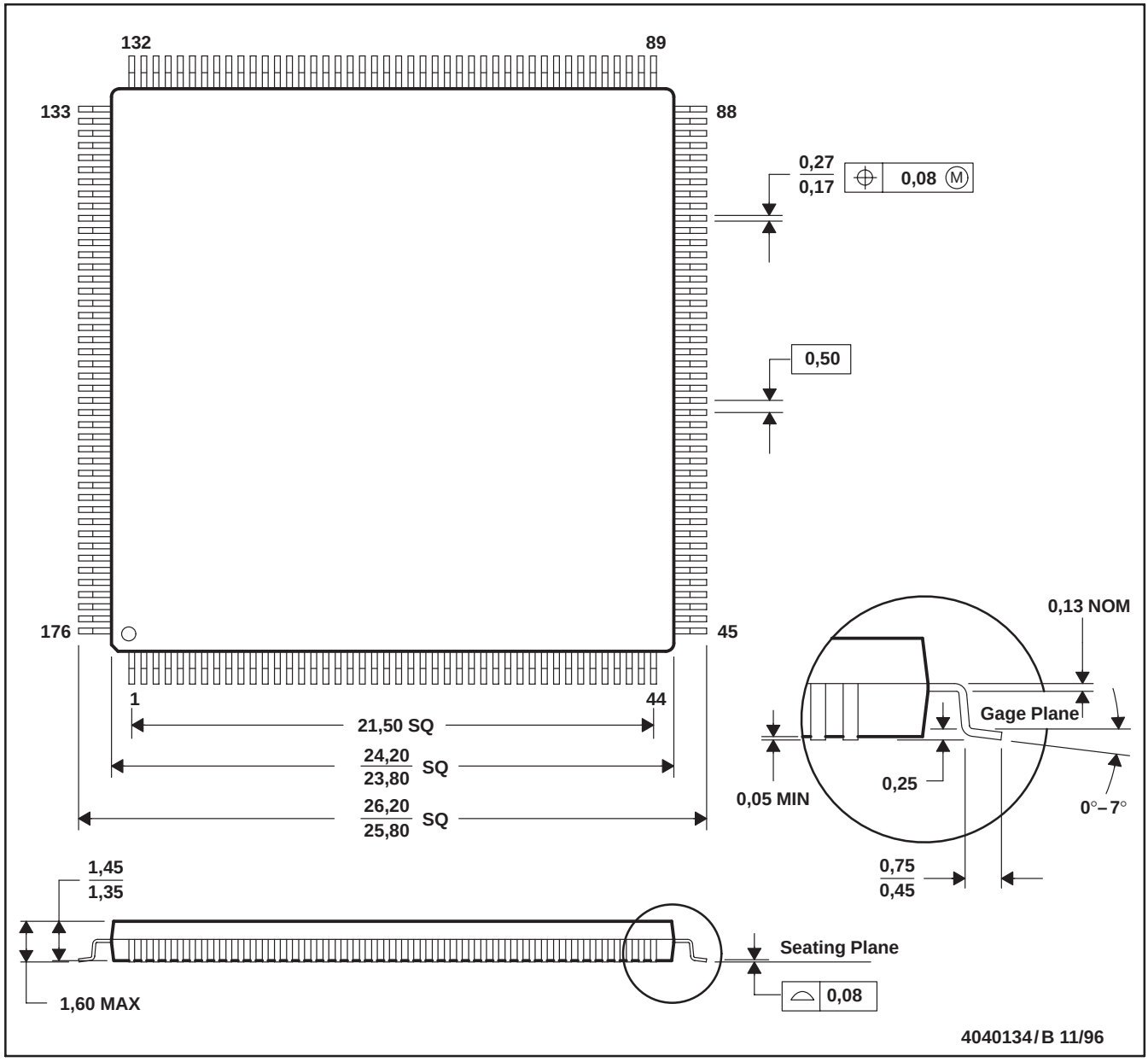


Figure 13. COPFULL Timing

MECHANICAL DATA

PGF (S-PQFP-G176) **PLASTIC QUAD FLATPACK**



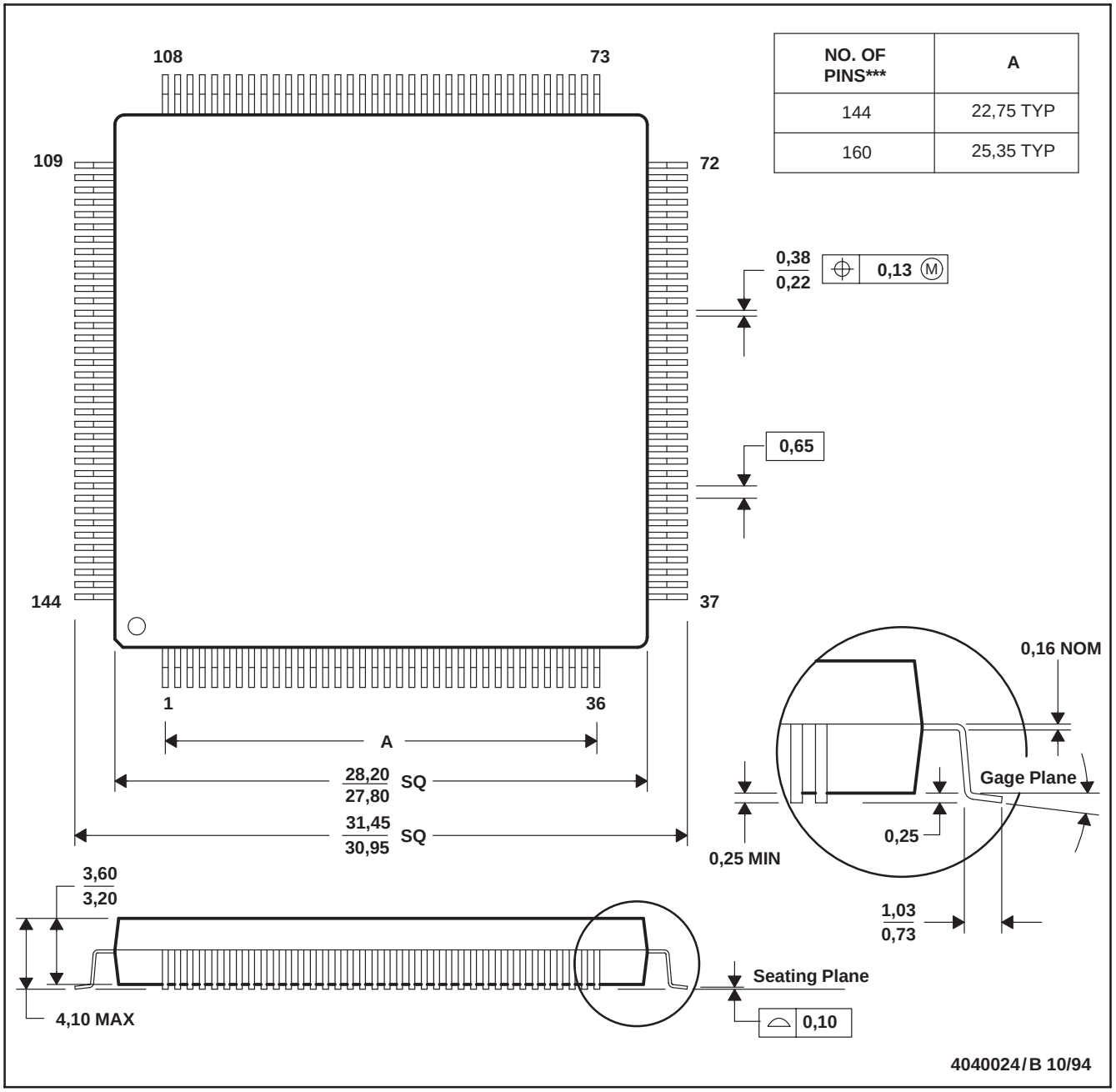
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

MECHANICAL DATA

PCM (S-PQFP-G*)** **PLASTIC QUAD FLATPACK**

(The TNETA1585 uses a 160-pin PCM package. See Note D).

144 PIN SHOWN



NO. OF PINS***	A
144	22,75 TYP
160	25,35 TYP

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-022
D. The 144 PCM is identical to the 160 PCM except that four leads per corner are removed.

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