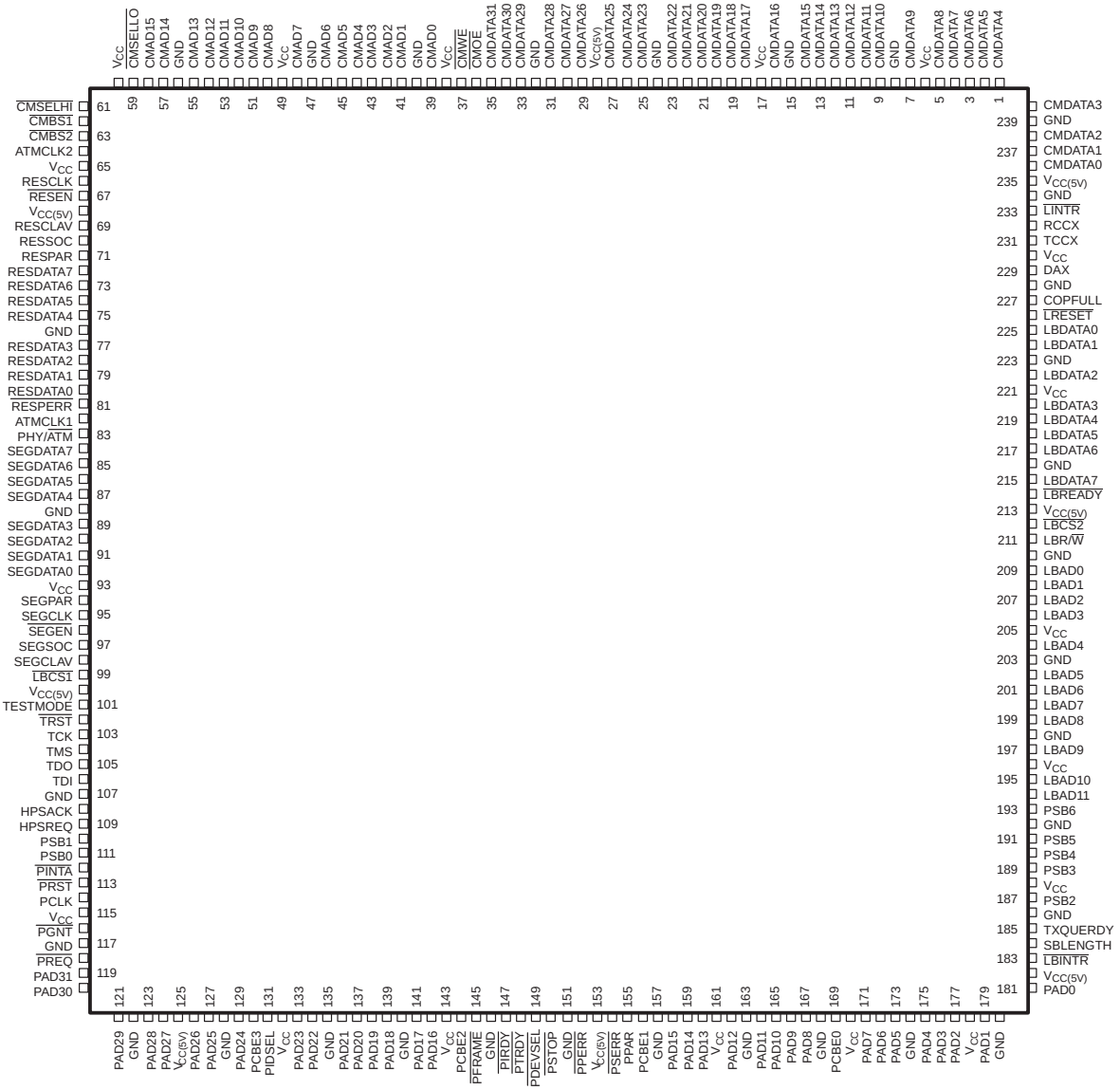
- **Supports Segmentation and Reassembly of AAL5 Packets in Accordance With ITU-T Specifications I.361 and I.363 (11/93 Update)**
- **Integrated 32-Bit PCI Bus 2.1 (06/95) Interface for Transferring Packet Data to and From Host Memory**
- **Provides Simultaneous Segmentation of up to 2048 Packets**
- **Provides Simultaneous Reassembly of up to 2048 Packets**
- **Provides Full VPI/VCI Support (12 VPI Bits and 16 VCI Bits) for Transmit and Receive Operations**
- **Supports Constant-Bit-Rate (CBR) Traffic via High-Priority Mechanism or Local Static Scheduler Table**
- **Backward Compatible With the TNETA1570 in 32-Bit PCI Mode**
- **Provides Support for Available-Bit-Rate (ABR) Traffic via External Coprocessor Interface (COPI)**
- **Provides Support for VBR-nrt Traffic via External COPI**
- **Transmit-Channel Sleep Mode Prevents the SAR Polling Channels When No Packets Are Queued**
- **High-Performance Features Include Use of Sideband Signals to Reduce Polling Across the PCI Bus**
- **Host Accesses to the PHY-Layer Device Can Be Performed Indirectly via the TNETA1575 Local Peripheral Bus**
- **Local Peripheral Bus Maps the PHY Device Into the TNETA1575 PCI-Bus Address Space**
- **Supports Easy Access to AAL5 Trailer Information**
- **Supports Buffer Scatter/Gather (Transmit and Receive Buffer Chaining)**
- **Optional Early Segmentation of Packets, So Segmentation Begins Once a Transmit Buffer Is Filled, Instead of Waiting for the Entire Packet to Be Available in Host Memory**
- **Calculates the HEC Byte for the Header of an Outgoing Cell**
- **Checks the HEC Byte of an Incoming Cell**
- **UTOPIA Level 1-Compliant Cell Interface**
- **Internal 32-Cell Receive FIFO**
- **Cell Interface Can Be Programmed to Operate as Either a Physical (PHY-Layer) Interface or as a SAR/Switch (ATM-Layer) Interface**
- **Provides Reassembly Time Out for Incoming Packets**
- **Provides an Internal Loopback Capability From Transmit to Receive**
- **Supports Boundary Scan Through a Five-Wire JTAG Interface in Accordance With IEEE Std 1149.1-1990 (Includes IEEE Std 1149.1a-1993)**

description

The TNETA1575 is an asynchronous transfer mode (ATM) segmentation and reassembly (SAR) device with a peripheral component interconnect (PCI)-bus interface and a coprocessor interface (COPI). The TNETA1575 continues the line of Texas Instruments (TI)™ ATM SAR devices directed toward the classical LAN-to-ATM translation market segment. Features have been extended to include the COPI interface, which interfaces to an external scheduler with high-performance features to eliminate polling on the PCI bus. The TNETA1575 is designed for the emerging class of high-performance enterprise networking hubs that utilize ATM in the backplane, in addition to the traditional frame-/packet-based bus systems. Some of the features required for this application include: high level of virtual channel/virtual path support, support for isochronous services, early segmentation, and high-performance, 32-bit PCI-bus support. The feature set required by cell-operating enterprise hubs is different from the sets being offered by other SAR devices, which are directed primarily toward the adapter card market.

PGC PACKAGE
(TOP VIEW)



description (continued)

The connection parameter cell-delay variation tolerance (CDVT) is not supported by the TNETA1575 scheduler on CBR connections.

This data sheet provides information on the hardware specifications of the TNETA1575 device. The document contains information on the device interfaces, timing diagrams, electrical characteristics, terminal and package information, and an overview of the device operation. All the information on the TNETA1575 data structures, configuration, and features is provided in the *TNETA1575 Programmer's Reference Guide*, literature number SDNU015.

Terminal Functions

PCI-bus interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
PAD31–PAD0	119–121, 123–124, 126–127, 129, 133–134, 136–139, 141–142, 158–160, 162, 164–167, 171–173, 175–177, 179, 181	I/O (3 state)	PCI address bus and data bus. PAD31–PAD0 are multiplexed on the same PCI terminals. During the first phase of the address phase of a transaction, PAD31–PAD0 contain a 32-bit physical address. This phase is the clock cycle when $\overline{\text{PFRAME}}$ is asserted. During the data phase, PAD7–PAD0 contain the least-significant byte and PAD31–PAD24 contain the most-significant byte. Write data is stable when $\overline{\text{PIRDY}}$ is asserted. Read data is stable when $\overline{\text{PTRDY}}$ is asserted. Data is transferred during those clock cycles when both $\overline{\text{PIRDY}}$ and $\overline{\text{PTRDY}}$ are asserted.
PCBE3–PCBE0	130, 144, 156, 169	I/O (3 state)	PCI-bus command and byte enable. PCBE3–PCBE0 lines are multiplexed on the same PCI terminals. During the address phase of a transaction, PCBE3–PCBE0 lines define the bus command. During the data phase, PCBE3–PCBE0 lines define which bytes are valid.
PCLK	114	I (TTL)	PCI clock. PCLK provides timing for all transactions on the PCI interface.
$\overline{\text{PDEVSEL}}$	149	I/O (3 state)	PCI device select. When actively driven, $\overline{\text{PDEVSEL}}$ indicates that the address of the driving device is decoded as the target of the current access. As an input, $\overline{\text{PDEVSEL}}$ indicates whether any device on the bus is selected.
$\overline{\text{PFRAME}}$	145	I/O (3 state)	PCI frame. $\overline{\text{PFRAME}}$ is driven by the current master to indicate the beginning and duration of an access. $\overline{\text{PFRAME}}$ is asserted at the beginning of the bus transaction and remains asserted during data transfer. When $\overline{\text{PFRAME}}$ is deasserted, the transaction is in the final data phase.
$\overline{\text{PGNT}}$	116	I (TTL)	PCI-bus grant. $\overline{\text{PGNT}}$ indicates to the agent that the arbiter has granted access to the bus. $\overline{\text{PGNT}}$ is a point-to-point signal and every master has its own.
PIDSEL	131	I (TTL)	PCI initialization and device select. PIDSEL is used as a chip select during configuration read and write transactions.
$\overline{\text{PINTA}}$	112	O (open drain)	PCI interrupt. $\overline{\text{PINTA}}$ is an interrupt request from PCI SAR. $\overline{\text{PINTA}}$ indicates to the host that a condition has occurred that may require attention. The TNETA1575 uses only a single interrupt line.
$\overline{\text{PIRDY}}$	147	I/O (3 state)	PCI initiator ready. $\overline{\text{PIRDY}}$ indicates the initiating agent's (bus master) ability to complete the current data phase of the transaction. During a write, $\overline{\text{PIRDY}}$ indicates valid data on PAD31–PAD0. During a read, $\overline{\text{PIRDY}}$ indicates the master is prepared to accept the data. $\overline{\text{PIRDY}}$ is used with $\overline{\text{PTRDY}}$. Wait cycles are inserted until both $\overline{\text{PIRDY}}$ and $\overline{\text{PTRDY}}$ are asserted.
PPAR†	155	I/O (3 state)	PCI parity. PPAR is even parity across PAD31–PAD0 and PCBE3–PCBE0. For data phases, PPAR is valid one clock after either $\overline{\text{PIRDY}}$ is asserted on a write or $\overline{\text{PTRDY}}$ is asserted on a read. Once asserted, PPAR remains valid until one clock after the completion of the current data phase. The master drives the PPAR for address- and write-data phases, and the target drives PPAR for the read-data phase.
$\overline{\text{PPERR}}$‡	152	I/O (3 state)	PCI parity error. $\overline{\text{PPERR}}$ reports a data-parity error on all commands except special cycle. An agent cannot report a $\overline{\text{PPERR}}$ until it has claimed the access by asserting $\overline{\text{PDEVSEL}}$ and completed a data phase.

† If the host does not desire to implement parity in the system, terminal 155 is connected through a resistor to a valid logic level and the $\overline{\text{SERR}}$ enable bit in the PCI command register is set to 0.

‡ If the host does not desire to implement parity in the system, terminal 152 is connected through a 1-MΩ pullup resister and the $\overline{\text{SERR}}$ enable bit in the PCI command register is set to 0.

Terminal Functions (Continued)

PCI-bus interface (continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{\text{PREQ}}$	118	O (CMOS)	PCI request. $\overline{\text{PREQ}}$ indicates to the arbiter that this agent desires use of the bus. Every master has its own $\overline{\text{PREQ}}$.
$\overline{\text{PRST}}$	113	I (TTL)	PCI reset. $\overline{\text{PRST}}$ forces the PCI sequence of each device to a known state.
PSB1–PSB0	110–111	O (CMOS)	PCI sideband. PSB1–PSB0 lines define the size of the transfer when the TNETA1575 is the bus master. The definitions of these signals are as follows: 00: 4-byte transfer 01: 16-byte transfer (except for receive-completion ring) 10: Payload transfer 11: Transfer to receive-completion ring (20-byte transfer) PSB1–PSB0 are synchronous to the address phase of the bus-master operations by the TNETA1575. The sideband signals do not change upon a bus retry after disconnect.
PSB2	187	I (TTL)	PCI sideband 2. PSB2 is an indication from the host to the SAR that the host has read an entry from the receive-completion ring without an interrupt. The SAR uses this signal to increment the receive-completion-ring entry counter. Pulse duration is for one clock cycle synchronous to the PCI clock. This input terminal has an internal 100-μA pulldown active terminator. This is a 3.3-V tolerant input signal. If it is driven by a 5-V signal, it must be connected to an external voltage divider consisting of a 36-kΩ down resistor and a 24-kΩ up resistor to ensure that the input is not driven above 3.3 V.
PSB3	189	O (CMOS)	PCI sideband 3. PSB3 is an indication from the SAR to the host that the SAR is reading an entry from sideband-controlled free-buffer ring 1. PSB3 is synchronous to the address phase of bus-master operations by the SAR. PSB3 does not change upon a bus retry after disconnect. Pulse duration is for one clock cycle synchronous to the PCI-address phase.
PSB4	190	I (TTL)	PCI sideband 4. PSB4 is an indication from the host to the SAR that the host has written a new entry into sideband-controlled free-buffer ring 1. The SAR uses this signal to increment the sideband-controlled free-buffer ring-1 entry counter. Pulse duration is for one clock cycle synchronous to the PCI clock. This input terminal has an internal 100-μA pulldown active terminator. This is a 3.3-V tolerant input signal. If it is driven by a 5-V signal, it must be connected to an external voltage divider consisting of a 36-kΩ down resistor and a 24-kΩ up resistor to ensure that the input is not driven above 3.3 V.
PSB5	191	O (CMOS)	PCI sideband 5. PSB5 is an indication from the SAR to the host that the SAR is reading an entry from sideband-controlled free-buffer ring 2. PSB5 is synchronous to the address phase of bus-master operations by the SAR. PSB5 does not change upon a bus retry after disconnect. Pulse duration is for one clock cycle synchronous to the PCI-address phase.
PSB6	193	I (TTL)	PCI sideband 6. PSB6 is an indication from the host to the SAR that the host has written a new entry into sideband-controlled free-buffer ring 2. The SAR uses this signal to increment the sideband-controlled free-buffer ring-2 entry counter. Pulse duration is for one clock cycle synchronous to the PCI clock. This input terminal has an internal 100-μA pulldown active terminator. This is a 3.3-V tolerant input signal. If it is driven by a 5-V signal, it must be connected to an external voltage divider consisting of a 36-kΩ down resistor and a 24-kΩ up resistor to ensure that the input is not driven above 3.3 V.
$\overline{\text{PSERR}}$	154	I/O (open drain)	PCI system error. $\overline{\text{PSERR}}$ reports address-parity errors and data-parity errors on special-cycle commands.
$\overline{\text{PSTOP}}$	150	I/O (3 state)	PCI stop. $\overline{\text{PSTOP}}$ indicates that the current target is requesting the master to stop the current transaction.
$\overline{\text{PTRDY}}$	148	I/O (3 state)	PCI target ready. $\overline{\text{PTRDY}}$ indicates the target agent's (selected device) ability to complete the current data phase of the transaction. During a read, $\overline{\text{PTRDY}}$ indicates that valid data is present on PAD31–PAD0. During a write, $\overline{\text{PTRDY}}$ indicates that the target is prepared to accept data.

Terminal Functions (Continued)

PCI-bus interface (continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
SBLENGTH	184	O (CMOS)	Sideband length. SBLENGTH indicates to the host when the TNETA1575 is bursting eight free-buffer entries by asserting SBLENGTH high, or that it is bursting one entry when inactive low. Pulse duration is for one clock cycle synchronous to the PCI-address phase.
TXQUERDY	185	O (CMOS)	Transmit queue ready. TXQUERDY indicates to the host when the transmit queue register is available for a write access by the host. TXQUERDY is a PCI-sideband signal and is synchronous with the PCI clock.

cell-segmentation interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION	
SEGCLAV	98	O (CMOS)	Segmentation cell available	
			PHY mode	SEGCLAV ($\overline{\text{RXEMPTY}}$/RXCLAV) indicates that a complete cell is available.
			ATM mode	SEGCLAV ($\overline{\text{TXENB}}$) is active low when SEGDATA contains a valid byte.
SEGCLK	95	I (TTL)	Segmentation clock	
			PHY mode	SEGCLK (RXCLK) is used to synchronize transfers on SEGDATA. SEGCLK is sourced from the UTOPIA interface.
			ATM mode	SEGCLK (TXCLK) is used to synchronize transfers on SEGDATA. SEGCLK is sourced from the ATMCLK.
SEGDATA7–SEGDATA0	84–87, 89–92	O (CMOS)	Segmentation data	
			PHY mode	SEGDATA7–SEGDATA0 (RXDATA) is byte-wide true data that is sourced by the TNETA1575. SEGDATA7 is the most significant bit.
			ATM mode	SEGDATA7–SEGDATA0 (TXDATA) is byte-wide true data that is sourced by the TNETA1575. SEGDATA7 is the most significant bit.
$\overline{\text{SEGEN}}$	96	I (TTL)	Segmentation enable	
			PHY mode	$\overline{\text{SEGEN}}$ ($\overline{\text{RXENB}}$) indicates that a valid byte of SEGDATA will be sent during the next clock cycle.
			ATM mode	$\overline{\text{SEGEN}}$ ($\overline{\text{TXFULL}}$/TXCLAV) indicates that at least one byte of SEGDATA will be accepted.
SEGPAR	94	O (CMOS)	Segmentation parity	
			PHY mode	SEGPAR (RXPAR) is the odd-parity bit over SEGDATA7–SEGDATA0.
			ATM mode	SEGPAR (TXPAR) is the odd-parity bit over SEGDATA7–SEGDATA0.
SEGSOC	97	O (CMOS)	Segmentation start of cell	
			PHY mode	SEGSOC (RXSOC) is active high when SEGDATA contains the first valid byte of the cell and is sourced by the TNETA1575.
			ATM mode	SEGSOC (TXSOC) is active high when SEGDATA contains the first valid byte of the cell and is sourced by the TNETA1575.

Terminal Functions (Continued)

high-priority segmentation (request and acknowledge)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
HPSACK	108	O (CMOS)	High-priority segmentation acknowledge. HPSACK is asserted for one PCI-bus clock cycle to acknowledge that HPSREQ is detected.
HPSREQ	109	I (TTL)	High-priority segmentation request. HPSREQ is sampled at each new segmentation opportunity and is synchronous to the PCI-bus clock. When HPSREQ is active, TNETA1575 initiates the procedure for transmitting a cell from TX DMA channel 1. To ensure that the high-priority segmentation request is processed, HPSREQ remains active until HPSACK is set low. HPSREQ is deasserted within two PCI-bus clock cycles of when HPSACK is asserted.

cell-reassembly interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION	
RESCLAV	69	O (CMOS)	Reassembly cell available	
			PHY mode	RESCLAV ($\overline{\text{TXFULL}}$/TXCLAV) indicates that a transfer of a complete cell can be accepted.
			ATM mode	RESCLAV ($\overline{\text{RXENB}}$) indicates that a valid byte RESDATA will be sent during the next clock cycle.
RESCLK	66	I (TTL)	Reassembly clock	
			PHY mode	RESCLK (TXCLK) is used to synchronize transfers on RESDATA. The UTOPIA interface is used as the source for RESCLK.
			ATM mode	RESCLK (RXCLK) is used to synchronize transfers on RESDATA. ATMCLK is used as the source for RESCLK.
RESDATA7–RESDATA0	72–75, 77–80	I (TTL)	Reassembly data	
			PHY mode	RESDATA7–RESDATA0 (TXDATA). RESDATA7 is the most significant bit.
			ATM mode	RESDATA7–RESDATA0 (RXDATA). RESDATA7 is the most significant bit.
$\overline{\text{RESEN}}$	67	I (TTL)	Reassembly enable	
			PHY mode	$\overline{\text{RESEN}}$ ($\overline{\text{TXENB}}$) goes active low when RESDATA contains a valid byte.
			ATM mode	$\overline{\text{RESEN}}$ ($\overline{\text{RXEMPTY}}$/RXCLAV) indicates that transfer of a complete cell can be accepted.
RESPAR	71	I (TTL)	Reassembly parity	
			PHY mode	RESPAR (TXPAR) is the odd-parity bit over RESDATA7–RESDATA0.
			ATM mode	RESPAR (RXPAR) is the odd-parity bit over RESDATA7–RESDATA0.
$\overline{\text{RESPERR}}$	81	O (CMOS)	Reassembly parity error (not required by UTOPIA)	
			PHY mode	$\overline{\text{RESPERR}}$ indicates that parity error was present at the previous rising edge of RESCLK.
			ATM mode	
RESSOC	70	I (TTL)	Reassembly start of cell	
			PHY mode	RESSOC (TXSOC) is received when RESDATA contains the first valid byte of the cell.
			ATM mode	RESSOC (RXSOC) is received when RESDATA contains the first valid byte of the cell.

Terminal Functions (Continued)

control-memory interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CMAD15–CMAD0	58–57, 55–50, 48, 46–41, 39	O (CMOS)	Control-memory address. CMAD15–CMAD0 contain a 16-bit physical address to the control memory.
$\overline{\text{CMBS1}}$	62	O (CMOS)	Control memory bank select 1. $\overline{\text{CMBS1}}$ selects bank 1, containing 32K × 32 SRAM addresses in the lower 64K addresses, when active low.
$\overline{\text{CMBS2}}$	63	O (CMOS)	Control memory bank select 2. $\overline{\text{CMBS2}}$ selects bank 2, containing 32K × 32 SRAM addresses in the lower 64K addresses, when active low.
CMDATA31–CMDATA0	35–33, 31–29, 27–25, 23–18, 16, 14–9, 7, 5–1, 240, 238–236	I (TTL) O (CMOS)	Control-memory data. CMDATA31–CMDATA0 contain 32-bit data to/from the control memory.
$\overline{\text{CMOE}}$	36	O (CMOS)	Control-memory output enable. When $\overline{\text{CMOE}}$ is active low, the address is valid and data is read on the rising edge of $\overline{\text{CMOE}}$.
$\overline{\text{CMSELHI}}$	61	O (CMOS)	Control memory select high. $\overline{\text{CMSELHI}}$ selects the upper 64K control-memory addresses when active low.
$\overline{\text{CMSELL0}}$	59	O (CMOS)	Control memory select low. $\overline{\text{CMSELL0}}$ selects the lower 64K control-memory addresses when active low.
$\overline{\text{CMWE}}$	37	O (CMOS)	Control-memory write enable. When $\overline{\text{CMWE}}$ is active low, the address and data are valid.

traffic coprocessor interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
RCCX	232	O (CMOS)	Receive-cell status indication. RCCX indicates to the traffic coprocessor that a cell was received on the UTOPIA interface, and the RX DMA channel was assigned to the cell.
TCCX	231	O (CMOS)	Transmit-cell status indication. TCCX indicates to the traffic coprocessor that a cell was transmitted from the SAR, and the TX DMA channel was assigned to the cell.
DAX	229	O (CMOS)	Data availability indication. DAX indicates to the traffic coprocessor when data is available on a particular channel or when the SAR has completed segmentation of a packet.
LRESET	226	O (CMOS)	Local reset. $\overline{\text{LRESET}}$ provides a reset indication to the traffic coprocessor. $\overline{\text{LRESET}}$ is derived from the PCI-bus reset input.
LINTR	233	I (TTL)	Local interrupt. $\overline{\text{LINTR}}$ provides an interrupt indication from the traffic coprocessor to the SAR. When $\overline{\text{LINTR}}$ goes active low, the SAR sets a bit in the status register and generates a PCI interrupt unless the interrupt is masked through the interrupt mask register. This terminal has an internal 100-μA pullup active terminator. This signal must be connected to an external 2.2-kΩ pullup resistor that is connected to a 3.3-V voltage source.
COPFULL	227	I (TTL)	Coprocessor full. COPFULL indicates that the traffic coprocessor RX FIFO is about to fill up. A 100-μA pulldown active terminator is connected to this input. The pulldown is disabled when the COPPRES bit is set in the SAR configuration register.

Terminal Functions (Continued)

local-bus interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
LBAD11–LBAD0	194–195, 197, 199–202, 204, 206–209	O (CMOS)	Local-bus address. LBAD11–LBAD0 are driven by the TNETA1575 and are used to address the peripheral attached to the local bus. Terminal 194 is the most significant bit.
LBR/W	211	O (CMOS)	Local-bus read/write. LBR/$\overline{W}$ is an active-low signal that indicates a write operation and is driven by the TNETA1575. A read operation is indicated as active high.
LBCS1	99	O (CMOS)	Local-bus chip select 1. $\overline{\text{LBCS1}}$ is an active-low signal that is used to select an external peripheral on the TNETA1575 local bus.
LBCS2	212	O (CMOS)	Local-bus chip select. 2 $\overline{\text{LBCS2}}$ is an active-low signal that is used to select an external peripheral on the TNETA1575 local bus.
LBREADY	214	I (TTL) (with internal pullup)	Local-bus ready. $\overline{\text{LBREADY}}$ is driven by a local-bus slave device. The TNETA1575 has two modes of operation on this input terminal. The default mode causes the TNETA1575 to complete the bus transaction after eight PCI-bus cycles, regardless of $\overline{\text{LBREADY}}$. Alternatively, the TNETA1575 can be placed in a mode using $\overline{\text{LBREADY}}$. This is a 3.3-V tolerant input signal. If it is driven by a 5-V signal, it must be connected to an external voltage divider consisting of a 36-kΩ down resistor and a 24-kΩ up resistor to ensure that the input is not driven above 3.3 V.
LBINTR	183	I (TTL) (with internal pullup)	Local-bus interrupt. $\overline{\text{LBINTR}}$ is an active-low interrupt that is generated and driven by a local-bus device. This signal must be connected to an external 2.2-kΩ pullup resistor that is connected to a 3.3-V voltage source.
LBDATA7–LBDATA0	215, 217–220, 222, 224–225	I/O (TTL input / CMOS output) and (with internal pullup)	Local-bus data. LBDATA7–LBDATA0 are used to transfer data to and from a local-bus slave device, and are driven by the TNETA1575 or a local-bus slave device. LBDATA7, (terminal 215) is the most significant bit.

boundary-scan interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
TCK	103	I (TTL)	Test clock. TCK clocks the test-access-port (TAP) operation.
TDI	106	I (TTL)	Test data input. TDI shifts serial-test data and instructions into the device during TAP operation.
TDO	105	O (TTL)	Test data output. TDO shifts serial-test data and instructions out of the device during TAP operation.
TMS	104	I (TTL)	Test-mode select. TMS controls the state of the TAP controller.
$\overline{\text{TRST}}$	102	I (TTL)	Test reset. $\overline{\text{TRST}}$ asynchronously forces the TAP controller to a known state. This terminal must be tied low when the JTAG port is not being used.

test signal

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
TESTMODE	101	I (TTL)	Test mode. TESTMODE is used for device testing. High is for test mode and low is for normal operation.

Terminal Functions (Continued)

miscellaneous signals

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION	
ATMCLK1	82	O (CMOS)	ATM clock1	
			PHY mode	ATMCLK1 is driven low and can be left as a no connection (NC).
			ATM mode	The ATMCLK1 is used as the clock source to provide for data transfers/ synchronization across the transmit UTOPIA interface between the SAR and external devices not connected to the PCI-host interface. The ATMCLK1 is connected to SEGCLK in the ATM mode. If the TNETA1585 is not used, the ATMCLK1 also can be used as the clock source for the receive UTOPIA interface. The clock generated by the interface is 33 MHz (nominal), using the PCI clock.
ATMCLK2	64	O (CMOS)	ATM clock2. ATMCLK2 is an auxiliary ATM clock that is used as the clock source to the TNETA1585 or a similar-type device. When the TNETA1585 is used, ATMCLK2 is also connected to the RESCLK input. The clock generated by the interface is 33 MHz (nominal), using the PCI clock.	
PHY/$\overline{\text{ATM}}$	83	I (TTL)	PHY/$\overline{\text{ATM}}$ mode select. PHY/$\overline{\text{ATM}}$ selects ATM mode when low and the PHY mode when high.	

power and ground

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
GND	8, 15, 24, 32, 40, 47, 56, 76, 88, 107, 117, 122, 128, 135, 140, 146, 151, 157, 163, 168, 174, 180, 186, 192, 198, 203, 210, 216, 223, 228, 234, 239	Ground. GND is the 0-V reference for the device.
V_{CC}	6, 17, 38, 49, 60, 65, 93, 115, 132, 143, 161, 170, 178, 188, 196, 205, 221, 230	Supply voltage. V_{CC} is the 3.3-V supply for the digital logic.
$V_{CC(5V)}$	28, 68, 100, 125, 153, 182, 213, 235	Supply voltage. $V_{CC(5V)}$ is the 5-V supply for the clamp diodes used with the 5-V tolerant input and output buffers for protection.

detail description

The TNETA1575 device contains the following interfaces:

- PCI-host interface
- Cell interface
- Local-bus interface
- Control-memory interface
- Traffic coprocessor interface
- JTAG interface

PCI-host interface

The TNETA1575 incorporates a PCI revision 2.1 host interface. The following section describes the features and operation of the PCI-host interface.

The TNETA1575 operates as a PCI-slave device for configuration cycles, accesses to internal registers, and accesses to the onboard control memory. It also acts as a PCI-master device for accessing data structures, which are contained in host memory.

As a slave, the TNETA1575 incorporates the following features:

- Directly supports the memory read, memory write, configuration read, and configuration write PCI commands and aliases the memory read multiple, memory read line, and memory write and invalidate to the basic memory commands.
- Supports single data-cycle transfers and disconnects with retry after the first data cycle.
- Does not retry single data accesses to any data structures accessed via the SAR, i.e., registers, control memory, or coprocessor.
- Responds to accesses as a 32-bit agent with medium $\overline{\text{DEVSEL}}$ timing (single wait state)
- Utilizes a 1-M block of addresses, which is mapped into the host memory space using a single base-address register.
- Does not support resource locking.

As a master, the TNETA1575 incorporates the following features:

- Utilizes the memory read, memory read line, memory read multiple, and memory write PCI bus commands.
- Initiates transactions as a 32-bit agent.
- Performs multiple data-cycle transfers, when possible, up to a maximum of 12 data cycles.
- The TNETA1575 asserts the $\overline{\text{IRDY}}$ signal one clock cycle after the $\overline{\text{FRAME}}$ signal is asserted.
- $\overline{\text{IRDY}}$ remains asserted during the burst cycle.

As described in the PCI local-bus specification rev 2.1, the TNETA1575 provides a 64-byte configuration space that can be accessed by system software for configuration, initialization, and error handling. The TNETA1575 responds to type 0 configuration accesses.

A configuration map of the 64-byte configuration space is as follows:

ADDRESS	BYTE 3	BYTE 2	BYTE 1	BYTE 0	READ/WRITE
0x00	**Device ID**		**Vendor ID**		R
0x04	**Status**		**Command**		R/W
0x08	**Class Code**			**Revision ID**	R
0x0C	BIST†	**Header Type**	**Latency Timer**	**Cache Line Size**	R/W
0x10	Base Address 0				R/W
0x14	Base Address 1†				R/W
0x18	Base Address 2†				R/W
0x1C	Base Address 3†				R/W
0x20	Base Address 4†				R/W
0x24	Base Address 5†				R/W
0x28	Cardbus CIS Pointer†				R
0x2C	Subsystem ID†		Subsystem Vendor ID†		R/W
0x30	Expansion ROM Base Address†				R/W
0x34	Reserved (returns 0 when read)				—
0x38	Reserved (returns 0 when read)				—
0x3C	**Max_Lat**	**Min_Gnt**	**Interrupt Pin**	**Interrupt Line**	R/W
0x40	Reserved	Reserved	Reserved	Reserved	R/W
0x44–0xFF	Reserved (returns 0 when read)				R

† Optional registers are not implemented for the TNETA1575, which return 0 when read.

The control memory is accessed via the host PCI interface in full 32-bit words. Byte enable is not supported. All four bytes in a 32-bit word in the control memory are read or written in a single instruction.

If none of the byte enables are asserted for a write instruction, none of the data in the 32-bit word is altered. If any byte enable is asserted, then the entire 32-bit word is overwritten.

cell interface

The TNETA1575 transfers and receives ATM cells through the cell interface. The cell interface is designed in accordance with the ATM forum UTOPIA level 1 specification and is configurable as either an 8-bit PHY or ATM interface. The ATM mode is chosen when the TNETA1575 interfaces with a framer such as the TNETA1500. The PHY mode is chosen when the TNETA1575 interfaces with a switch port. The operation of this dual ATM/PHY interface requires the use of two external terminals – ATMCLK and PHY/$\overline{\text{ATM}}$. The ATMCLK output is a buffered version of the PCI clock.

When PHY/$\overline{\text{ATM}}$ is high (PHY mode), the segmentation interface functions as a PHY-RX port and the reassembly interface functions as a PHY-TX port. The clock speed supported by the interface is a maximum of 33 MHz. In this mode, the ATMCLK output normally is not used by the cell interface.

When PHY/$\overline{\text{ATM}}$ is low (ATM mode), the segmentation interface functions as an ATM-TX port and the reassembly interface functions as an ATM-RX port. The clock speed supported by the interface is a maximum of 33 MHz. In this mode, the ATMCLK can be used as the clock source to provide for data transfers/synchronization or another external-clock source(s) can be used.

The interface operates as a synchronous 8-bit (byte-wide) data path. The interface functions with both octet-level and cell-level handshaking.

segmentation interface, PHY mode

The segmentation-unit interface on the TNETA1575 operates as the RX UTOPIA interface on a PHY device when the TNETA1575 is operating in PHY mode. The PHY/$\overline{\text{ATM}}$ input terminal has to be high to operate in PHY mode.

This cell interface works on the low-to-high transition of SEGCLK to sample and generate signals. All signals are active high, unless noted with a bar above the signal name.

TNETA1575 SIGNAL NAME	TNETA1575 TERMINAL NUMBER	UTOPIA SIGNAL NAME
SEGCLK	95	RXCLK
SEGDATA7–SEGDATA0	84–87, 89–92	RXDATA7–RXDATA0
SEGPAR	94	RXPRTY
SEGSOC	97	RXSOC
$\overline{\text{SEGEN}}$	96	RXENB
SEGCLAV	98	RXCLAV/$\overline{\text{RXEMPTY}}$

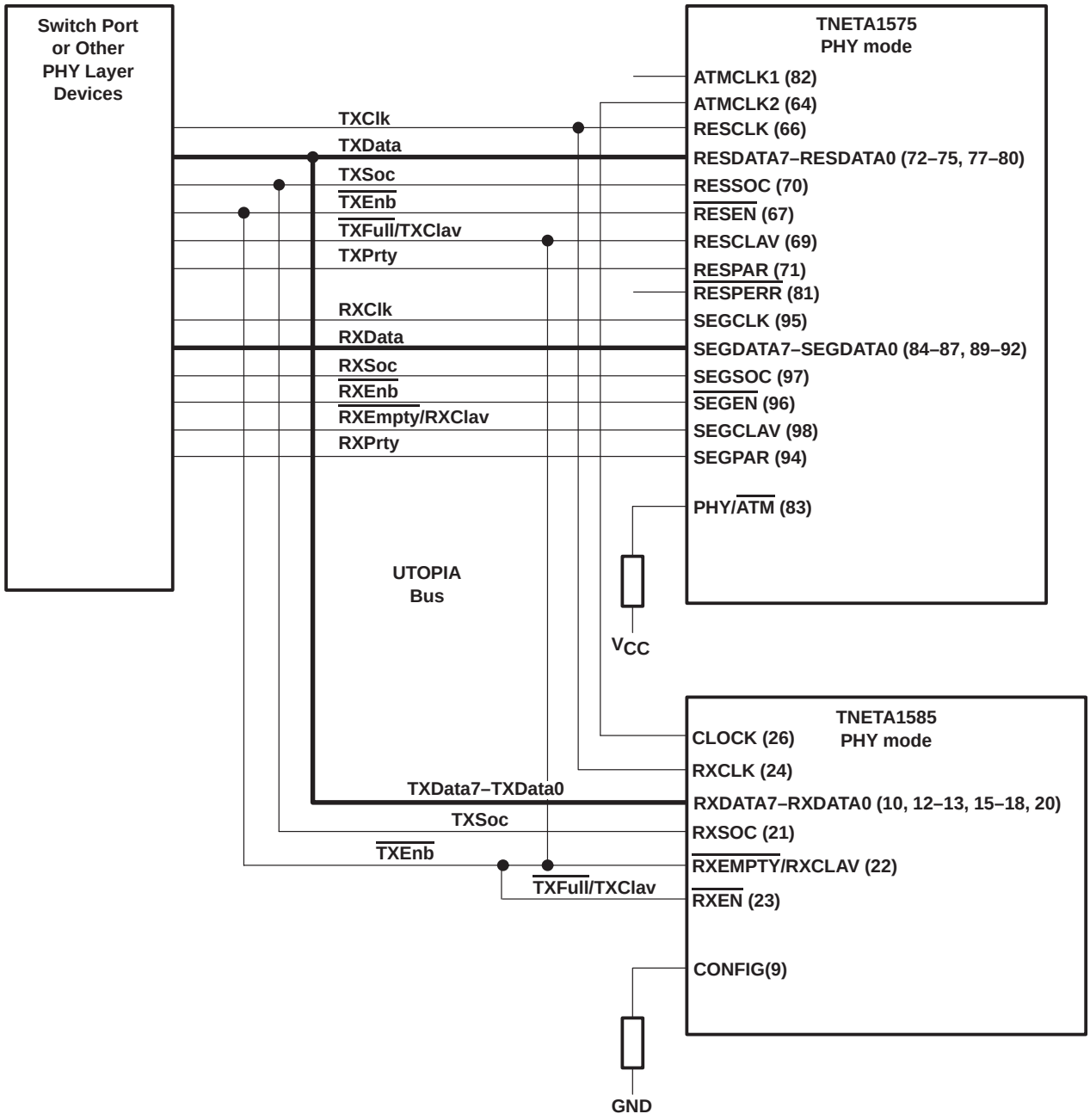
reassembly interface, PHY mode

The reassembly-unit interface on the TNETA1575 functions as the TX UTOPIA interface in a PHY device when the TNETA1575 is operating in PHY mode.

This reassembly-cell interface works on the low-to-high transition of RESCLK to sample and generate signals. All signals are active high, unless noted with a bar above the signal name.

TNETA1575 SIGNAL NAME	TNETA1575 TERMINAL NUMBER	UTOPIA SIGNAL NAME
RESCLK	66	TXCLK
RESDATA7–RESDATA0	72–75, 77–80	TXDATA7–TXDATA0
RESPAR	71	TXPRTY
RESSOC	70	TXSOC
RESEN	67	TXENB
RESCLAV	69	TXCLAV/$\overline{\text{TXFULL}}$
$\overline{\text{RESPERR}}$	81	N/A

connecting the TNETA1575 to the UTOPIA bus (See Figure 1 and Note A)



NOTE A: Figures 1 and 2 show the interconnections needed to interface to a TNETA1585 device. If the TNETA1575 is operated without the external scheduler device, then the lines going to the TNETA1585 are ignored, and everything remains as depicted above.

Figure 1. UTOPIA Bus Connections In PHY Mode

segmentation interface in ATM mode

The segmentation-unit interface on the TNETA1575 operates as a TX UTOPIA interface in an ATM-layer device. The PHY/$\overline{\text{ATM}}$ terminal must be driven low to make the TNETA1575 operate in ATM mode.

This cell interface works on the low-to-high transition of SEGCLK to sample and generate signals. All signals are active high, unless noted with a bar above the signal name.

TNETA1575 SIGNAL NAME	TNETA1575 TERMINAL NUMBER	UTOPIA SIGNAL NAME
SEGCLK	95	TXCLK
SEGDATA7–SEGDATA0	84–87, 89–92	TXDATA7–TXDATA0
SEGPAR	94	TXPRTY
SEGSOC	97	TXSOC
$\overline{\text{SEGEN}}$	96	TXCLAV/$\overline{\text{TXFULL}}$
SEGCLAV	98	$\overline{\text{TXENB}}$

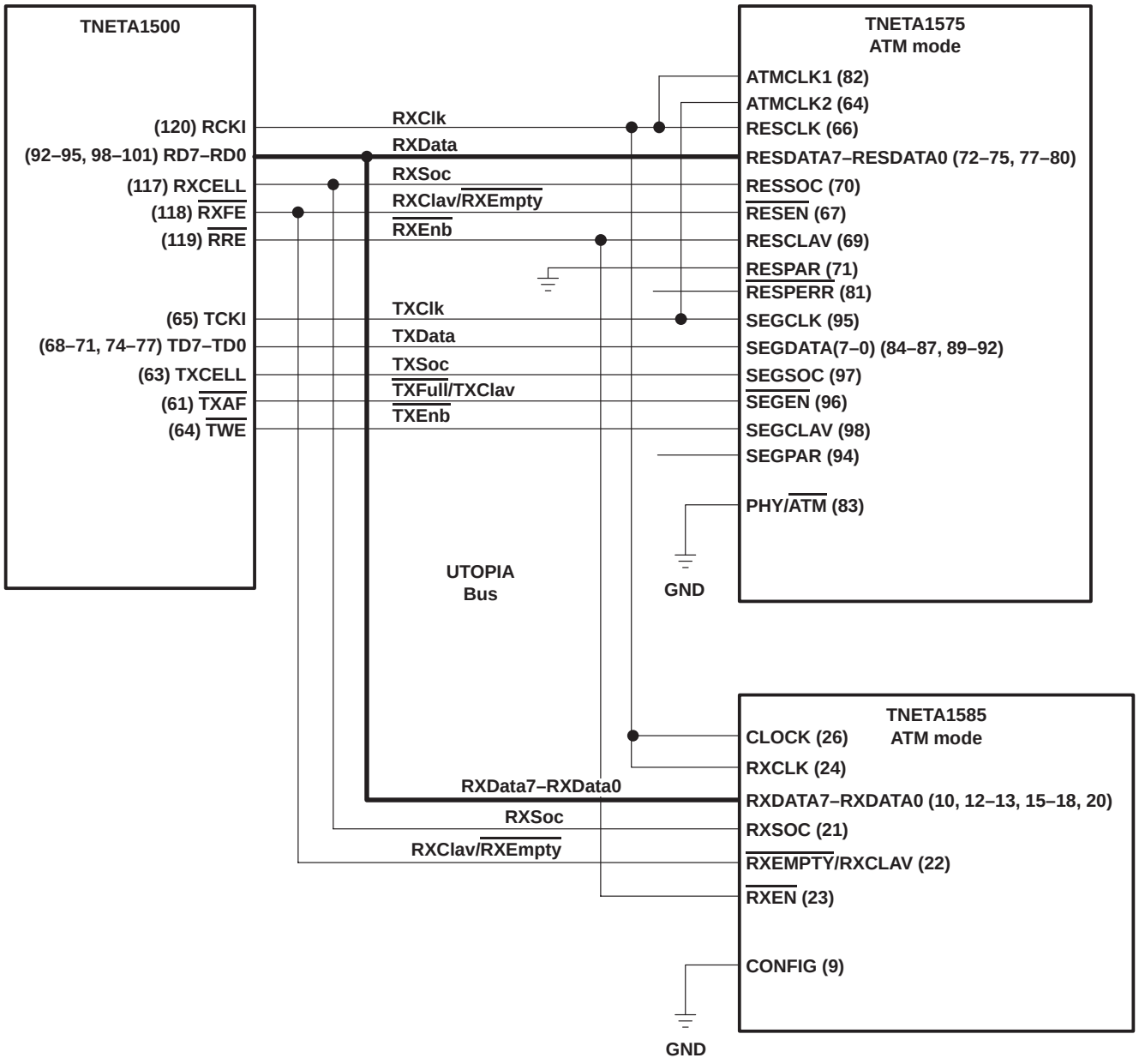
reassembly interface in ATM mode

The reassembly-unit interface on the TNETA1575 operates as the RX UTOPIA interface in an ATM device when the TNETA1575 is configured in ATM mode.

This receive cell interface works on the low-to-high transition of RESCLK to sample and generate signals. All signals are active high, unless noted with a bar above the signal name.

TNETA1575 SIGNAL NAME	TNETA1575 TERMINAL NUMBER	UTOPIA SIGNAL NAME
RESCLK	66	RXCLK
RESDATA7–RESDATA0	72–75, 77–80	RXDATA7–RXDATA0
RESPAR	71	RXPRTY
RESSOC	70	RXSOC
$\overline{\text{RESEN}}$	67	RXCLAV/$\overline{\text{RXEMPTY}}$
RESCLAV	69	$\overline{\text{RXENB}}$
$\overline{\text{RESPERR}}$	81	N/A

connecting the TNETA1575 to the UTOPIA bus (see Figure 2 and Note A)



NOTE A: Figures 1 and 2 show the interconnections needed to interface to a TNETA1585 device. If the TNETA1575 is operated without the external scheduler device, then the lines going to the TNETA1585 are ignored, and everything remains as depicted above.

Figure 2. UTOPIA Bus Connections in ATM Mode

local-bus interface

This interface allows access to the registers in two devices on the local bus. The TNETA1575 accepts a ready signal from devices on the bus as a handshake. This accommodates slow devices, and also can be used to relax timing constraints on the register interface for PHY-layer devices. The local bus is accessed exclusively via PCI-bus transactions with TNETA1575 as the slave, with the exception of the local-bus interrupt signal. The 12-bit address of the local bus comprises the PCI-bus address lines (bits 13–2). These directly drive the local-bus address bits (11–0). The signals in this interface are defined in the terminal-function table of this document.

control-memory interface

Control memory contains the local data structures and state information used by the device to transmit and receive data on a virtual connection (VC) or channel. The scheduler table, transmit active-packet counters, free-buffer ring-pointer table, and TX/RX DMA state table are located in control memory. The scheduler table contains 2,048 entries, consisting of one word each. The transmit active-packet counters contain the number of packets that have been queued for transmit on each packet segmentation ring. The free-buffer ring-pointer table contains the pointers to the receive free-buffer rings. There are 256 entries in the free-buffer ring-pointer table (one entry for each free-buffer ring), and each entry consists of two words. The TX/RX DMA state table contains 2,048 entries, one entry for each transmit-/receive-channel pair. Each entry consists of 16 words; eight words for the transmit operation and eight words for the receive operation. The definitions and functional description of the TNETA1575 data structures are discussed in detail in the *TNETA1575 Programmer's Reference Guide*, literature number SDNU015.

These local data structures are located off the chip in external SRAM. The TNETA1575 is designed to operate with 15-ns (or faster) asynchronous SRAM devices. The total SRAM requirement to support a full implementation of control memory is approximately 37K $\times$ 32. The device can operate with a control-memory SRAM of size 32K $\times$ 32. A system design with the 32K $\times$ 32 SRAM size only supports up to 1,792 TX/RX-channel pairs. To support the entire range of 2,048 TX/RX-channel pairs, the TNETA1575 requires a SRAM configuration of 64K $\times$ 32.

The control-memory map for the TNETA1575 device follows:

control-memory map

MEMORY BLOCK	SIZE (IN 32-BIT WORDS)	CONTROL-MEMORY ADDRESS (HEX)	PCI-OFFSET ADDRESS (HEX)
Scheduler table	2,048	00000–007FF	00000–01FFC
Active packet counters	1,024	00800–00BFF	02000–02FFC
Reserved	512	00C00–00DFF	03000–037FC
Free-buffer ring pointer-table	512	00E00–00FFF	03800–03FFC
TX/RX DMA state table	32,768	01000–08FFF	04000–23FFC
DMA lookup table†	4,096	09000–09FFF	24000–27FFF
Local-bus device 1 ($\overline{\text{LBCS1}}$)	4,096	0A000–0AFFF	28000–2BFFC
Local-bus device 2 ($\overline{\text{LBCS2}}$)	4,096	0B000–0BFFF	2C000–2FFFC
Reserved	16,384	0C000–0FFFF	30000–3FFFC
Traffic coprocessor memory space	65,536	10000–1FFFF	40000–7FFFC

† The DMA lookup table is physically located on the chip and is not located off of the chip in the control memory.

control-memory interface (continued)

The SAR control-memory port is used to select both the external SRAM that stores the local-data structures and state information for the TNETA1575 and an external device that can be used to provide an external scheduler and other transmit data structures. The total control-memory address space consists of 128K locations, with 64K locations dedicated to the TNETA1575 SRAM, and the remaining 64K dedicated to an external device such as an external scheduler (see Figure 3).

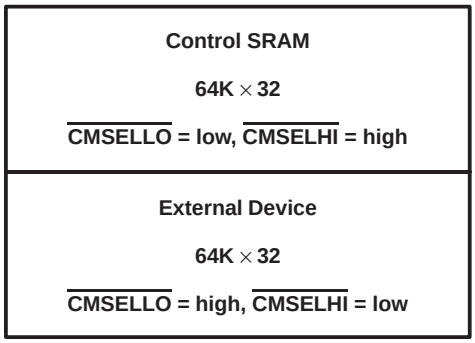


Figure 3. Control-Memory Address Space

Control memory select bit $\overline{\text{CMSELHI}}$ is used to select the upper 64K-address space. $\overline{\text{CMSELHI}}$ is active low when the higher 64K addresses are selected, and inactive when the lower 64K addresses are selected. The control-memory select bit $\overline{\text{CMSELLO}}$ is used to select the lower 64K-address space.

In addition, when the $\overline{\text{CMSELLO}}$ terminal is active low and the lower 64K addresses are selected, the user can select between a single 64K × 32 SRAM bank or two 32K × 32 SRAM banks. The two terminals $\overline{\text{CMSB1}}$ and $\overline{\text{CMSB2}}$ are active low and allow the user to select between the two banks, as follows:

1. $\overline{\text{CMSELLO}}$ is active low and CMA15 is low to select bank 1 ($\overline{\text{CMSB1}}$ is enabled).
2. $\overline{\text{CMSELLO}}$ is active low and CMA15 is high to select bank 2 ($\overline{\text{CMSB2}}$ is enabled).

There are 16 control-memory address terminals that are used to address the various blocks of control memory. Together with the two select terminal ($\overline{\text{CMSELLO}}$ and $\overline{\text{CMSELHI}}$) and the two bank operating terminals, these 20 terminals provide for a total of 128K addressable-memory locations.

CONTROL-MEMORY ADDRESS SPACE SELECTED (HEXADECIMAL)	$\overline{\text{CMSELLO}}$	$\overline{\text{CMSB1}}$	$\overline{\text{CMSB2}}$	$\overline{\text{CMSELHI}}$
00000–07FFF	L	L	H	H
08000–0FFFF	L	H	L	H
10000–1FFFF	H	H	H	L

traffic coprocessor interface

The TNETA1575 provides a traffic coprocessor interface (COPI) to add flexibility to the segmentation scheduling algorithm. The COPI is implemented using the control-memory interface and three unidirectional serial channels that transfer information from the TNETA1575 to the coprocessor and COPI-full indicator signal.

The TNETA1575 acts as an initiator of all transfers to and from the coprocessor.

The primary method of communication between the TNETA1575 and a coprocessor is via the control-memory interface. It is intended that an external coprocessor be mapped into the control-memory space, starting at address 10000 and extending to address 1FFFF. This equates to a total address space of 64K 32-bit words that is reserved for use by the coprocessor.

The mapping of the coprocessor in control memory provides a means for the TNETA1575 to initialize the coprocessor, to obtain information related to the scheduling of cells, and to obtain RM cell contents.

In this document, the three serial channels and the COPI-full indicator signal are described.

received cell-indication channel

A serial-bit interface allows the TNETA1575 to signal to the coprocessor that a cell has been received on a particular DMA channel. This interface is necessary to avoid duplicating the hardware that is used to resolve a VPI/VCI to a DMA channel. When a cell is received, the VPI/VCI value from the header is extracted and is used as a key in a lookup algorithm. When the lookup is complete, the TNETA1575 sends a 13-bit frame to the coprocessor, which is formatted as follows:

DMA NUMBER	GOOD/BAD CELL INDICATOR	FRAMING
(12–2)	(1)	(0)

The frame is transmitted to the coprocessor through the RCCX terminal, starting with bit 0. When a frame is not actively being transmitted, the RCCX terminal is driven to a 0.

transmitted cell-indication channel

A single-bit interface allows the TNETA1575 to signal to the coprocessor that a cell will be transmitted on a particular DMA channel. This interface is necessary to facilitate statistics processing in the coprocessor and to aid in ATM-forum available-bit-rate (ABR) scheduling. As soon as the TNETA1575 determines that it has the data to send a cell, it simultaneously sends an 18-bit frame to the coprocessor, which is formatted as follows:

DMA NUMBER	CLP INDICATOR	CELL TYPE	SCHEDULING SOURCE	SEND ACKNOWLEDGE	FRAMING
(17–7)	(6)	(5–3)	(2)	(1)	(0)

The frame is transmitted to the coprocessor through the TCCX terminal, starting with bit 0. When a frame is not actively being transmitted, the TCCX terminal is driven to a 0.

data-availability channel

A single-bit interface allows the TNETA1575 to signal to the coprocessor when data is available or unavailable on a particular channel. When the host writes to the transmit queue register to notify the TNETA1575 that a packet has been queued, or if the TNETA1575 completes segmentation of the last packet on a particular DMA channel, a 13-bit frame is sent to the coprocessor, which is formatted as follows:

DMA NUMBER	DATA AVAILABLE/UNAVAILABLE	FRAMING
(12–2)	(1)	(0)

The frame is transmitted to the coprocessor through the DAX terminal, starting with bit 0. When a frame is not actively being transmitted, the DAX terminal is driven to a 0.

COP – interface full-indication signal

The COPI interface on the TNETA1575 provides a COPFULL input terminal that indicates when the traffic coprocessor interface receive FIFOs are within one cell of filling up. The TNETA1575 reacts by deasserting the UTOPIA receive enable signal (RESCLAV or $\overline{\text{RXENABLE}}$, depending on whether PHY or ATM mode is selected) according to the UTOPIA specification. After the COPFULL input terminal goes inactive low, the TNETA1575 asserts the UTOPIA receive enable signal RESCLAV or $\overline{\text{RXENABLE}}$, depending on whether PHY or ATM mode is selected on the UTOPIA interface. If this terminal is not connected, the TNETA1575 operates under normal conditions.

TNETA1575 / TNETA1585 interconnect

Figure 4 shows the interconnect of the TNETA1575 (SAR) and the TNETA1585 traffic cop, including information on connection of the control-memory interface, the coprocessor interface, and the cell interfaces.

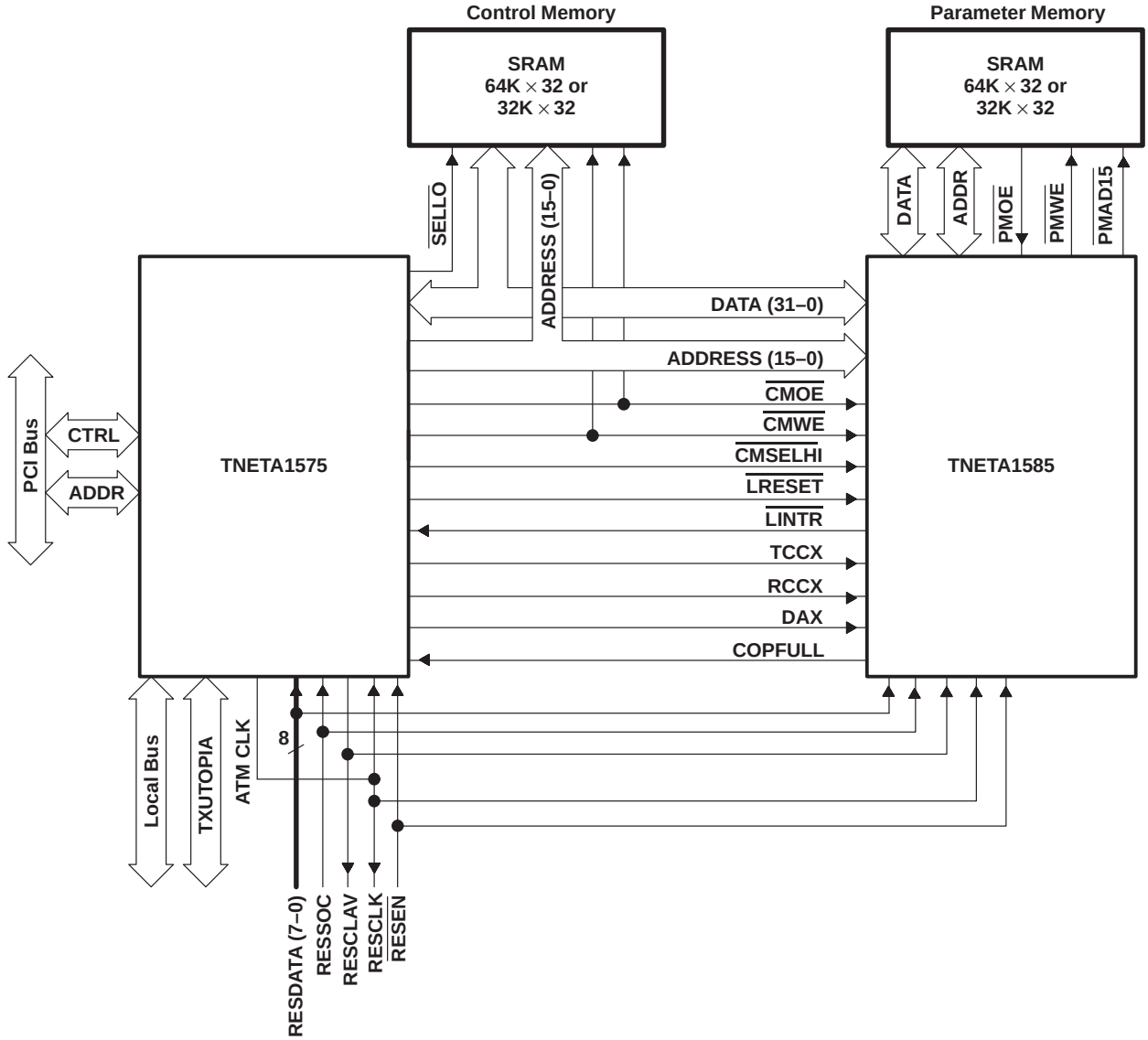


Figure 4. TNETA1575 Interconnect to TNETA1585

JTAG interface

The TNETA1575 supports boundary scan through a five-wire JTAG interface in accordance with IEEE Std 1149.1–1990 (includes IEEE Std 1149.1a–1993), IEEE Standard Test Access Port and Boundary-Scan Architecture.

The maximum operating frequency is 10 MHz for the JTAG interface.

JTAG instruction set.

The TNETA1575 supports the following instructions:

INSTRUCTION	OP CODE (BINARY FORMAT)
Extest	000
Idcode	100
Sample/Preload	001
Bypass	111
Internal Scan	010
High Z	101

idcode

	VARIANT	PART NUMBER	MANUFACTURER	LEAST SIGNIFICANT BIT
Bit number	31–28	27–12	11–1	0
Binary code	0000		00000010111	1

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.5 V to 4 V
Supply voltage range, $V_{CC(5V)}$ (see Note 1) . . . . . –0.5 V to 5.5 V
Input voltage range, standard TTL, 3-V PCI, V_I . . . . . –0.5 V to V_{CC} + 0.5 V
Input voltage range, 5-V tolerant TTL, V_I . . . . . $V_{CC(5V)}$ + 0.5 V
Output voltage range, standard TTL, 3-V PCI, V_O . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, 5-V tolerant TTL, V_O . . . . . 5 V to V_{CC} + 0.5 V
Input clamp current, TTL, I_{IK} (V_I < 0 or V_I > V_{CC}) (see Note 2) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) (see Note 3) . . . . . ±20 mA
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the GND terminals.
2. Applies for external input and bidirectional buffers without hysteresis. $V_I > V_{CC}$ does not apply to fail-safe terminals. Use $V_I > V_{CC(5V)}$ for 5-V tolerant terminals.
3. Applies for external output and bidirectional buffers. $V_O > V_{CC}$ does not apply to fail-safe terminals. Use $V_O > V_{CC(5V)}$ for 5-V tolerant terminals.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	Commercial	3	3.3	3.6	V
$V_{CC(5V)}$	Supply voltage, 5-V tolerant TTL	Commercial	4.5	5	5.5	V
V_I	Input voltage	TTL, 3-V PCI	0		V_{CC}	V
		5-V tolerant TTL	0		$V_{CC(5V)}$	
V_O	Output voltage	TTL, 3-V PCI	0		V_{CC}	V
		5-V tolerant TTL†	0		V_{CC}	
V_{IH}	High-level input voltage	TTL	2		V_{CC}	V
		3-V PCI	0.475 V_{CC}		V_{CC}	
		5-V tolerant TTL	2		$V_{CC(5V)}$	
V_{IL}	Low-level input voltage	TTL	0		0.8	V
		3-V PCI	0		0.325 V_{CC}	
		5-V tolerant TTL	0		0.8	
T_A	Operating free-air temperature		0		70	°C

† V_{CC} must be applied to drive the output to a high-impedance state (Z) for 5-V tolerant operation.

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	TTL	I_{OH} = 8 mA	V_{CC}–0.6		V
			I_{OH} = 4 mA			
		5-V tolerant TTL	I_{OH} = 8 mA	V_{CC}–0.6		
			I_{OH} = 4 mA			
		3-V PCI	I_{OH} = 8.6 V_{CC} (mA)	0.5 V_{CC}		
V_{OL}	Low-level output voltage	TTL	I_{OL} = 8 mA		0.4	V
			I_{OL} = 4 mA		0.4	
		5-V tolerant TTL	I_{OL} = 8 mA		0.4	
			I_{OL} = 4 mA		0.4	
		3-V PCI	I_{OL} = 8 V_{CC} (mA)		0.3 V_{CC}	
I_{IH}	High-level input current	TTL	$V_I = V_{IH\ (max)}$, See Note 4		±1	µA
		5-V tolerant TTL	$V_I = V_{IH\ (min)}$		–760	
		3-V PCI	$V_I = V_{IH\ (max)}$, See Note 4		±1	
I_{IL}	Low-level input current	TTL	$V_I = V_{IL\ (min)}$, See Note 5		±1	µA
		5-V tolerant TTL			±1	
		3-V PCI			±1	
I_{OZ}	High-impedance-state output current	TTL			±20	µA
		5-V tolerant TTL			±20	
		3-V PCI			±20	

NOTES: 4. These specifications apply only when the pulldown terminator is turned off.
5. These specifications apply only when the pullup terminator is turned off.

recommended power-supply sequencing for mixed-voltage devices

The recommended power-supply sequencing in a mixed-voltage system is as follows:

- When turning on the power supply, all 3.3-V and 5-V supplies should start ramping from 0 V and reach 95 percent of their end-point values within a 25-ms time window. All bus contention between the TNETA1575 and external devices is eliminated by the end of the 25-ms time window. The preferred order of supply ramping is to ramp the 3.3-V supply, followed by the 5-V supply. This order is not mandatory, but it allows a larger cumulative number of power-supply on events than does the reverse order.
- When turning off the power supply, all 3.3-V and 5-V supplies should start ramping from steady-state values and reach 5 percent of these values within a 25-ms time window. All bus contention between the TNETA1575 and external devices is eliminated by the end of the 25-ms time window. The preferred order of supply ramping is to ramp down the 5-V supply, followed by the 3.3-V supply. This order is not mandatory, but it allows a larger cumulative number of power supply off events than the reverse order.

If these precautions and guidelines are not followed, the TNETA1575 device may experience failures.

timing requirements
PCI-bus interface

NO.			MIN	NOM	MAX	UNIT
	$f_{clock(PCLK)}$	Clock frequency, PCLK†		33		MHz
	$t_{su(BUS)}$	Setup time, bused signals valid before PCLK↑ (see Note 6)	7			ns
	$t_{su(PGNT)}$	Setup time, $\overline{PGNT}$ low before PCLK↑ (see Note 6)	10			ns
	$t_{su(PREQ)}$	Setup time, $\overline{PREQ}$ low before PCLK↑ (see Note 6)	12			ns
	$t_{h(IN)}$	Hold time, inputs valid after PCLK↑	0			ns

† The UTOPIA-clock (ATMCLK) frequency cannot be greater than three times the PCI-clock (PCLK) frequency or less than one-third the PCI-clock (PCLK) frequency because synchronization can break down on the FIFOs and cells can be lost. If this relationship is maintained between the PCLK clock and the ATMCLK clock, the PCLK clock can operate at or below 33 MHz and cells are not lost.

NOTE 6: $\overline{PREQ}$ and $\overline{PGNT}$ are point-to-point signals, and have different output valid delay and input setup times than do bused signals. PGNT has a setup time of 10 ns; $\overline{PREQ}$ has a setup time of 12 ns. All other signals are bused.

operating characteristics over recommended operating conditions
PCI-bus interface

NO.	PARAMETER		MIN	MAX	UNIT
	$t_{d(BUSV)}$	Delay time, PCLK↑ to bused signals valid (see Note 6)	2	11	ns
	$t_{d(PGNT)}$	Delay time, PCLK↑ to $\overline{PGNT}$ low (see Note 6)	2	12	ns
	$t_{d(PREQ)}$	Delay time, PCLK↑ to $\overline{PREQ}$ low (see Note 6)	2	12	ns
	$t_{on(FLT–ACT)}$	Turn-on time, float to active	2		ns
	$t_{off(ACT–FLT)}$	Turn-off time, active to float		28	ns
	$t_{on(RST)}$	Turn-on time, power stable to reset active	1		ms
	$t_{on(PCLK–RST)}$	Turn-on time, PCLK stable to reset active	100		µs
	$t_{off(RST–OF)}$	Turn-off time, reset active to output float		40	ns

NOTE 6. $\overline{PREQ}$ and $\overline{PGNT}$ are point-to-point signals, and have different output valid delay and input setup times than do bused signals. PGNT has a setup time of 10 ns; $\overline{PREQ}$ has a setup time of 12 ns. All other signals are bused.

timing requirements (see Figure 5)
PCI-bus interface

NO.			MIN	MAX	UNIT
1	$t_{w(PCLKH)}$	Pulse duration, PCLK high	12		ns
2	$t_{w(PCLKL)}$	Pulse duration, PCLK low	12		ns
3	$t_{su(PGNT)}$	Setup time, PGNT low before PCLK↑	10		ns
4	$t_{su(PAD)}$	Setup time, PAD31–PAD0 valid before PCLK↑	7		ns
5	$t_{su(PTRDY)}$	Setup time, $\overline{\text{PTRDY}}$ low before PCLK↑	7		ns
6	$t_{su(PDEVSEL)}$	Setup time, $\overline{\text{PDEVSEL}}$ low before PCLK↑	7		ns
7	$t_{h(PAD)}$	Hold time, PAD31–PAD0 valid after PCLK↑	0		ns
8	$t_{h(PTRDY)}$	Hold time, $\overline{\text{PTRDY}}$ low after PCLK↑	0		ns
9†	$t_{h(PDEVSEL)}$	Hold time, $\overline{\text{PDEVSEL}}$ low after PCLK↑	1		ns

† This 1-ns minimum hold time deviates from the 0-ns minimum hold time specified in PCI-Local Bus Specification (Revision 2.1).

operating characteristics (see Figure 5)
PCI-bus interface

NO.	PARAMETER		MIN	MAX	UNIT
10	$t_{d(PFRAME)}$	Delay time, PCLK↑ to $\overline{\text{PFRAME}}$↓	2	11	ns
11	$t_{d(PAD)}$	Delay time, PCLK↑ to PAD31–PAD0 valid	2	11	ns
12	$t_{d(PCBE)}$	Delay time, PCLK↑ to PCBE3–PCBE0 valid	2	11	ns
13	$t_{d(PIRDY)}$	Delay time, PCLK↑ to $\overline{\text{PIRDY}}$↓	2	11	ns
14	$t_{d(PREQ)}$	Delay time, PCLK↑ to $\overline{\text{PREQ}}$↓	2	12	ns

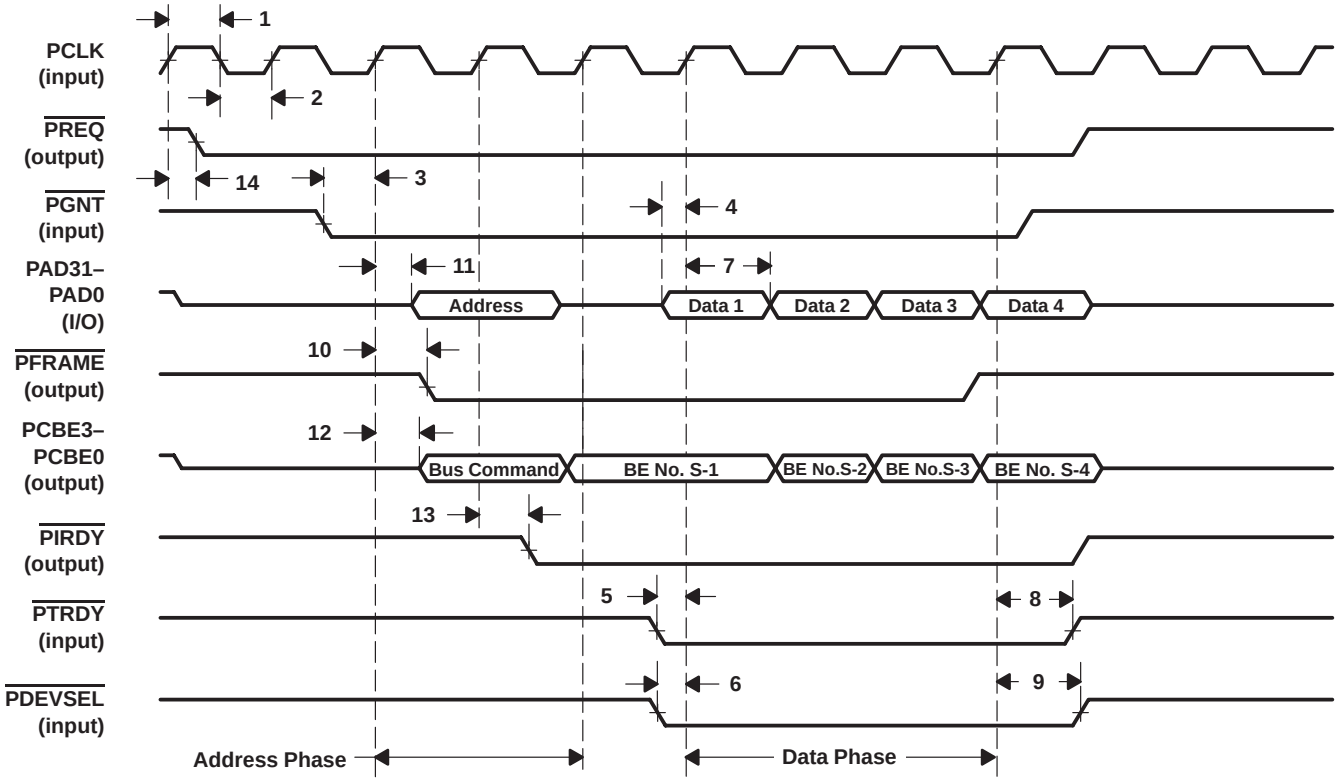


Figure 5. Read Operation (PCI SAR as Master)

timing requirements (see Figure 6)
PCI-bus interface

NO.			MIN	MAX	UNIT
1	$t_{su(PGNT)}$	Setup time, $\overline{\text{PGNT}}$ low before PCLK↑	10		ns
2	$t_{su(PTRDY)}$	Setup time, $\overline{\text{PTRDY}}$ low before PCLK↑	7		ns
3	$t_{su(PDEVSEL)}$	Setup time, $\overline{\text{PDEVSEL}}$ low before PCLK↑	7		ns
4	$t_{h(PTRDY)}$	Hold time, $\overline{\text{PTRDY}}$ low after PCLK↑	0		ns
5†	$t_{h(PDEVSEL)}$	Hold time, $\overline{\text{PDEVSEL}}$ low after PCLK↑	1		ns

† This 1-ns minimum hold time deviates from the 0-ns minimum hold time specified in PCI-Local Bus Specification (Revision 2.1).

operating characteristics (see Figure 6)
PCI-bus interface

NO.	PARAMETER		MIN	MAX	UNIT
6	$t_{d(PREQ)}$	Delay time, PCLK↑ to $\overline{\text{PREQ}}$↓	2	12	ns
7	$t_{d(PFRAME)}$	Delay time, PCLK↑ to $\overline{\text{PFRAME}}$↓	2	11	ns
8	$t_{d(PCBE)}$	Delay time, PCLK↑ to PCBE valid	2	11	ns
9	$t_{d(PIRDY)}$	Delay time, PCLK↑ to $\overline{\text{PIRDY}}$↓	2	11	ns
10	$t_{d(PAD)}$	Delay time, PCLK↑ to PAD31–PAD0 valid	2	11	ns
11	$t_{d(PSB)}$	Delay time, PCLK↑ to PSB1–PSB0 valid	2	11	ns

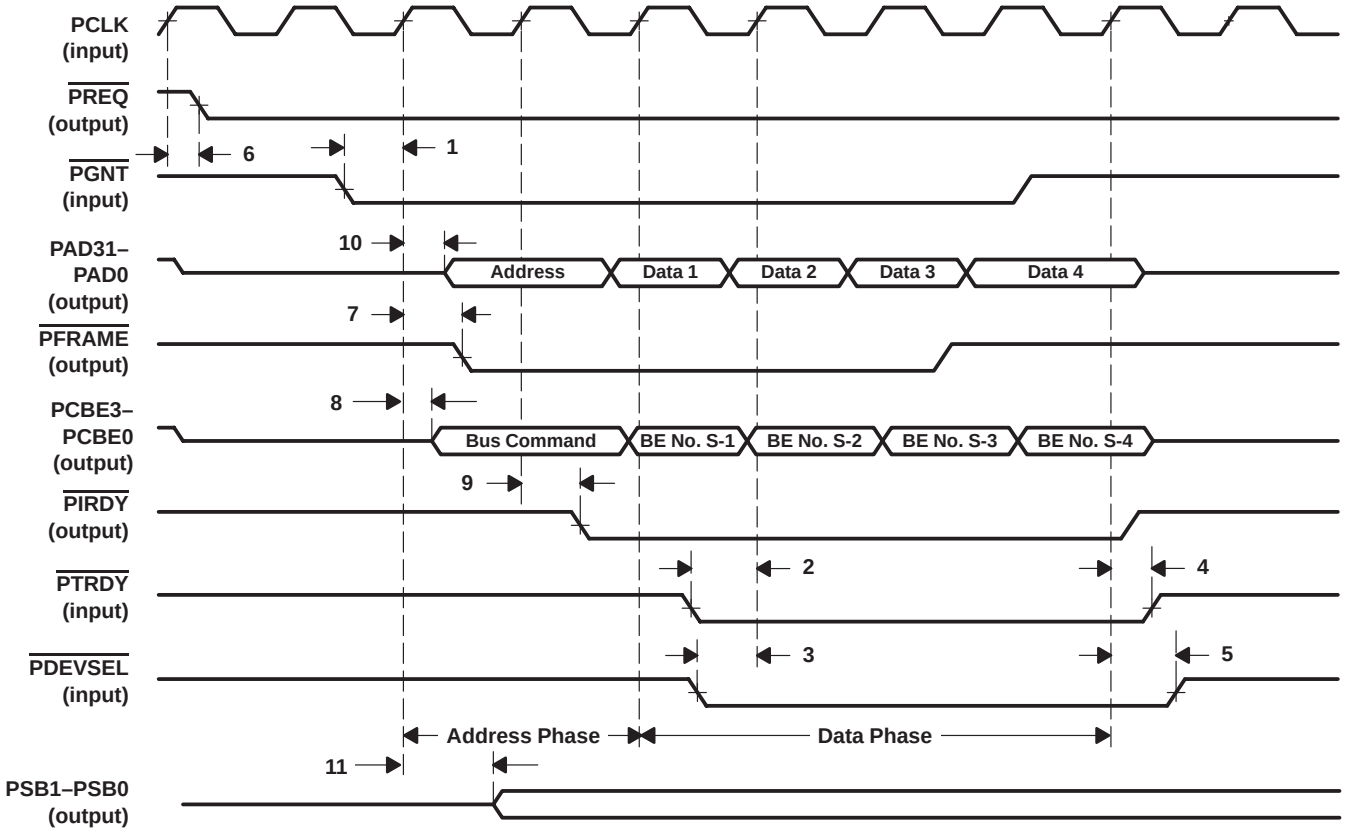


Figure 6. Write Operation (PCI SAR as Master)

timing requirements (see Figure 7)
PCI-bus interface

NO.			MIN	MAX	UNIT
1	$t_{su(PIDSEL)}$	Setup time, PIDSEL high before PCLK↑	7		ns
2	$t_{su(PAD)}$	Setup time, PAD31–PAD0 valid before PCLK↑	7		ns
3	$t_{su(PCBE)}$	Setup time, PCBE3–PCBE0 valid before PCLK↑	7		ns
4	$t_{su(PIRDY)}$	Setup time, $\overline{\text{PIRDY}}$ low before PCLK↑	7		ns
5†	$t_{h(PIDSEL)}$	Hold time, PIDSEL high after PCLK↑	1		ns
6	$t_{h(PAD)}$	Hold time, PAD31–PAD0 valid after PCLK↑	0		ns
7†	$t_{h(PCBE)}$	Hold time, PCBE3–PCBE0 valid after PCLK↑	1		ns
8†	$t_{h(PIRDY)}$	Hold time, $\overline{\text{PIRDY}}$ low after PCLK↑	1		ns

† This 1-ns minimum hold time deviates from the 0-ns minimum hold time specified in PCI-Local Bus Specification (Revision 2.1).

operating characteristics (see Figure 7)
PCI-bus interface

NO.	PARAMETER		MIN	MAX	UNIT
9	$t_{d(PAD)}$	Delay time, PCLK↑ to PAD31–PAD0 valid	2	11	ns
10	$t_{d(PTRDY)}$	Delay time, PCLK↑ to $\overline{\text{PTRDY}}$↓	2	11	ns
11	$t_{d(PDEVSEL)}$	Delay time, PCLK↑ to $\overline{\text{PDEVSEL}}$↓	2	11	ns

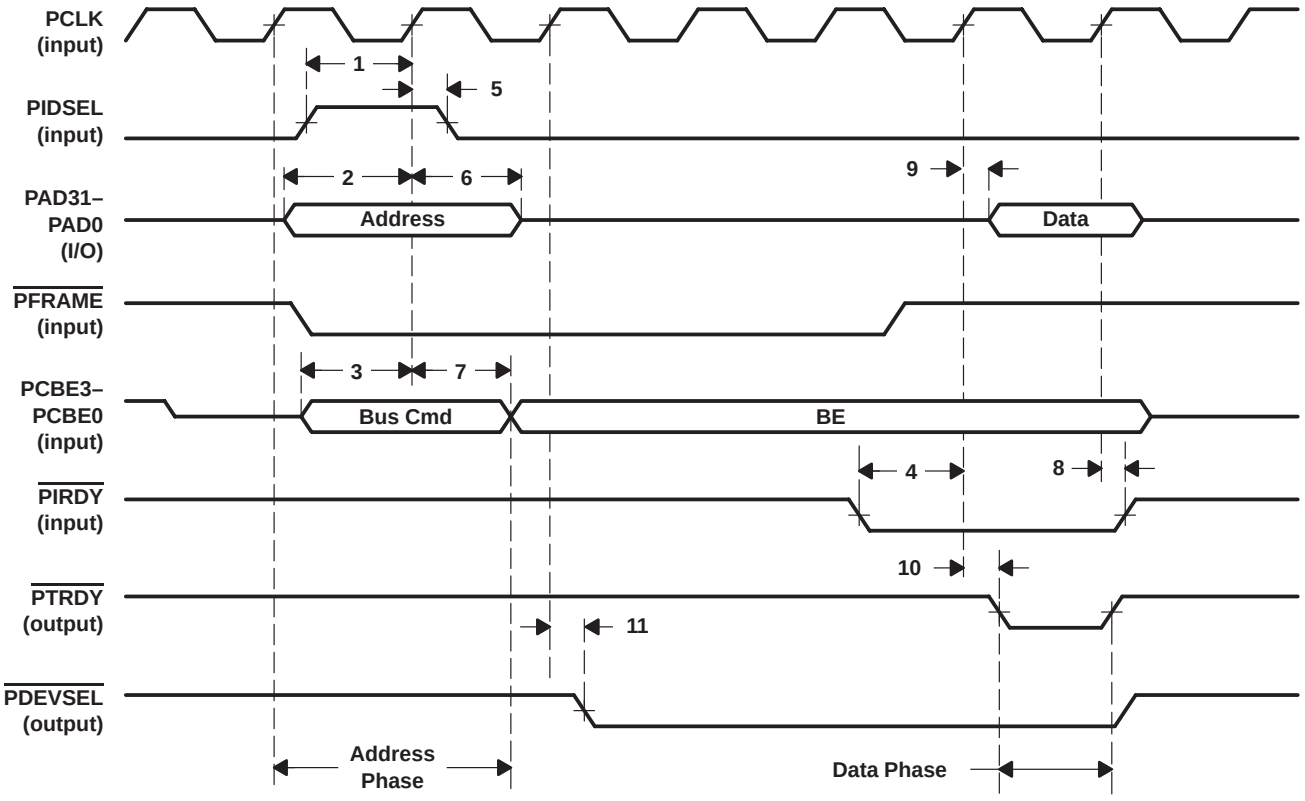


Figure 7. Read Operation (PCI SAR as Slave)

timing requirements (see Figure 8)
PCI-bus interface

NO.			MIN	MAX	UNIT
1	$t_{su(PIDSEL)}$	Setup time, PIDSEL high before PCLK↑	7		ns
2	$t_{su(PAD)}$	Setup time, PAD31–PAD0 valid before PCLK↑	7		ns
3	$t_{su(PFRAME)}$	Setup time, $\overline{\text{PFRAME}}$ low before PCLK↑	7		ns
4	$t_{su(PIRDY)}$	Setup time, $\overline{\text{PIRDY}}$ low before $\overline{\text{PCLK}}$↑	7		ns
5†	$t_{h(PIDSEL)}$	Hold time, PIDSEL high after PCLK↑	1		ns
6†	$t_{h(PIRDY)}$	Hold time, $\overline{\text{PIRDY}}$ low after PCLK↑	1		ns

† This 1-ns minimum hold time deviates from the 0-ns minimum hold time specified in PCI-Local Bus Specification (Revision 2.1).

operating characteristics (see Figure 8)
PCI-bus interface

NO.	PARAMETER		MIN	MAX	UNIT
7	$t_{d(PTRDY)}$	Delay time, PCLK↑ to $\overline{\text{PTRDY}}$↓	2	11	ns

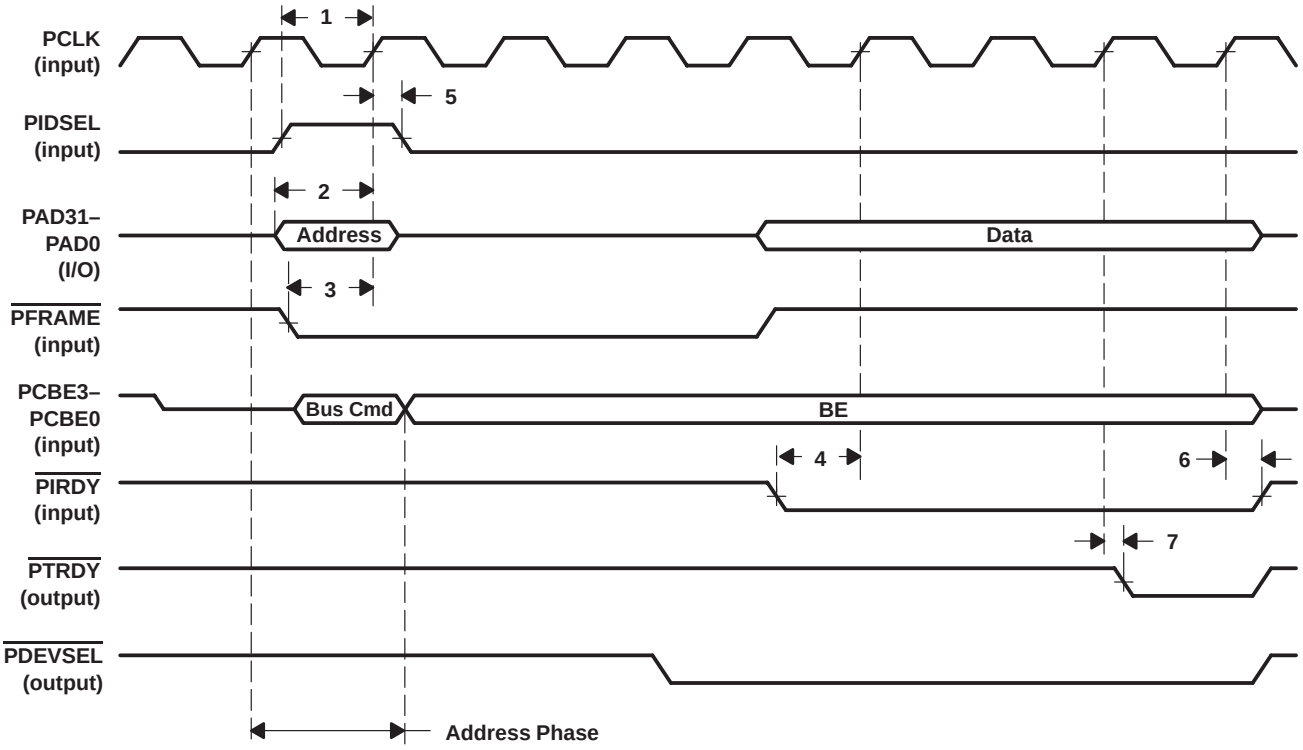


Figure 8. Write Operation (PCI SAR as Slave)

operating characteristics (see Figure 9)
PCI sideband

NO.	PARAMETER		MIN	MAX	UNIT
1	$t_{d(PAD)}$	Delay time, PCLK high to PAD31–PAD0 valid	2	11	ns
2	$t_{d(PSB)}$	Delay time, PCLK high to PSB1–PSB0 valid	2	11	ns

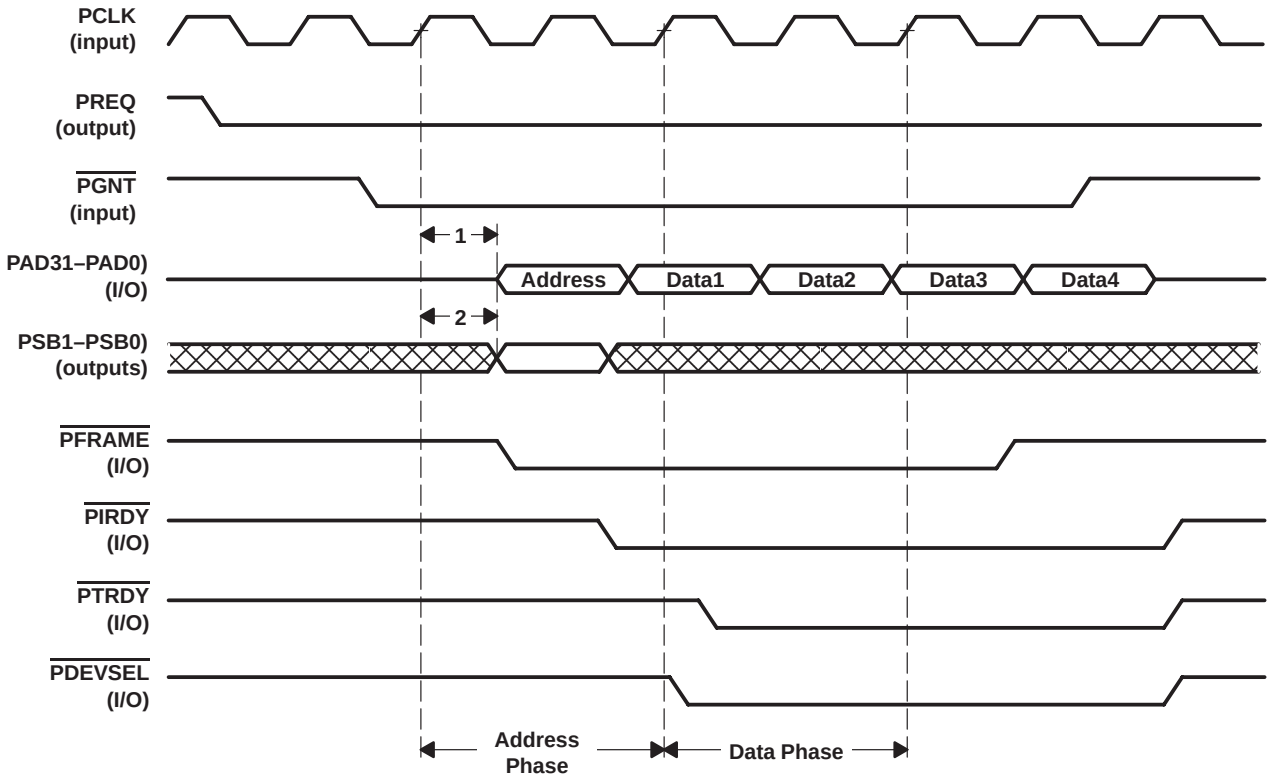


Figure 9. Master Write Operation and PCI-Sideband (PSB1–PSB0 Signals) Timing

timing requirements (see Figure 10)
PCI sideband

NO.			MIN	MAX	UNIT
1	$t_{d(PAD)}$	Delay time, PCLK high to PAD31–PAD0 valid	2	11	ns
2	$t_{su(PSB2)}$	Setup time, PSB2 high before PCLK↑	7		ns
2	$t_{su(PSB4)}$	Setup time, PSB4 high before PCLK↑	7		ns
2	$t_{su(PSB6)}$	Setup time, PSB6 high before PCLK↑	7		ns
3†	$t_{h(PSB2)}$	Hold time, PSB2 high after PCLK↑	1		ns
3†	$t_{h(PSB4)}$	Hold time, PSB4 high after PCLK↑	1		ns
3†	$t_{h(PSB6)}$	Hold time, PSB6 high after PCLK↑	1		ns

† This 1-ns minimum hold time deviates from the 0-ns minimum hold time specified in PCI-Local Bus Specification (Revision 2.1).

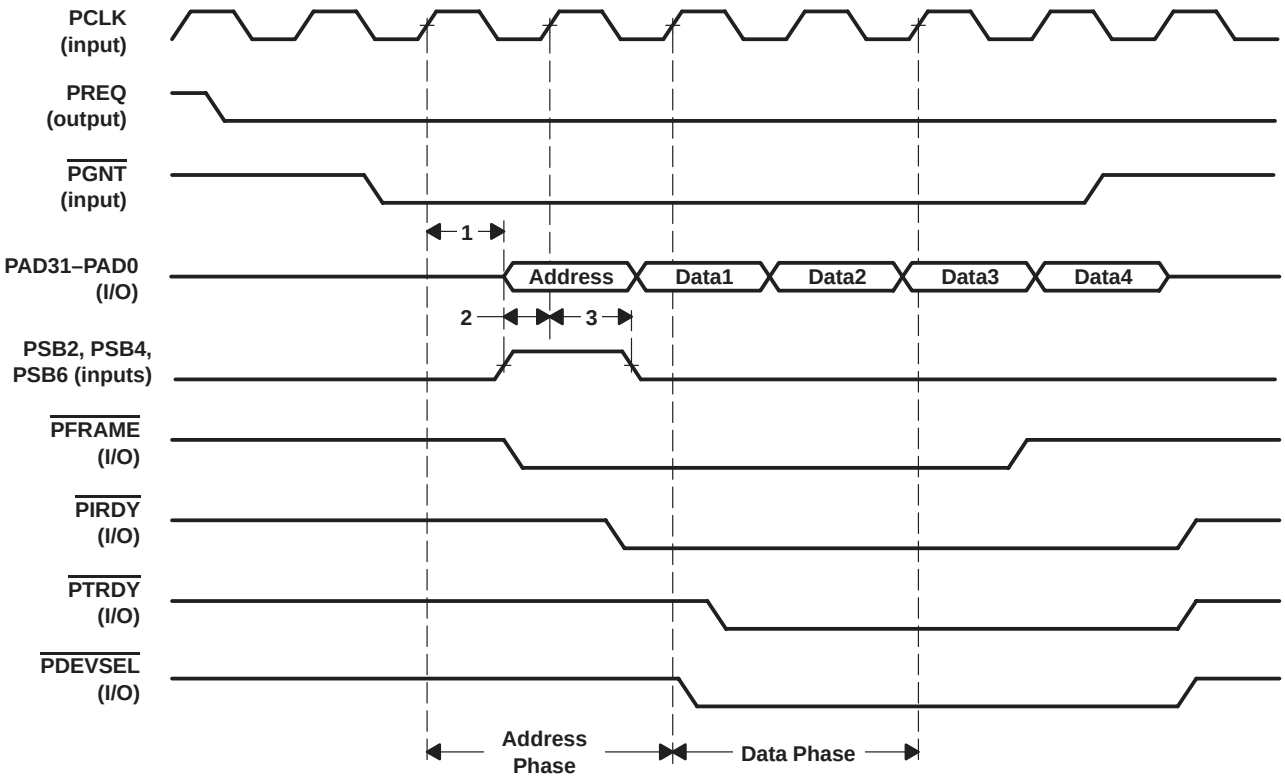


Figure 10. Master Write Operation and PCI Sideband (PSB2, PSB4,and PSB6 Signals) Timing

operating characteristics (see Figure 11)
PCI bus (TXQUERDY)

NO.	PARAMETER		MIN	MAX	UNIT
1	$t_{d(TXQUERDY)}$	Delay time, PCLK high to TXQUERDY inactive		15	ns

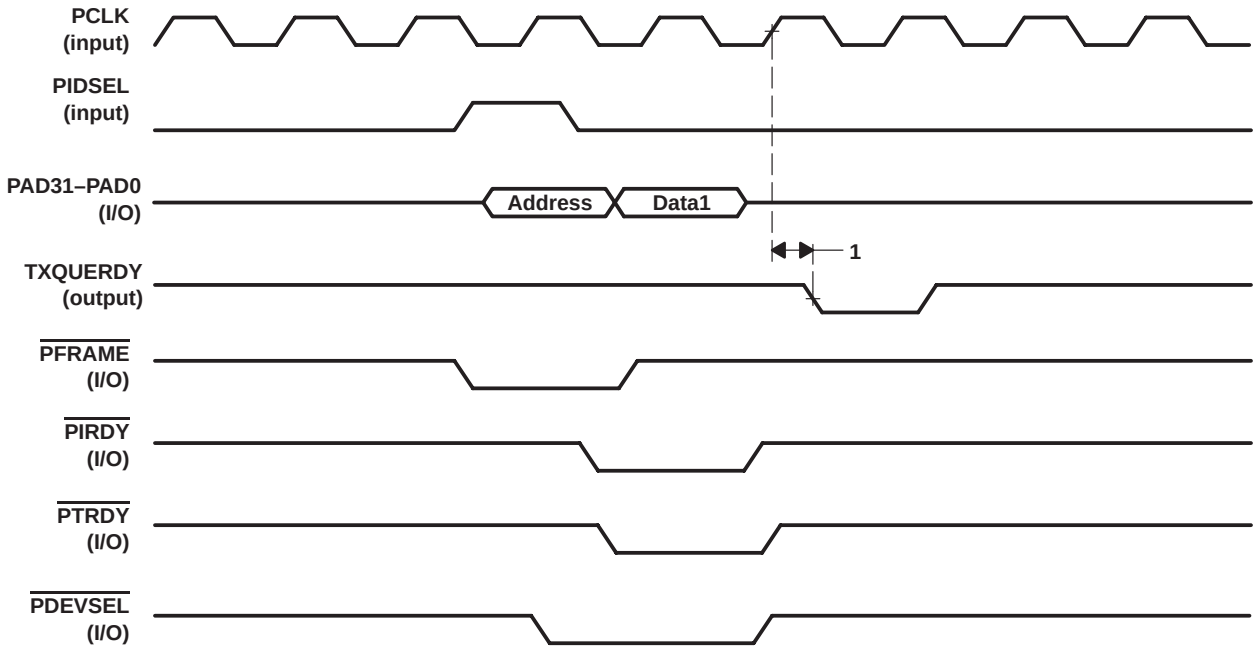


Figure 11. Write Operation to the TXQUERDY Register and Timing (TXQUERDY Going Inactive)

operating characteristics (see Figure 12)
control-memory interface – write operation

NO.	PARAMETER		MIN	MAX	UNIT
1	$t_{d(CMAD)}$	Delay time, from PCLK↑ to CMAD15–CMAD0 valid	2	15	ns
2	$t_{d(CMDATA)}$	Delay time, from PCLK↑ to CMDATA31–CMDATA0 valid	5	15	ns
3	$t_{d(CMOE)}$	Delay time, from PCLK↑ to $\overline{\text{CMOE}}$↑	5	15	ns
4	$t_{d(CMWE)1}$	Delay time, from PCLK↓ to $\overline{\text{CMWE}}$↓	5	15	ns
5	$t_{d(CMWE)2}$	Delay time, from PCLK↓ to $\overline{\text{CMWE}}$↑	5	15	ns

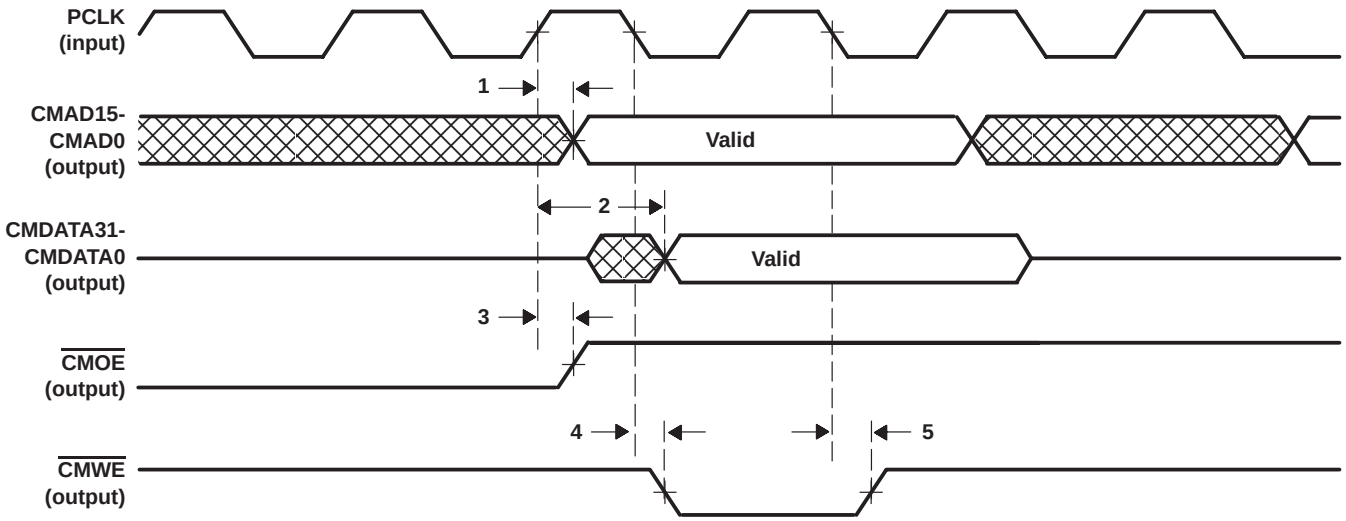


Figure 12. Control-Memory Interface – Write Operation

operating characteristics (see Figure 13)
control-memory interface (write operation)
data bus enable and disable times

NO.	PARAMETER		MIN	MAX	UNIT
1	$t_{en(PH-CE)}$	Enable time, from PCLK↑ to CMDATA31–CMDATA0 enabled	5	10	ns
2	$t_{dis(PH-CZ)}$	Disable time, from PCLK↑ to CMDATA31–CMDATA0 disabled (Z state)	6	11	ns

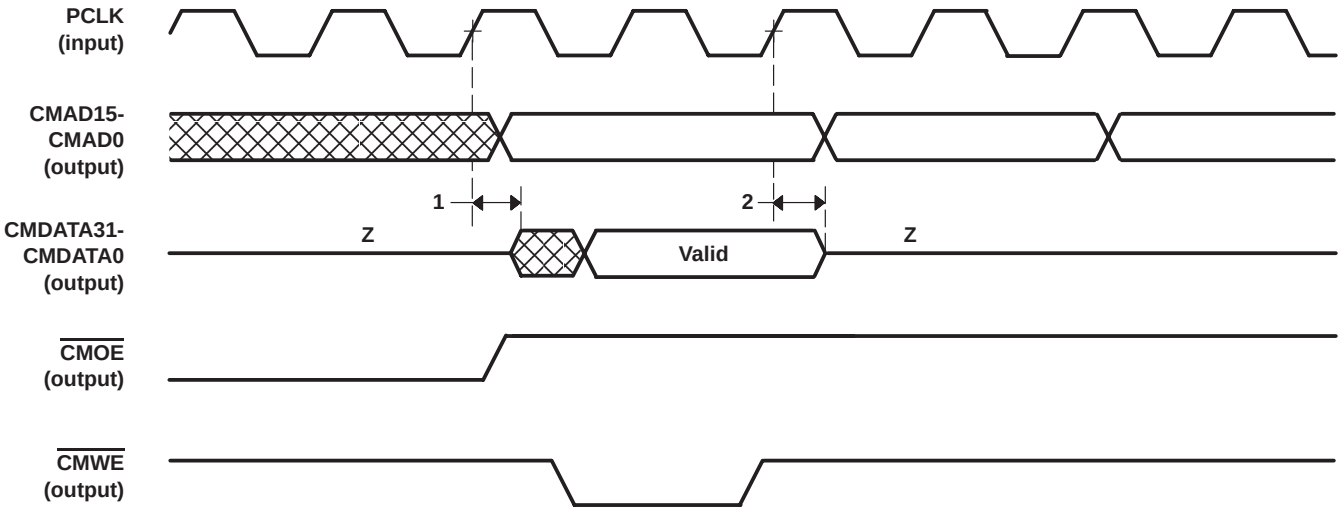


Figure 13. Control-Memory Interface (Write Operation) – Data Bus Enable and Disable Times

timing requirements (see Figure 14)
control-memory interface – read operation

NO.			MIN	MAX	UNIT
1	$t_{su(CMDATA)}$	Setup time, CMDATA31–CMDATA0 valid before PCLK↑	3		ns
2	$t_{h(CMDATA)}$	Hold time, CMDATA31–CMDATA0 valid after PCLK↑	3		ns

operating characteristics (see Figure 14)
control-memory interface read operation

NO.	PARAMETER		MIN	MAX	UNIT
3	$t_{d(CMAD)}$	Delay time, from PCLK↑ to CMAD15–CMAD0 valid	5	15	ns
4	$t_{d(CMOE)}$	Delay time, from PCLK↑ to $\overline{CMOE}$↓	8	15	ns

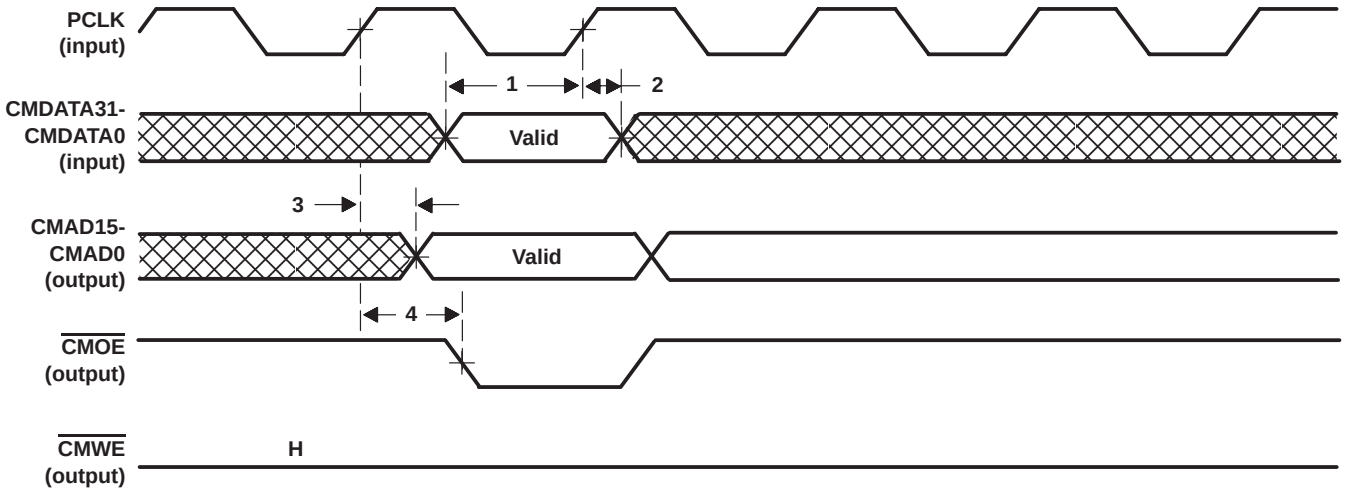


Figure 14. Control-Memory Interface – Read Operation

operating characteristics (see Figure 15)
traffic coprocessor interface outputs

NO.	PARAMETER		MIN	MAX	UNIT
1	$t_{d(RCCX)}$	Delay time, ATMCLK1↑ to RCCX valid	2	11	ns
2	$t_{d(TCCX)}$	Delay time, ATMCLK1↑ to TCCX valid	2	11	ns
3	$t_{d(DAX)}$	Delay time, ATMCLK1↑ to DAX valid	2	11	ns

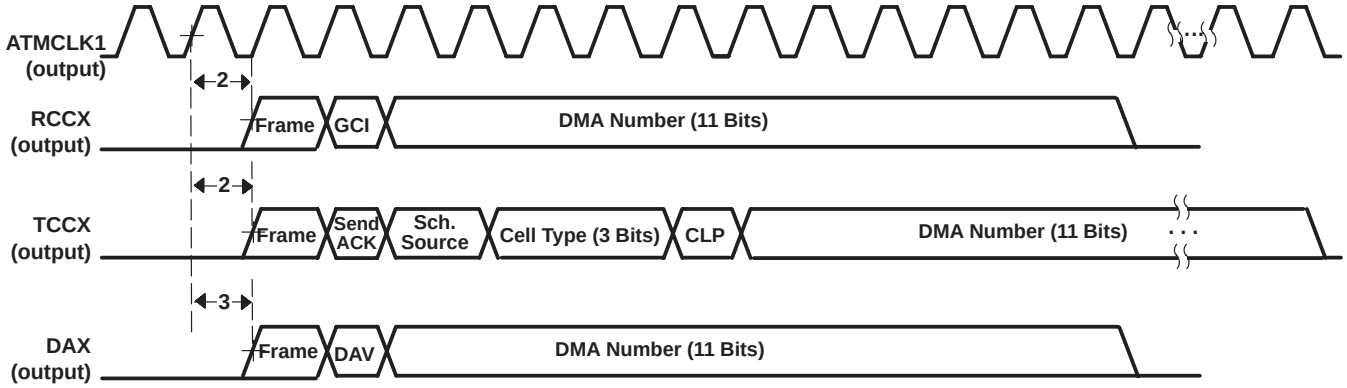


Figure 15. Traffic Coprocessor Interface Outputs

operating characteristics (see Figure 16)
ATMCLK1/ATMCLK2 clock timing

NO.	PARAMETER		MIN	MAX	UNIT
1	$t_{d(ATMCLK1)}$	Delay time, PCLK↑ to ATMCLK1↑	3	7	ns
2	$t_{d(ATMCLK2)}$	Delay time, PCLK↑ to ATMCLK2↑	3	7	ns

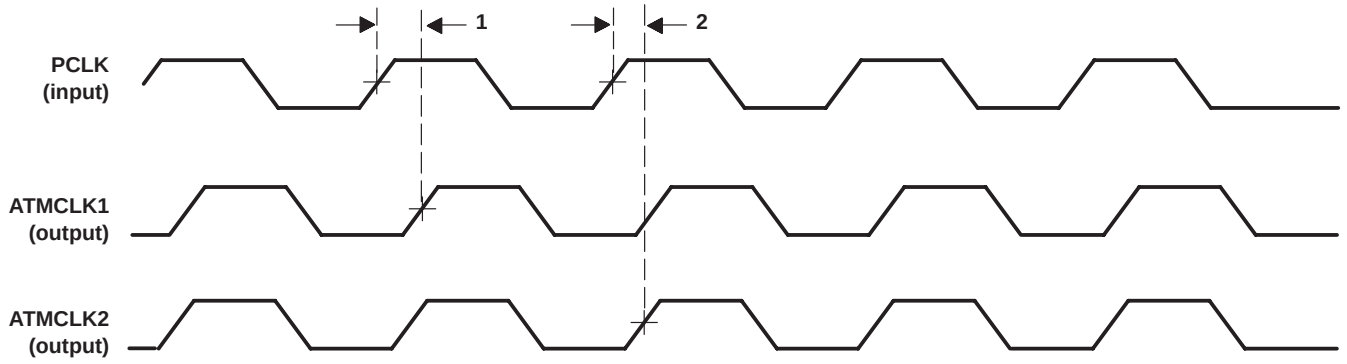


Figure 16. ATMCLK1/ATMCLK2 Clock Timing

timing requirements (see Figure 17)
traffic coprocessor interface inputs

NO.			MIN	MAX	UNIT
1	$t_{su(COPFULL)}$	Setup time, COPFULL high before RESCLK↑	4		ns
2	$t_{h(COPFULL)}$	Hold time, COPFULL high after RESCLK↑	1		ns

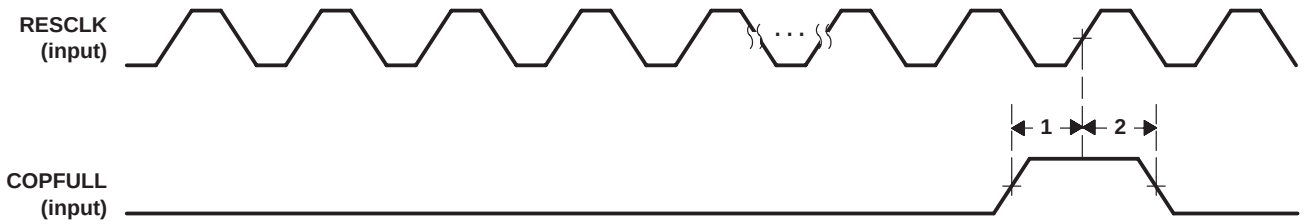


Figure 17. Traffic Coprocessor Interface Inputs

timing requirements (see Note 7 and Figure 18)
UTOPIA interface

NO.			MIN	MAX	UNIT
	$f_{clock(ACLK)}$	Clock frequency, ATMCLK†	0.33 $f_{clock(PCLK)}$	3 $f_{clock(PCLK)}$	MHz
1	$t_{w(SEGCLKH)}$	Pulse duration, SEGCLK high	12		ns
2	$t_{w(SEGCLKL)}$	Pulse duration, SEGCLK low	12		ns
3	$t_{su(SEGEN)}$	Setup time, $\overline{\text{SEGEN}}$ low before SEGCLK↑	10		ns
4	$t_{h(SEGEN)}$	Hold time, $\overline{\text{SEGEN}}$ low after SEGCLK↑	1		ns

† The UTOPIA-clock (ATMCLK) frequency cannot be greater than three times the PCI-clock (PCLK) frequency or less than one-third the PCI-clock (PCLK) frequency because synchronization can break down on the FIFOs and cells can be lost. If this relationship is maintained between the PCLK clock and the ATMCLK clock, the PCLK clock can operate at or below 33 MHz and cells are not lost.

NOTE 7: All output signals are generated on the rising edge of SEGCLK. All inputs are sampled on the rising edge of SEGCLK.

operating characteristics (see Note 7 and Figure 18)
UTOPIA interface

NO.	PARAMETER		MIN	MAX	UNIT
5	$t_{d(SEGCLAV)}$	Delay time, SEGCLK↑ to SEGCLAV↓	1	20	ns
6	$t_{d(SEGSOC)}$	Delay time, SEGCLK↑ to SEGSOC↑	1	20	ns
7	$t_{d(SEGDATA)}$	Delay time, SEGCLK↑ to SEGDATA7–SEGDATA0 valid	1	20	ns
8	$t_{d(SEGPAR)}$	Delay time, SEGCLK↑ to SEGPAR valid	1	20	ns

NOTE 7. All output signals are generated on the rising edge of SEGCLK. All inputs are sampled on the rising edge of SEGCLK.

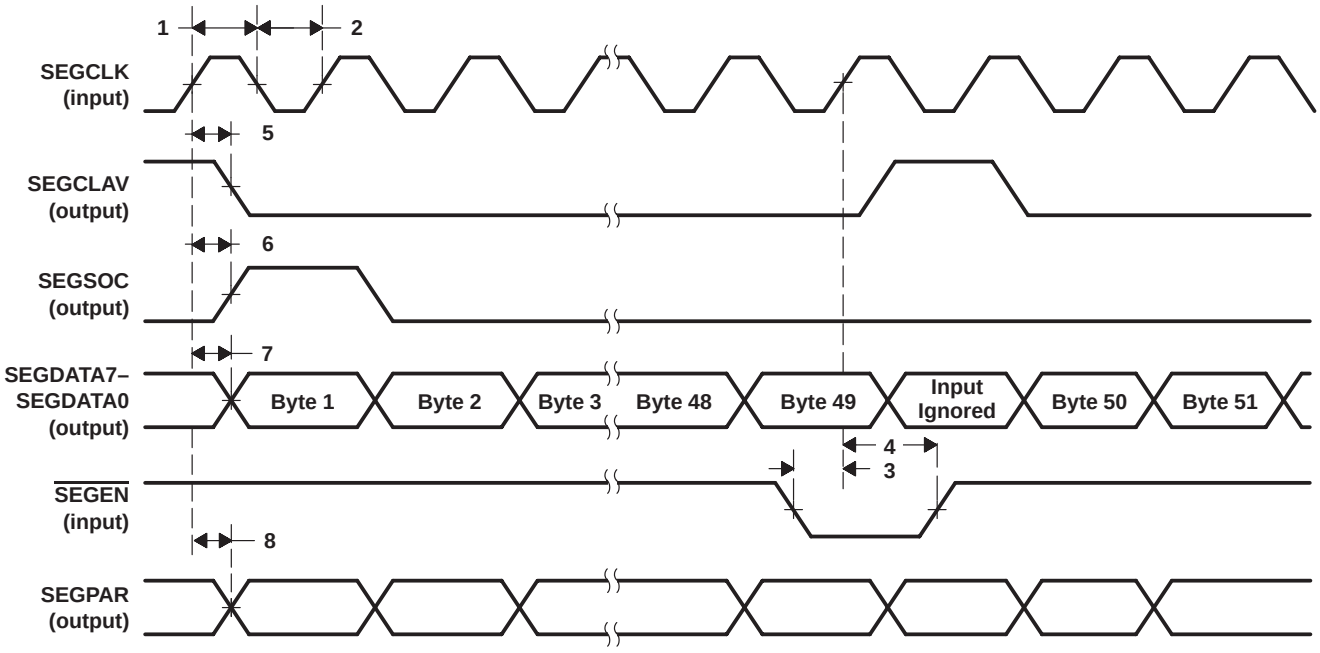


Figure 18. Segmentation-Cell Interface (PHY/$\overline{\text{ATM}}$ Low)

timing requirements (see Note 7 and Figure 19)
UTOPIA interface

NO.			MIN	MAX	UNIT
1	$t_{w(SEGCLKH)}$	Pulse duration, SEGCLK high	12		ns
2	$t_{w(SEGCLKL)}$	Pulse duration, SEGCLK low	12		ns
3	$t_{su(SEGEN)}$	Setup time, $\overline{\text{SEGEN}}$ high before SEGCLK↑	10		ns
4	$t_{h(SEGEN)}$	Hold time, $\overline{\text{SEGEN}}$ high after SEGCLK↑	1		ns

NOTE 7. All output signals are generated on the rising edge of SEGCLK. All inputs are sampled on the rising edge of SEGCLK.

operating characteristics (see Note 7 and Figure 19)
UTOPIA interface

NO.	PARAMETER		MIN	MAX	UNIT
5	$t_{d(SEGSOC)}$	Delay time, SEGCLK↑ to SEGSOC↑	1	20	ns
6	$t_{d(SEGDATA)}$	Delay time, SEGCLK↑ to SEGDATA7–SEGDATA0 valid	1	20	ns
7	$t_{d(SEGPAR)}$	Delay time, SEGCLK↑ to SEGPAR↑	1	20	ns
8	$t_{d(SEGCLAV)1}$	Delay time, SEGCLK↑ to SEGCLAV↑	1	20	ns
9	$t_{d(SEGCLAV)2}$	Delay time, SEGCLK↑ to SEGCLAV↓	1	20	ns

NOTE 7. All output signals are generated on the rising edge of SEGCLK. All inputs are sampled on the rising edge of SEGCLK.

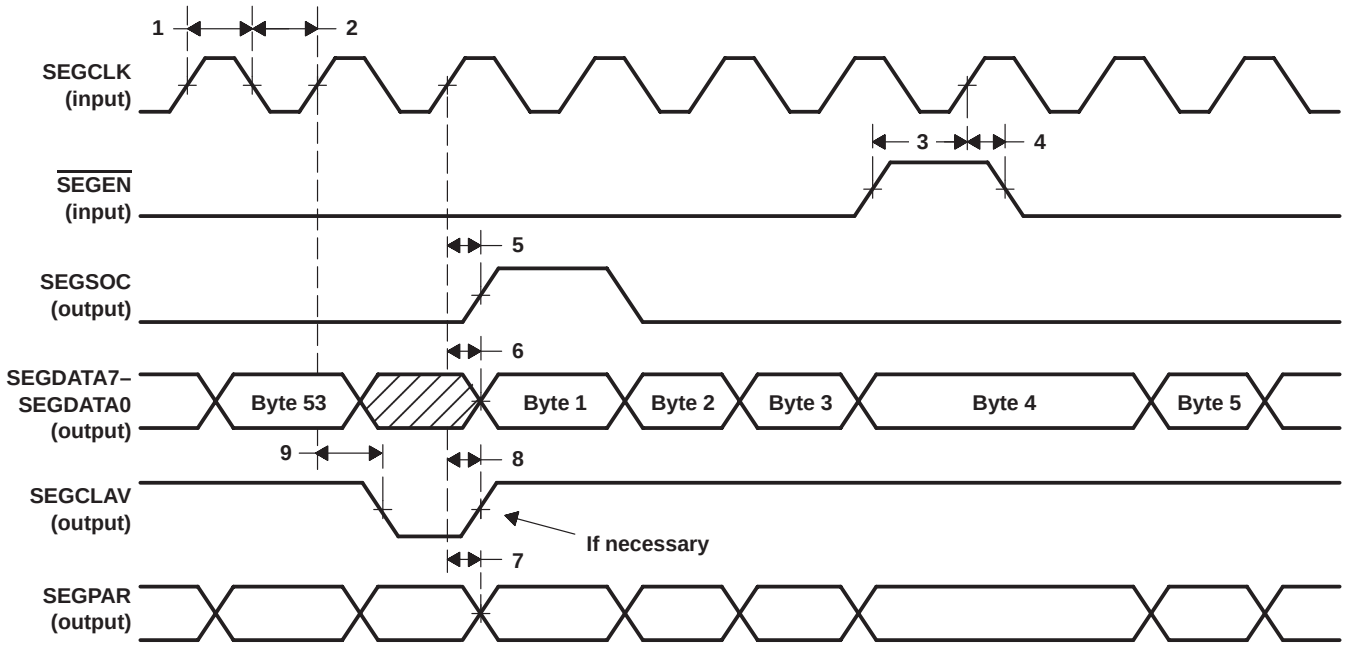


Figure 19. Segmentation-Cell Interface (PHY/$\overline{\text{ATM}}$ High)

timing requirements (see Note 8 and Figure 20)
UTOPIA interface

NO.			MIN	MAX	UNIT
1	$t_{w(RESCLKH)}$	Pulse duration, RESCLK high	12		ns
2	$t_{w(RESCLKL)}$	Pulse duration, RESCLK low	12		ns
3	$t_{su(RESSOC)}$	Setup time, RESSOC high before RESCLK↑	10		ns
4	$t_{su(RESEN)}$	Setup time, $\overline{\text{RESEN}}$ low before RESCLK↑	10		ns
5	$t_{su(RESDATA)}$	Setup time, RESDATA7–RESDATA0 valid before RESCLK↑	10		ns
6	$t_{su(RESPAR)}$	Setup time, RESPAR valid before RESCLK↑	10		ns
7	$t_{h(RESSOC)}$	Hold time, RESSOC high after RESCLK↑	1		ns
8	$t_{h(RESEN)}$	Hold time, $\overline{\text{RESEN}}$ low after RESCLK↑	1		ns

NOTE 8: All output signals are generated on the rising edge of RESCLK.

operating characteristics (see Note 8 and Figure 20)
UTOPIA interface

NO.	PARAMETER		MIN	MAX	UNIT
9	$t_{d(RESCLAV)}$	Delay time, RESCLK ↑ to RESCLAV↑	1	20	ns
10	$t_{d(RESPERR)1}$	Delay time, RESCLK ↑ to $\overline{\text{RESPERR}}$↓	1	20	ns
11	$t_{d(RESPERR)2}$	Delay time, RESCLK ↑ to $\overline{\text{RESPERR}}$↑	1	20	ns

NOTE 8. All output signals are generated on the rising edge of RESCLK.

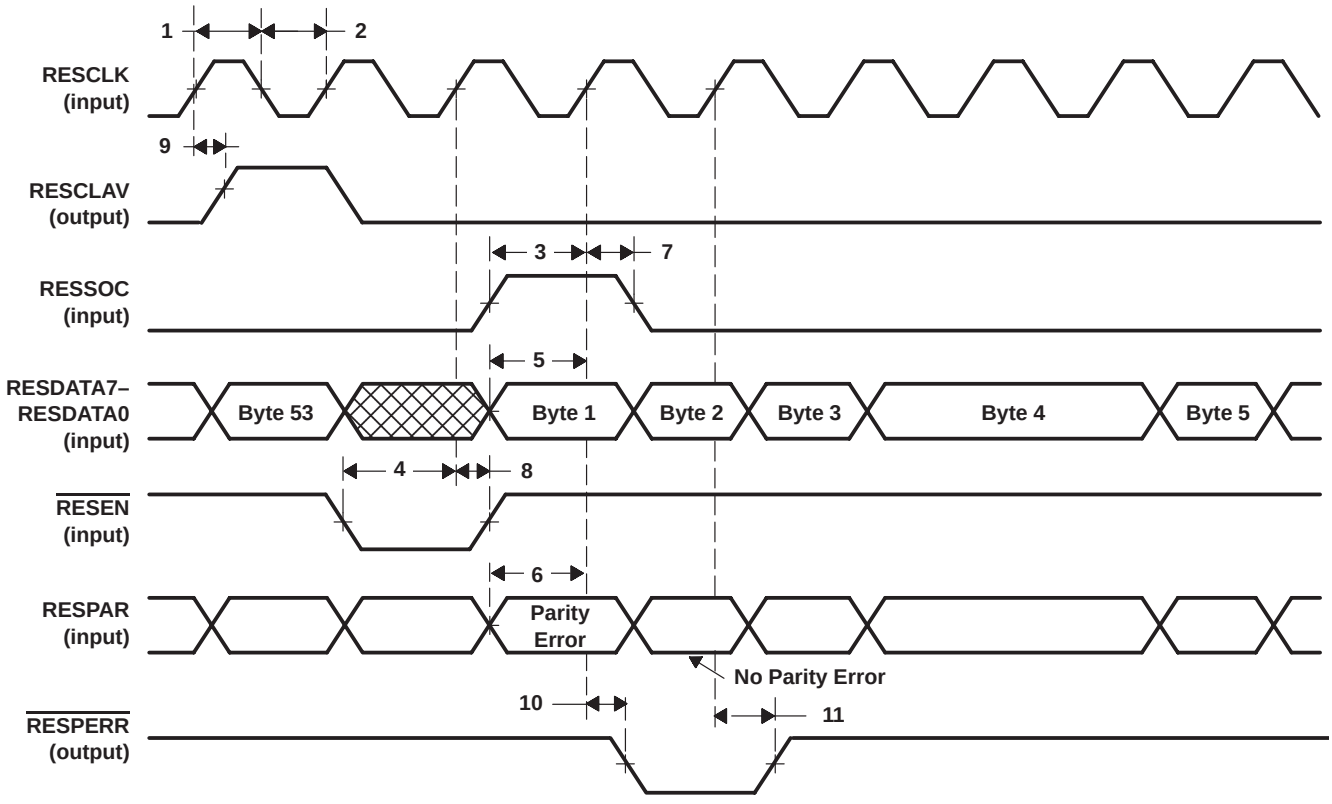


Figure 20. Reassembly-Cell Interface – PHY/$\overline{\text{ATM}}$ Low

timing requirements (see Note 9 and Figure 21)
UTOPIA interface

NO.			MIN	MAX	UNIT
1	$t_{w(RESCLKH)}$	Pulse duration, RESCLK high	12		ns
2	$t_{w(RESCLKL)}$	Pulse duration, RESCLK low	12		ns
3	$t_{su(RESEN)}$	Setup time, $\overline{\text{RESEN}}$ high before RESCLK↑	10		ns
4	$t_{su(RESSOC)}$	Setup time, RESSOC high before RESCLK↑	10		ns
5	$t_{su(RESDATA)}$	Setup time, RESDATA7–RESDATA0 valid before RESCLK↑	10		ns
6	$t_{su(RESPAR)}$	Setup time, RESPAR valid before RESCLK↑	10		ns
7	$t_{h(RESEN)}$	Hold time, $\overline{\text{RESEN}}$ high after RESCLK↑	1		ns
8	$t_{h(RESSOC)}$	Hold time, RESSOC high after RESCLK↑	1		ns
9	$t_{h(RESDATA)}$	Hold time, RESDATA7–RESDATA0 valid after RESCLK↑	1		ns
10	$t_{h(RESPAR)}$	Hold time, RESPAR valid after RESCLK↑	1		ns

NOTE 9: All output signals are generated on the rising edge of RESCLK. All input signals are sampled on the rising edge of RESCLK.

operating characteristics (see Note 9 and Figure 21)
UTOPIA interface

NO.	PARAMETER		MIN	MAX	UNIT
11	$t_{d(RESCLAV)}$	Delay time, RESCLK↑ to RESCLAV↓	1	20	ns
12	$t_{d(RESPERR)1}$	Delay time, RESCLK↑ to $\overline{\text{RESPERR}}$↓	1	20	ns
13	$t_{d(RESPERR)2}$	Delay time, RESCLK↑ to $\overline{\text{RESPERR}}$↑	1	20	ns

NOTE 9. All output signals are generated on the rising edge of RESCLK. All input signals are sampled on the rising edge of RESCLK.

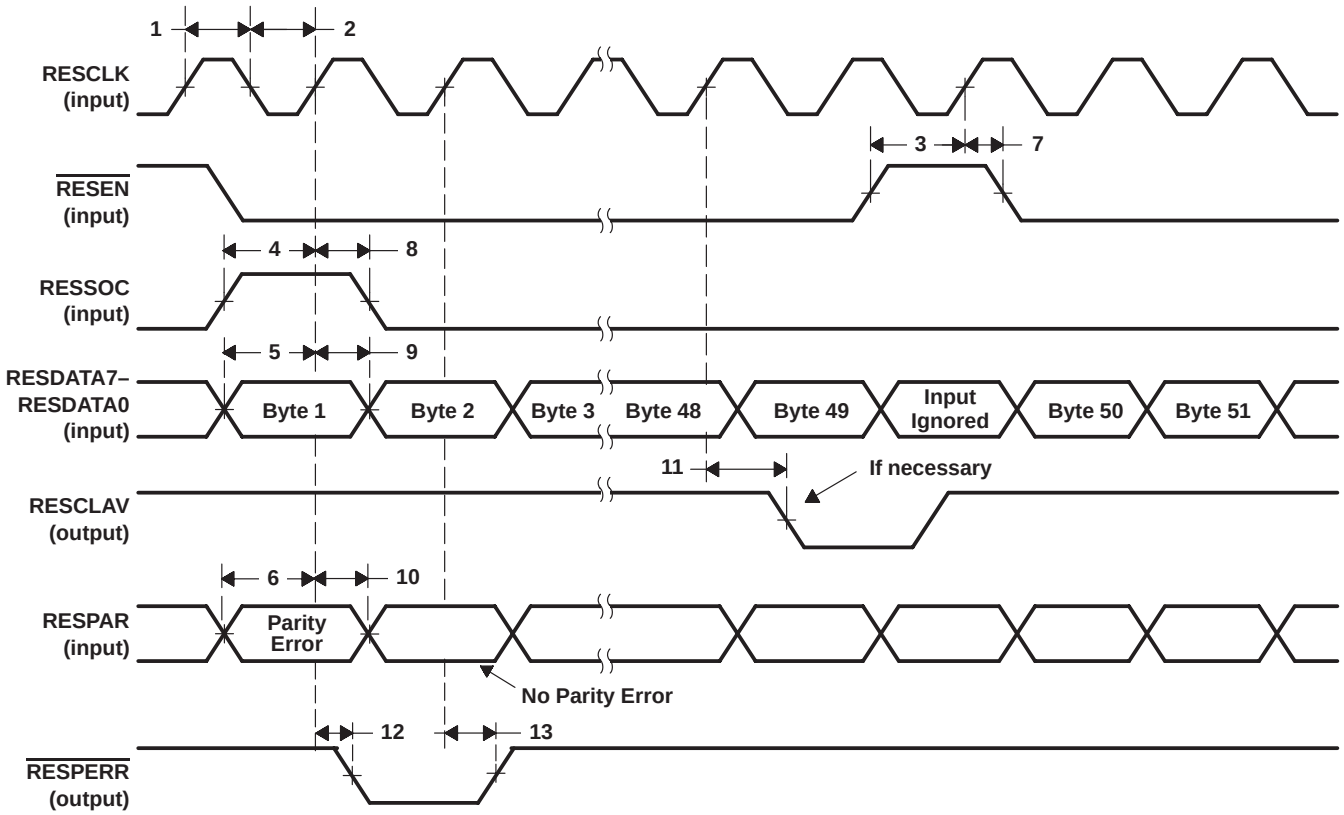


Figure 21. Reassembly-Cell Interface – PHY/$\overline{\text{ATM}}$ High

operating characteristics (see Note 10 and Figure 22)
local-bus interface – read operation

NO.	PARAMETER		MIN	MAX	UNIT
1	$t_{d(LBCS1)1}$	Delay time, LBR/$\overline{W}\uparrow$ to $\overline{LBCS1}\downarrow$	57	67	ns
2	$t_{d(LBREADY)}$	Delay time, $\overline{LBREADY}\downarrow$ to $\overline{LBCS1}\uparrow$	115	125	ns

NOTE 10: If $\overline{LBREADY}$ does not go low within eight PCI-clock cycles after $\overline{LBCS1}$ goes active low, TNETA1575 latches in the data of the LBDATA7–LBDATA0 bus and terminates the read operation.

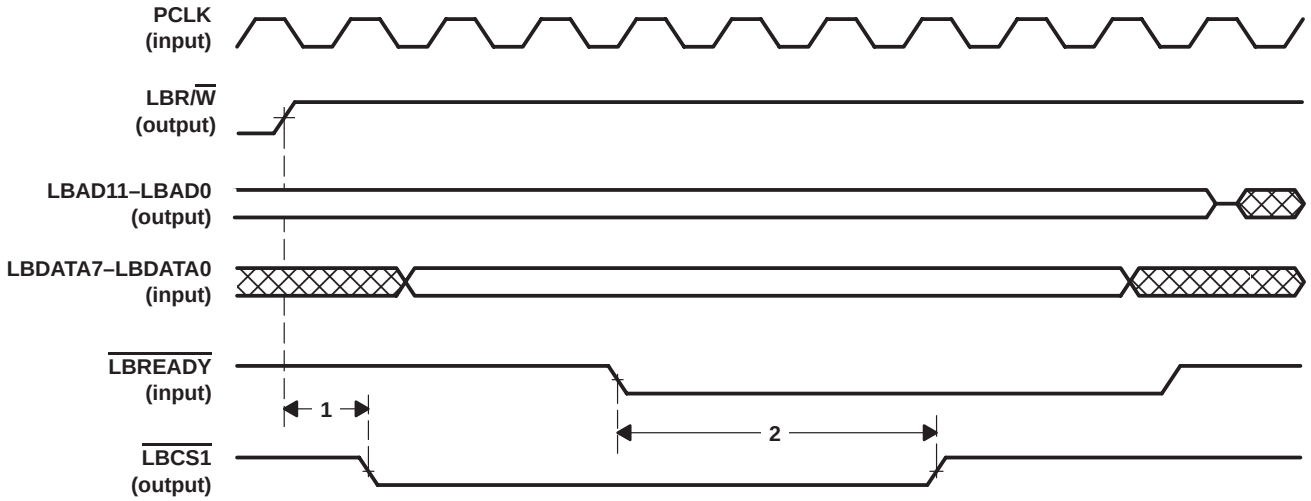


Figure 22. Local-Bus Interface – Read Operation

operating characteristics (see Note 11 and Figure 23)
local-bus interface – write operation

NO.	PARAMETER		MIN	MAX	UNIT
1	$t_{d(LBCS1)1}$	Delay time, LBR/$\overline{W}\downarrow$ to $\overline{LBCS1}\downarrow$	57	67	ns
2	$t_{d(LBCS1)2}$	Delay time, LBAD11–LBAD0 valid to $\overline{LBCS1}\downarrow$	145	155	ns
3	$t_{d(LBCS1)3}$	Delay time, LBDATA7–LBDATA0 valid to $\overline{LBCS1}\downarrow$	57	67	ns
4	$t_{d(LBAD)}$	Delay time, $\overline{LBCS1}\uparrow$ to LBAD11–LBAD0 invalid	265	275	ns

NOTE 11: The $\overline{LBCS1}$ is asserted low for eight PCI-clock cycles during a write operation to allow access to slow devices.

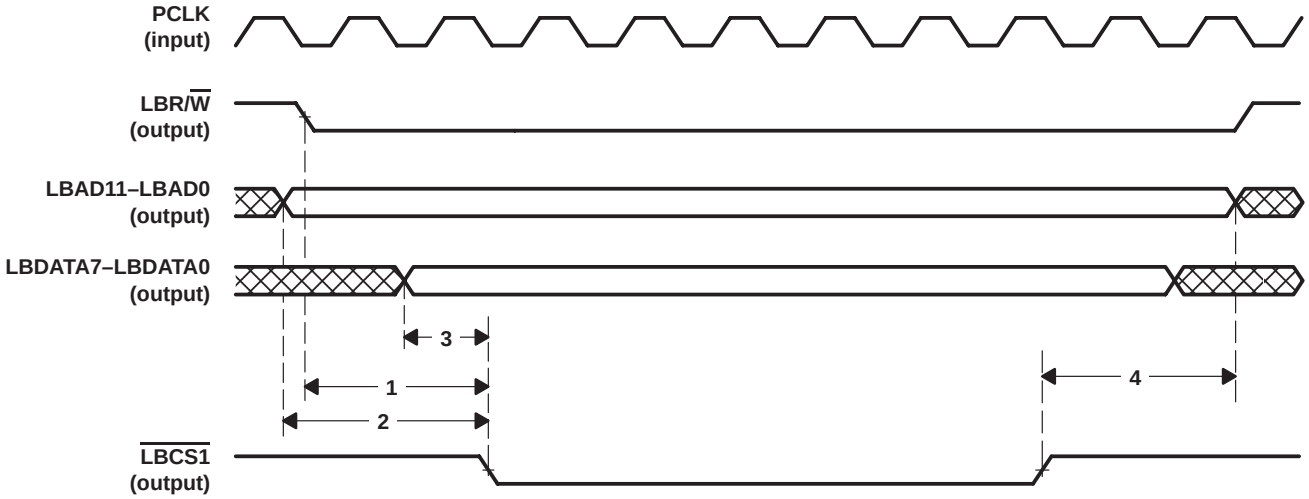


Figure 23. Local-Bus Interface – Write Operation

APPLICATIONS INFORMATION

introduction

The TNETA1575 implements a range of features targeted for cell-operating enterprise hubs. The growth in acceptance of ATM in the backbone transfers quickly to the backplane (the collapsed backbone). The TNETA1575 also is suited for lower-cost applications such as stackable hubs. The growth in acceptance of ATM in the backbone can lead to an increase in demand for ATM connectivity in the installed base of stackable classical-LAN operating products.

To support these applications, a different SAR architecture is required that includes the following characteristics:

- Cell interface that can go beyond 155-Mbit/s transfer rates. This increases the number of front-end legacy interfaces that can be supported by a single SAR device.
- Direct support for constant-bit-rate (CBR) traffic via a dedicated input, a scheduling mechanism and priority-queue scheme make isochronous services available to enterprise hubs and to stackable hubs. The connection parameter cell-delay variation tolerance (CDVT) is not supported by the TNETA1575 scheduler.
- Support for the full range of virtual paths and virtual channels, and 2K-ABR channels that are required to enable the deployment of large and scaleable virtual LANs
- Support for an internal scheduler. The COPI is used to interface to an external scheduler, which would provide support for all the ATM classes of service.
- High-performance features. On the transmit side, these include the transmit-channel sleep mode, which prevents polling of transmit channels with no data queued. On the receive side, these include features that utilize PCI-bus sideband signals to eliminate polling across the PCI bus completely.
- Early segmentation. This is very important to systems that require reduced latency (isochronous hubs). Early segmentation enables multimedia applications to take full advantage of ATM facilities.
- Support for the full range of virtual paths and virtual channels. This is a requirement for the collapsed backbones that are a part of virtual LANs, and the feature offers support for multimedia applications.
- An option to program the UTOPIA-cell interface as either a PHY or ATM-layer system. This option provides the TNETA1575 a capability to function as a PHY where the cell switch is distributed or as an ATM-layer interface for adapter cards or ATM uplinks.

system-level overview

The TNETA1575 and the TNETA1585 provide a flexible, high-performance solution that implements the ATM forum's available-bit-rate (ABR) service category, as specified in the ATM-forum traffic management 4.0 interoperability specification. A summary of these two devices follows:

TNETA1575 HyperSAR-PLUS

The TNETA1575 is a SAR engine based on TI's TNETA1570 architecture. Its primary interfaces are:

- 32-bit PCI for host transfers
- UTOPIA for cell transfers
- COPI for traffic-COP flow-control management
- Control memory for status information
- Local-bus interface for accessing the PHY device via the SAR

APPLICATIONS INFORMATION

system-level overview (continued)

The TNETA1575 has the following internal FIFO capabilities:

- A transmit FIFO for internal interfacing between the segmentation engine and the cell transmit block. The TX FIFO holds four cells.
- A receive FIFO for internal interfacing between the reassembly engine and the cell receive block. The RX FIFO holds 32 cells.

TNETA1585 traffic coprocessor†

The TNETA1585 is an ABR scheduler that conforms to the ATM-forum's interoperability specifications. Other than scheduling cells, the primary function is to handle the processing of resource management (RM) cells in both the transmit and receive directions.

A system-level interconnect of the chip set, with associated systems, is shown in Figure 24.

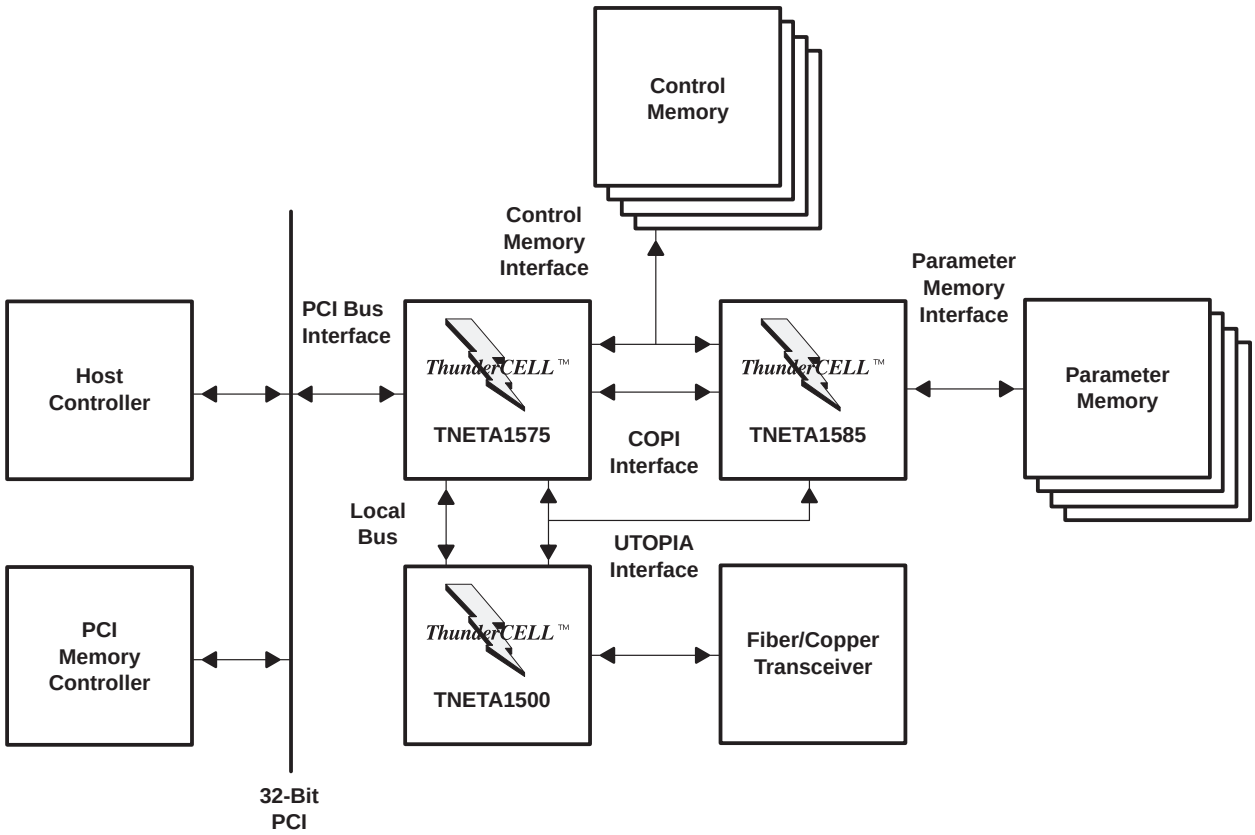
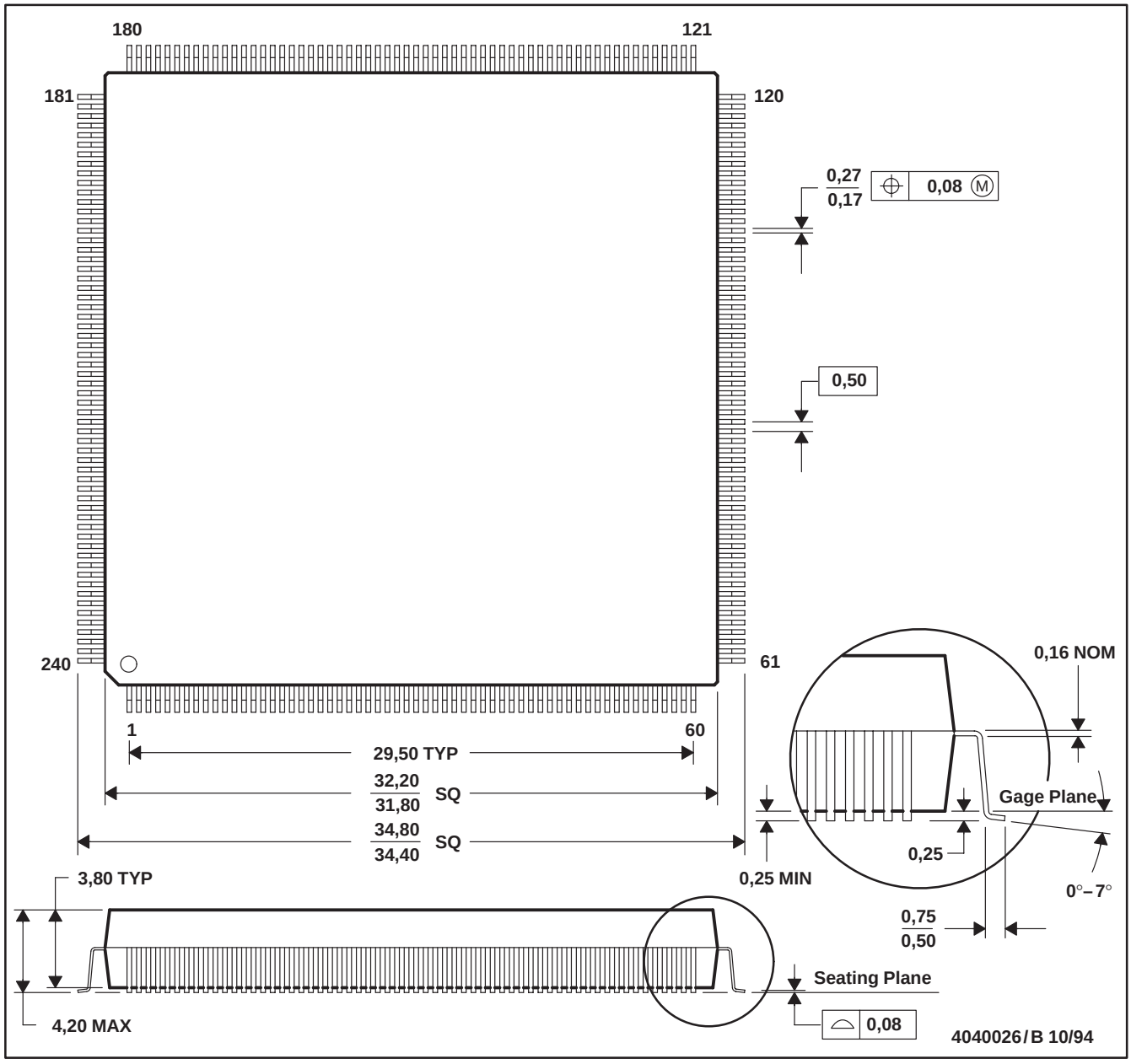


Figure 24. System-Level Chip Set (TNETA1575, TNETA1585, and TNETA1500)

† Vendors can develop their own second-tier schedulers, which conform to the coprocessor interface as defined in this data sheet, in advance of the availability of the TNETA1585 device.

MECHANICAL DATA

PGC (S-PQFP-G240) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

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