Product Brief
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Lucent Technologies
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Asynchronous Transfer Mode (ATM) Interconnect T8206

Features

- Seamlessly extends *WildWire*™ central site family to the backplane
- Compatible with *Transwitch*[1] *CellBus*[2]
- UTOPIA cell-level handshake interface (ATM or PHY layers)
- Multi-PHY (MPHY) operation
- Programmable ATM layer supports up to 16 PHY ports
- Programmable number of UTOPIA output queues with four levels of priority
- Egress SDRAM buffer support to extend UTOPIA output priority queues for 32K to 256K cells
  - — Configurable up to four queues per PHY with programmable sizes
  - — Programmable insertion of the explicit forward congestion indication (EFCI) bit
- Support of ATM traffic management via early packet discard (EPD), forward explicit congestion notification (FECN), and the cell loss priority (CLP) bit
- Controlled slew rate GTL+ I/O
  - — Programmable as bus arbiter
  - — >1 Gbit cell bus operation
- Flexible per virtual channel (VC) cell counters
- Cell header insertion with virtual path identifier (VPI) and virtual channel identifier (VCI) translation via external SRAM (up to 64K entries)
- Support of network node interface (NNI) and user network interface (UNI) header types with optional generic flow control (GFC) insertion
- Programmable operations and maintenance and resource management (OAM/RM) cell routing
- Support of multicast and broadcast addresses per PHY
- Optional monitoring of misrouted cells
- Microprocessor interface, supporting both *Motorola*[3] and *Intel*[4] modes (multiplexed and non-multiplexed)
- Control cell transmission and reception through microprocessor port
- 3.3 V power supply
- 3.3 V TTL I/O (5 V tolerant)
- 272-pin BGA package

Applications

- Asymmetric digital subscriber line (ADSL) digital subscriber line access multiplexer (DSLAMs)
- Access gateways
- Access multiplexers/concentrators
- Multi-service platforms

Description

The T8206 device meets the ATM Forum's universal test and operations PHY interface for ATM (UTOPIA) Level 1, version 2.01 and Level 2, version 1.0 specifications for cell-level handshake and MPHY data path operation. The T8206 supports MPHY operation with one transmit cell available (TxCLAV) signal and one receive cell available (RxCLAV) signal for up to 16 PHY ports. In addition to the required UTOPIA signals, the optional transmit parity (TxPRTY) and receive parity (RxPRTY) signals are provided.

1. *Transwitch* is a registered trademark of Transwitch Corp.
2. *CellBus* is a registered trademark of Transwitch Corp.
3. *Motorola* is a registered trademark of Motorola, Inc.
4. *Intel* is a registered trademark of Intel Corporation.

Description (continued)

The T8206 may be configured as an ATM or PHY level device providing cell routing between UTOPIA and a 32-bit wide GTL+ bus. In addition to the 32 data signals, the bus has the following signals:

- Read clock
- Write clock
- Frame sync
- Acknowledge
- Multipurpose

ATM cells arriving at the UTOPIA receive interface may get VPI and VCI translation and routing information from a look-up table in external SRAM. An external synchronous dynamic random access memory (SDRAM) is used to extend the buffering for ATM cells destined for the UTOPIA transmit interface. This external SDRAM may be partitioned into four or less independently sized queues per PHY. The four queues may be used to implement QOS using different priorities for each queue.

The T8206 provides a shared UTOPIA mode, which allows two devices on different cell buses to share the same UTOPIA bus in ATM mode. Using a glueless interface between the two T8206s, the chips resolve queue priorities for the PHYs and arbitrate the use of the UTOPIA bus. This shared mode can be used to provide redundancy or increase the system capacity.

In addition, an external microprocessor may send or receive control or loopback cells through the microprocessor interface. The 8-bit microprocessor interface may be configured to be *Motorola* or *Intel* compatible and is used to configure and monitor the device.

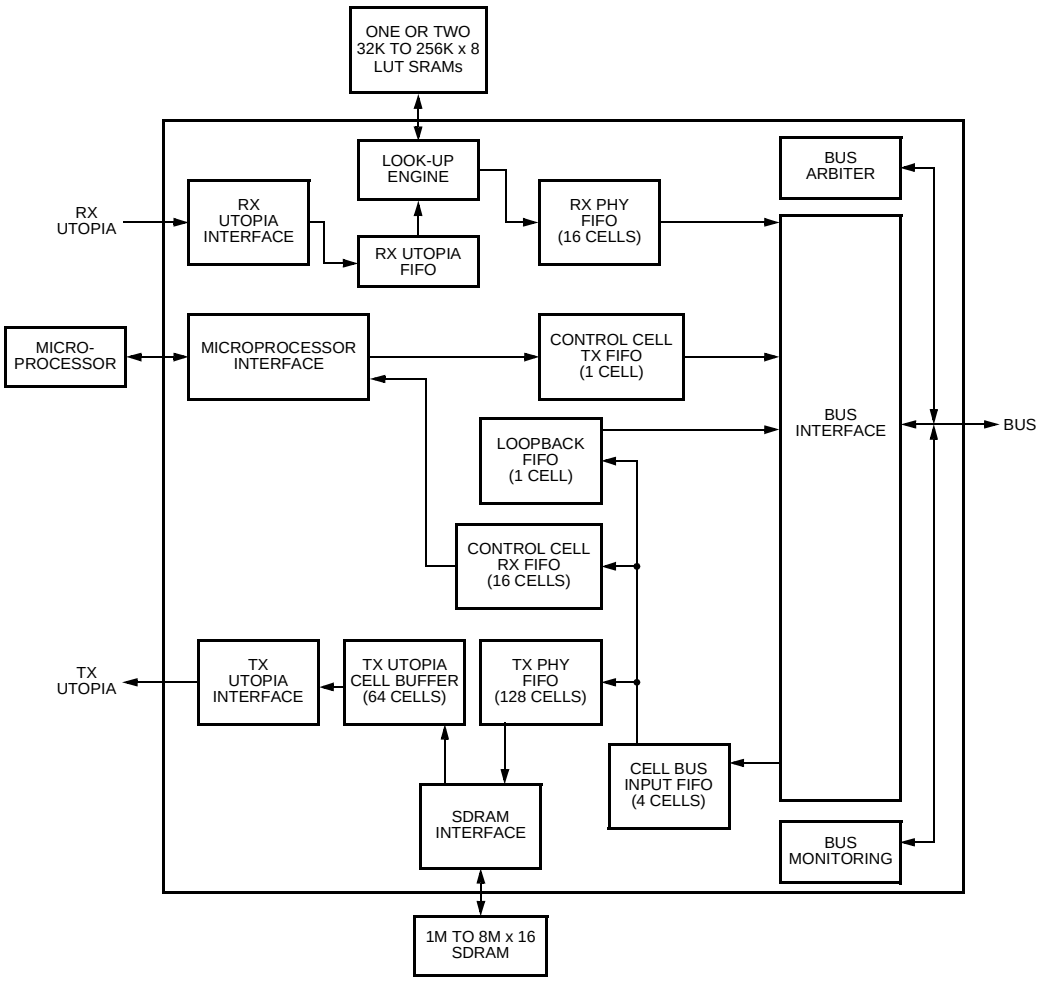

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Figure 1. Functional Block Diagram

Description (continued)

Figure 2 illustrates usage of the T8206 in a system with dual busses. In this configuration, both chips receive cells from the UTOPIA bus and use their respective translation tables to determine if the cell should be placed on the backplane bus. In the egress direction each T8206 receives cells from its cell bus to place on the UTOPIA bus. While a single ATM connection cannot use both cell busses simultaneously, there are no restrictions on a single PHY using both backplane busses for different connections. A two-wire interface between the two chips allows them to resolve priorities of the queues they are each serving. In the event of a bus failure, a single microprocessor write to the T8206 will allow it to “take over” the connections of the other.

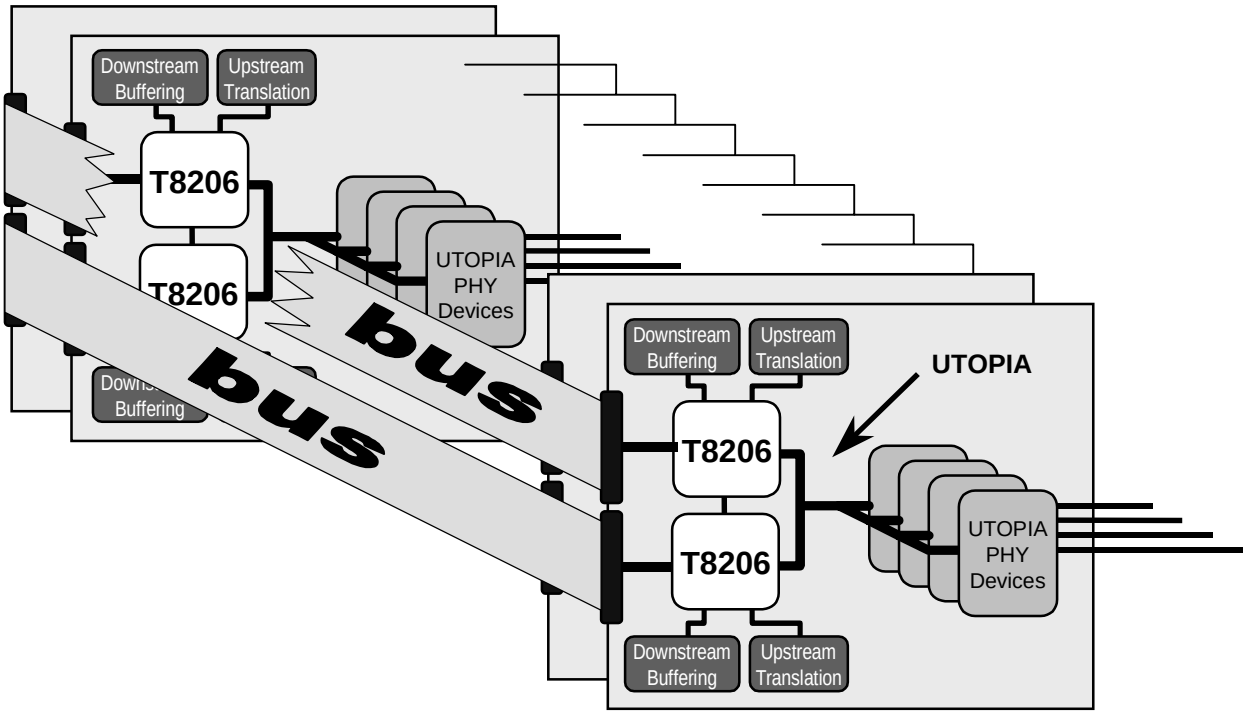

Figure 2. Dual Bus Implementation

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