TOSHIBA

TC222C Standard Cell CMOS ASIC Series

0.3µm 2/3V ASICs

The TC222C series is a low power, high density 0.3µm CMOS Standard Cell ASIC optimized for a 2/2.5V core and 3/3.3V I/O.

Benefits

- 2 to 2.5V core reduces power requirements by over 50% compared to standard 3.3V processes
- Over 2M usable gates make the TC222C the highest density standard cell ASIC series available
- 0.09µW/MHz low power cell for maximum power savings
- High level cores for System IC implementation
- 3 ranges of macrocells for speed/power optimization
- Technology libraries compatible with TC200 series ASIC family for ease of migration
- New accurate delay modeling ensuring system predictability
- Commercial EDA sign-off for flexibility
- Advanced 62µm TAB inner lead bonding provides double the I/O pads available on a die
- A wide range of packaging options available including BGA, TAB-BGA, heatspreader plastic, QFP, TAB-QFP and others to suit all applications

Applications

The TC222C series has been targeted at markets where density is critical, and for 3 volt designs using a 2 volt core for power savings. Applications include handheld and portable systems and consumer electronics which require extended battery life and reduced chip package size.

Note: Series is available only as TC222C Standard Cell.

System IC Application Support

The TC222C series offers the ability to design System ICs with previously unattainable levels of integration. System architectures are not bound by the same physical constraints as before, cache may become just a memory and time to market gets ever smaller.

With over 2M gates available there can be a paradigm shift in how designs are done; more than 1M gates is probably beyond the complexity of a mainframe computer design.

TC222C Standard Cell Product Listing (additional Master Slices are available from Toshiba)

Reference	Usable Gates		I/O Pads		
	DLM	TLM	Wirebond Pads	TAB 62µm	TAB 83µm
TC222C10/60	137,000	225,000	160	316	236
TC222C12/62	167,000	273,000	176	348	260
TC222C14/64	200,000	327,000	192	380	284
TC222C16/66	224,000	360,000	208	420	312
TC222C20/70	299,000	481,000	240	484	360
TC222C24/74	385,000	618,000	272	548	408
TC222C32/82	589,000	945,000	336	—	504
TC222C36/86	723,000	1,116,000	384	—	576
TC222C40/90	916,000	1,477,000	432	—	648
TC222C42/92	1,288,000	2,077,000	512	—	768

Note: DLM = Double Layer Metal, TLM = Triple Layer Metal

System level cores include an R3900 MIPS microprocessor, 8/16 bit CISC embedded controller, high density DRAM, MPEG and ATM. These advanced customized solutions are available through partnership designs.

Optimized Macrocell Performance

The TC222C family has three ranges of macrocells for speed/power optimization.

	Cell Type*		
	Low Power	**Normal**	**HIgh Drive**
Delay	163ps	125ps	100ps
Power	0.09μW/MHz	0.13μW/MHz	0.21μW/MHz

* 2-input NAND, fanout = 1 plus typical interconnect load

High Performance I/O

The TC222C series is supported by a range of high performance I/O options including Analog PLL, PCI, high performance GTL, 3V failsafe and low undershoot buffers. 2 volt I/O options will also be available.

Accurate Models

The TC222C series incorporates the new Toshiba highly accurate delay model which includes the following new features:

- Pin-to-Pin Type
- State Dependent Delay
- Table Look Up Delay
- Input Slew
- Non-Linear Equation

Delay model also includes effect of via resistance and interwire capacitance.

Commerical EDA Sign-off

The TC222C series is supported by Toshiba's Open EDA Strategy that is based on sign-off on multiple commercial EDA tools. This leads to the following benefits:

- Sign-off convenience at designer's site
- Shorter design cycle time
- Higher design efficiency
- Highly accurate simulation model
- Faster time-to-market

Initial support will be for Verilog-XL.

EDA Support

EDA support is available for most of the commercial EDA tools. For System IC designs, Toshiba engineering will work with the customer to develop the EDA flow required for a given design.

In addition, Toshiba has a range of DFT support including SCAN, Partial SCAN, BIST and Boundary SCAN.

Technology Resource Centers provide technical support and design expertise

Toshiba ASIC Technology Resource Centers are located throughout the U.S. and provide a high level of technical expertise for support before, during and after the design of a Toshiba ASIC. This includes support issues dealing with EDA environments and design kits, Toshiba design methodologies, Toshiba ASIC technologies and Toshiba ASIC design implementation. Design consultation is also available.

In addition, Toshiba's North America Semiconductor Engineering Development Center in San Jose, CA is staffed with system, technology and EDA design expertise to work with their partners on advanced System IC applications.

Rigorous production quality control and monitoring coupled with a sophisticated batch tracking system enables Toshiba to meet the requirements of fast ramping, high volume markets.

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