UTOPIA Multiplexer

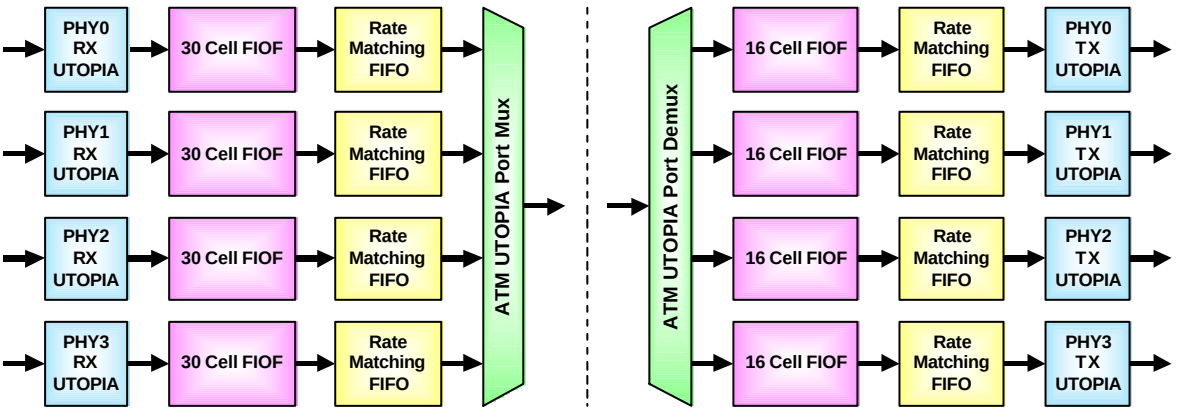
General Description

The TC35885TB UTOPIA Multiplexer is a full-duplex 4:1 ATM cell multiplexer/demultiplexer with built in FIFO buffering per port.
It enables connection of several Physical layer devices (8-bit mode) to a single ATM layer device (16-bit mode) using the ATM-FORUM UTOPIA Level 2 specification. Each port has a built in FIFO capable of storing up to 30 ATM cells in the receive direction and up to 16 cells in the transmit direction. This configuration allows four full duplex ATM cell streams to be multiplexed/de-multiplexed into a data stream of up to 800Mbps. When two 8-bit PHY ports are configured in 16-bit mode, the receive and transmit FIFO port capability can be expanded to 60 cells and 30 cells respectively.
One of the key features of TC35885TB is that it was designed to operate in stand-alone mode, capable of handling Idle/Unassigned/SOC-error condition, and has a self-learning mechanism in order to detect the active UTOPIA ports. The TC35885TB also has a timeout mechanism to detect if a logical UTOPIA port is disabled, thus preventing Head of Line blocking.

Features

•Full-duplex 4:1 ATM cell mux/demuxUp to 200Mbps transfer rate at each PHY layer interface (8-bit / 50MHz)
•Up to 800Mbps transfer rate at the ATM layer interface (16-bit / 50MHz)
•Idle/unassigned cells discarded in PHY-to-ATM interface, forwarded in ATM-to-PHY interface
•Per port buffering on chipSelectable 8/16 bit wide UTOPIA Level 2 ports on PHY side
•16 bit wide UTOPIA Level 2 interface on ATM layer side.
•Independent PHY UTOPIA clocks per port Standalone operation without microprocessor
•Build-in Timeout mechanism to detect when ports have been disabled
•Port wise TX/RX FIFO flush
•Weighted Round Robin algorithm to poll Logical UTOPIA Ports (LUP)
•JTAG port for boundary scan testing
•Advanced low power 0.35-micron CMOS
•Space saving T-BGA 256 package
•3.3V power supply
•+5V tolerant inputs

Block Diagram



ATM to PHY(Receive)

ATM to PHY(Transmit)

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Applications

- ATM switches and concentrators
- Remote Access Concentrator's, DSLAM
- Bridge single to multi-PHY, 8-bit to 16-bit
- Port Fan-out expansion and concentration

Application Examples

The herein described application, a DSLAM Concentrator Board, multiplex 16 ADSL lines with UTOPIA-Level-2 8-bit PHY interface to one UTOPIA-Level-2 16-bit ATM interface. ADSL lines are implemented with TOSHIBA TC35831F ADSL Analog Front-End LSI and TC35830FADSL DMT Modem. Controlling of the ADSL lines is done by a RISC type CPU like TOSHIBA TX39 family. The control and OAM cells are handled by TOSHIBA TC35856CF ATM SAR-Controller. Note that TC35885TB operates without CPU control.