# CUBIT-622™ Device
## Multi-PHY *CellBus*® Access Device
## TXC-05805

**TECHNICAL OVERVIEW**
*PRODUCT PREVIEW*

## FEATURES

- 622 Mbit/s performance (without multicast)
- UTOPIA Level 1/2 interface (8/16-bit) with support for 64 ports at 50 MHz
- Tandem operation for two devices, supporting dual *CellBus* cell switching in load sharing or redundancy
- Inlet-side address translation and routing header insertion, using external SRAM
- Programmable OAM cell routing
- Outlet cell queuing, using external synchronous SRAM (SSRAM) cell buffer
- Ability to insert GFC field in real time
- Ability to insert EFCI indication, under programmable conditions
- Support for spatial multicast for 256 connections
- Support for packet discard in outlet direction
- Support for over-reservation of GFR, UBR, and VBR traffic
- *CellBus* traffic monitor mode
- Cell insertion and extraction via microprocessor interface port
- Master *CellBus* arbiter included in each CUBIT-622
- Internal GTL+ transceivers for *CellBus* connection
- Microprocessor control port, selectable for Intel or Motorola interfaces
- Test Access Port for IEEE 1149.1 boundary scan
- +3.3 V and +2.5 V power supplies
- 376-lead Plastic Ball Grid Array package, 23 mm x 23 mm

## DESCRIPTION

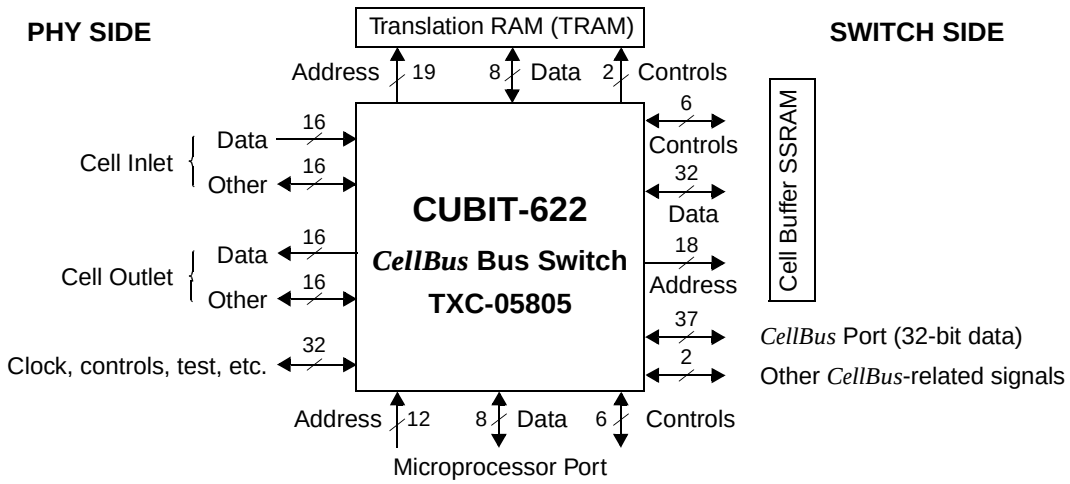
The CUBIT-622 device is an enhanced version of the CUBIT-3 (TXC-05804) device. The two major enhancements include a throughput increase to 622 Mbit/s and a port density increase to 64 ports. The rate decoupling FIFO has been increased from 4 to 32 cells on ingress to accommodate the higher bandwidth interface. Tandem mode has been added to enable two CUBIT-622 devices to share the UTOPIA master function and service different *CellBus* switches.

The CUBIT-622 device is a single-chip solution for implementing low-cost ATM multiplexing and switching systems, based on the *CellBus* architecture. Such systems are built from a number of CUBIT-3 (TXC-05804), CUBIT-*Pro* (TXC-05802B), CUBIT-622 or ASPEN (TXC-05810) devices, all interconnected by a 37-line common bus, the *CellBus*. CUBIT-622 supports unicast and multicast transfers, and has all necessary functions for implementing a switch: cell address translation, cell routing, and outlet cell queuing.

The CUBIT-622 is designed to interface directly with UTOPIA Level 1/2, 8/16-bit compliant devices.

## APPLICATIONS

- xDSL access multiplexer
- Remote access equipment
- Cable modem access multiplexer
- ATM LAN hub
- ATM multiplexer/concentrator
- Small stand-alone ATM switch
- Add-drop ring switch
- Edge switching equipment
- *CellBus* monitor for any of the above applications






Document Number:
*PRODUCT PREVIEW* TXC-05805-MA
Ed. 1, April 2001

*TranSwitch Corporation • 3 Enterprise Drive • Shelton, Connecticut 06484 • USA*
*Tel: 203-929-8810 • Fax: 203-926-9453 • www.transwitch.com*

*PRODUCT PREVIEW*

## TABLE OF CONTENTS



* Please note that TranSwitch provides documentation for all of its products. Current editions of many documents are available from the Products page of the TranSwitch Web site at www.transwitch.com. Customers who are using a TranSwitch Product, or planning to do so, should register with the TranSwitch Marketing Department to receive relevant updated and supplemental documentation as it is issued. They should also contact the Applications Engineering Department to ensure that they are provided with the latest available information about the product, especially before undertaking development of new designs incorporating the product.

## LIST OF FIGURES

## OVERVIEW

The CUBIT-622 device is an enhanced version of the CUBIT-3 (TXC-05804) device. The two major enhancements include a throughput increase to 622 Mbit/s and a port density increase to 64 ports. The rate decoupling FIFOs has been increased from 4 to 32 cells on ingress to accommodate the higher bandwidth interface. Tandem mode has been added to enable two CUBIT-622 devices to share the UTOPIA master function and service different *CellBus* switches.

The CUBIT-622 device is a single-chip solution for implementing low-cost ATM multiplexing and switching systems, based on the *CellBus* architecture. Such systems are built from a number of CUBIT-3, CUBIT-*Pro*, CUBIT-622 or ASPEN (TXC-05810) devices, all interconnected by a 37-line common bus, the *CellBus*. The CUBIT-622 supports unicast and multicast transfers, and has all necessary functions for implementing a switch: cell address translation, cell routing, and outlet cell queuing.

The CUBIT-622 is designed to interface directly with UTOPIA Level 1/2, 8/16-bit compliant devices such as the PHAST-3P (TXC-06203) and PHAST-12E (TXC-06212) at up to 50 MHz. The CUBIT-622 switch side interface is a *CellBus* interface which interfaces directly with *CellBus* devices such as the CUBIT-*Pro* (TXC-05802B), CUBIT-3 (TXC-05804) and ASPEN (TXC-05810).

***PRODUCT PREVIEW***

## FEATURES

The CUBIT-622 device provides the following features:

- 622 Mbit/s performance (without multicast)
- UTOPIA Level 1/2 interface (8/16-bit) with support for 64 ports at 50 MHz
- Tandem operation for two devices, supporting dual *CellBus* cell switching in load sharing or redundancy
- Inlet-side address translation and routing header insertion, using external SRAM
- Programmable OAM cell routing
- Outlet cell queuing, using external synchronous SRAM (SSRAM) cell buffer
- Ability to insert GFC field in real time
- Ability to insert EFCI indication, under programmable conditions
- Support for spatial multicast for 256 connections
- Support for packet discard in outlet direction
- Support for over-reservation of GFR, UBR, and VBR traffic
- *CellBus* traffic monitor mode
- Cell insertion and extraction via microprocessor interface port
- Master *CellBus* arbiter included in each CUBIT-622
- Internal GTL+ transceivers for *CellBus* connection
- Microprocessor control port, selectable for Intel or Motorola interfaces
- Test Access Port for IEEE 1149.1 boundary scan
- +3.3 V and +2.5 V power supplies
- 376-lead Plastic Ball Grid Array package, 23 mm x 23 mm

## APPLICATION EXAMPLE

Figure 1 shows the usage of the CUBIT-622 in a DSLAM with STS-3/STM-1 and STS-12/STM-3 Uplinks.

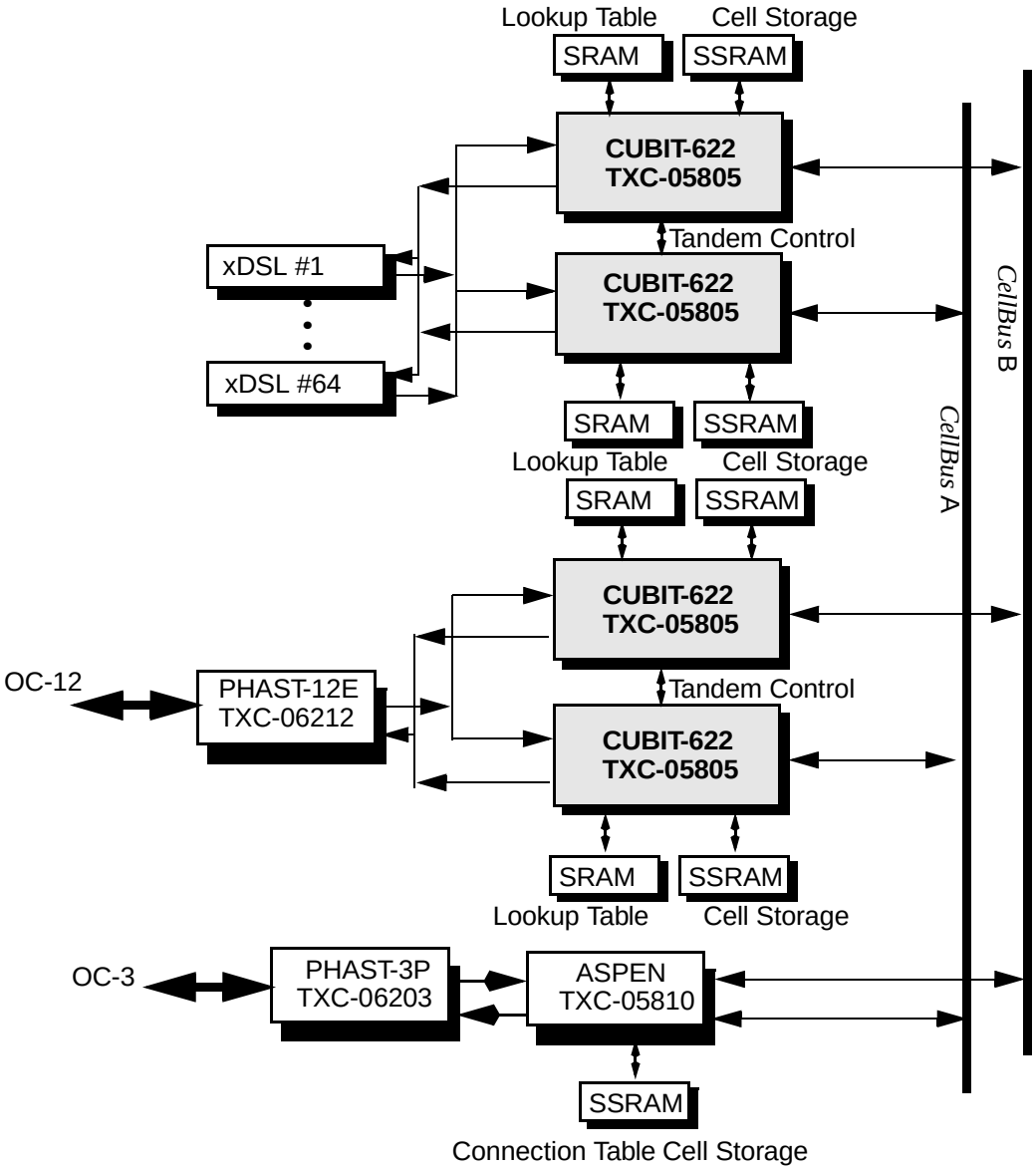



**Figure 1. DSLAM Application with STS-3/STM-1 and STS-12/STM-3 Uplinks**

### INTEROPERABILITY

The CUBIT-622 works directly with the following TranSwitch devices:

- CUBIT-*Pro* (TXC-05802B)
- CUBIT-3 (TXC-05804)
- ASPEN (TXC-05810)
- PHAST-3P (TXC-06203)
- PHAST-12E (TXC-06212)

## FUNCTIONAL DESCRIPTION

A block diagram of the CUBIT-622 device is shown in Figure 2. Further information on device operation and the interfaces to external circuits is provided in the following subsections.

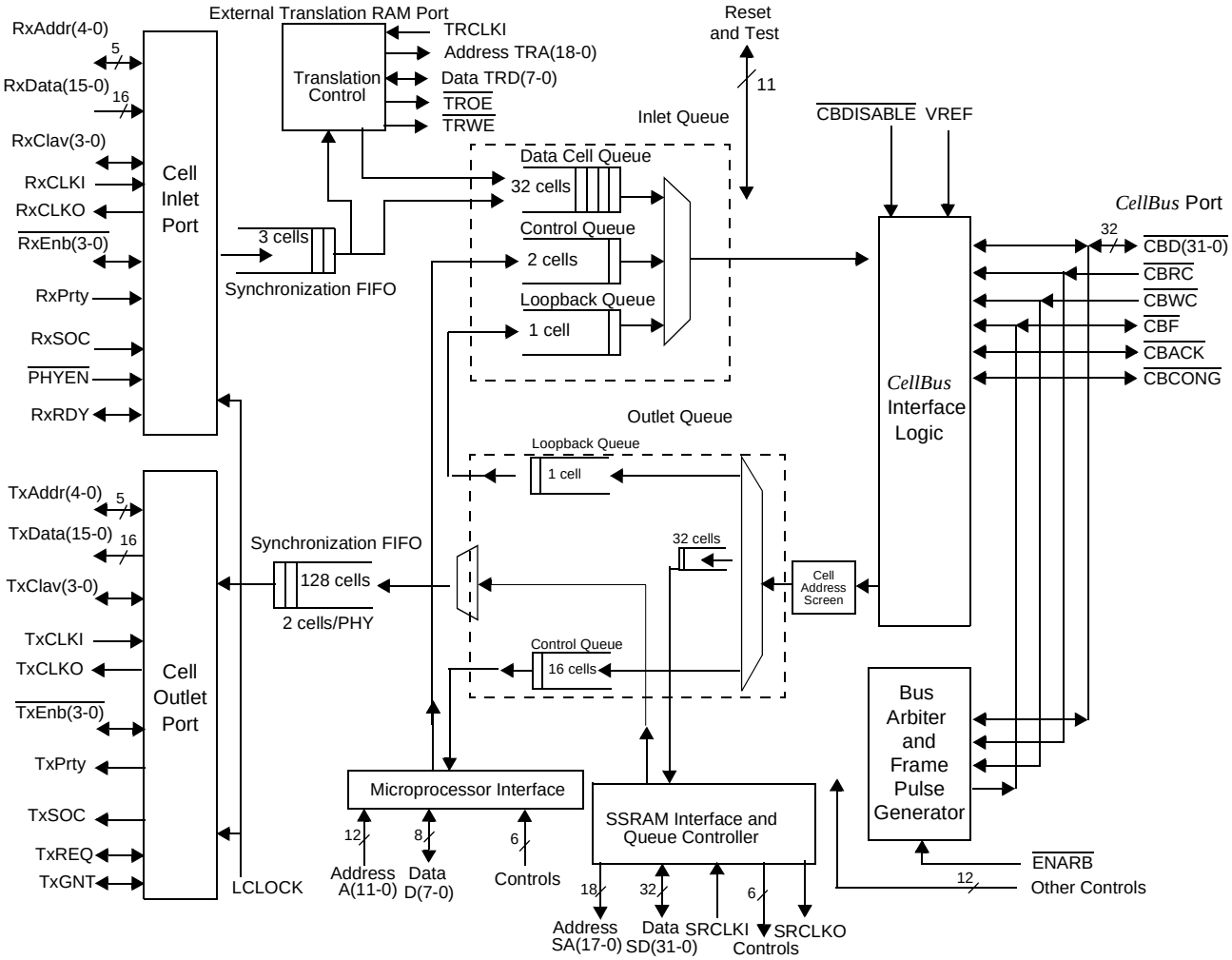



**Figure 2. CUBIT-622 TXC-05805 Block Diagram**

### CELL INLET TO *CellBus*

On the cell inlet side of the CUBIT-622 is circuitry associated with accepting cells from the line and passing them to the *CellBus* with an appropriate header. The Cell Inlet Port block is selectable to be compatible with either the ATM Forum UTOPIA (Universal Test and Operations Physical Interface for ATM) Level 1 or 2 interface. Incoming cells may be translated using the CUBIT-622 Translation Control block. Translation and routing header tables to support this function are contained in an external static RAM (TRAM, up to 512k x 8 bits). The configuration of the TRAM is identical to that used in the CUBIT-*Pro* (TXC-05802B). The CUBIT-622 provides support for VPI- or VPI/VCI-based translation while operating in both 8- and 16-bit modes. Operating in UTOPIA Level 2 ATM emulation mode will provide translation based on 64 ports (UNI bit set to 1) or 4 ports (UNI bit set to 0).

The CUBIT-622 also supports an external translation function where the incoming cell already carries a *CellBus* Routing Header, and Tandem Routing Header, and translated outgoing VPI/VCI address. The incoming cells then pass through a FIFO queue in the Inlet Queue block to the *CellBus* Port via the *CellBus* Interface Logic block.

When there is a cell in this 32-cell data cell queue, the CUBIT-622 makes a bus access request, and upon receiving a grant will send the cell to the bus, in standard *CellBus* format. In addition to data cells, the CUBIT-622 can also send Control cells from the local microprocessor to the bus. Loopback cells received from the bus may also be returned to the bus, re-directed back to the originating *CellBus* device which launched the Loopback cell. Both the Control cells and the Loopback cells have inlet queues, consisting of FIFOs with two cells and one cell, respectively. Statistics are kept for total numbers of misrouted cells, and received cells.

### *CellBus* TO CELL OUTLET

On the cell outlet side, cells of proper unicast address, broadcast address or selected multicast address, received from the *CellBus*, are recognized by the Cell Address Screen block and routed into a 32-cell FIFO queueing structure in the Outlet Queue block. The *CellBus* unicast address is unique per device, set by device straps. Each CUBIT-622 may be programmed to accept cells associated with multicast sessions. Up to 256 multicast sessions may be accepted independently by each CUBIT-622 on the bus. Each multicast session contains a list of destination ports to which a cell will be forwarded (max. all 64 ports). Control cells and Loopback cells arriving from the bus are routed to the 16-cell outlet control queue, and the 1-cell outlet loopback queue, respectively.

The outlet data cell FIFO structure can be configured as a single bulk queue per outlet port, or it can be subdivided into four individual queues for traffic of different service types per physical port (as shown in Figure 3). The four priority-queue split is typically into CBR cells, VBR-rt (real-time) cells, VBR-nrt (non real-time) cells, and GFR/UBR cells, in decreasing order of outlet service priority. This allows for delay minimization of critical service types, and for more efficient traffic management. The queue threshold limit for each individual queue may be configured independently. The Tandem Routing Header (TRH) bits 11-4 are used for queue selection (bits 11-6 indicate port number and bits 5-4 indicate priority), while TRH bits 3-0 hold a CRC-4 to protect bits 11-4.

The CUBIT-622 supports queue over-reservation, which accommodates the traffic burstiness inherent in ATM traffic. Using this technique, a traffic burst is allowed to consume buffer space up to the specified queue threshold. However, an additional constraint is that the sum of all queues in that service category must be less than or equal to the entire class allocation. Service class limits for VBR-nrt, VBR-rt and GFR/UBR are programmable. If the sum of all buffers utilized by all queues within one of these service categories exceeds the service category limit, then cells are not enqueued. To relieve congestion when it occurs and increase system goodput, the CUBIT-622 can be configured for packet discard. Packet discard is enabled on a global basis for the GFR/UBR queues. When an individual GFR/UBR queue limit is exceeded, the packet discard state is entered.

At the cell outlet, provisions are made for insertion of an outgoing Generic Flow Control (GFC) field and Explicit Forward Congestion Indication (EFCI) marking. Statistics are kept for discarded cells (per port).

Additionally, if enabled, the CUBIT-622 may be placed in a *CellBus* monitoring mode. In this mode, the CUBIT-622 accepts all traffic coming in from the *CellBus* regardless of *CellBus* ID. The cells are enqueued based on *CellBus* ID. *CellBus* IDs 0-15 are enqueued in service class 0 queues for ports 0-15, and IDs 16-31 are enqueued in service class 1 queues for ports 0-15. Additionally, all broadcast and multicast traffic is sent to queue 0.

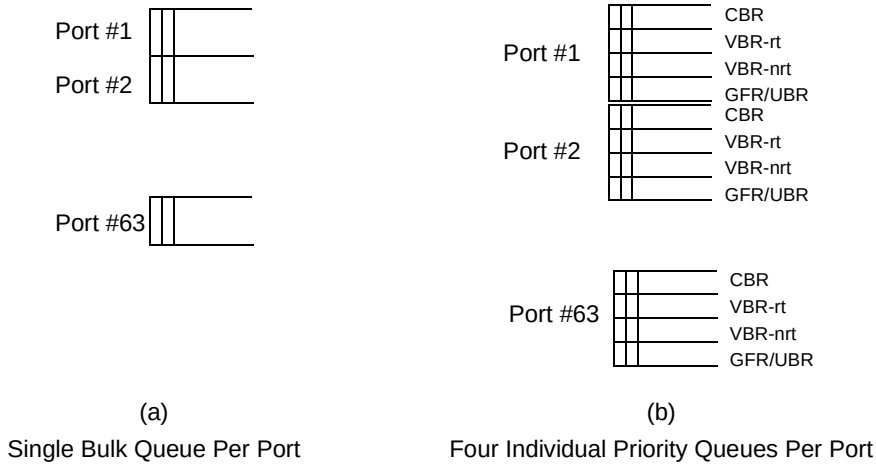



**Figure 3. CUBIT-622 Outlet Queue Modes**

## OTHER INTERFACES

### Microprocessor Interface

Registers are used for device configuration and indicating alarm conditions. Access to the CUBIT-622 registers is provided by the microprocessor interface, consisting of an 8-bit data bus, 12-bit address bus, and control signals. The interface can be configured for Motorola or Intel microprocessors.

### UTOPIA Interface

The CUBIT-622's UTOPIA 2 port constitutes the main interface for the cell traffic between the CUBIT-622 and other physical layer devices. The ATM Forum-compatible Level 1 and Level 2 interface can address up to 64 physical devices in ATM layer emulation (master) mode. The standard 5-bit address is used along with additional sets of CLAV and ENB signals for both transmit and receive. Multiple PHY devices may be configured for the same UTOPIA address (up to four), but each will have an individual CLAV and ENB signal pair. The UTOPIA master (CUBIT-622) will poll all PHY addresses with the same address simultaneously but will receive individual responses. Only one PHY is selected for a cell transfer at a time.

CUBIT-622 supports both master and slave modes of operation. In slave mode, the CUBIT-622 emulates a single-PHY device in UTOPIA 2 multi-PHY mode.

Additionally the CUBIT-622 supports cell sizes of 53 bytes and 57 bytes in 8-bit mode and 54 and 58 bytes in 16-bit interface mode when external header translation is used, i.e., where the incoming cell already carries a *CellBus* Routing Header, Tandem Routing Header, and translated outgoing VPI/VCI address. For all applications, timing and logical flow of the cell input/output is still identical to that of UTOPIA, except that potentially cell lengths differing from 53 bytes are transferred.

Tandem operation is available so that two CUBIT-622 devices in ATM emulation mode can both communicate to the PHY devices and each may be connected to a different *CellBus*. The tandem operation allows for one device to be a primary UTOPIA master while the other device is configured as a secondary master. The primary master arbitrates the UTOPIA bus to designate which master gets to transmit on each cell cycle. Both devices must receive all traffic and process it through the normal cell address screen. This feature enables the use of two *CellBus* devices in a load sharing configuration

### TRAM Memory Interface

An external local memory is required by the CUBIT-622 for address translation. The CUBIT-622 integrates a complete memory controller to support this local memory. The on-chip memory controller provides a glueless interface to a medium speed asynchronous SRAM. No external timing or control logic is required. The TRAM memory controller directly addresses up to 4 Mbits (512 kbytes). The TRAM access time requirement is dependent on the TRAM clock (TRCLKI) speed. An access time of 17 nanoseconds or less will support the maximum UTOPIA speed.

### SSRAM Memory Interface

An external local memory is required by the CUBIT-622 for cell queuing. The CUBIT-622 integrates a complete memory controller to support this local memory. The on-chip memory controller provides a glueless interface to a high speed synchronous SRAM. No external timing or control logic is required. The SSRAM memory controller directly addresses up to 8 Mbits of external memory to accommodate a maximum queue size of 16,000 cells. The memory controller is configured to use 256k x 32-bit memories at 100 MHz.

### Boundary Scan (Test Access) Port

The test interface includes a five-lead Test Access Port (TAP) as the boundary scan port that conforms to the IEEE 1149.1 standard. This standard provides external boundary scan functions to read and write the external input/output leads from the TAP for board and component test.

PRODUCT PREVIEW

## SELECTED PARAMETER VALUES

### ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

| Parameter | Symbol | Min | Max | Unit | Conditions |
|---|---|---|---|---|---|
| Supply voltage (I/O) | $V_{DD3.3}$ | -0.3 | +3.6 | V | Note 1 |
| Supply voltage (Core) | $V_{DD2.5}$ | -0.3 | +2.75 | V | Note 1 |
| DC input voltage | $V_{IN}$ | -0.5 | $V_{DD3.3}$ + 0.3 | V | Note 1 |
| Storage temperature range | $T_S$ | -40 | 125 | $^oC$ | Note 1 |
| Ambient operating temperature | $T_A$ | -40 | 85 | $^oC$ | 0 ft/min linear airflow |
| Component Temperature x Time | TI | | | $^oC$ x s | Note 1 |
| Moisture Exposure Level | ME | 5 | | Level | per EIA/JEDEC JESD22-A112-A |
| Relative Humidity, during assembly | RH | 30 | 60 | % | Note 2 |
| Relative Humidity, in-circuit | RH | 0 | 100 | % | non-condensing |
| ESD Classification | ESD | Absolute Value 2000 | | V | Note 3 |
| LATCH-UP | LU | | | | Meets JEDEC STD-78 |

Notes:
1. Operating conditions outside the min-max ranges specified may cause permanent device failure. Exposure to conditions near the min or max limits for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the "CAUTION" label on the drypack bag in which devices are supplied.
3. Test method for ESD per MIL-STD-883D, Method 3015.7.

### THERMAL CHARACTERISTICS

| Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| Thermal resistance - junction to ambient | | 22 | | $^oC/W$ | 0 ft/min linear airflow |

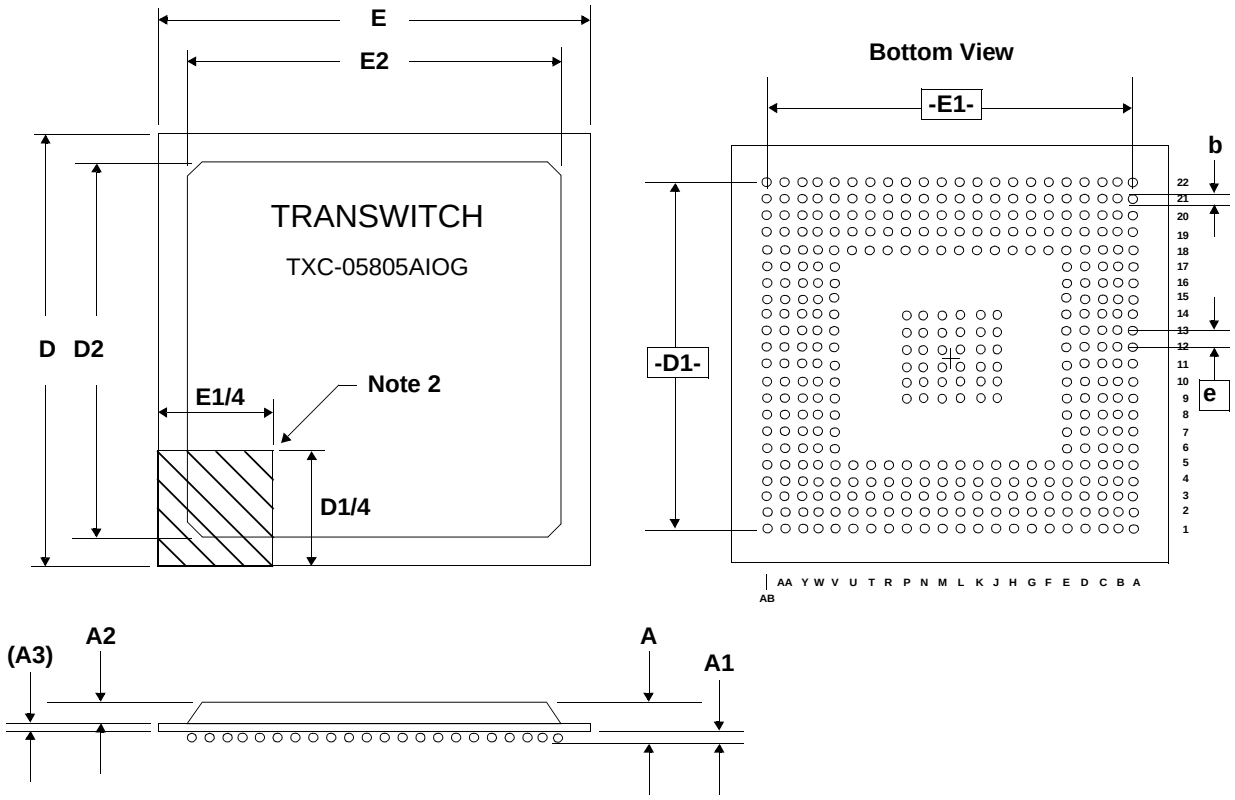
### POWER REQUIREMENTS

| Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| $V_{DD3.3}$ | 3.15 | 3.3 | 3.45 | V | |
| $I_{DD3.3}$ | | | TBD | mA | See Notes 1 and 2 |
| $P_{DD3.3}$ | | | TBD | W | See Notes 1 and 2 |
| $V_{DD2.5}$ | 2.38 | 2.5 | 2.62 | V | |
| $I_{DD2.5}$ | | | TBD | mA | See Notes 1 and 2 |
| $P_{DD2.5}$ | | | TBD | W | See Notes 1 and 2 |

Notes:
1. Typical values are based on measurements made with nominal voltages at 25° C
2. All $I_{DD}$ and $P_{DD}$ values are dependent upon $V_{DD}$.

## PACKAGE INFORMATION

The CUBIT-622 device is packaged in a 376-lead plastic ball grid array package suitable for surface mounting, as illustrated in Figure 4.




| Dimension (Note 1) | Min | Max |
|---|---|---|
| A | 2.02 | 2.44 |
| A1 | 0.40 | 0.60 |
| A2 | 1.12 | 1.22 |
| A3 (Ref.) | 0.56 | |
| b | 0.50 | 0.70 |
| D | 23.00 | |
| D1 (Nom) | 21.00 | |
| D2 | 19.45 | 20.20 |
| E | 23.00 | |
| E1 (Nom) | 21.00 | |
| E2 | 19.45 | 20.20 |
| e (Ref.) | 1.00 | |

Notes:
1. All dimensions are in millimeters. Values shown are for reference only.
2. Identification of the solder ball A1 corner is contained within this shaded zone. Package corner may not be a 90° angle.
3. Size of array: 22 x 22, JEDEC code MO-151.

**Figure 4. CUBIT-622 TXC-05805 376-Lead Plastic Ball Grid Array Package**

## ORDERING INFORMATION

Part Number: TXC-05805AIOG 376-lead Plastic Ball Grid Array Package (PBGA)

## RELATED PRODUCTS

TXC-05802B, CUBIT-*Pro* VLSI Device (ATM *CellBus* Switch). Implements cost effective ATM multiplexing and switching systems, based on the 32-bit *CellBus* architecture. A single-chip solution, the CUBIT has the ability to send and also receive cells for control purposes over the same *CellBus*. *CellBus* technology works at aggregate rates of up to 1 gigabit per second and provides header translation, multiplexing, concentration and switching functions for a wide variety of small-to-medium size ATM systems.

TXC-05804, CUBIT-3 VLSI Device (Multi-PHY *CellBus* Switch Access Device). A single-chip solution for implementing low-cost ATM multiplexing and switching systems, based on the *CellBus* architecture. Such systems are constructed from a number of CUBIT-3 devices, all interconnected by a 37-line common bus, the *CellBus.* CUBIT-3 supports unicast, broadcast and spatial multicast transfers, and has all necessary functions for implementing a switch: cell address translation, cell routing and outlet cell queuing. This device interfaces with CUBIT-*Pro* devices.

TXC-05810, ASPEN VLSI Device (Multi-Service *CellBus* Switch). ASPEN supports *CellBus* operation in both Cell and Packet modes via two independent *CellBus* ports. These may be configured to support redundant system operation or alternatively, to provide greater system throughput. Line interface is via UTOPIA 1 or 2 for ATM cells or UTOPIA 2P for variable length packets. Buffering of data traffic and control information, such as connection tables is stored in an external synchronous SRAM.

TXC-06203, PHAST-3P VLSI Device (STM-1/STS-3c SDH/SONET Overhead Terminator with CDB/PPP UTOPIA Interface). This is an STM-1/STS-3c section, line and path overhead termination device that provides CDB or PPP (HDLC) processing using an 8-bit or 16-bit UTOPIA single-PHY or multi-PHY interface for downstream access. A bit-serial or byte-parallel line interface is provided.

TXC-06212, PHAST-12E VLSI Device (Four-channel SONET STS-3c or STM-1 Overhead Terminator). This PHAST-12E device provides programmable, high performance ATM/Packet/Transmission for Level 12 applications with enhanced features.

## REFERENCE DOCUMENTS

- The ATM Forum: UTOPIA Specification Level 2, Version 1.0, June 1995
- The ATM Forum: Traffic Management Specification, Version 4.1, March 1999

**- NOTES -**

***PRODUCT PREVIEW***


TRANSWITCH®
Engines for Global Connectivity

## DOCUMENTATION UPDATE REGISTRATION FORM

If you would like to receive updated documentation for selected devices as it becomes available, please provide the information requested below (print clearly or type) then tear out this page, fold and mail it to the Marketing Communications Department at TranSwitch. Marketing Communications will ensure that the relevant Product Information Sheets, Data Sheets, Application Notes, Technical Bulletins and other publications are sent to you. You may also choose to provide the same information by fax **(203.926.9453)**, or by e-mail **(info@txc.com)**, or by telephone **(203.929.8810)**. Most of these documents will also be made immediately available for direct download as Adobe PDF files from the TranSwitch World Wide Web Site (**www.transwitch.com**).

Name: _____

Company: _____ Title: _____

Dept./Mailstop: _____

Street: _____

City/State/Zip: _____

If located outside U.S.A., please add - Country: _____ Postal Code: _____

Telephone: _____ Ext.: _____ Fax: _____

E-mail: _____

Please provide the following details for the managers in charge of the following departments at your company location.

| Department | Title | Name |
|---|---|---|
| Company/Division | _____ | _____ |
| Engineering | _____ | _____ |
| Marketing | _____ | _____ |

Please describe briefly your intended application(s) and indicate whether you would like to have a TranSwitch applications engineer contact you to provide further assistance:

_____

_____

_____

_____

If you are also interested in receiving updated documentation for other TranSwitch device types, please list them below rather than submitting separate registration forms:

_____ _____ _____ _____ _____ _____ _____

_____ _____ _____ _____ _____ _____ _____

*Please fold, tape and mail this page (see other side) or fax it to Marketing Communications at 203.926.9453.*


(Fold back on this line second, then tape closed, stamp and mail.)

TRANSWITCH

**3 Enterprise Drive**
**Shelton, CT 06484-4694**
**U.S.A.**

First Class Postage Required

**TranSwitch Corporation**

**Attention: Marketing Communications Dept.**
**3 Enterprise Drive**
**Shelton, CT 06484-4694**
**U.S.A.**

(Fold back on this line first.)

Please complete the registration form on this back cover sheet, and fax or mail it, if you wish to receive updated documentation on this TranSwitch product as it becomes available.