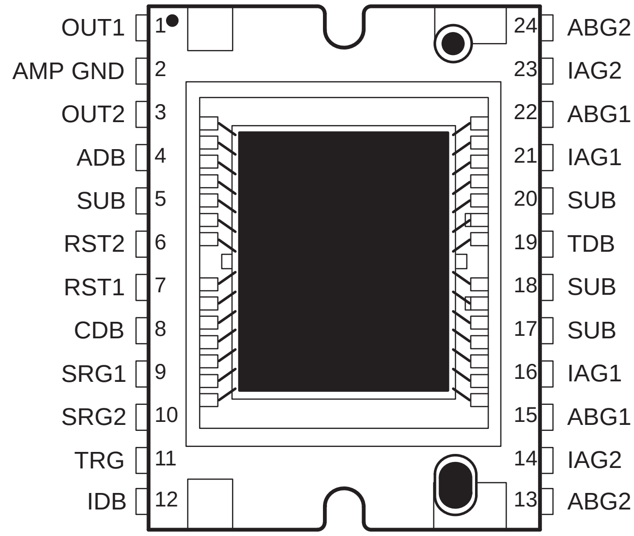
- **High-Resolution, Solid-State Frame-Transfer Image Sensor**
- **17.2-mm Image-Area Diagonal**
- **1000 (H) x 1018 (V) Active Elements in Image-Sensing Area**
- **Square Pixels**
- **Low Dark Current**
- **Electron-Hole Recombination Antiblooming**
- **Dynamic Range . . . More Than 60 dB**
- **High Sensitivity**
- **High Photoresponse Uniformity**
- **High Blue Response**
- **Single-Phase Clocking**
- **Solid-State Reliability With No Image Burn-in, Residual Imaging, Image Distortion, Image Lag, or Microphonics**

DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The TC215 is a full-frame charge-coupled-device (CCD) image sensor that provides very high-resolution image acquisition for image-processing applications such as robotic vision, medical X-ray analysis, and metrology. The image format measures 12 mm horizontally by 12.216 mm vertically; the image-area diagonal is 17.2 mm. The image-area pixels are 12-µm square. The image area contains 1018 active lines with 1000 active pixels per line. Six additional dark reference lines give a total of 1024 lines in the image area, and 24 additional dark reference pixels per line give a total of 1024 pixels per horizontal line.

The full-frame image sensor should be used with a shutter or with strobed illumination to prevent smearing of the image during readout. To prepare the imaging area for image capture, the photoelectric charge that has accumulated in the image pixels can be transferred into the clearing drain in one millisecond. After image capture (integration time), the readout is accomplished by transferring the charge, one line at a time, into two serial registers, each of which contains 512 data elements and 12 dummy elements. The typical serial-register clocking rate is 10 megapixels per second. Operating the TC215 at the typical data rate of one field per frame generates video output at a continuous 15 frames per second.

Gated floating-diffusion detection structures are used with each serial register to convert charge to signal voltage. External reset allows the application of off-chip correlated clamp sample-and-hold amplifiers for low-noise performance. To provide high output-drive capability, both outputs are buffered by low-noise, two-stage, source-follower amplifiers. These two output signals can provide a data rate of 20 megapixels per second when combined off chip. At room temperature, the readout noise is 55 electrons and a minimum dynamic range of 60 dB is available.

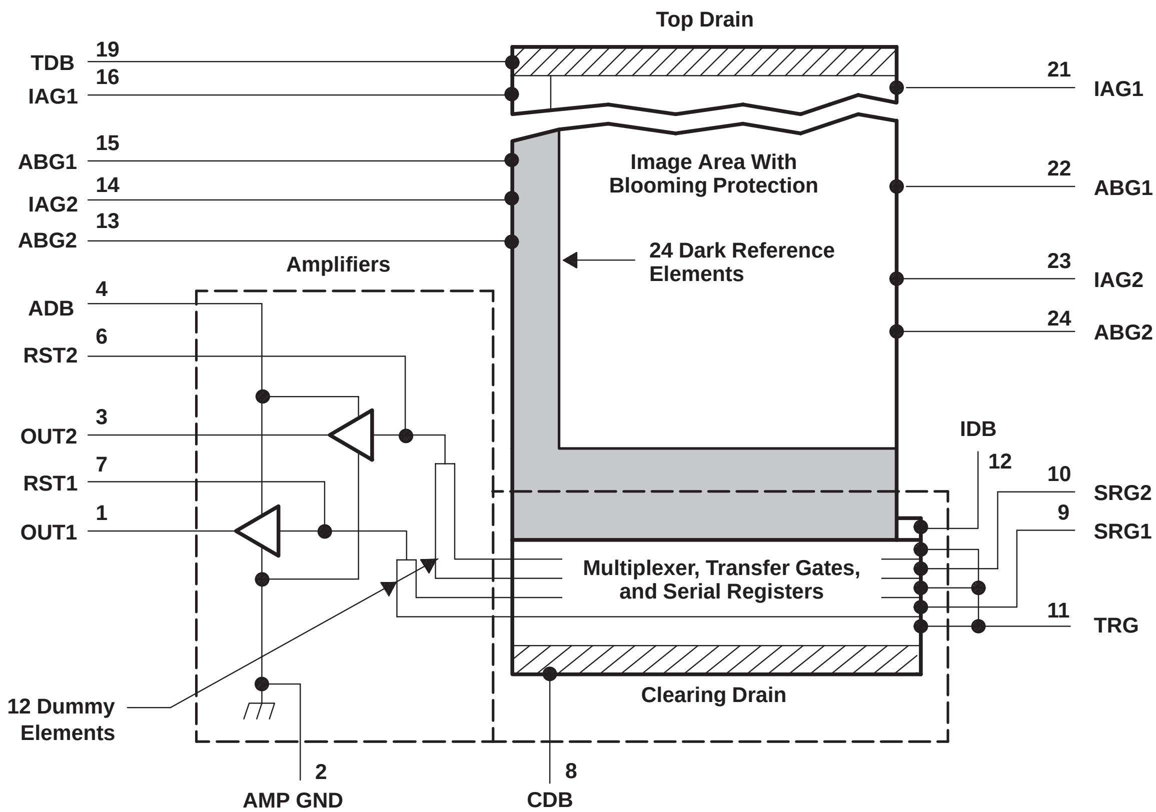
This MOS device contains limited built-in gate protection. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to SUB. Under no circumstances should pin voltages exceed absolute maximum ratings. Avoid shorting OUTn to ADB during operation to prevent damage to the amplifier. The device can also be damaged if the output terminals are reverse-biased and an excessive current is allowed to flow. Specific guidelines for handling devices of this type are contained in the publication *Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies* available from Texas Instruments.

description (continued)

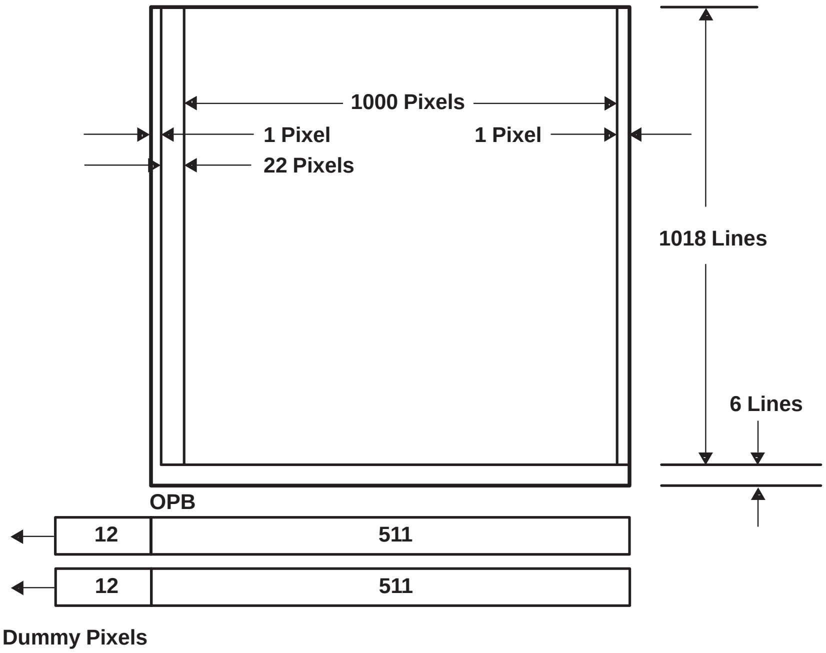
The blooming protection incorporated into the sensor is based on recombining excess charge with charge of oppositie polarity in the substrate. This antiblooming is activated by supplying clocking pulses to the antiblooming gate, which is an integral part of each image-sensing element.

The TC215 is built using TI-proprietary virtual-phase technology, which provides devices with high blue response, low dark signal, good uniformity, and single-phase clocking. The TC215 is characterized for operation from –10°C to 40°C.

functional block diagram



sensor topology diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ABG1†	15	I	Antiblooming gate for upper image area
ABG1†	22	I	Antiblooming gate for upper image area
ABG2†	13	I	Antiblooming gate for lower image area
ABG2†	24	I	Antiblooming gate for lower image area
ADB	4	I	Supply voltage for amplifier drain bias
AMP GND	2		Amplifier ground
CDB	8	I	Supply voltage for clearing drain bias
IAG1†	16	I	Upper image-area gate
IAG1†	21	I	Upper image-area gate
IAG2†	14	I	Lower image-area gate
IAG2†	23	I	Lower image-area gate
IDB	12	I	Supply voltage for input diode bias
OUT1	1	O	Output signal 1
OUT2	3	O	Output signal 2
RST1	7	I	Reset gate 1
RST2	6	I	Reset gate 2
SRG1	9	I	Serial-register gate 1
SRG2	10	I	Serial-register gate 2
SUB†	5		Substrate and clock return
SUB†	17		Substrate and clock return
SUB†	18		Substrate and clock return
SUB†	20		Substrate and clock return
TDB	19	I	Supply voltage for top drain bias
TRG	11	I	Transfer gate

† All terminals of the same name should be connected together externally (i.e., pin 15 to pin 22, pin 13 to pin 24, etc.).

detailed description

The TC215 consists of three basic functional blocks: (1) the image-sensing area, (2) the multiplexer block with serial registers and transfer gates, and (3) the low-noise signal-processing amplifier block with charge-detection nodes. The location of each of these blocks is identified in the functional block diagram.

image-sensing area

Figures 1 and 2 show cross sections with potential well diagrams and top views of image-sensing elements. As light enters the silicon in the image-sensing area, free electrons are generated and collected in the potential wells of the sensing elements. During this time, blooming protection is activated by applying a burst of pulses to the antiblooming gate inputs every horizontal blanking interval. This prevents blooming caused by the spilling of charge from overexposed elements into neighboring elements. After integration is complete, the signal charge is transferred in the dark to the two serial registers, where it is read out line by line.

There are 24 full columns of elements at the left edge of the image-sensing area that are shielded from incident light; these elements provide the dark reference used in subsequent video-processing circuits to restore the video black level. There are also six dark lines at the bottom of the sensor.

multiplexer with transfer gates and serial registers

The multiplexer and transfer gates transfer charge line by line from the image-sensing columns into the corresponding serial registers and prepare it for readout. Figure 3 illustrates the layout of the multiplexing gate that vertically separates the pixels for input into the serial registers. Figure 4 shows the layout of the interface region between the serial-register gates and the transfer gates. Multiplexing is activated during the horizontal blanking interval by applying appropriate pulses to the transfer gates and serial registers; the required pulse timing is shown in Figure 5. A drain is also included to provide the capability to clear the image-sensing area of unwanted charge. Such charge can accumulate in the imager during the start-up of operation or under special circumstances. The clearing timing is illustrated in Figure 6.

serial-register readout and video processing

After transfer into the serial registers, the pixels are normally read out 180° out of phase (see Figure 7). Each serial register must be reset to the reference level before the next pixel is read out. The timing for the resets and their relationships to the serial-register pulses is shown in Figure 8. Figure 8 also shows the timing for the pixel clamp and sample and hold needed for an off-chip double-correlated sampling circuit. These two output signals can provide a data rate of 20 million pixels per second when combined off chip. After the charge is placed on the detection node, it is buffered and amplified by a low-noise, dual-stage source follower. Each serial register contains 12 dummy elements that are used to span the distance between the serial register and the output amplifier. A schematic is shown in Figure 9. The location of the dummy elements, which are considered to be part of the amplifiers, is shown in the functional block diagram. Figure 10 gives the timing for a single frame of video. Operating the TC215 at the typical data rate of one field per frame generates video output at a continuous 15 frames per second.

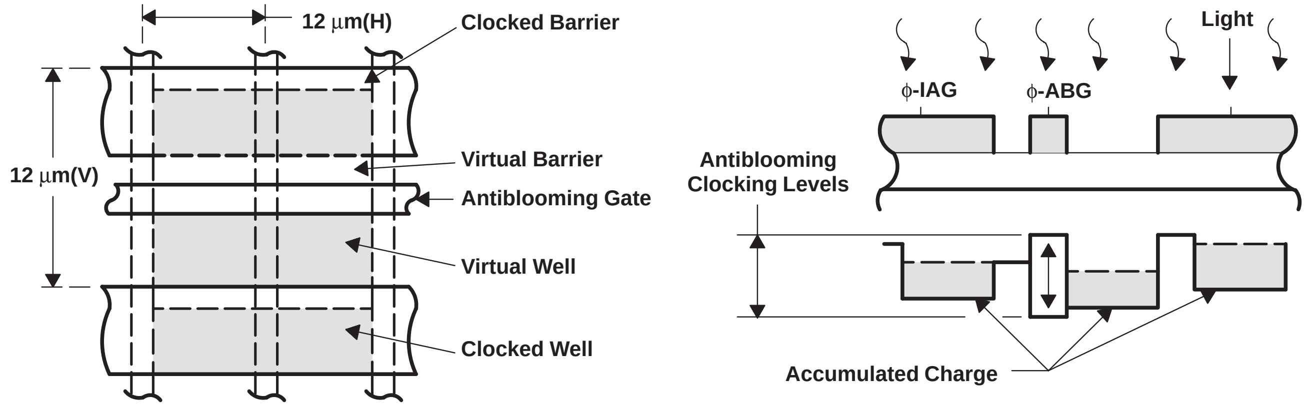


Figure 1. Charge-Accumulation Process

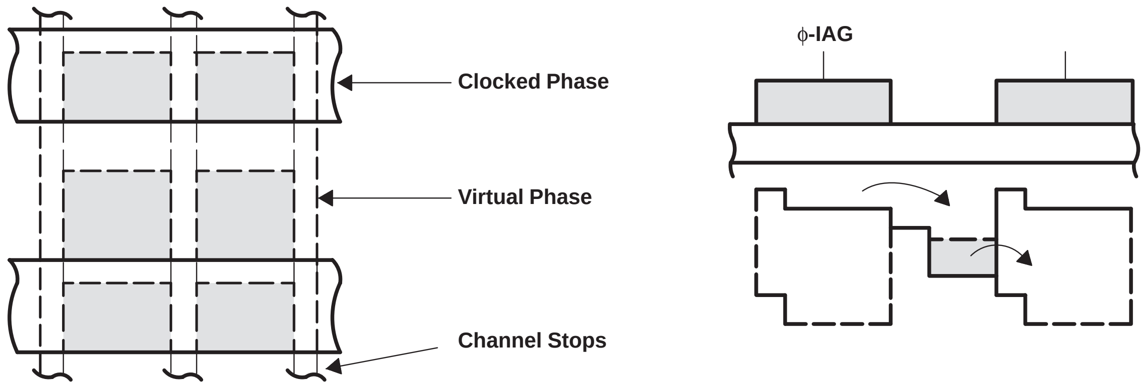


Figure 2. Charge-Transfer Process

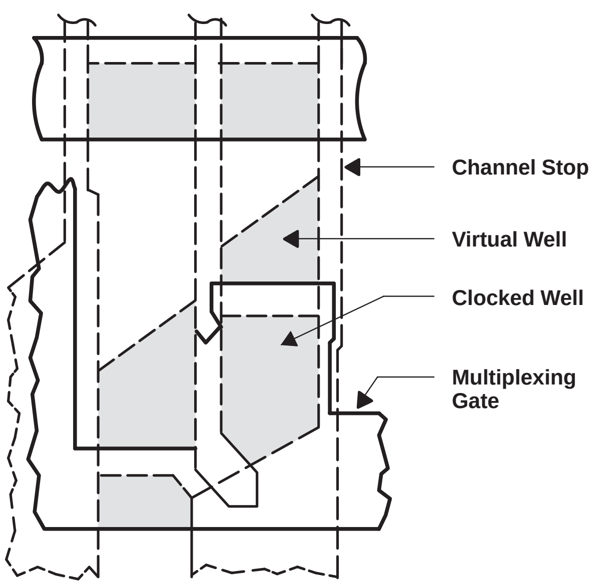


Figure 3. Multiplexing-Gate Layout

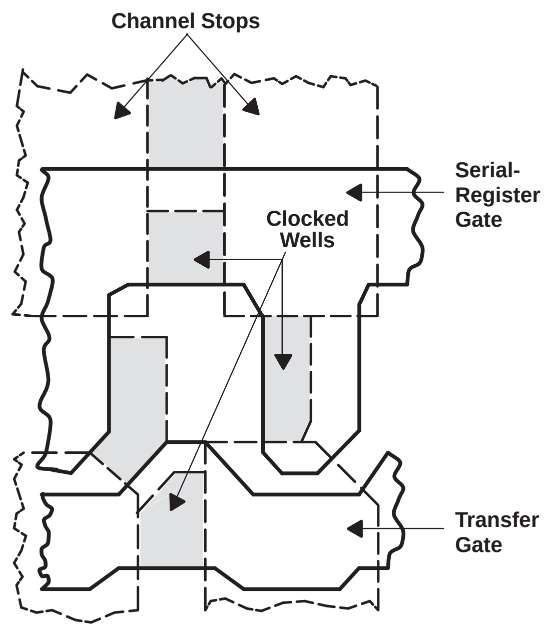


Figure 4. Interface-Region Layout

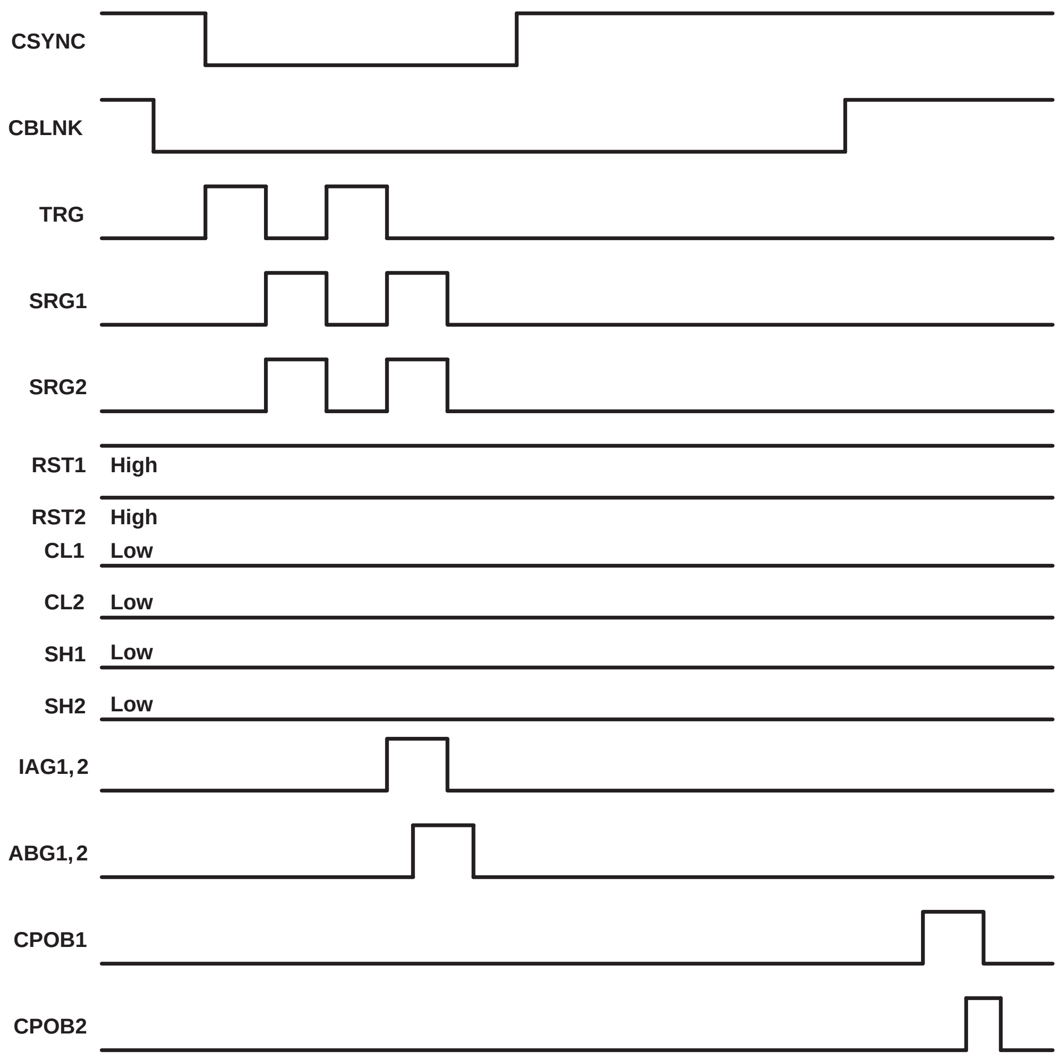


Figure 5. Horizontal Timing

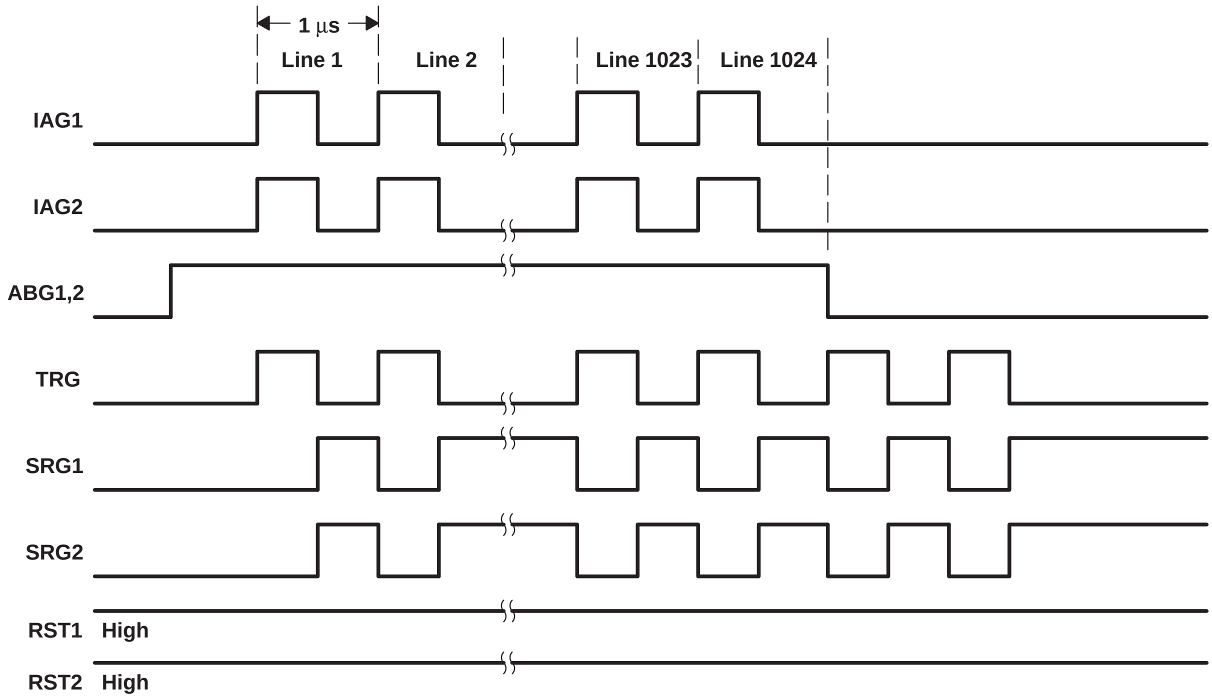
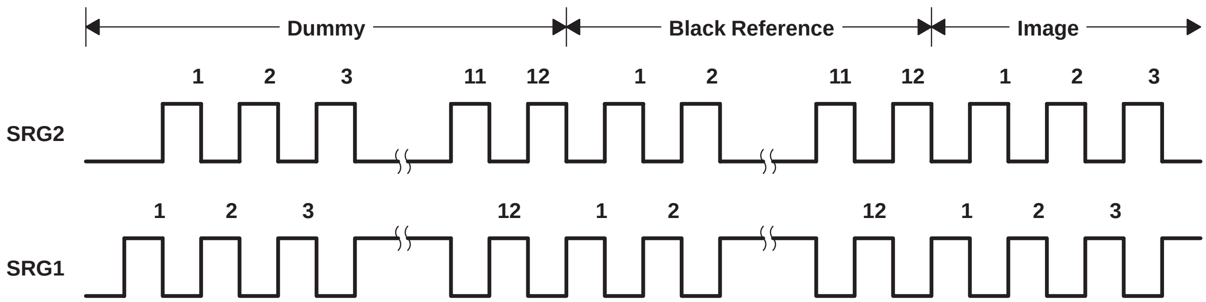
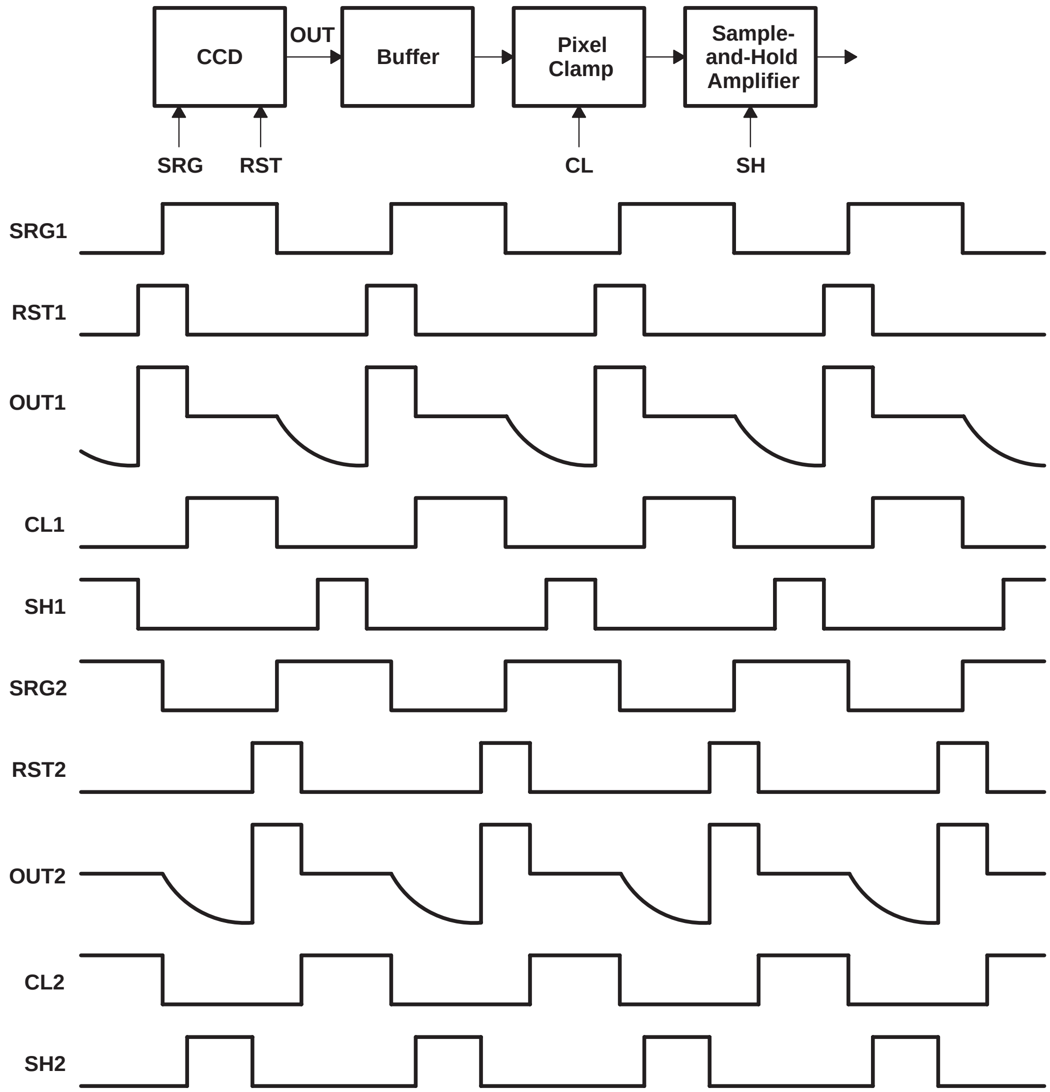


Figure 6. Clearing Timing



NOTE A: A minimum of 524 clock pulses is required to transfer out all elements of a serial register. Overclocking is recommended.

Figure 7. Start of Serial-Transfer Timing



NOTE A: The video-processing (off-chip) pulses are defined as follows:
- CL1 = Clamp pulse for video from OUT1
- CL2 = Clamp pulse for video from OUT2
- SH1 = Sample pulse for the sample-and-hold amplifier for video 1
- SH2 = Sample pulse for the sample-and-hold amplifier for video 2
- CSYNC = Composite video-sync pulse
- CBLNK = Composite video-blanking pulse
- CPOB1 = Dark-reference clamp pulse for video from OUT1
- CPOB2 = Dark-reference clamp pulse for video from OUT2

Figure 8. Video-Process Timing

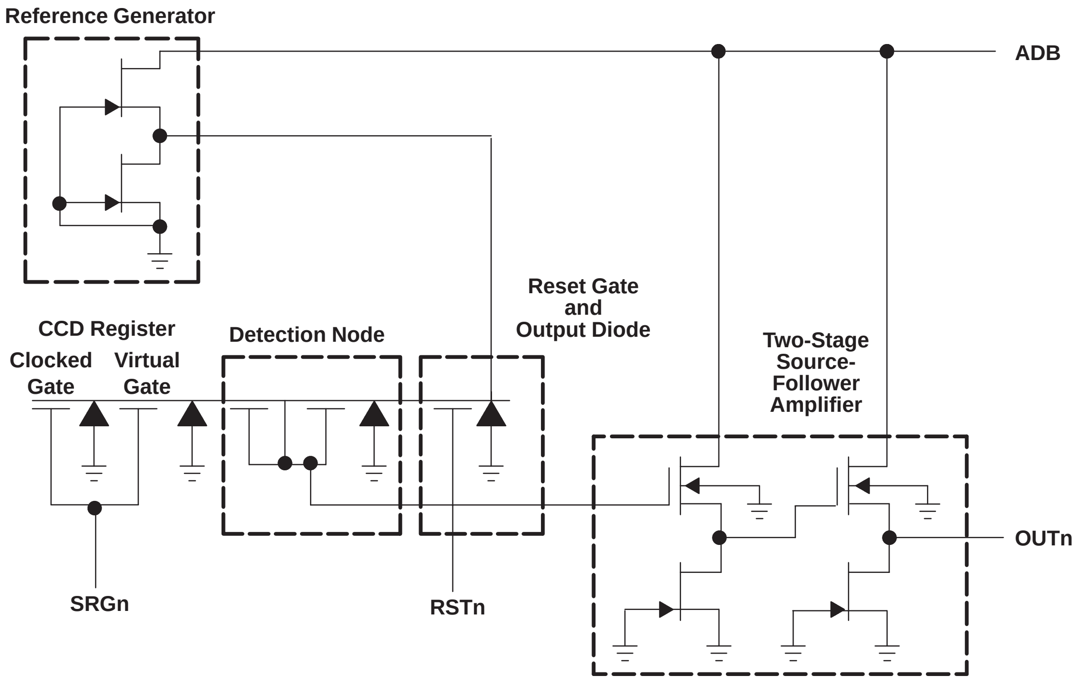


Figure 9. Buffer Amplifier and Charge-Detection Node

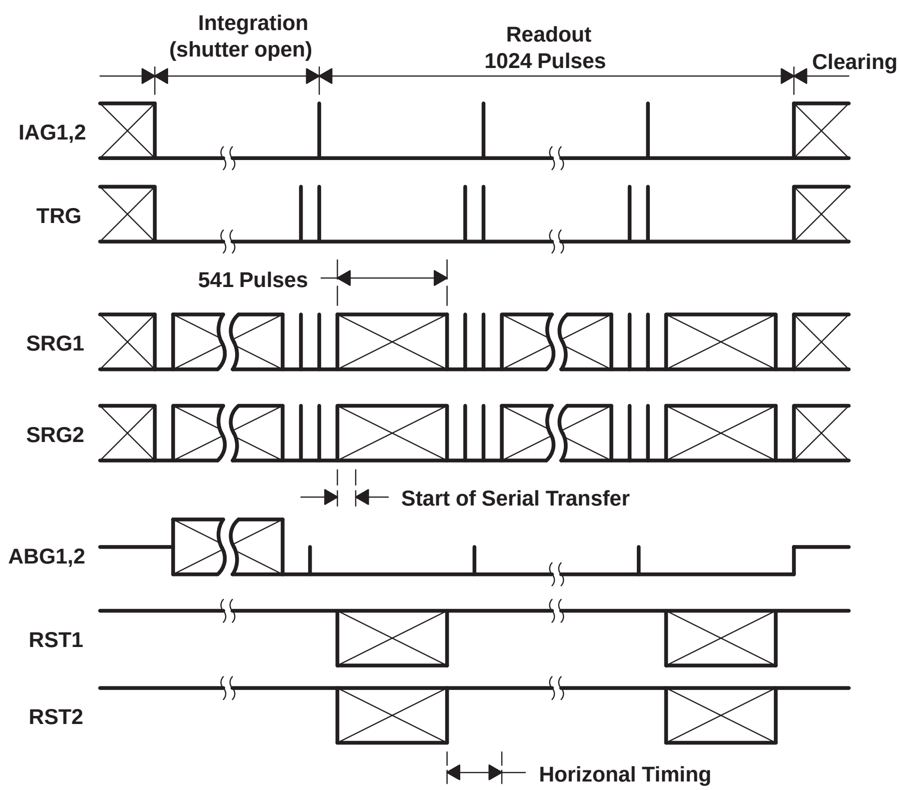


Figure 10. Clock Timing Requirements – Single-Frame Mode

spurious nonuniformity specification

The spurious nonuniformity specification of the TC215 CCD grades –30 and –40 is based on several sensor characteristics:

- Amplitude of the nonuniform line or pixel
- Polarity of the nonuniform pixel
  - Black
  - White
- Nonuniform line or pixel count

The CCD sensors are characterized in both an illuminated condition and a dark condition. In the dark condition, the nonuniformity is specified in terms of absolute amplitude as shown in Figure 11. In the illuminated condition, the nonuniformity is specified as a percentage of the total illumination as shown in Figure 12.

The pixel nonuniformity specification for the TC215 is as follows (CCD video-output signal is 50 mV ±10 mV):

NONUNIFORMITY TYPE	TC215-30	TC215-40
Line	Maximum amplitude = 1.4 mV	
	Number with amplitude greater than 1 mV is ≤ 5	
White spot (40°C)	Maximum amplitude = 25 mV	
White spot (25°C)	Maximum amplitude = 15 mV	Maximum amplitude = 20 mV
	Number with amplitude greater than 10 mV = B	
Black spot (% of total illumination)	Maximum amplitude = 25%	Maximum amplitude = 30%
	Number with amplitude greater than 10% = C	
Total number of nonuniformities	B + C < 20	

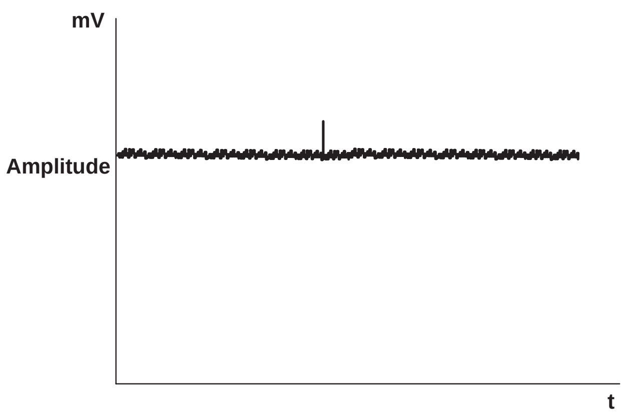


Figure 11. Pixel Nonuniformity, Dark Condition

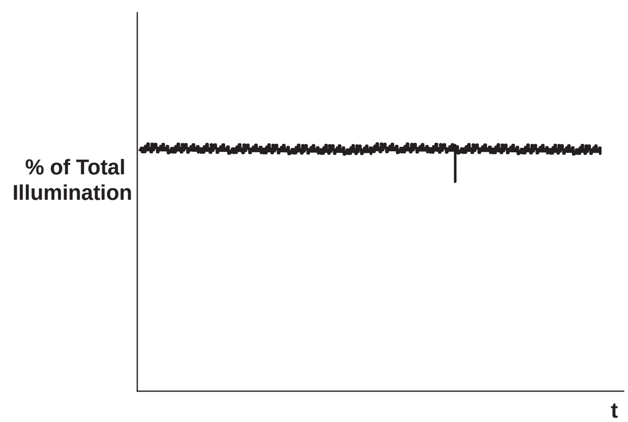


Figure 12. Pixel Nonuniformity, Illuminated Condition

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range for ADB, CDB, IDB, TDB (see Note 1) . . . . 0 V to 15 V
Input voltage range for ABG1, ABG2, IAG1, IAG2, RST1, RST2, SRG1, SRG2, TRG . . . . . . –15 V to 15 V
Operating free-air temperature range, T_A . . . . –10°C to 40°C
Storage temperature range . . . . –30°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the substrate terminal.

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply voltage for ADB, CDB, IDB, TDB			11	12	13	V
Substrate bias voltage				0		V
Input voltage, V_I‡	IAG1, IAG2	High level	1.5	2	2.5	V
		Low level	–11		–9	
	SRG1, SRG2	High level	1.5	2	2.5	
		Low level	–11		–9	
	RST1, RST2	High level	1.5	2	2.5	
		Low level	–11		–9	
	ABG1, ABG2	High level	5	5.5	6	
		Intermediate level§	–1.5	–1.2	–0.9	
		Low level	–7.5	–7	–6.5	
	TRG	High level	1.5	2	2.5	
		Low level	–11		–9	
Clock frequency, f_{clock}	TRG, SRG1, SRG2, RST1, RST2				10	MHz
	IAG1, IAG2				1	
	ABG1, ABG2				1	
Capacitive load	OUT1, OUT2				8	pF
Operating free-air temperature, T_A			–10		40	°C

‡ The algebraic convention, in which the least-positive (most negative) value is designated minimum, is used in this data sheet for clock voltage levels.

§ Adjustment is required for optimal performance.

electrical characteristics over recommended operating ranges of supply voltage and free-air temperature

PARAMETER		MIN	TYP†	MAX	UNIT
Dynamic range (see Note 2)		60			dB
Charge conversion factor			6		μV/e
Charge transfer efficiency (see Note 3)		0.99990			
Signal response delay time, τ (see Note 4 and Figure 16)		18	20	22	ns
Gamma (see Note 5)		0.89	0.94	0.99	
Output resistance				1000	Ω
Noise voltage	1/f noise (5 kHz)		0.1		μV/√Hz
	Random noise (f = 100 kHz)		0.08		
Noise equivalent signal			60		electrons
Rejection ratio at 10 MHz	ADB (see Note 6)		20		dB
	SRGn (see Note 7)		40		
	ABGn (see Note 8)		30		
Supply current				9	mA
Input capacitance, C_i	IAG1, IAG2		15000		pF
	ABG1, ABG2		8000		
	TRG		350		
	SRG1, SRG2		200		

† All typical values are at T_A = 25 °C.

NOTES: 2. Dynamic range is –20 times the logarithm of the mean noise signal divided by the saturation output signal.
3. Charge transfer efficiency is one minus the charge loss per transfer in the output register (1046 transfers). The test is performed in the dark using an electrical input signal.
4. Signal-response delay time is the time between the falling edge of the SRG clock pulse and the output signal valid state.
5. Gamma (γ) is the value of the exponent in the equation below for two points on the linear portion of the transfer function curve (this value represents points near saturation):

$$\left(\frac{\text{Exposure (2)}}{\text{Exposure (1)}}\right)^{\gamma} = \left(\frac{\text{Output signal (2)}}{\text{Output signal (1)}}\right)$$

6. ADB rejection ratio is –20 times the logarithm of the ac amplitude on OUTn divided by the ac amplitude on ADB.
7. SRGn rejection ratio is –20 times the logarithm of the ac amplitude on OUTn divided by the ac amplitude on SRGn.
8. ABGn rejection ratio is –20 times the logarithm of the ac amplitude on OUTn divided by the ac amplitude on ABGn.

optical characteristics, T_A = 25°C, integration time = 33 ms (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
Sensitivity (see Note 9)	No IR filter	Measured at V_U (see Note 10)		518		mV/lx
	With IR filter			64		
Saturation signal, V_{sat} (see Note 11)			320			mV
Maximum usable signal, V_{use}			200			mV
Blooming overload ratio (see Note 12)			100			
Image-area well capacity				60 x 10^3		electrons
Dark current		T_A = 21°C		0.027		nA/cm^2
Dark signal (see Note 13)	T_A = 40°C	TC215-30			5	mV
		TC215-40			5	
Pixel uniformity		TC215-30			15	mV
		TC215-40			20	
Column uniformity		TC215-30			1.4	mV
		TC215-40			1.4	
Shading	V_O = 1/2 V_U (see Note 10)				15%	

NOTES: 9. Sensitivity is measured at an integration time of 33 ms with a source temperature of 2859 K. A CM-500 filter is used. Sensitivity is measured at any illumination level that gives an output voltage level less than V_U.

10. V_U is the output voltage that represents the threshold of operation of antiblooming. $V_U \approx$ 1/2 saturation signal.

11. Saturation is the condition in which further increase in exposure does not lead to further increase in output signal.

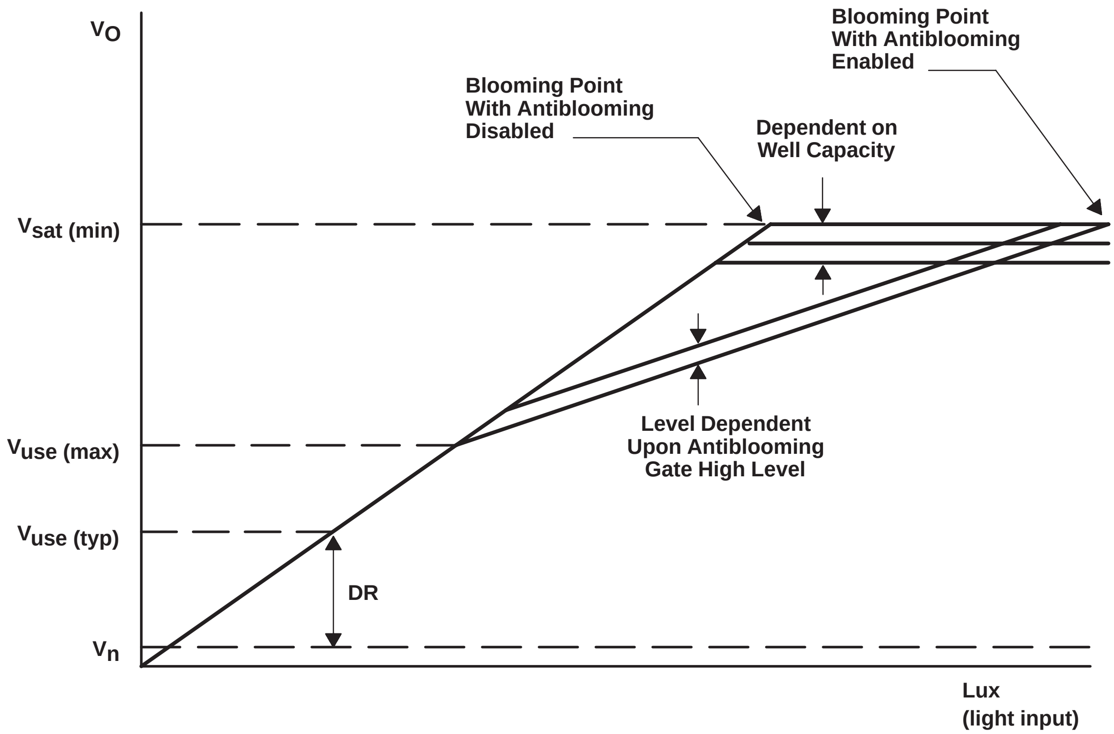
12. Blooming is the condition in which charge is induced in an element by light incident on another element. Blooming overload ratio is the ratio of blooming exposure to saturation exposure.

13. Dark-signal level is measured from the dark dummy pixels.

timing requirements

			MIN	MAX	UNIT
t_r	Rise time	IAG1, IAG2	200		ns
		SRG1, SRG2	10		
		RST1, RST2	10		
		TRG	200		
		ABG1, ABG2	100		
t_f	Fall time	IAG1, IAG2	200		ns
		SRG1, SRG2	10		
		RST1, RST2	10		
		TRG	200		
		ABG1, ABG2	100		

PARAMETER MEASUREMENT INFORMATION



$$\text{DR (dynamic range)} = \frac{\text{camera white clip voltage}}{V_n}$$

V_n = noise floor voltage
$V_{sat\ (min)}$ = minimum saturation voltage
$V_{use\ (max)}$ = maximum usable voltage
$V_{use\ (typ)}$ = typical user voltage (camera white clip)

NOTES: A. $V_{use\ (typ)}$ is defined as the voltage determined to equal the camera white clip. This voltage must be less than $V_{use\ (max)}$.
B. A system trade-off is necessary to determine the system light sensitivity versus the signal/noise ratio. By lowering the $V_{use\ (typ)}$, the light sensitivity of the camera is increased; however, this sacrifices the signal/noise ratio of the camera.

Figure 13. Typical V_{sat}, V_{use} Relationship

PARAMETER MEASUREMENT INFORMATION

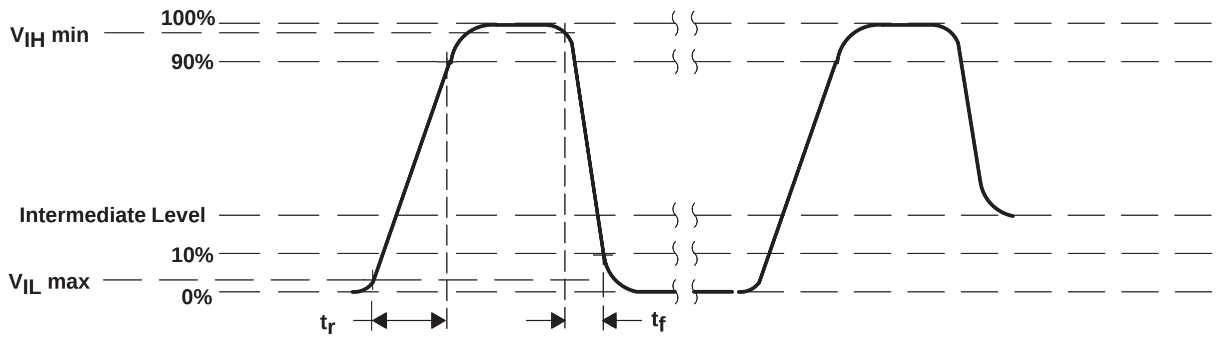


Figure 14. Typical Clock Waveform for ABG1, ABG2, IAG1, and IAG2

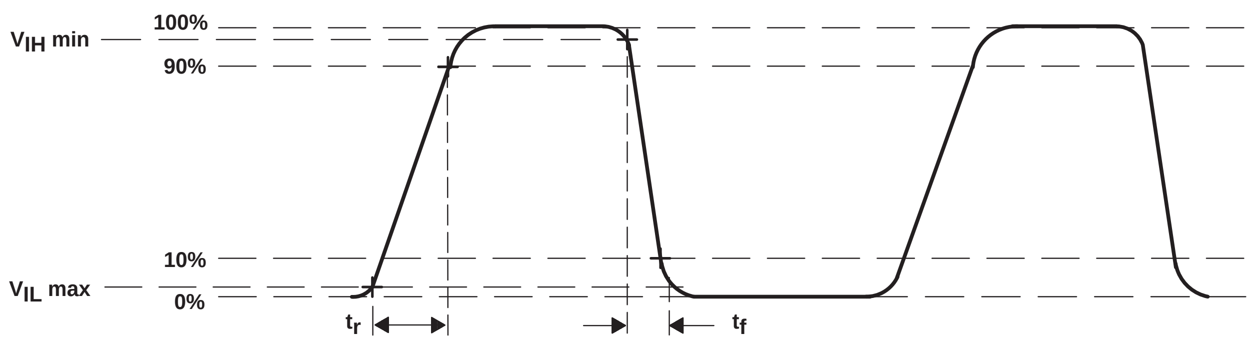


Figure 15. Typical Clock Waveform for RST1, RST2, SRG1, SRG2, and TRG

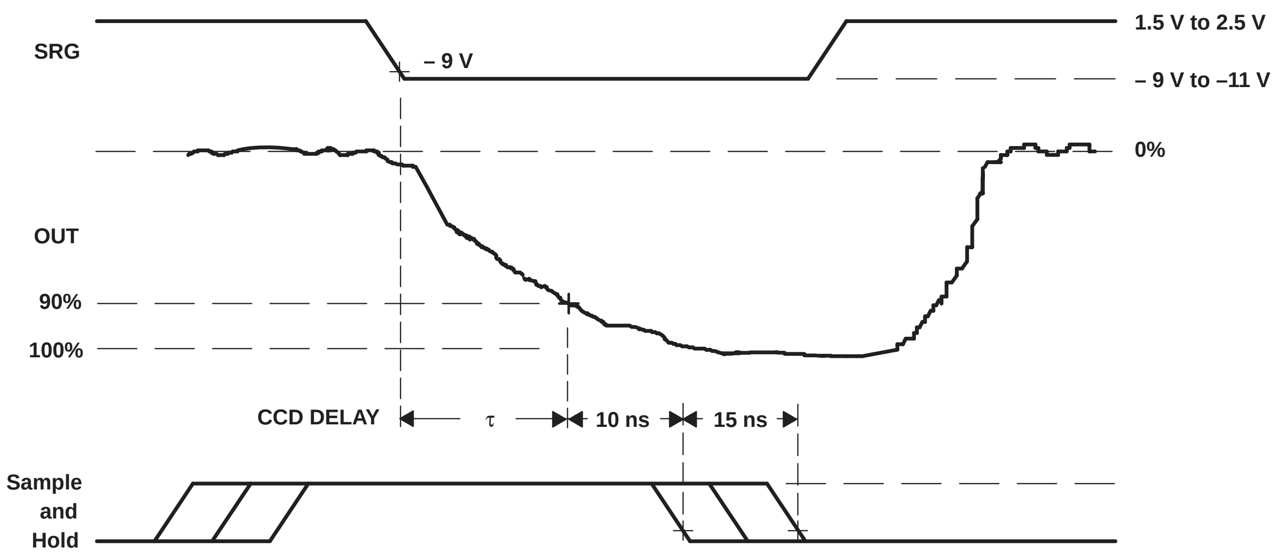
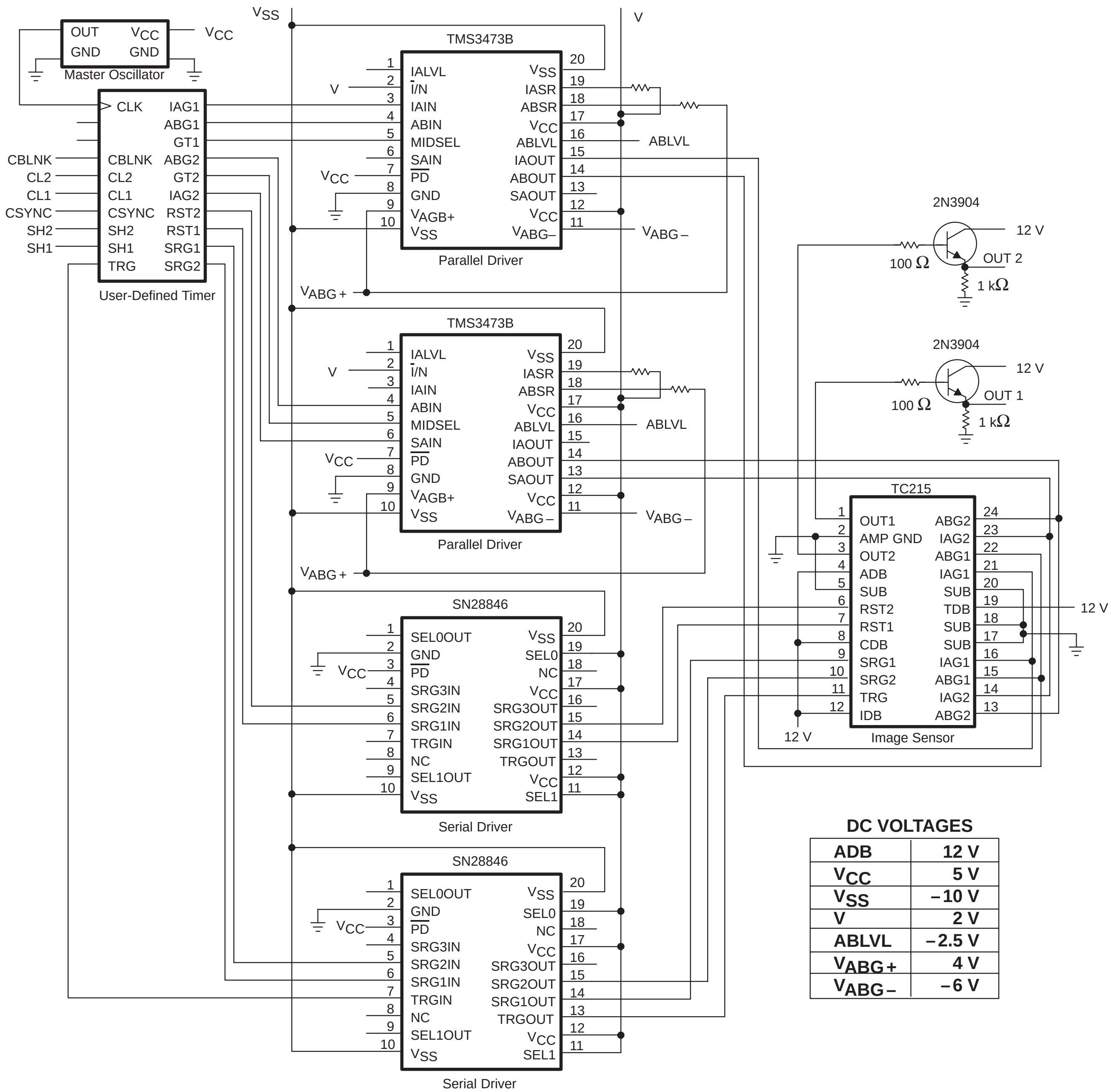


Figure 16. SRG and CCD OUT Waveforms

APPLICATION INFORMATION



DC VOLTAGES

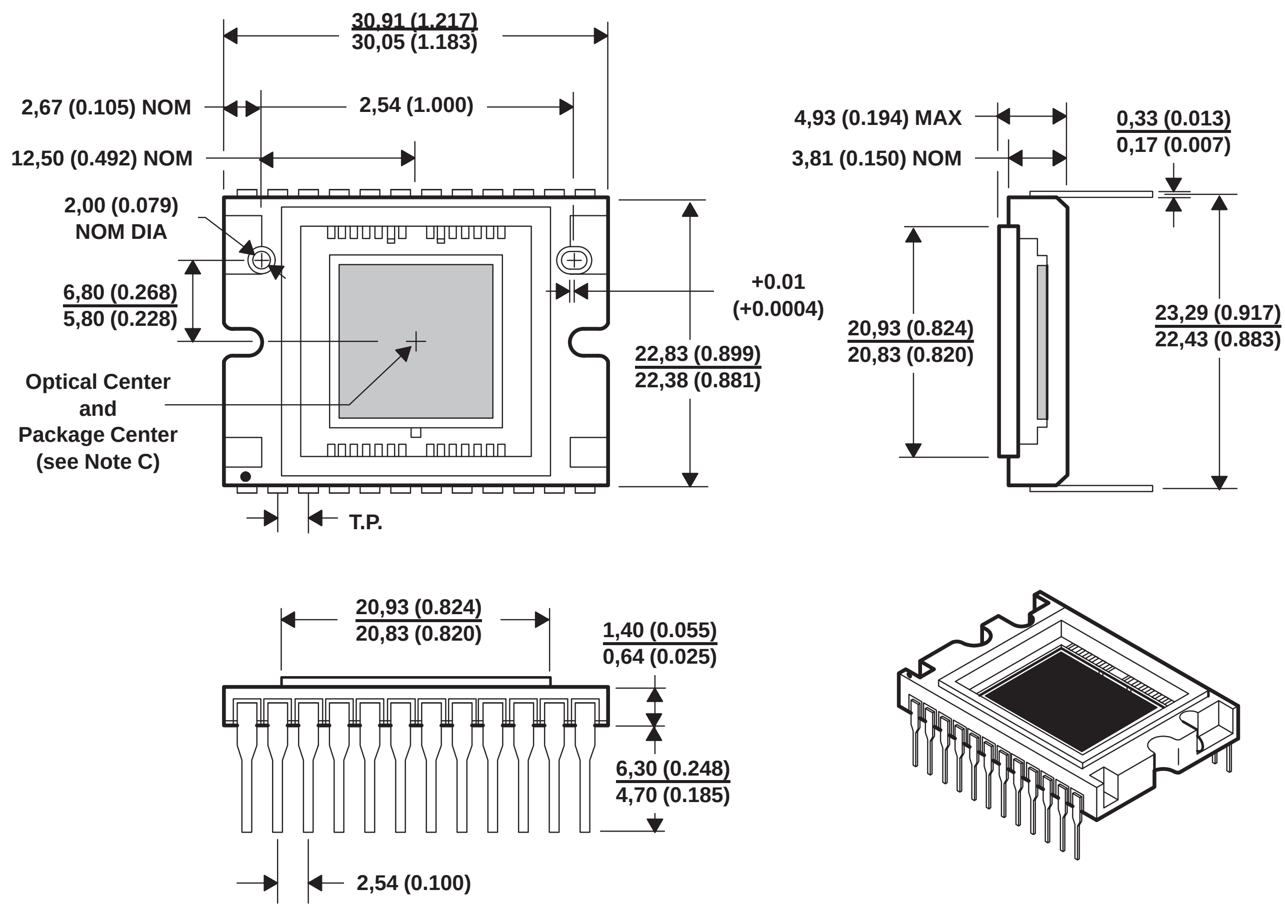
ADB	**12 V**
V_{CC}	**5 V**
V_{SS}	**–10 V**
V	**2 V**
ABLVL	**–2.5 V**
V_{ABG+}	**4 V**
V_{ABG-}	**–6 V**

SUPPORT CIRCUITS			
DEVICE	**PACKAGE**	**APPLICATION**	**FUNCTION**
SN28846DW	20 pin small outline	Serial driver	Driver for TRG, SRG1, SRG2, RST1, RST2
TMS3473BDW	20 pin small outline	Parallel driver	Driver for IAG1, IAG2, ABG1, ABG2

Figure 17. Typical Application Circuit Diagram

MECHANICAL DATA

The package for the TC215 consists of a ceramic base, a glass window, and a 24-lead frame. The glass window is sealed to the package by an epoxy adhesive. The package leads are configured in a dual in-line organization and fit into mounting holes with 2,54 mm (0.1 in) center-to-center spacings.



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES 7/94

NOTES: A. Each pin centerline is located within 2,54 mm (0.1 inch) of its true longitudinal position.
B. The center of the package and the center of the image area are not coincident.
C. Maximum rotation is ±3.5°.