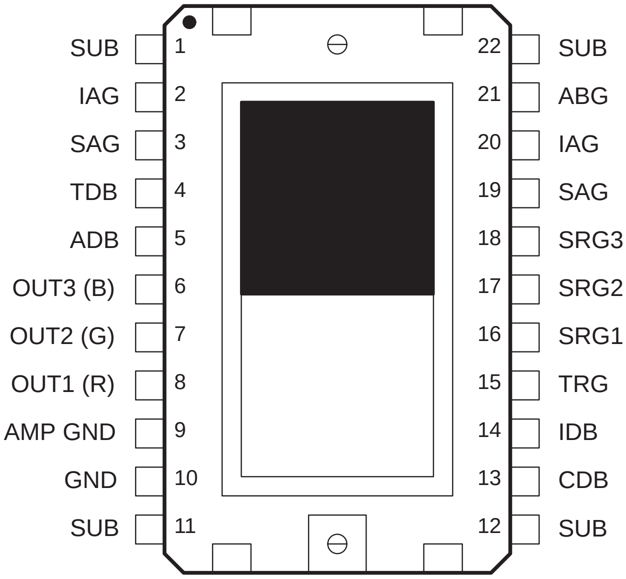
TC240
780- × 488-PIXEL CCD IMAGE SENSOR

SOCS005A – OCTOBER 1985 – REVISED DECEMBER 1991

- **High-Resolution, Solid-State Image Sensor for NTSC Color TV Applications**
- **11-mm Image-Area Diagonal, Compatible With 2/3” Vidicon Optics**
- **754 (H) x 244 (V) Active Elements in Image-Sensing Area**
- **Low Dark Current**
- **Electron-Hole Recombination Antiblooming**
- **Dynamic Range . . . More Than 60 dB**
- **High Sensitivity**
- **High Photoresponse Uniformity**
- **High Blue Response**
- **Single-Phase Clocking**
- **Separate Outputs for Each Color (RGB)**
- **Solid-State Reliability With No Image Burn-in, Residual Imaging, Image Distortion, Image Lag, or Microphonics**

DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The TC240 is a frame-transfer charge-coupled device (CCD) image sensor designed for use in single-chip color NTSC TV applications. The device is intended to replace a 2/3-inch vidicon tube in applications requiring small size, high reliability, and low cost.

The image-sensing area of the TC240 is configured into 244 lines with 780 elements in each line. Twenty-four elements are provided in each line for dark reference. The blooming protection incorporated into the sensor is based on recombining excess charge with charge of opposite polarity in the substrate. This antiblooming is activated by supplying clocking pulses to the antiblooming gate, an integral part of each image-sensing element.

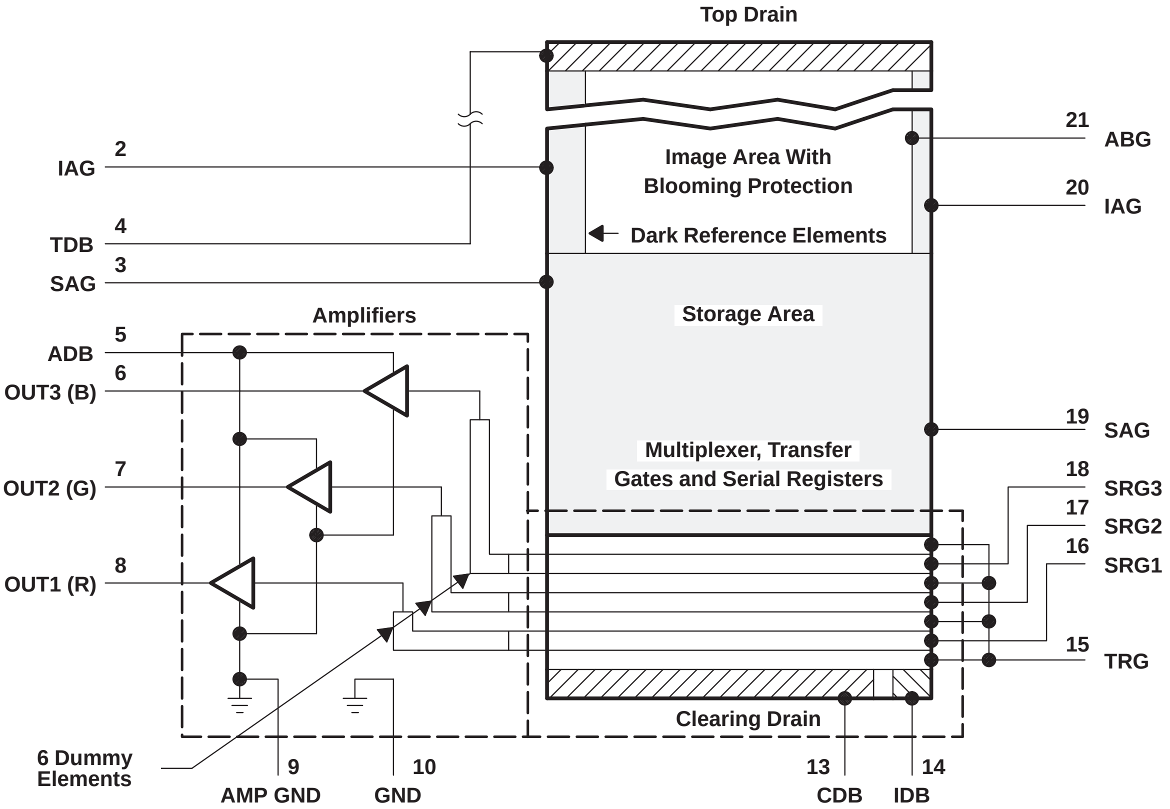
The sensor is designed to operate in an interlace mode, electronically displacing the image-sensing elements by one-half of a vertical line during the charge integration period in alternate fields, effectively increasing the vertical resolution and minimizing aliasing. The single-chip color-sensing capability of the TC240 is achieved by laminating a striped color filter with RGB organization on top of the image-sensing area. The stripes are precisely aligned to the sensing elements, and the signal charge columns are multiplexed during the readout into three separate registers with three separate outputs corresponding to each individual color.

A gated floating-diffusion detection structure with an automatic reset and voltage reference incorporated on chip converts charge to signal voltage. A low-noise, two-stage, source-follower amplifier buffers the output and provides high output-drive capability.

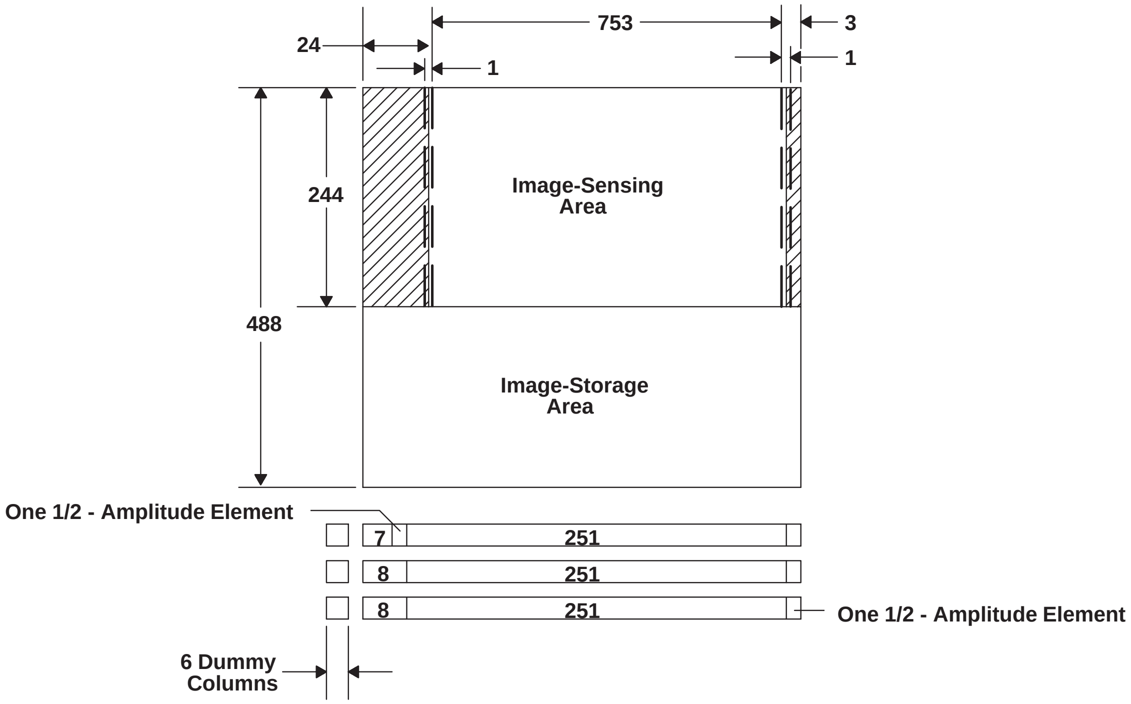
The TC240 is built using TI-proprietary virtual-phase technology, which provides devices with high blue response, low dark signal, good uniformity, and single-phase clocking. The TC240 is characterized for operation from –10°C to 45°C.

This MOS device contains limited built-in gate protection. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to SUB. Under no circumstances should pin voltages exceed absolute maximum ratings. Avoid shorting OUT to ADB during operation to prevent damage to the amplifier. The device can also be damaged if the output terminals are reverse-biased and an excessive current is allowed to flow. Specific guidelines for handling devices of this type are contained in the publication *Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies* available from Texas Instruments.

functional block diagram



sensor topology diagram



Terminal Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
ABG	21	I	Antiblooming gate
ADB	5	I	Supply voltage for amplifier-drain bias
AMP GND	9		Amplifier ground
CDB	13	I	Supply voltage for clearing-drain bias
GND	10		Ground
IAG†	2	I	Image-area gate
IAG†	20	I	Image-area gate
IDB	14	I	Supply voltage for input-diode bias
OUT1 (R)	8	O	Output signal 1
OUT2 (G)	7	O	Output signal 2
OUT3 (B)	6	O	Output signal 3
SAG†	3	I	Storage-area gate
SAG†	19	I	Storage-area gate
SRG1	16	I	Serial-register gate 1
SRG2	17	I	Serial-register gate 2
SRG3	18	I	Serial-register gate 3
SUB†	1		Substrate and clock return
SUB†	11		Substrate and clock return
SUB†	12		Substrate and clock return
SUB†	22		Substrate and clock return
TDB	4	I	Supply voltage for top-drain bias
TRG	15	I	Transfer gate

† All pins of the same name should be connected together externally.

detailed description

The TC240 consists of four basic functional blocks: (1) the image-sensing area, (2) the image-storage area, (3) the multiplexer with serial registers and transfer gates, and (4) the buffer amplifier with charge-detection nodes. Location of each of these blocks is shown in the functional block diagram.

image-sensing and storage areas

Cross sections with potential-well diagrams and top views of image-sensing and storage-area elements are shown in Figure 1 and Figure 2. As light enters the silicon in the image-sensing area, free electrons are generated and collected in the potential wells of the sensing elements. During this time, the antiblooming gate is activated by the application of a burst of pulses every horizontal blanking interval. This prevents blooming caused by the spilling of charge from overexposed elements into neighboring elements. After the completion of integration, the signal charge is transferred into the storage area. To generate the dark reference that is necessary in subsequent video processing circuits for restoration of the video black level, there are 23 full columns and one half-column of elements at the left edge of the image-sensing area that are shielded from incident light. Two full columns and one half-column of elements at the right of the image-sensing area are also shielded from incident light. Thus, the total number of elements per row is 780 (753 active elements plus 25 shielded elements and 2 transitional elements).

multiplexer with transfer gates and serial registers

The color sensitivity of the TC240 is obtained by laminating a color stripe filter on top of the image-sensing area and aligning it precisely with the vertical columns of sensing elements. This separates the columns into three groups corresponding to the red, green, and blue colors used in the filter. The function of the multiplexer and transfer gates is to transfer the charge line by line from each group of columns into the corresponding serial register and to prepare it for readout. Multiplexing is activated during the horizontal blanking interval by applying appropriate pulses to the transfer gates and serial registers. The required pulse timing is shown in Figure 3. A drain is included in this area to provide the capability to quickly clear the image-sensing and storage areas of unwanted charge. Such charge can accumulate in the imager during the start-up of operation or under special circumstances when nonstandard TV operation is desired.

buffer amplifier with charge-detection nodes

The buffer amplifier converts charge into a video signal. Figure 4 shows the circuit diagram of a charge-detection node and one of the three amplifiers. As charge is transferred into the detection node, the potential of this node changes in proportion to the amount of signal received. This change is sensed by an MOS transistor and, after proper buffering, the signal is supplied to the output terminal of the image sensor. After the potential change has been sensed, the node is reset to a reference voltage supplied by an on-chip reference generator. The reset is accomplished by a reset gate that is connected internally to the serial register. The detection nodes and corresponding amplifiers are located some distance away from the edge of the storage area; six dummy elements are used to span this distance. The location of the dummy elements is shown in the functional block diagram.

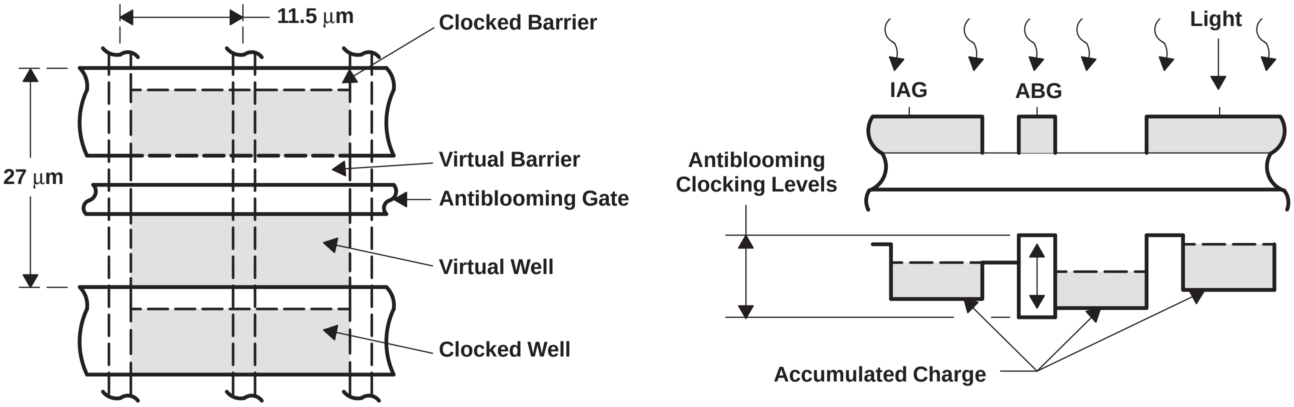


Figure 1. Charge-Accumulation Process

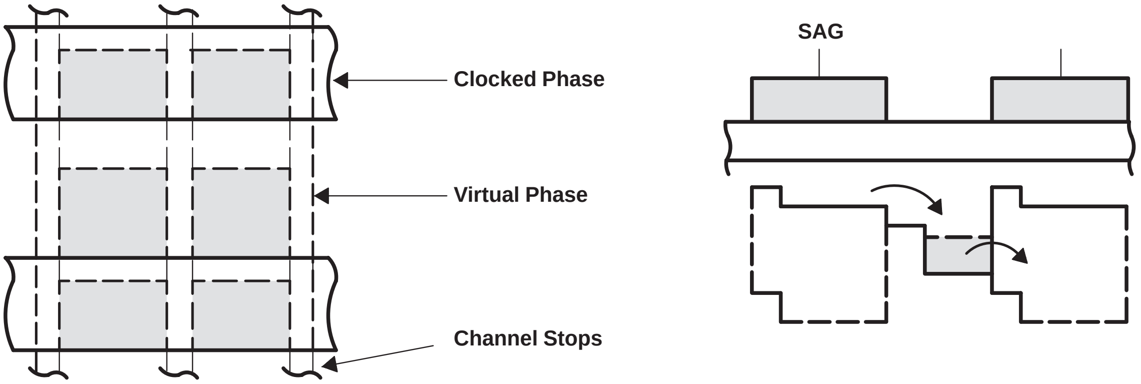


Figure 2. Charge-Transfer Process

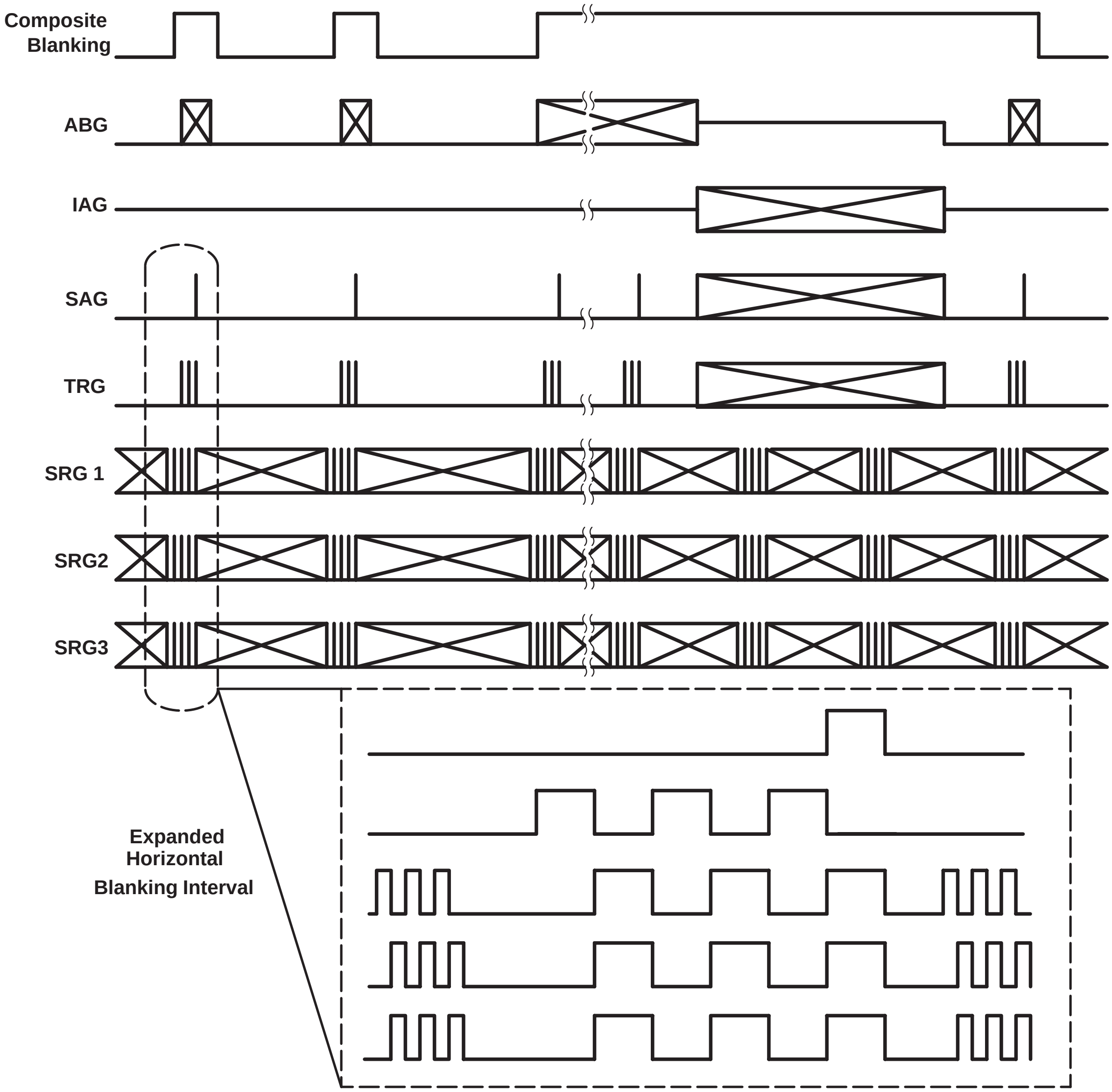


Figure 3. Timing Diagram

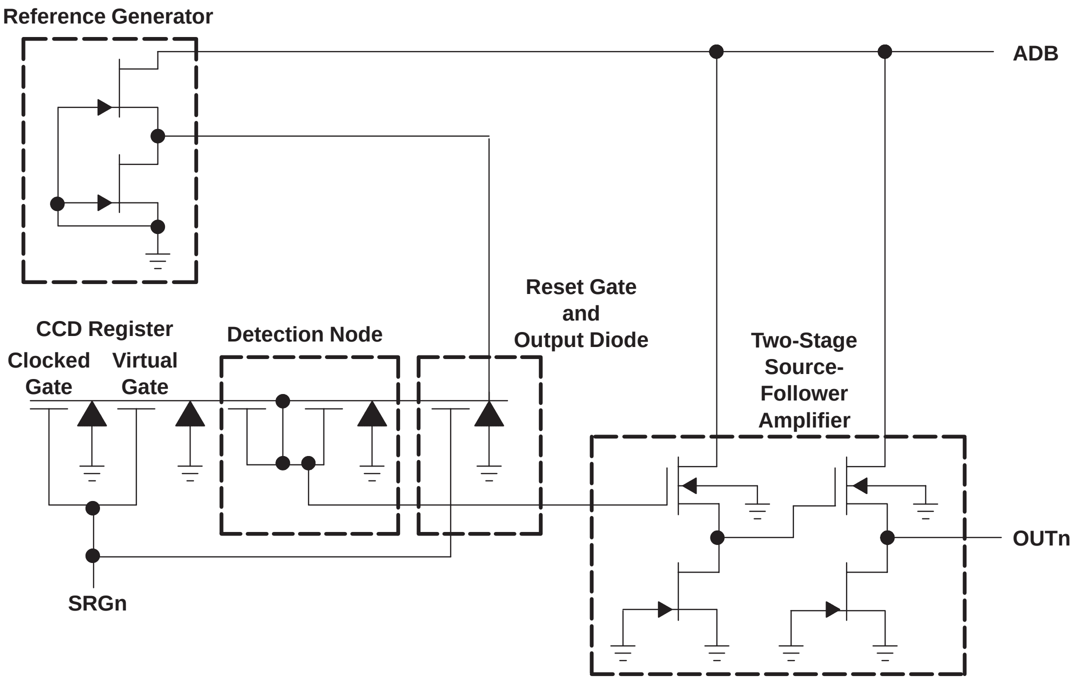


Figure 4. Buffer Amplifier and Charge Detection Node

spurious nonuniformity specification

The spurious nonuniformity specification of the TC240 CCD grades –10, –20, –30, and –40 is based on several sensor characteristics:

- Amplitude of the nonuniform pixel
- Polarity of the nonuniform pixel
  - Black
  - White
- Location of the nonuniformity (see Figure 5)
  - Area A
    - Element columns near horizontal center of the area
    - Element rows near vertical center of the area
  - Area B
    - Up to the pixel or line border
    - Up to Area A
  - Other
    - Edge of the imager
    - Up to Area B
- Nonuniform pixel count
- Distance between nonuniform pixels
- Column amplitude

The CCD sensors are characterized in both an illuminated condition and a dark condition. In the dark condition, the nonuniformity is specified in terms of absolute amplitude as shown in Figure 6. In the illuminated condition, the nonuniformity is specified as a percentage of the total illumination as shown in Figure 7.

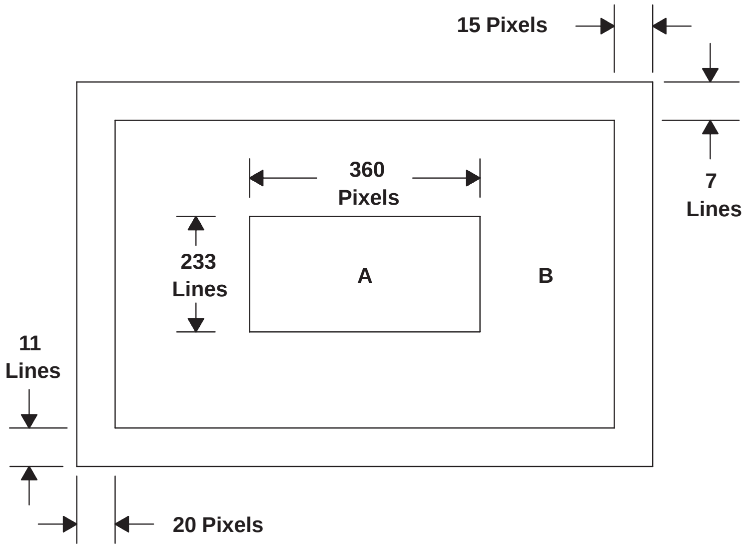


Figure 5. Sensor Area Map

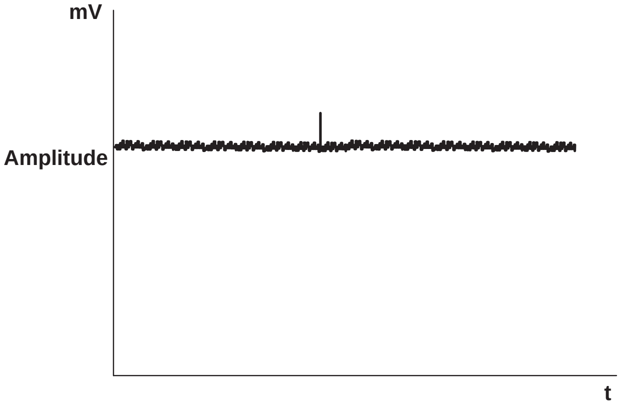


Figure 6. Pixel Nonuniformity, Dark Condition

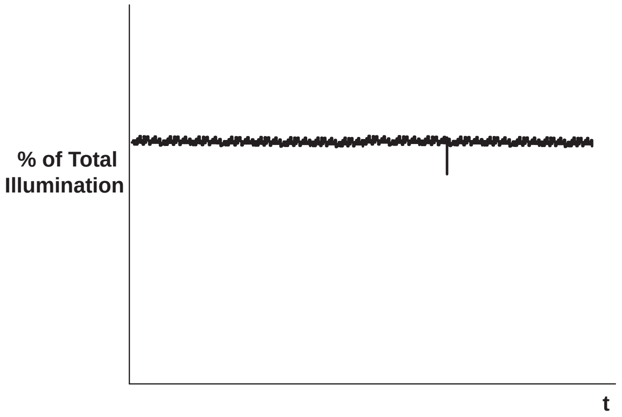


Figure 7. Pixel Nonuniformity, Illuminated Condition

The grade specification for the TC240 is as follows (CCD video output signal is 50 mV ±10 mV):

Pixel nonuniformity:

PART NUMBER	DARK CONDITION							ILLUMINATED CONDITION			TOTAL COUNT[‡]	DISTANCE SEPARATION		
	PIXEL AMPLITUDE, x (mV)	NONUNIFORM PIXEL TYPE						% OF TOTAL ILLUMINATION	AREA A	AREA B		X	Y	AREA
		WHITE		BLACK		W/B[†]								
		AREA		AREA		AREA								
		A	B	A	B	A	B							
TC240-10	x ≤ 2.5	2	5	2	5	2	5	x ≤ 5	2	5	10	150	100	A, B
	x > 2.5	0	0	0	0	0	0	x > 5	0	0				
TC240-20	x > 3.5	0	0	0	0	0	0	x > 5	0	0	—	—	—	—
TC240-30	2.5 < x ≤ 3.5	2	5	2	5	2	5	5 < x ≤ 7.5	2	5	12	100	80	A
	x > 3.5	0	0	0	0	0	0	x > 7.5	0	0				
TC240-40	3.5 < x ≤ 7	3	7	3	7	3	7	7.5 < x ≤ 15	3	7	15	—	—	—
	x > 7	0	0	0	0	0	0	x > 15	0	0				

[†] White and black nonuniform pixel pair

[‡] The total spot count is the sum of 1) the numbers of nonuniform white pixels, nonuniform black pixels, and nonuniform white/black pixel pairs while the sensor is in the dark condition and 2) the number of nonuniform black pixels while the sensor is in the illuminated condition. The total spot count will not exceed the values shown in this column.

Column nonuniformity:

PART NUMBER	COLUMN AMPLITUDE, x (mV)	WHITE AREAS A AND B	BLACK AREAS A AND B
TC240-10	x > 0.3	0	0
TC240-20	x > 0.3	0	0
TC240-30	x > 0.5	0	0
TC240-40	x > 0.7	0	0

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range for ADB, CDB, IDB, TDB (see Note 1)	0 V to 15 V
Input voltage range for ABG, IAG, SAG, SRG, TRG	–15 V to 15 V
Operating free-air temperature range	–30°C to 85°C
Storage temperature range	–30°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the substrate terminal.

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply voltage, ADB, CDB, IDB, TDB			11	12	13	V
Substrate bias voltage				0		V
Input voltage, V_I[‡]	IAG	High level	1.5	2	2.5	V
		Intermediate level[§]		–5		
		Low level	–10	–9	–8	
	SRG (1, 2, 3)	High level	1.5	2	2.5	
		Low level	–10	–9	–8	
	ABG	High level	2	4	6	
		Intermediate level[§]		–2.5		
		Low level		–7		
	SAG	High level	1.5	2	2.5	
		Low level	–10	–9	–8	
	TRG	High level	1.5	2	2.5	
		Low level	–10	–9	–8	
Clock frequency, f_{clock}	IAG, SAG				2.05	MHz
	SRG, TRG				4.77	
	ABG				2.05	
Capacitive load	OUT1 (R), OUT2 (G), OUT3 (B)				8	pF
Operating free-air temperature, T_A			–10		45	°C

[‡] The algebraic convention, in which the least-positive (most negative) value is designated minimum, is used in this data sheet for clock voltage levels.

[§] Adjustment is required for optimal performance.

electrical characteristics over recommended operating range of supply voltage, $T_A = -10°C$ to $45°C$

PARAMETER		MIN	TYP†	MAX	UNIT
Dynamic range (see Note 2)	Antiblooming disabled (see Note 3)	60			dB
Charge conversion factor		1.4	1.6	1.8	μV/e
Charge transfer efficiency (see Note 4)		0.9999	0.99995		
Signal response delay time, τ (see Note 5 and Figure 11)		18	20	22	ns
Gamma (see Note 6)		0.97	0.98		
Output resistance			700	800	Ω
Noise voltage	1/f noise (5 kHz)		0.13		$\mu V/\sqrt{HZ}$
	Random noise (f = 100 kHz)		0.11		
Noise equivalent signal			120		electrons
Rejection ratio at 4.77 MHz	ADB (see Note 7)		20		dB
	SRG_n (see Note 8)		40		
	ABG (see Note 9)		20		
Supply current			5		mA
Input capacitance, C_i	IAG		12000		pF
	SRG 1, 2, 3		120		
	ABG		4000		
	TRG		350		
	SAG		14000		

† All typical values are at $T_A = 25°C$.

NOTES: 2. Dynamic range is –20 times the logarithm of the mean noise signal divided by the saturation output signal.
3. For this test, the antiblooming gate must be biased at the intermediate level.
4. Charge transfer efficiency is one minus the charge loss per transfer in the output register. The test is performed in the dark using an electrical input signal.
5. Signal response delay time is the time between the falling edge of the SRG clock pulse and the output signal valid state.
6. Gamma (γ) is the value of the exponent in the equation below for two points on the linear portion of the transfer function curve (this value represents points near saturation):

$$\left(\frac{\text{Exposure (2)}}{\text{Exposure (1)}}\right)^{\gamma} = \left(\frac{\text{Output signal (2)}}{\text{Output signal (1)}}\right)$$

7. ADB rejection ratio is –20 times the logarithm of the ac amplitude at the output divided by the ac amplitude at ADB.
8. SRG_n rejection ratio is –20 times the logarithm of the ac amplitude at the output divided by the ac amplitude at SRG_n.
9. ABG rejection ratio is –20 times the logarithm of the ac amplitude at the output divided by the ac amplitude at ABG.

optical characteristics, T_A = 40°C and integration time = 16.67 ms (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
Sensitivity	Red	Measured at V_U (see Notes 10 and 11)		120		mV/lx
	Green			0.9		mV
	Blue			0.6		
Saturation signal, V_{sat} (see Note 12)	Antiblooming disabled, interlace off		320	400		mV
Maximum usable signal, V_{use}	Antiblooming enabled, interlace on		180	360		mV
Blooming overload ratio (see Note 13)		Interlace on	100			
		Interlace off	200			
Image-area well capacity				200 x 10^3		electrons
Smear (see Note 14)		See Note 15		0.00072		
Dark current	Interlace off	T_A = 21°C		0.027		nA/cm^2
Dark signal (see Note 16)	T_A = 45°C	TC240-10			15	mV
		TC240-30			15	
		TC240-40			20	
Pixel uniformity	Output signal = 50 mV ±10 mV	TC240-10			2.5	mV
		TC240-30			3.5	
		TC240-40			5	
Column uniformity	Output signal = 50 mV ±10 mV	TC240-10			0.3	mV
		TC240-30			0.5	
		TC240-40			0.7	
Shading	Output signal = 100 mV				17%	

NOTES: 10. The following standard imaging condition is used in the test: light box SA702 (made by Canon) is used with a lens (FL = 92 mm) stopped to f14.3. The light power is 1.5 µW/cm^2 (color temperature = 3000 K). No IR filter is used.

11. V_U is the output voltage that represents the threshold of operation of antiblooming. $V_U \approx 1/2$ saturation signal.

12. Saturation is the condition in which further increase in exposure does not lead to further increase in output signal.

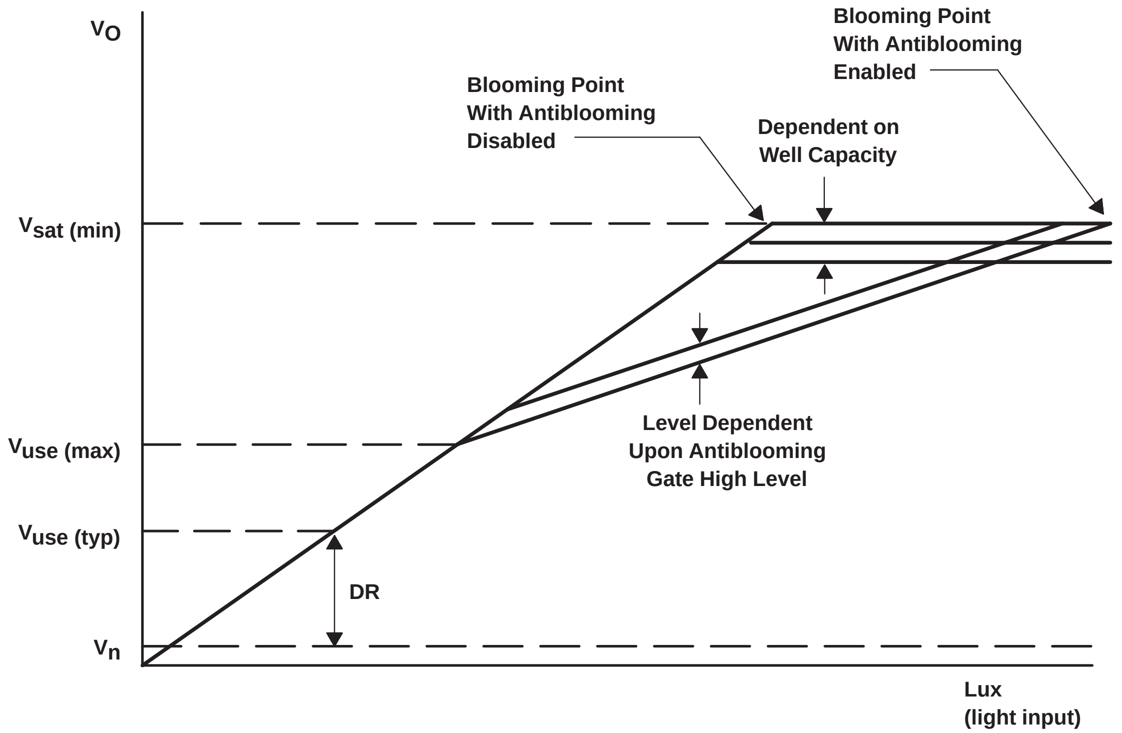
13. Blooming overload ratio is the ratio of blooming exposure to saturation exposure.

14. Smear is a measure of the error induced by transferring charge through an illuminated pixel in shutterless operation. It is equivalent to the ratio of the single-pixel transfer time during a fast dump to the exposure time using an illuminated section that is 1/10 of the image- area vertical height with recommended clock frequencies.

15. Exposure time is 16.67 ms and the fast dump clocking rate during vertical timing is 2.05 MHz.

16. Dark signal level is measured from the dummy pixels.

PARAMETER MEASUREMENT INFORMATION



$$\text{DR (dynamic range)} = \frac{\text{camera white clip voltage}}{V_n}$$

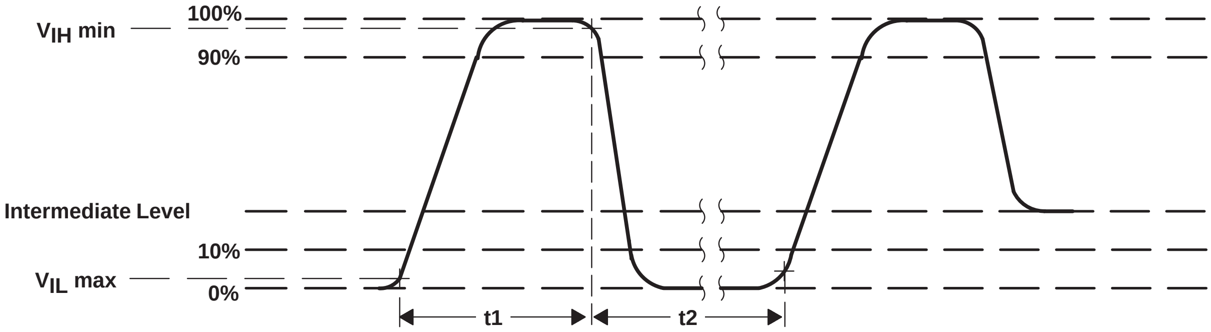
V_n = noise floor voltage
$V_{sat\ (min)}$ = minimum saturation voltage
$V_{use\ (max)}$ = maximum usable voltage
$V_{use\ (typ)}$ = typical user voltage (camera white clip)

NOTES: A. $V_{use\ (typ)}$ is defined as the voltage determined to equal the camera white clip. This voltage must be less than $V_{use\ (max)}$.

B. A system trade-off is necessary to determine the system light sensitivity versus the signal/noise ratio. By lowering the $V_{use\ (typ)}$, the light sensitivity of the camera is increased; however, this sacrifices the signal/noise ratio of the camera.

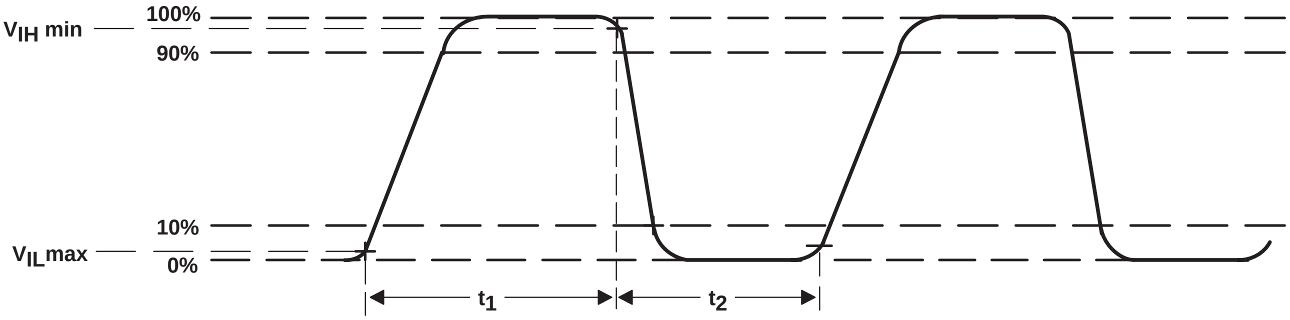
Figure 8. Typical V_{sat}, V_{use} Relationship

PARAMETER MEASUREMENT INFORMATION



Slew rate between 10% and 90% = 70 to 120 V/µs
Ratio t1 : t2 at 2 MHz = 4:3
Ratio t1 : t2 at 1 MHz = 1:1

Figure 9. Typical Clock Waveform for ABG, IAG, and SAG



Slew rate between 10% and 90% = 300 V/µs
Ratio t1 : t2 = 1:1

Figure 10. Typical Clock Waveform for SRG1, SRG2, SRG3, and TRG

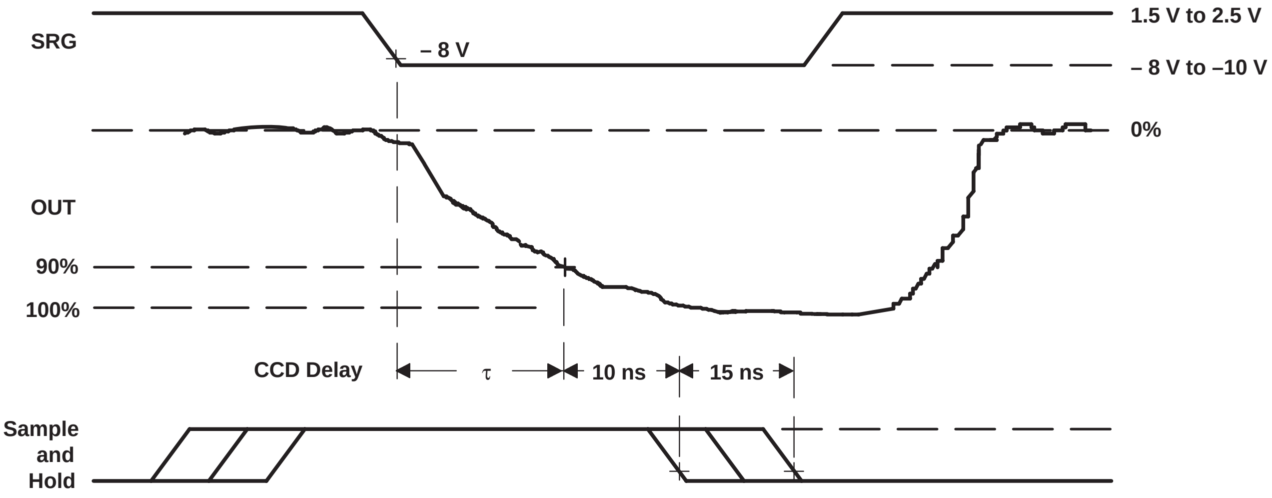


Figure 11. SRG and CCD Output Waveforms

TYPICAL CHARACTERISTICS

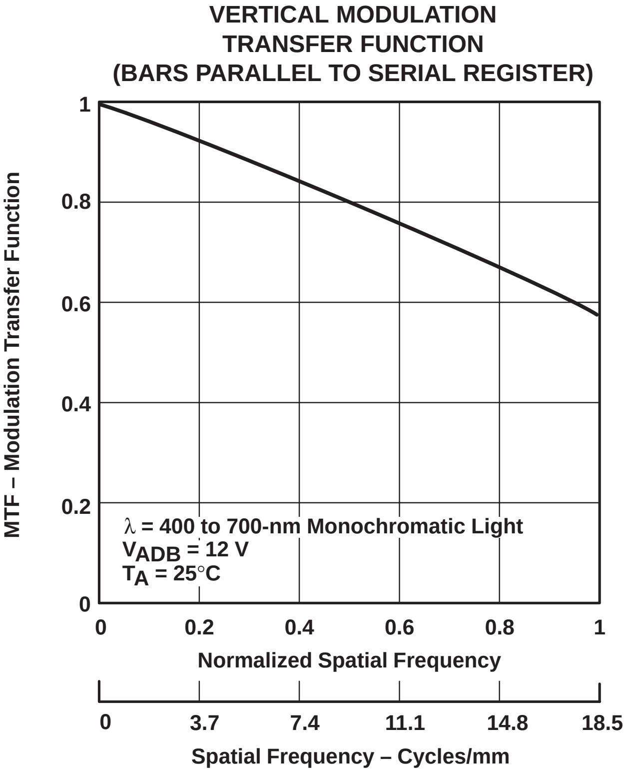


Figure 12

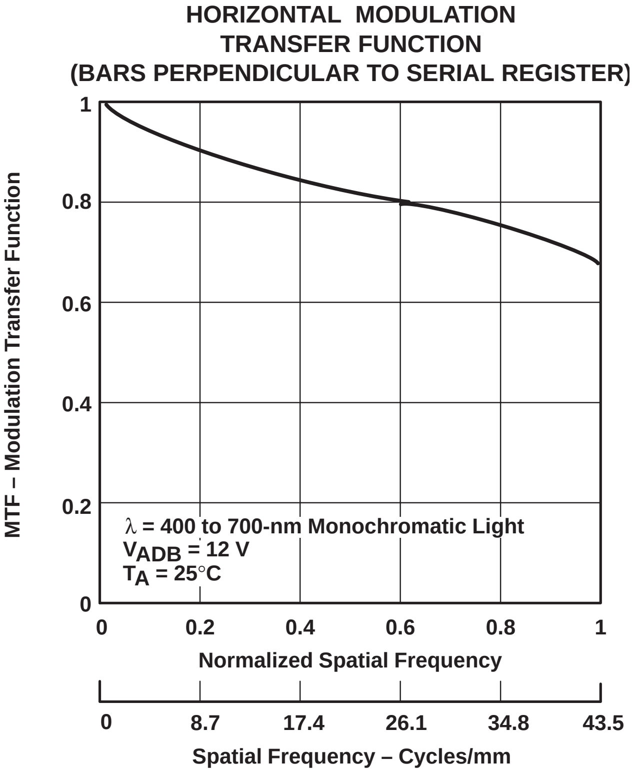


Figure 13

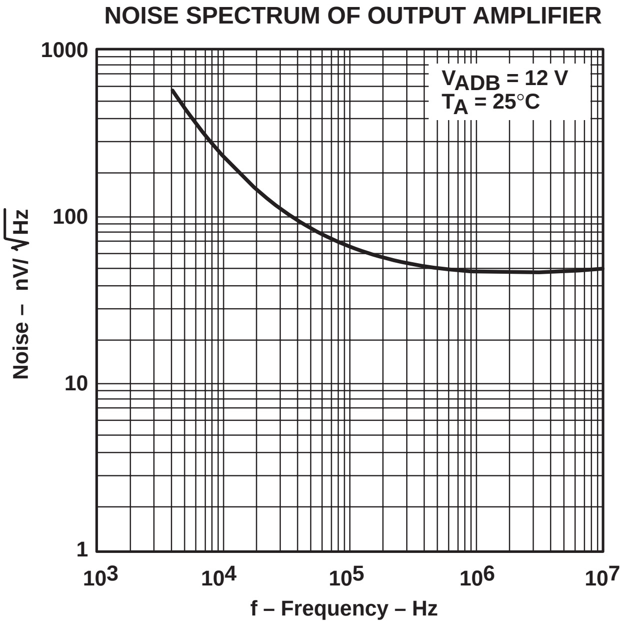


Figure 14

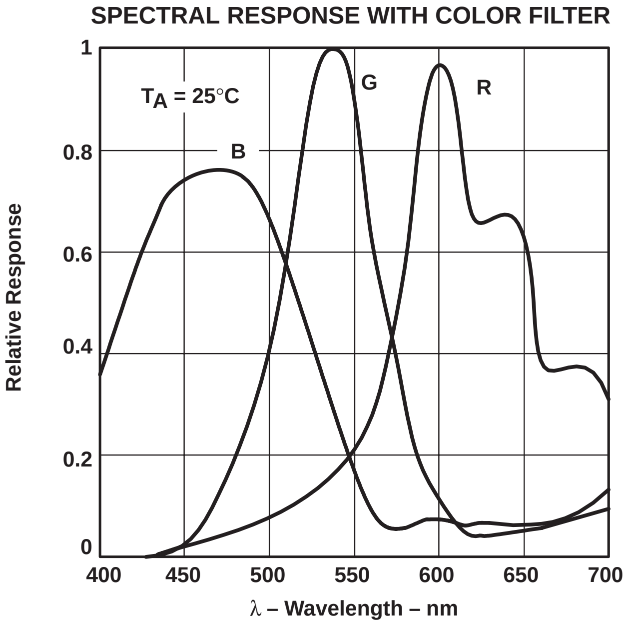


Figure 15

TYPICAL CHARACTERISTICS

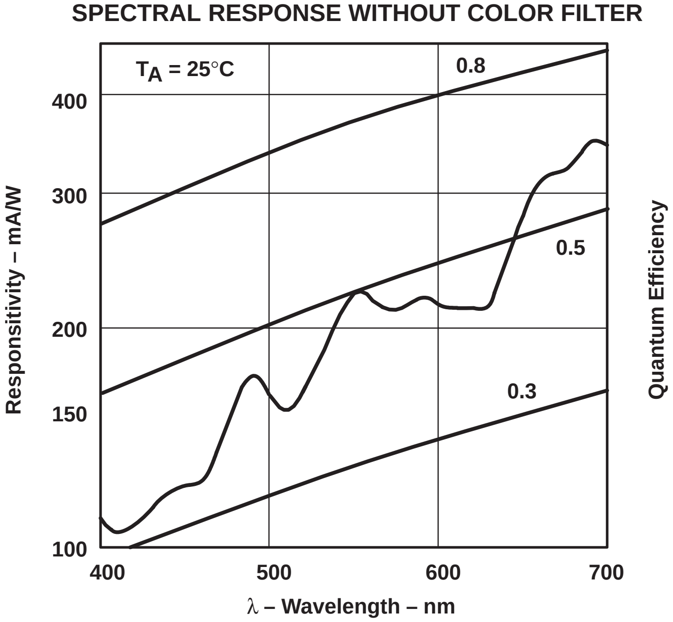
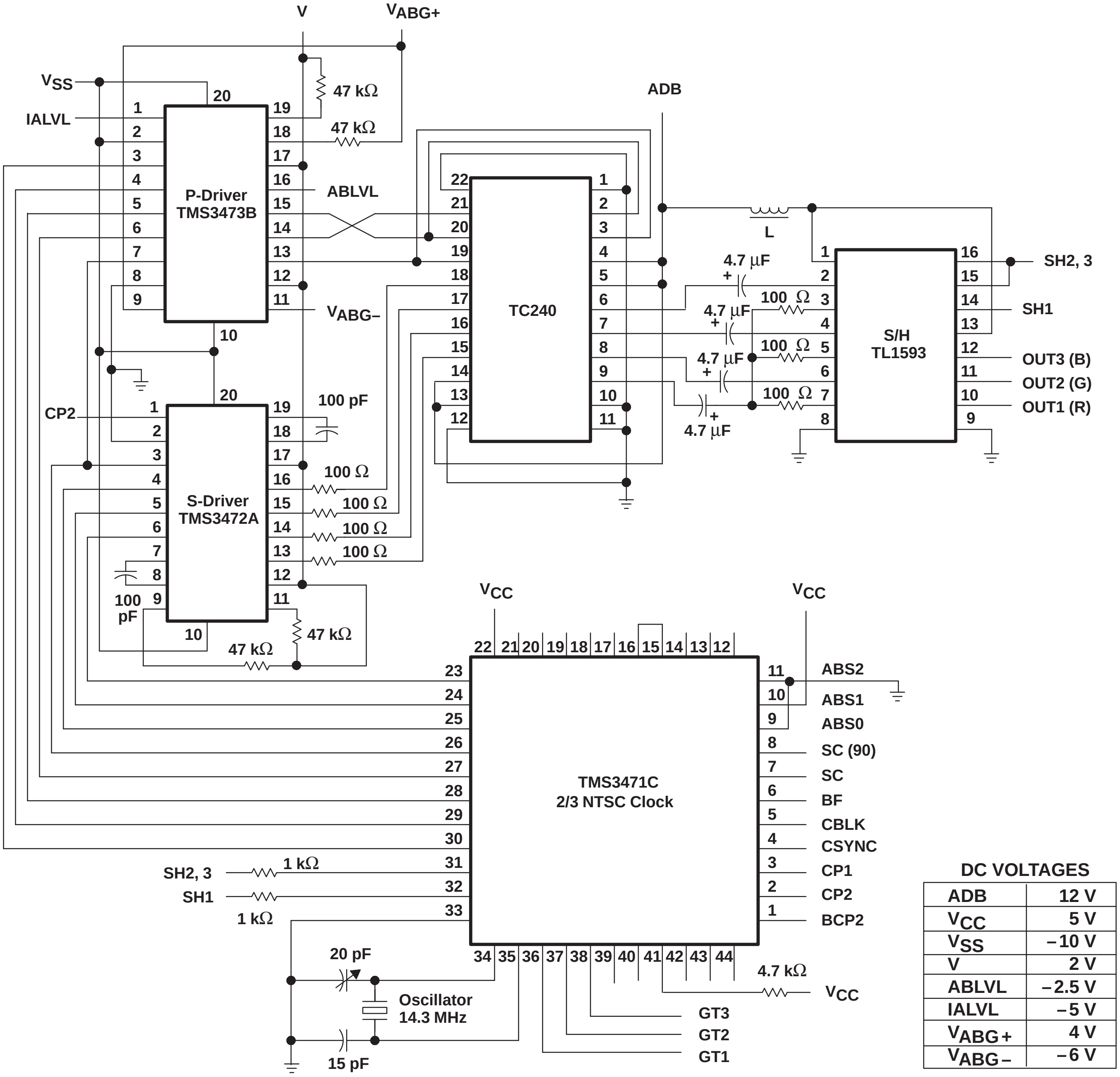


Figure 16

APPLICATION INFORMATION



DC VOLTAGES	
ADB	12 V
V_{CC}	5 V
V_{SS}	–10 V
V	2 V
ABLVL	–2.5 V
IALVL	–5 V
V_{ABG+}	4 V
$V_{ABG–}$	–6 V

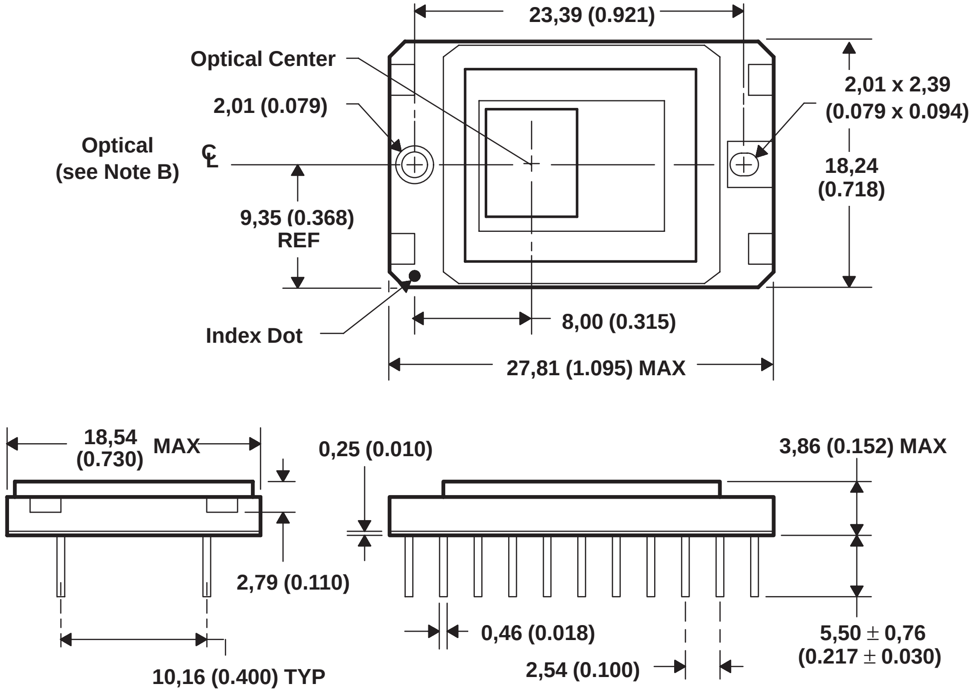
SUPPORT CIRCUITS			
DEVICE	PACKAGE	APPLICATION	FUNCTION
TMS3471CFS	44-pin flat pack	Timing generator	NTSC timing generator
TMS3472AKL	20-pin flat pack with tabs	Serial driver	Driver for TRG, SRG1, SRG2, and SRG3
TMS3473BDW	20-pin small-outline package	Parallel driver	Driver for IAG, SAG, and ABG
TL1593CNS	16-pin SO (EIAJ)	Sample and hold	Three-channel sample-and-hold IC

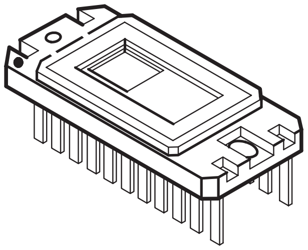
Figure 17. Typical Application Circuit Diagram

MECHANICAL DATA

The package for the TC240 consists of a ceramic base, a glass window, and a 22-lead frame. The glass window is sealed to the package by an epoxy adhesive. The package leads are configured in a dual in-line organization and fit into mounting holes with 2.54 mm (0.10 inch) center-to-center spacings.

TC240 (22-pin)





ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES:
- A. Single dimensions are nominal.
- B. The center of the package and the center of the image area are not coincident.
- C. The distance from the top of the glass to the image sensor surface is typically 1,46 mm (0.057 inch). The glass is 0,95 ±0,08 mm and has an index of refraction of 1.53.
- D. Each pin centerline is located within 0,25 mm (0.010 inch) of its true longitudinal position.

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

Copyright © 1998, Texas Instruments Incorporated