Sundance Technology

TC9021

Triple Speed Ethernet MAC

Features

- **IEEE 802.3z compliant MAC supporting full wire speed at 1Gbps**
- **1000Mbps, 100Mbps, and 10Mbps triple speed support**
- **GMII, MII or TBI interface with integrated 1000BASE-X PCS with Auto-Negotiation**
- **Half duplex carrier extension and packet bursting**
- **Symmetrical and asymmetrical flow control support**
- **v2.2 compliant 32/64-bit, 33/66MHz PCI bus master**
- **Scatter/gather DMA capable of 1Gbps transaction**
- **TCP/UDP/IP checksum offloading**
- **Adaptive interrupt coalescing**
- **Supports "interrupt-less" transmit operation**
- **Support for IEEE 802.1p prioritizing via priority queuing and interrupts**
- **Extensive IEEE 802.1Q VLAN support**
- **Jumbo frame support**
- **Rich statistic register set**
- **Provides a variety of flexible receive filtering modes, including VLAN, IP multicast, and hash table**
- **On-chip transmit and receive FIFO buffers for cost effective applications**
- **Flash ROM interface for remote network boot**
- **ACPI and WakeOnLAN support**
- **Windows NT 4.0, Windows 9x, Windows 2000, Novell Netware 4.x/5.x, Linux 2.x**
- **Low power 2.5/3.3V CMOS design with 5V tolerant I/O**
- **0.25um CMOS technology**
- **208-pin PQFP**

Functional Description

Sundance Technology's TC9021 is part of a new generation of high performance, host-optimized network interface cards designed for mission critical systems such as servers and high-end workstations. Offering two gigabits per second of aggregate bandwidth, the TC9021 optimizes performance while minimizing network overhead on the host system. Compared to leading Fast Ethernet solutions, the TC9021 transfers data at less than one tenth of the host CPU utilization rate.

IEEE 802.3z Gigabit Ethernet MAC

The TC9021 implements IEEE 802.3z half duplex functions such as Carrier Extension and Packet Bursting. In full duplex mode, the TC9021 implements both symmetrical and asymmetrical flow control via IEEE 802.3x PAUSE MAC Control frames. PAUSE frames can be automatically generated by the TC9021 according to programmable flow control thresholds within the on-chip receive FIFO. The TC9021 MAC has been carefully implemented to ensure full wire speed at 1Gbps with 96-bit transmit and 64-bit receive inter-frame spacing.

GMII, MII and TBI Interface

The TC9021 implements both a GMII and MII interface, which offers a simple, cost-effective migration from Fast Ethernet networks to high-speed Gigabit Ethernet networks over existing Category 5 cabling. For fiber optics applications, the TC9021 implements an IEEE 802.3z 1000BASE-X Physical Coding Sublayer (PCS). The PCS includes an 8B10B encoder and decoder, Auto-Negotiation, and Ten Bit Interface (TBI). With the industry standard SERDES devices, the TC9021 allows for gigabit optical link connections to the host system.

32/64-bit, 33/66MHz PCI Bus

The TC9021 can operate in systems utilizing a 32-bit or 64-bit wide PCI bus running at 33MHz or 66 MHz. The TC9021 is compliant with PCI specification revision 2.2, and is capable of accessing up to 1 terabytes of system memory via the PCI Dual Address Cycle (DAC) command. Advanced PCI commands, such as Write and Invalidate, Read Line, and Read Multiple, are also implemented to further improve system performance.

Bus Master Dual Channel DMA

The TC9021 implements independent scatter/gather DMA engines to support full duplex Gigabit Ethernet connectivity. These two DMA engines are capable of accessing data on any byte boundary and moving data to and from discontiguous memory locations. This capability

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eliminates CPU-intensive data copying. Furthermore, each DMA engine has been carefully designed to sustain well over 1 gigabit per second of throughput across a PCI bus. This ensures that the TC9021 will not be a bottleneck in high performance data networking applications.

Protocol Offloading

The TC9021 also off-loads network protocol tasks from the host CPU. It generates TCP, UDP and IP checksum values for outgoing frames and verifies the checksum value on incoming frames. Ethernet MAC frame CRC calculation is also implemented on-chip.

Interrupt Coalescence

While receiving frames, the TC9021 can be configured to operate with adaptive interrupts to maximize the host CPU efficiency. For heavy traffic, the TC9021 issues a single interrupt for a series of back-to-back receive frames which reduces CPU interrupt overhead significantly. For light traffic, the TC9021 issues an interrupt when a frame arrives to minimize the latency. On the transmit side, the frequency of interrupt is programmable on a frame by frame basis. An “interrupt-less’ transmit operation is provided to further reduce interrupt to the host CPU.

IEEE 802.1p Priority Support

The TC9021 supports transmit packet priority queuing, allowing the host to insert higher priority frames into the front of the transmit queue for lower latency transfer. The TC9021 also examines the IEEE standard priority field of appropriately tagged receive frames and generates a host system interrupt according to a user programmable priority threshold. This mechanism provides immediate notification to the host of high priority frame arrivals.

IEEE 802.1Q VLAN Support

The TC9021 can be programmed to insert VLAN tags automatically into outgoing frames on a global or individual frame basis. On the receive side, the TC9021 examines all incoming frames for 802.1Q compliant VLAN tags. Once a VLAN tag is detected, the TC9021 will optionally remove the VLAN tag before uploading the frame into system memory. The TC9021 also offers a receive filtering mode based on either a VLAN ID exact or hashed match.

Jumbo Frame Support

The TC9021 can be configured to use a maximum frame size of up to 9,018 bytes. This Jumbo Frame size reduces packet processing overhead on the host CPU by as much as 85 percent. In systems that are CPU bound, it can provide for layer 4 throughput increases of greater than 100%.

Network Management

The TC9021 implements management statistic counters based on IEEE 802.3 MIB and IETF RMON statistic register sets.

Power Management

The TC9021 is fully compliant with PCI Power Management v1.1 and ACPI Power Management specification v1.0. It implements multiple wakeup events including Wakeup Packets, Magic Packets, and Link Status change. The TC9021 also supports legacy Wake-On-LAN and Magic Packet power management mechanisms.

Advanced ASIC Technology

The TC9021 integrates value added capabilities such as dual DMA engines, a 64-bit 66MHz PCI bus interface, and a Gigabit Ethernet MAC with integrated 1000BASE-X PCS. This high level of integration enables the TC9021 to support numerous high performance, cost effective networking applications. The TC9021 also integrates large on-chip data buffers, eliminating the need for external memory and further reducing system cost.