



Trident II

Features

- Memory complement:
 - DSP: 20K x 16 RAM, 144K x 16 mask-programmable ROM.
 - *ARM*^{*}: 4K x 32 mask-programmable ROM, 2K x 32 RAM (byte writable).
 - Processor interface memory: 512 x 16 shared RAM.
- DSP peripherals:
 - Timer.
 - Bit input/output unit (BIO).
 - JTAG.
 - CSP interface.
 - Hardware development system (HDS).
 - 16 software patch registers.
- *ARM* peripherals:
 - External memory interface (EMI).
 - 24 address lines.
 - 6 chip select lines.
 - Programmable interrupt controller (PIC).
 - Reset/power/clock unit.
 - DMA controller.
 - Test interface controller (TIC).
 - Peripheral bridge.
 - Programmable peripheral interface (PPI).
 - Synchronous serial interface (SSI).
 - Two asynchronous communications controllers (ACCs), one with IrDA.
 - Timer.
 - Analog-to-digital converter (A/D).
 - Real-time clock (RTC).
 - One smartcard.
 - Keyboard interface.
 - One SIM multiplexed with an additional smartcard.
- Package: 196-pin FSBGA.
- Operating voltage:
 - Internal circuitry: 1.8 V $\pm$ 5% (except RTC and ADC).
 - I/O buffers, RTC, and ADC: 3.0 V $\pm$ 10%.
- On-chip, programmable PLL clock synthesizer for both DSP and *ARM* cores.
- Speed:
 - DSP: 60 MHz at minimum operating voltage.
 - *ARM*: 26 MHz at minimum operating voltage.
- Power consumption:
 - DSP: 440 μ A/MHz at 1.8 V.
 - *ARM*: 250 μ A/MHz at 1.8 V.
- Temperature:
 - Ambient: -40 °C—+85 °C.
 - Storage: -65 °C—+150 °C.
- Flexible power management modes for both DSP and *ARM* processors.
- Separate *IEEE*[†] P1149.1 test ports for DSP and *ARM* sections.

Description

Trident is a platform designed for wireless terminals. It is composed of several major blocks: a DSP block using the DSP16000 core and peripherals, a CP block using the ARM7TDMI microcontroller core and peripherals, an ICP/IDP block for communication between the DSP and the CP, and a standard set of peripherals for the DSP and *ARM*. Figure 1 contains a block diagram of the Trident.

* *ARM* is a trademark of Advanced RISC Machines Limited.

† *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.

Description (continued)

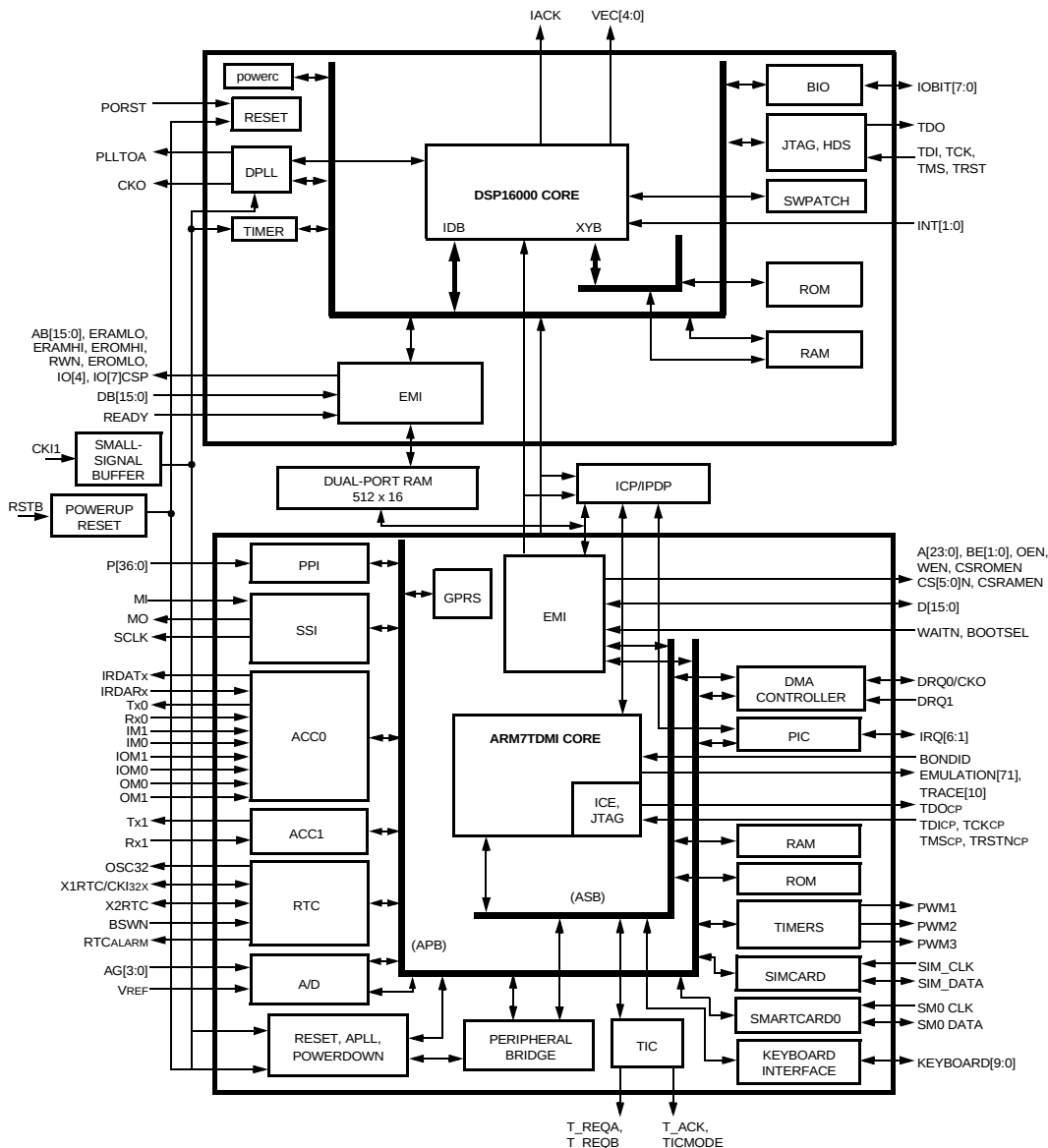


Figure 1. Trident II Block Diagram

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