Product Brief
May 2001

T8538B Quad Programmable Codec

Features

- 3.3 V operation
- Per-channel programmable gains, equalization, termination impedance, and hybrid balance
- Programmable μ-law, linear, or A-law modes
  — Up to 256 time slots per frame
  — Supports PCM data rates of 512 kbits/s to 16.384 Mbits/s
  — Double-clock mode timing compatible with ISDN standard interfaces
- Fully programmable time-slot assignment with bit offset
- Analog and digital loopback test modes
- Serial microprocessor interface
  — Normal and byte-by-byte control modes
  — Fast scan mode
- Six bidirectional control leads per channel, for SLIC and line card function control
- Differential analog output
  — Mates directly to SLICs, eliminating external components
- Sigma-delta converters with dither noise reduction
- Quad design to minimize package count on dense line card applications
- Meets or exceeds ITU-T G.711—G.712 and relevant *Telcordia Technologies** requirements

Description

The device consists of four independent channels of codec and digital signal processing functions on one chip. In addition to the classic A-to-D and D-to-A conversion, each channel provides termination impedance synthesis and a hybrid balance network.

The device is controlled by a serial microprocessor interface, and a series of bidirectional I/O leads are provided so that this control mechanism can be utilized to operate the battery feed device, ringing voltage switches, etc. Common data and clock paths can be shared over any number of devices. All the filter coefficients, signal processing, SLIC, and test features are accessible through this interface. This serial interface can be operated at speeds up to 16 Mbits/s.

The choice of a PCM bus is also programmable, with any channel capable of being assigned to any time slot. The PCM bus can be operated at speeds up to 16.384 Mbits/s, allowing for a maximum of 256 time slots. Separate transmit and receive interfaces are available for 4-wire bus designs, or they can be strapped together for a 2-wire PCM bus.

The device is available in two packages.

The T8538B 64-pin TQFP features five data latches per channel and the 100-pin TQFP features six data latches per channel.

Both devices are pin-compatible with the T8536B 5 V Quad Programmable Codecs.

* *Telcordia Technologies* is a trademark of Telcordia Technologies, Inc.

General Description

Refer to Figure 1 for the following discussion.

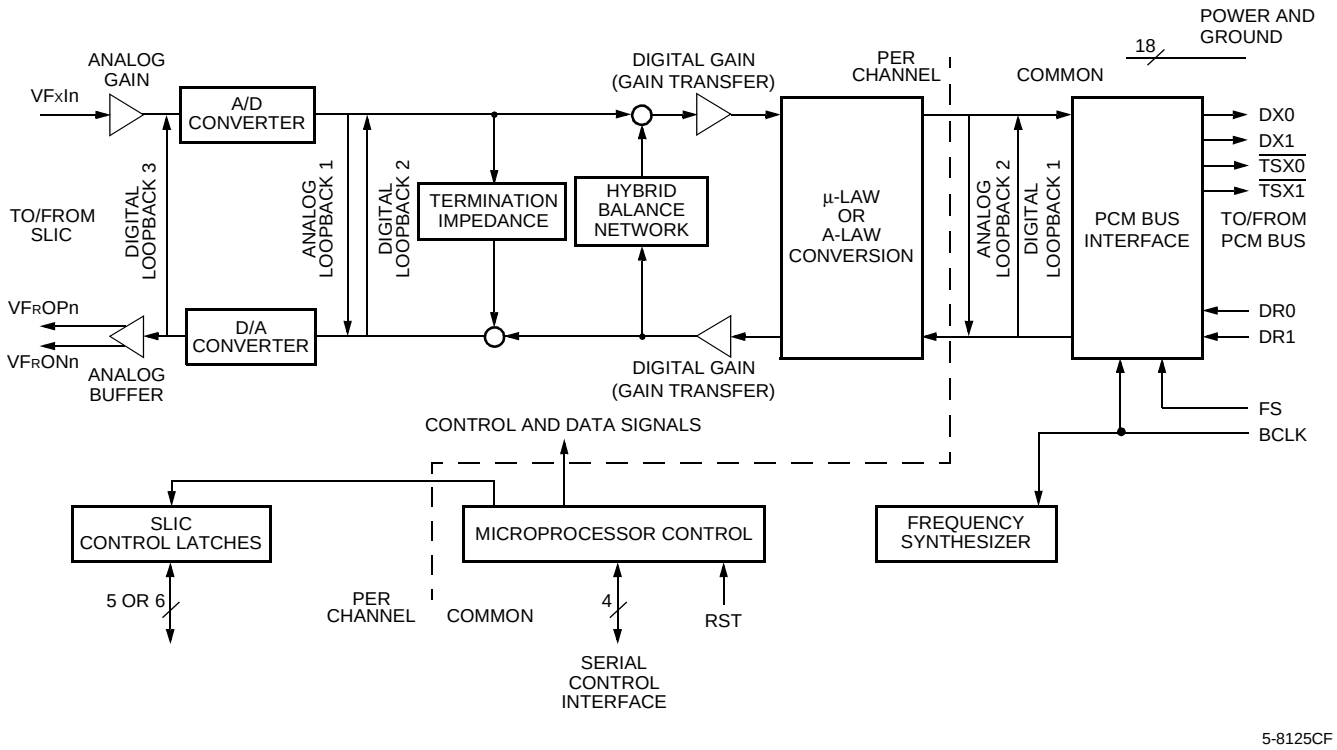

Figure 1. Functional Block Diagram, Each Section

This device performs virtually all the signal processing functions associated with a central office line termination. Functionality includes line termination impedance synthesis, fixed hybrid balance impedance synthesis, and level conversion both in the analog sense to accommodate various subscriber line interface circuits (SLICs) and in the digital sense for adjustment of the levels on the PCM bus. In general, the termination impedance synthesis generates the equivalent of a circuit with the parallel combination of a capacitor and a resistor in series with a resistor or the parallel combination of a resistor and the series combination of a resistor and capacitor. These general forms of impedance characteristic will satisfy most of the requirements specified throughout the world. Programmable selection of either μ-law or A-law encoding further aids worldwide deployment. All coefficients used in the filtering algorithms can be computed off-line in advance and downloaded to the device at the time of powerup. All signal processing is contained within the device, and there are only three interfaces of consequence to the system designer: the SLIC interface, the PCM interface, and the control interface.

The SLIC interface is designed to be flexible and convenient to use with a variety of SLIC circuits. With an appropriate choice of SLIC, few external components are required in the interface.

General Description (continued)

The PCM bus interface is flexible in that it allows, independently, the transmit and receive data for any channel to be placed in any time slot. The bus can be operated at a maximum 16.384 Mbits/s rate to accommodate a maximum 256 time slots. Separate pins are provided for each direction of transmission to allow 4-wire bus operation. The frame strobe signal is an 8 kHz signal that defines the beginning of the frame structure for all four channels. The interface will count 8 bits per time slot and insert or read the data for each channel as programmed. Lower speeds of the PCM bus are allowed. The PCM clock must be synchronous with the frame strobe signal.

The microprocessor control interface is a serial interface that uses the classical chip select type of operation. The interface controls the device by writing or reading various internal addresses. The command set consists of simple read and write operations, with the address determining the effect. All the memory locations, including the per-chip functions, are organized by channel.

There are several test modes included to facilitate confirmation of correct operation. In the signal path, two analog and three digital loopback tests are available, while in the microprocessor interface, there is a write/read test mode that tests the operation of the memory. Use of external test access switches allows a complete test of the signal path through the line card so that correct operation of various operational modes can be verified.

Applications

The following reference circuit shows a complete schematic for interfacing to the Agere L9215G SLIC. All ac parameters are programmed by the T8538B. Note that this implementation differentiates itself in that no external components are required in the ac interface to provide a dc termination impedance or for stability. For illustration purposes, 0.5 Vrms PPM injection was assumed in this example and no meter pulse rejection is used. Also, this example illustrates the device using programmable overhead and current limit.

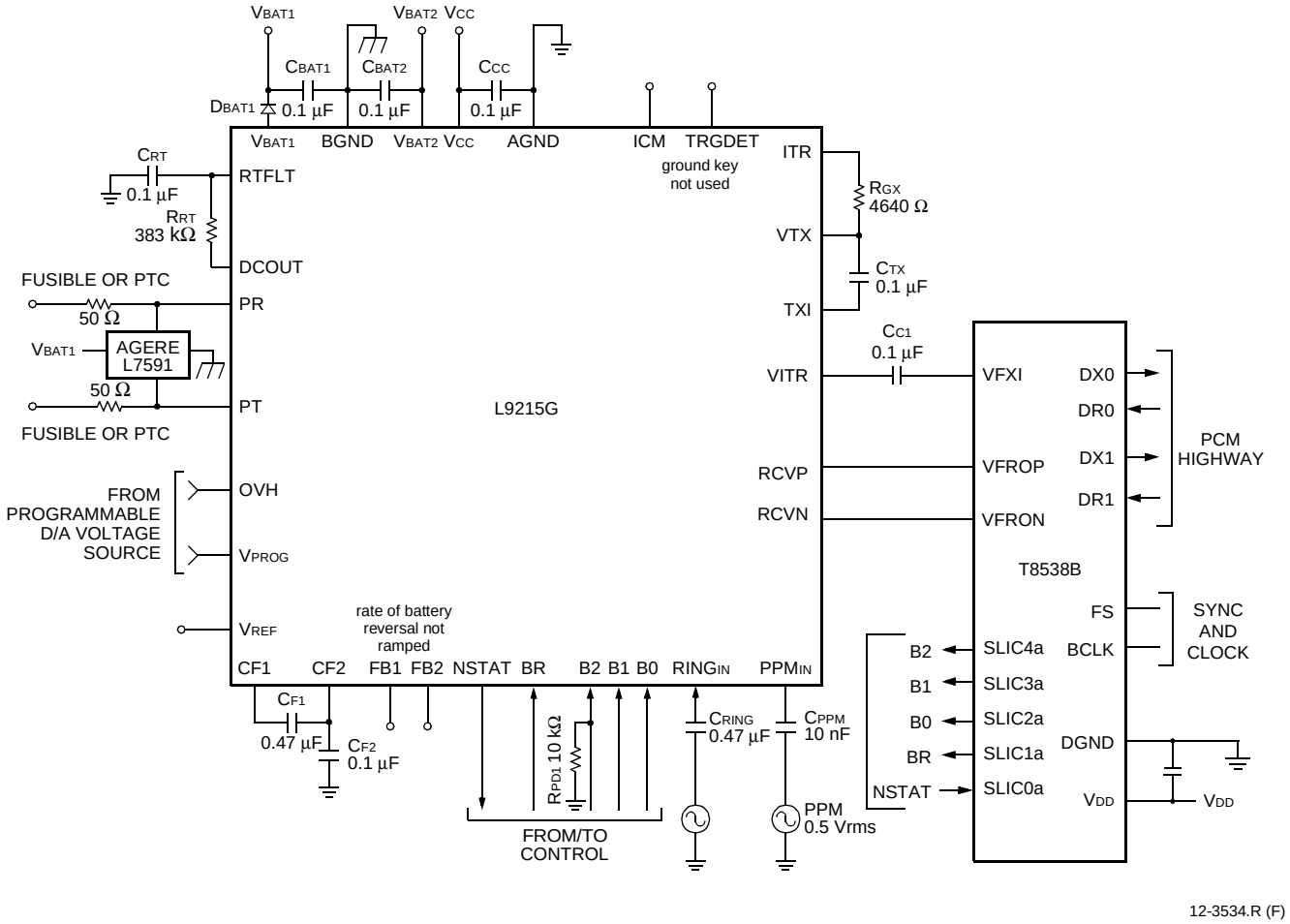

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Figure 2. POTS Interface

For additional information, contact your Agere Systems Account Manager or the following:
INTERNET: **http://www.agere.com**
E-MAIL: **docmaster@micro.lucent.com**
N. AMERICA: Agere Systems Inc., 555 Union Boulevard, Room 30L-15P-BA, Allentown, PA 18109-3286
1-800-372-2447, FAX 610-712-4106 (In CANADA: **1-800-553-2448**, FAX 610-712-4106)
ASIA PACIFIC: Agere Systems Singapore Pte. Ltd., 77 Science Park Drive, #03-18 Cintech III, Singapore 118256
Tel. (65) 778 8833, FAX (65) 777 7495
CHINA: Agere Systems (Shanghai) Co., Ltd., 33/F Jin Mao Tower, 88 Century Boulevard Pudong, Shanghai 200121 PRC
Tel. (86) 21 50471212, FAX (86) 21 50472266
JAPAN: Agere Systems Japan Ltd., 7-18, Higashi-Gotanda 2-chome, Shinagawa-ku, Tokyo 141, Japan
Tel. (81) 3 5421 1600, FAX (81) 3 5421 1700
EUROPE: Data Requests: DATALINE: **Tel. (44) 7000 582 368**, FAX (44) 1189 328 148
Technical Inquiries: GERMANY: **(49) 89 95086 0** (Munich), UNITED KINGDOM: **(44) 1344 865 900** (Ascot),
FRANCE: **(33) 1 40 83 68 00** (Paris), SWEDEN: **(46) 8 594 607 00** (Stockholm), FINLAND: **(358) 9 3507670** (Helsinki),
ITALY: **(39) 02 6608131** (Milan), SPAIN: **(34) 1 807 1441** (Madrid)