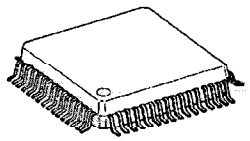
CMOS 8-Bit Microcontroller

TMP86FS41F

The TMP86FS41F is a high-speed, high-performance 8-bit microcomputer built around the TLCS870/C Series core with built-in 60-Kbyte ROM and it is pin compatible with its mask ROM version, the TMP86CM41F. Writing programs in the built-in flash memory enables this microcomputer to perform the same operations as the TMP86CM41F. The built-in flash memory can be rewritten on-board (without removing it from the PCB) by a built-in boot program and it can also be rewritten by executing a user-made rewrite program on RAM.

Part No.	Flash EEPROM	RAM	Package
TMP86FS41F	60 Kbyte	2 Kbyte	P-QFP64-1414-0.80B

P-QFP64-1414-0.80B



TMP86FS41F

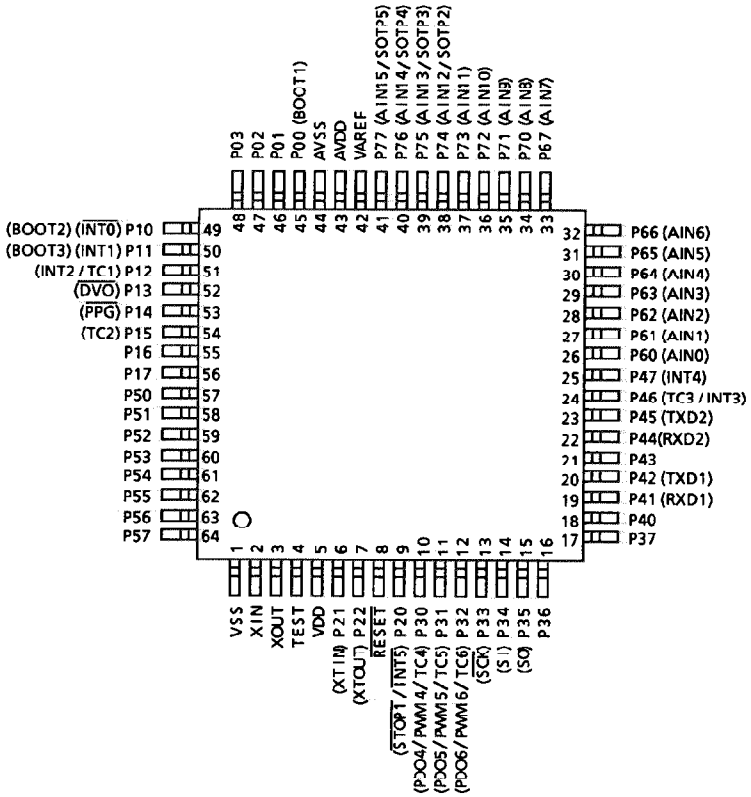
Features

- 8-bit single chip microcomputer TLCS-870/C series
- Instruction execution time: 0.25 μs (at 16 MHz)
  122 μs (at 32.768 kHz)
- 132 types & 731 basic instructions
- 21 interrupt sources (External: 6, Internal: 15)
- Input / Output ports (55 pins)
  High current output: 8 pins (typ. 20 mA)
- 16-bit timer counter: 2 ch
  - Timer, Event counter, Pulse width measurement, Programmable pulse Generator (PPG), External triggered timer, Window modes
- 8-bit timer counter: 4 ch
  - Timer, Event counter, Pulse Width Modulation (PWM) output, Programmable Divider Output (PDO), PPG modes
- Time Base Timer (TBT)
- Divider output function
- Watchdog Timer
  - Interrupt source / reset output (programmable)

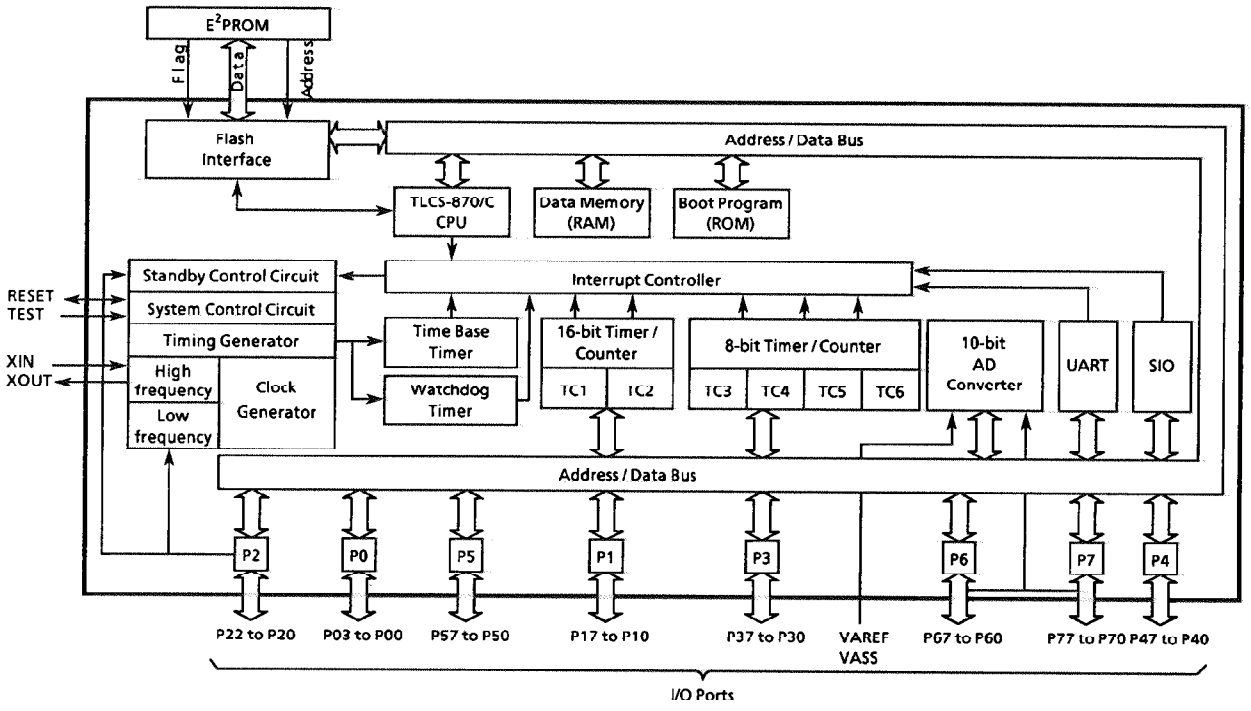
- Serial interface
  - 8-bit SIO: 1ch
  - 8-bit UART: 1ch (IrDA output, selection of used pin)
- 10-bit successive approximation type AD converter
  - Analog input: 16 ch
- Key On Wake Up: 4 ch
- Dual clock operation
  - Single / Dual-clock mode
- Nine power saving operating modes
  - STOP mode: Oscillation stops. Battery / Capacitor back-up. Port output hold / High-impedance.
  - SLOW 1, 2 mode: Low power consumption operation using low-frequency clock (32.768 kHz)
  - IDLE 0 mode: CPU stops, and peripherals operate using high-frequency clock of Time-Base-Timer. Release by INTTBT interrupt.
  - IDLE 1 mode: CPU stops, and peripherals operate using high-frequency clock. Release by interrupts.
  - IDLE 2 mode: CPU stops, and peripherals operate using high and low frequency clock. Release by interrupts.
  - SLEEP 0 mode: CPU stops, and peripherals operate using low-frequency clock of Time-Base-Timer. Release by INTTBT interrupt.
  - SLEEP 1 mode: CPU stops, and peripherals operate using low-frequency clock. Release by interrupts.
  - SLEEP 2 mode: CPU stops, and peripherals operate using high and low frequency clock. Release by interrupts.
- Wide operating voltage: 4.5 to 5.5 V at 16 MHz / 32.768 kHz

Pin Assignments (Top View)

P-QFP64-1414-0.80B



Block Diagram



Pin Function

The TMP86FS41 has MCU mode and single boot mode.

(1) MCU Mode

This mode is the same as that of the TMP86CM41 except that TEST pin does not have a built-in pull-down resister. (Be sure to fix TEST pin at low level.)

(2) Single Boot Mode

The boot mode is set by fixing TEST pin at "H", P00 pin at "H", P10 pin at "H" and P11 pin at "H" respectively when RESET pin is set to "L". Setting RESET pin to "H" (releasing RESET) activates the built-in boot ROM and the flash memory is rewritten by serial transfer (UART).

Pin Name	Input / Output	Function		Single Boot Mode
P00 P01 P02 P03	I/O	4-bit I/O port. Each bit of these ports can be individually configured as an input or an output under software control.	–	High level (Boot1)
P10 ($\overline{INT0}$)	I/O (Input)	8-bit I/O port with latch. Each bit of these ports can be individually configured as an input or an output under software control. When used as divider output, PPG output, the latch of used bit must be set to "1", and used bits are configured outputs.	External Interrupt input	Low level (Boot2)
P11 (INT1)			External Interrupt input	High level (Boot3)
P12 (INT2 / TC1)			External interrupt input Timer	
P13 ($\overline{DVO}$)	I/O (Output)		Divider output	
P14 ($\overline{PPG}$)			PPG output	
P15 (TC2)	I/O (Input)		Timer / Counter input	
P16 P17	I/O		–	
P20 ($\overline{INT5}$ / $\overline{STOP1}$)	I/O (Input)	3-bit I/O port with latch. When used as input port, external interrupt input, and STOP mode release signal input, the latch must be set to "1".	External interrupt input STOP mode release signal input	
P21 (XTIN)	I/O (Output)		Low Frequency Clock input	
P22 (XOUT)			Low Frequency Clock output	
P30 (TC4 / PWM4 / PDO4)	I/O (Input / Output / Output)	8-bit I/O port with latch. Each bit of these ports can be individually configured as an input or an output under software control. When used as Timer / Counter input, SI, used bits are configured inputs. When used as PWM output, PDO output, and SO, used bits are configured outputs.	Timer / Counter input PWM output PDO output	
P31 (TC5 / PWM5 / PDO5)				
P32 (TC6 / PWM6 / PDO6)				
P33 ($\overline{SCK}$)	I/O (I/O)		SIO input / output	
P34 (SI)	I/O (Input)			
P35 (SO)	I/O (Output)			
P36 P37	I/O		–	
P40	I/O	8-bit I/O port with latch. Each bit of these ports can be individually configured as an input or an output under software control. When used as UART mode, the latch must be set to "1". When used as Open-Drain output, P4ODE and P4CR must be set to "1".	–	
P41 (RXD1)	I/O (Input)		UART Data input	Data input
P42 (TXD1)	I/O (Output)		UART Data output	Data output
P43	I/O		–	
P44 (RXD2)	I/O (Input)		UART Data input	
P45 (TXD2)	I/O (Output)		UART Data output	
P46 (TC3 / INT3)	I/O (Input)		Timer / Counter input External Interrupt input	
P47 (INT4)			External Interrupt input	

Pin Name	Input / Output	Function		Single Boot Mode
P50 P51 P52 P53 P54 P55 P56 P57	I/O	8-bit I/O port. Each bit of these ports can be individually configured as an input or output under software control. These ports are High current output ports, can be drive LED direct.	–	
P60 (AIN0) P61 (AIN1) P62 (AIN2) P63 (AIN3) P64 (AIN4) P65 (AIN5) P66 (AIN6) P67 (AIN7)	I/O (Input)	8-bit I/O port. Each bit of these ports can be individually configured as an input or output under software control.	AD Convertor analog inputs	
P70 (AIN8) P71 (AIN9) P72 (AIN10) P73 (AIN11) P74 (AIN12 / STOP2) P75 (AIN13 / STOP3) P76 (AIN14 / STOP4) P77 (AIN15 / STOP5)	I/O (Input)	8-bit I/O port. Each bit of these ports can be individually configured as an input or output under software control.	AD Convertor analog inputs AD Convertor analog input STOP mode release signal input	
TEST	Input	Test pin for out-going test. Be fixed to Low.		Low level
$\overline{\text{RESET}}$	I/O	Reset signal input or watchdog timer output / address-trap-reset output.		Low → High level
XIN	Input	Resonator connecting pins for high-frequency clock. For inputting external clock, XIN is used and XOUT is opened.		
XOUT	Output			
VSS	Power Supply	00 [V] (GND)		0.0 [V] (GND)
VDD		+ 5.0 [V]		+ 5.0 [V]
AVSS		0.0 [V] (GND)		
AVDD		+ 5.0 [V] AD circuit power supply		
VAREF		Analog reference voltage inputs (High, Low)		

Operational Description

The TMP86FS41 is a version of the TMP86CM41 incorporating flash memory in place of the built-in mask ROM. The configuration and functions of the TMP86FS41 is the same as those of the TMP86CM41 except that TEST pin does not have a built-in pull-down resister.
For functions not included herein, please refer to the data sheets of the TMP86CM41.

1. Operational Mode

The TMP86FS41 has MCU mode, single boot mode and user boot mode.

1.1 MCU Mode

The MCU mode is set by fixing TEST pin at "L" level.
Operations in the MCU mode are the same as those of the TMP86CM41.
(Because TEST pin does not have a pull-down register, it cannot be used in the released state.)

1.2 Single Boot Mode

The boot mode is set by fixing TEST pin at "H", P00 pin at "H", P10 pin at "L" and P11 pin at "H" respectively when RESET pin is fixed at "L". After release of reset, the built-in boot ROM program is activated and the built-in flash memory is rewritten by serial transfer (UART).

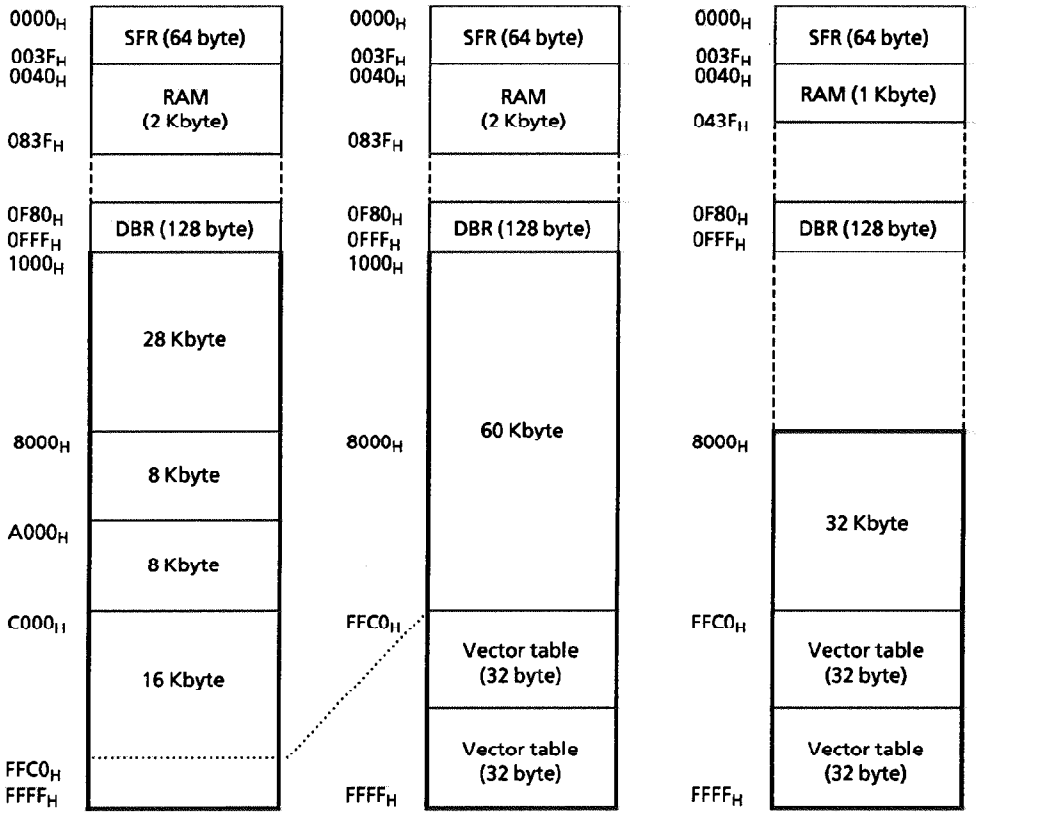
1.3 User Boot Mode

In this mode, rewriting is performed by running a user-made flash memory rewrite program on RAM. After transferring the rewrite program to RAM in the user program, set the address trap area to only the SFR area and then jump to the start address of the rewrite program on RAM. Running that rewrite program effects the rewrite of flash memory.

2. Program Memory

The TMP86FS41 has a 60K×8-bit (address 1000_H to $FFFF_H$: MCU / Boot mode) of Flash memory.

2.1 Address map



Sector division in boot mode

When used as 86FS41

When used for system evaluation of mask ROM product (86CM41)

3. Data memory

The TMP86FS41 has a built-in 2 Kbyte Data memory (static RAM ; address 0040_H to $083F_H$)

4. Input / Output Circuit

(1) Control Pins

The control pins of the TMP86FS41 are same as these of TMP86CM41 except that the TEST pin dose not have a built-in Pull-down resister.

(2) I/O port

The I/O circuities of TMP86FS41 I/O ports are the same as those of TMP86CM41.

5. Single Boot Mode

5.1 Overview

The TMP86FS41 is provided with the single boot mode as an operational mode to perform on-board programming. In the single boot mode, a program written in the built-in boot ROM effects the rewrite of the built-in flash memory by serial transfer (UART). The built-in boot ROM is a mask ROM incorporating a program for performing the on-board rewrite of flash memory.

5.2 Mode Setting

In order to set the single boot mode, fix TEST pin at "H", P00 pin at "L", P10 pin at "L" and P11 pin at "H" respectively during the RESET operation (RESET pin = "L") and release RESET.

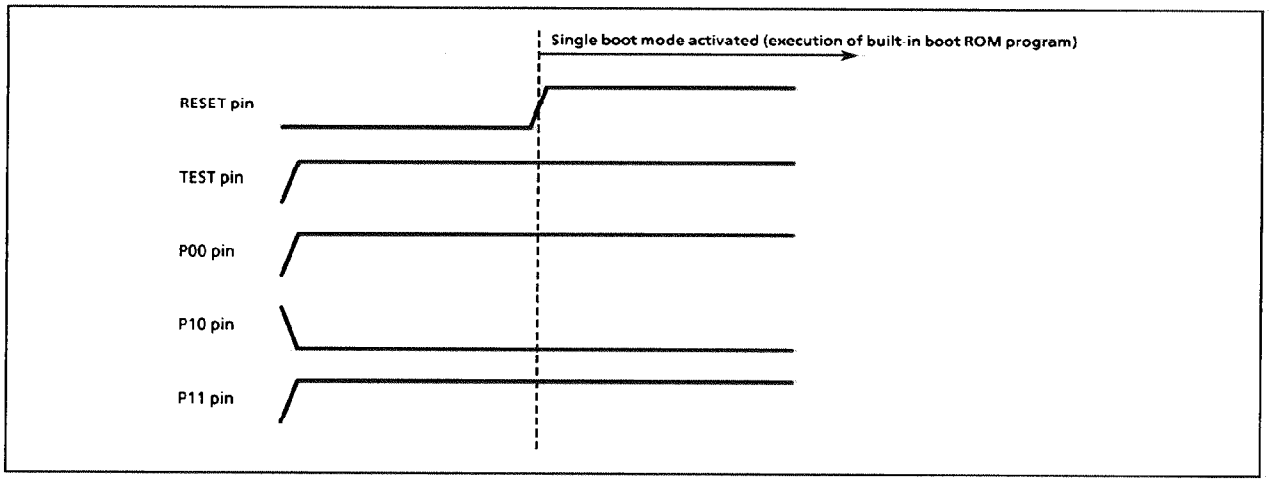


Figure 5.1 Single Boot Mode

When the single boot mode is activated, the built-in boot ROM program is executed and external commands are sent to the TMP86FS41 by serial transfer (UART) and the flash memory is rewritten. (Operation of the program will be described in detail later.)

5.3 Example of Connection for On-board Write

An example of connection for writing on-board in the single boot mode is shown below. Changing to the single boot mode is to be carried out on-board.

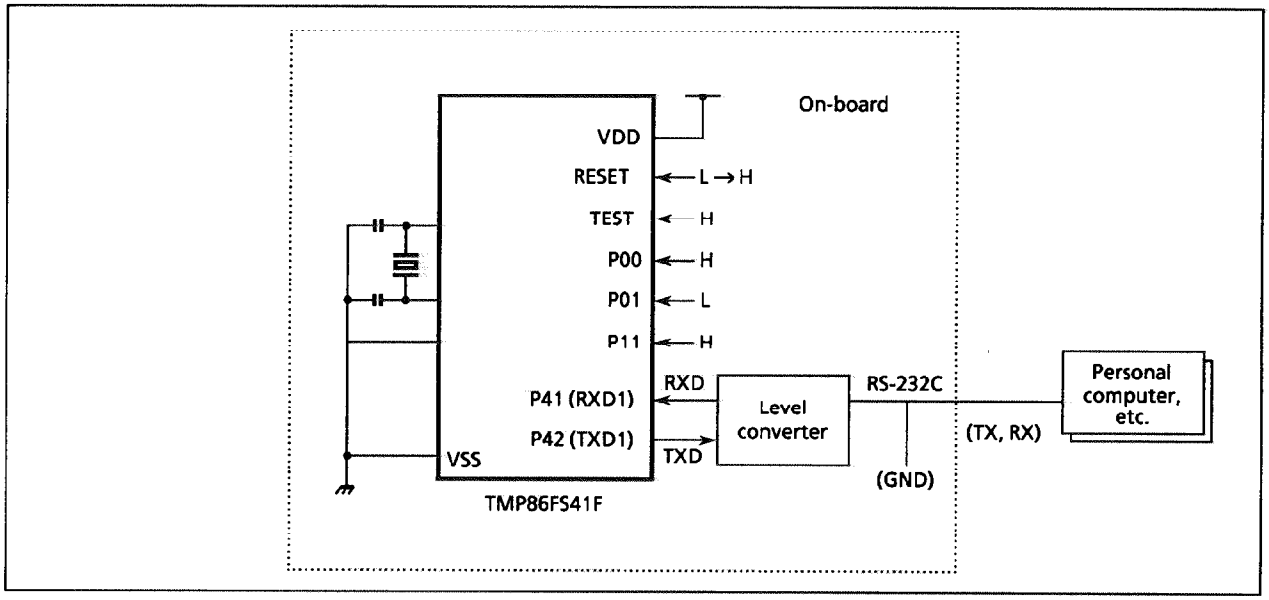


Figure 5.2 Example of Connection for On-board Write

5.4 Specifications of Built-in Boot ROM Program

Specifications of the built-in boot ROM program are shown below.

5.4.1 Outline of Built-in Boot ROM Program

1. Start executing the built-in boot ROM program.
2. UART receive (Initial setting: 9600 bps @ 16 MHz)
3. Wait to receive the matching data (5A).
4. After receiving 5A, echo it back.
5. Wait to receive the operation command data.
6. After receiving the operation command data, echo them back.
7. Perform operation according to the received operation command data.
8. After completing the operation, go back to waiting to receive the operation command data.

5.4.2 Initial Setting of UART Baud Rate

The setting of the UART baud rate immediately after the built-in boot program execution is as follows:

Baud rate: 9600 bps (fc = 16 MHz)
Data length: 8 bits
Parity bit: none
STOP bit: 1 bit

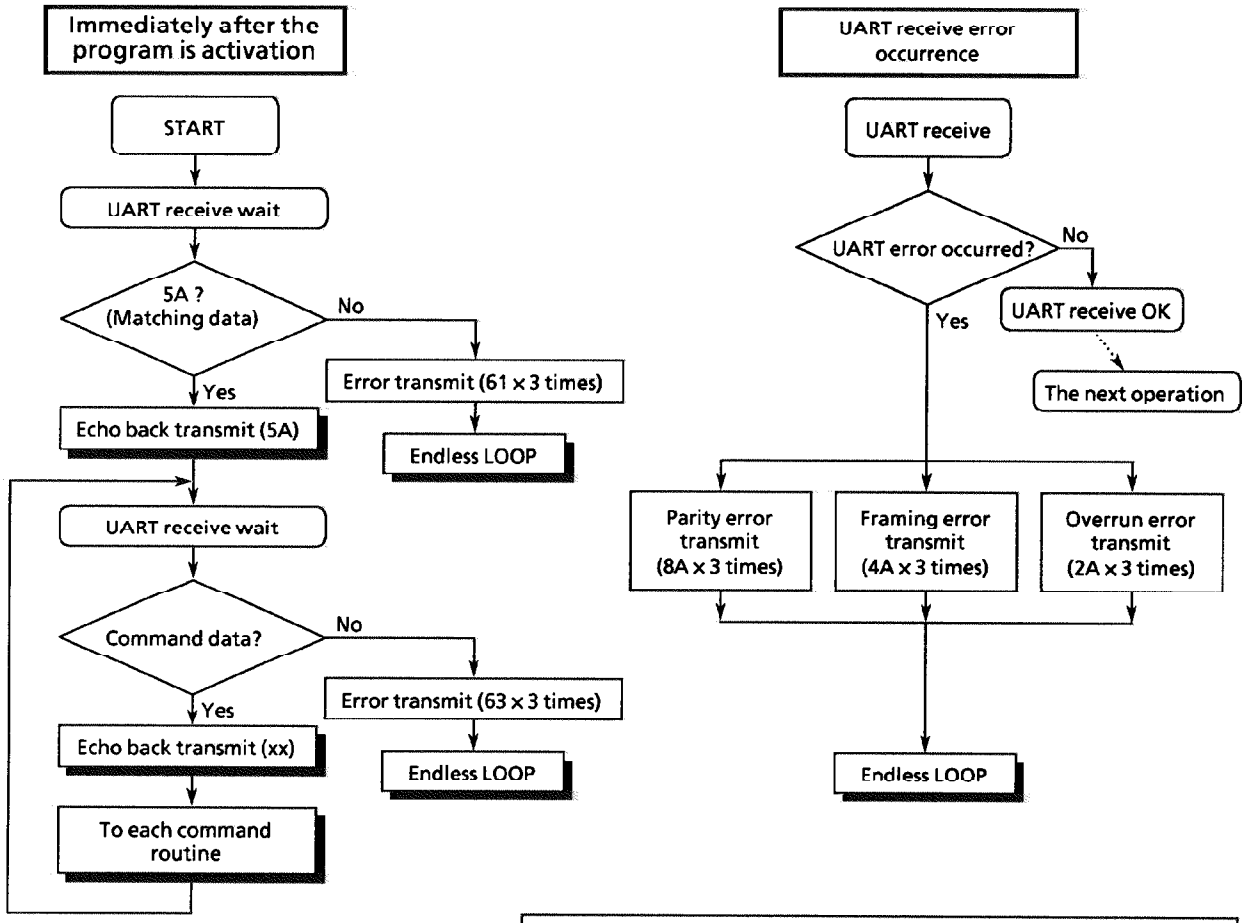
5.4.3 Operation Command Data

Operation command data	Operation mode	Operation description
30_H	Rewrite flash memory	After erasing all the contents of the flash memory, write data in the specified address and then transmit the checksum.
60_H	RAM loader	Read the program in RAM and execute. Password required.
90_H	Calculate checksum	Calculate the checksum of the flash memory (1000_H to $FFFF_H$)
$A0_H$	Change baud rate	Change the UART baud rate. (Refer to 5.4.4)

5.4.4 Baud Rate Changing Data

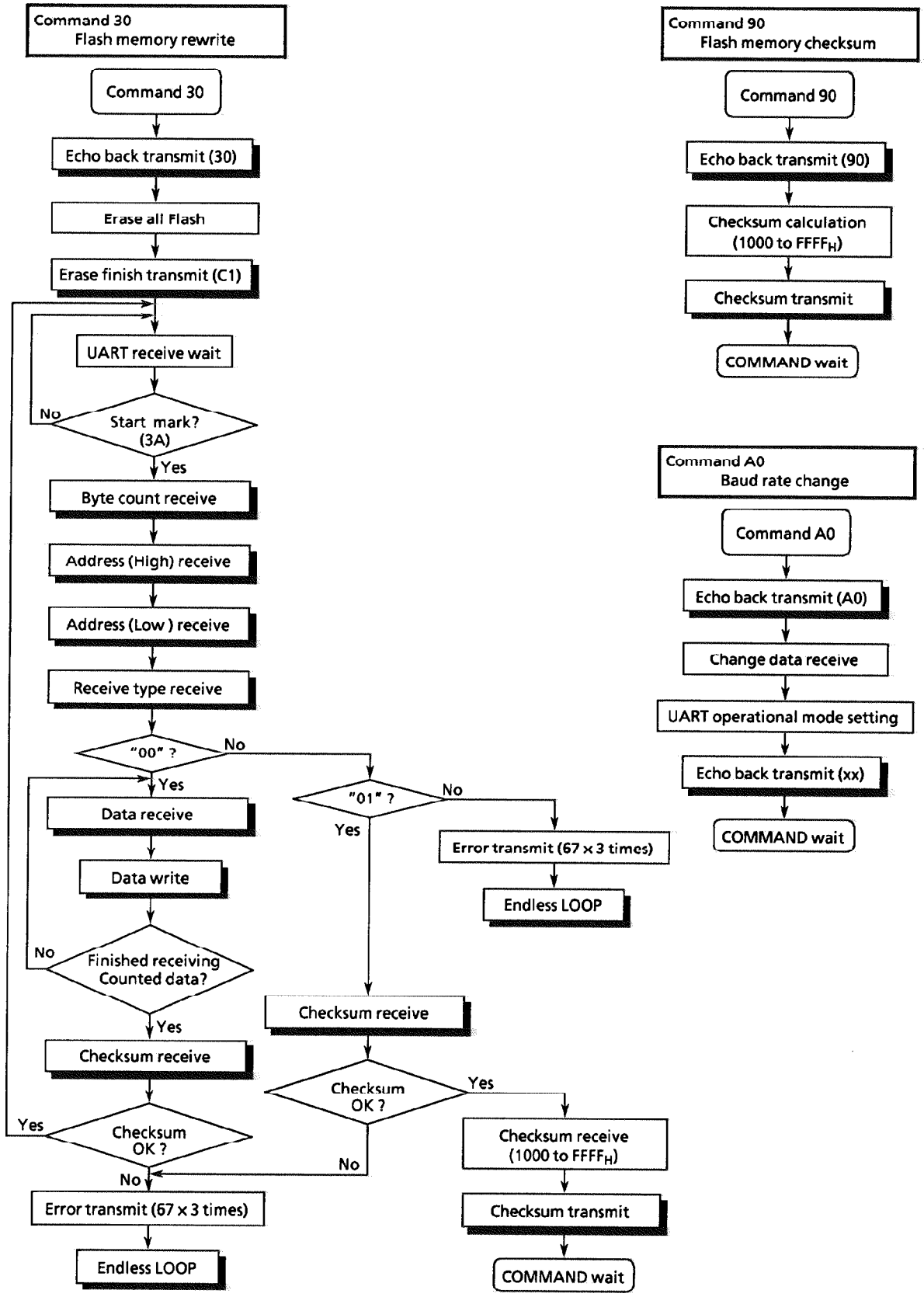
Bit	7 6	5	4	3	2 1 0
Data contents	Select the time to eliminate noise of RXD input	Stop bit	Select odd or even parity	Select addition to parity	Select transfer clock
	00: do not eliminate 01: 31/fc 10: 63/fc 11: 127/fc	0: 1 bit 1: 2 bits (transmit / send)	0: odd 1: even	0: with 1: withoug	000: fc/13 001: fc/26 010: fc/52 011: fc/104 100: fc/208 101: fc/416 110: – 111: fc/96

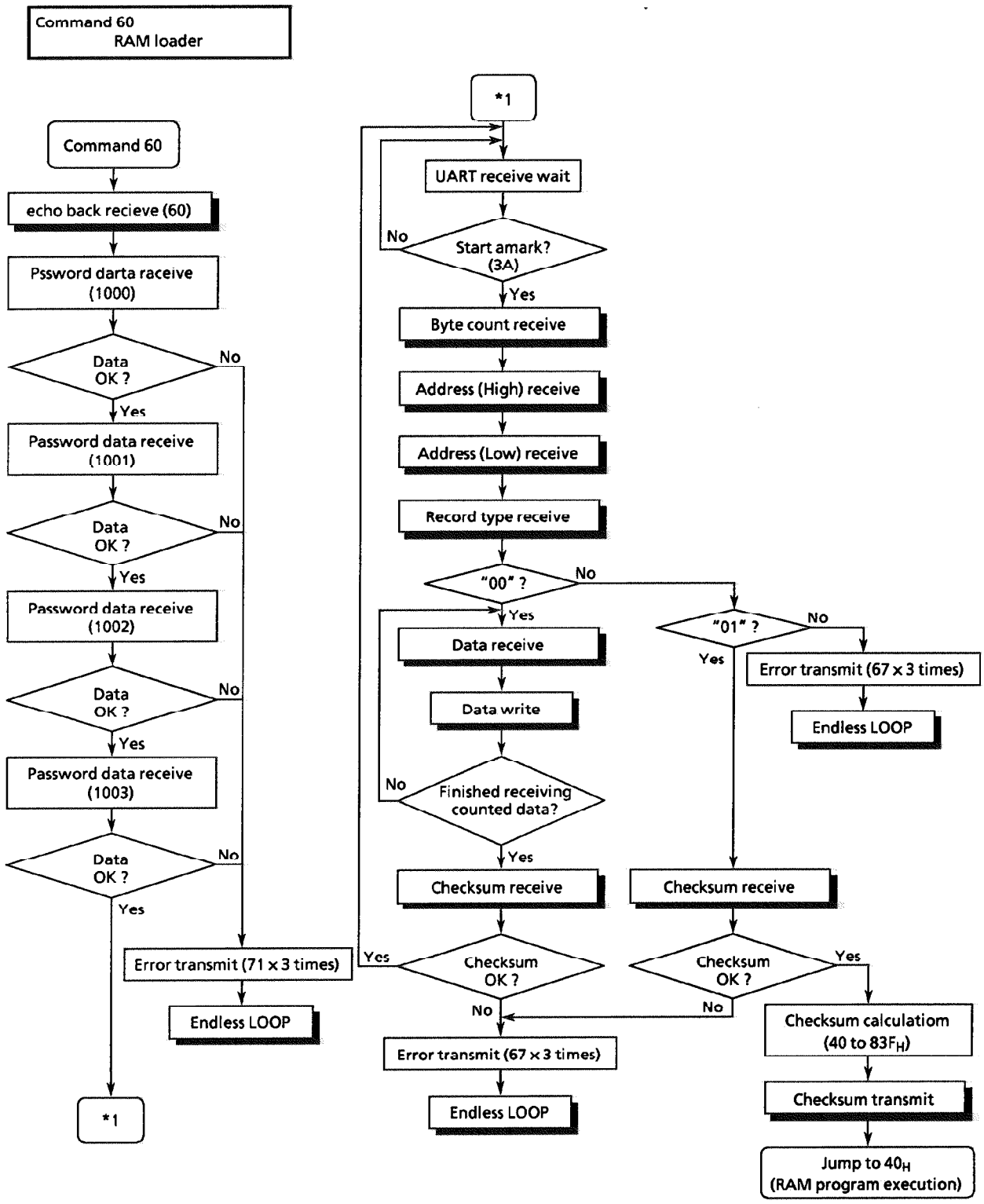
5.4.5 Program Flowchart



If an error occurs, error send is performed and then endless LOOP starts.
To re-execute, set the single boot mode again.

- Command routine Flowchart




Command 60
RAM loader
Command 60
echo back recieve (60)
Pssword darta raceive (1000)
Data OK ?
No
Yes
Password data receive (1001)
Data OK ?
No
Yes
Password data receive (1002)
Data OK ?
No
Yes
Password data receive (1003)
Data OK ?
No
Yes
Error transmit (71 x 3 times)
Endless LOOP
*1
*1
UART receive wait
No
Start amark? (3A)
Yes
Byte count receive
Address (High) receive
Address (Low) receive
Record type receive
"00" ?
No
Yes
Data receive
Data write
No
Finished receiving counted data?
Yes
Checksum receive
Yes
Checksum OK ?
No
Error transmit (67 x 3 times)
Endless LOOP
"01" ?
No
Yes
Error transmit (67 x 3 times)
Endless LOOP
Checksum receive
Checksum OK ?
Yes
No
Checksum calculatiom (40 to 83FH)
Checksum transmit
Jump to 40H (RAM program execution)

6. User Boot Mode

6.1 Overview

In the user boot mode, a user-made program is expanded on RAM and by executing that program the rewrite of the program is achieved on-board.Because this mode can only be used in the RAM area, interrupts cannot be used in the program.

6.2 Mode Setting

The user boot mode does not require setting of external pins.
The program is executed by transferring the program data to RAM and jumping to the execution start address of that program. Note that it is necessary to disable the address trap before jumping to the RAM address. It is also necessary to disable interrupts.

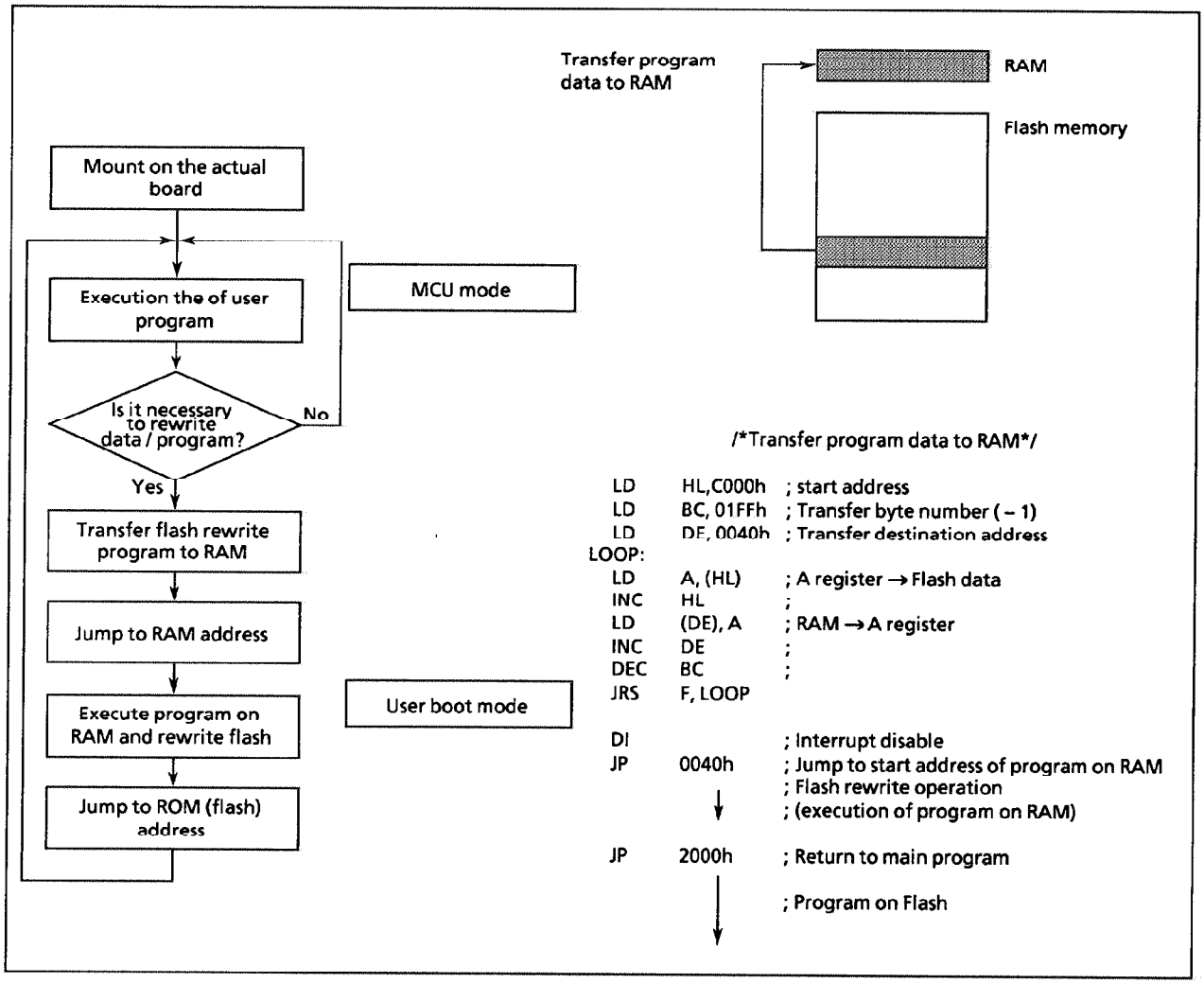


Figure 6.1 User Boot Mode

6.3 Description of Operation in User Mode

In the user mode, flash memory is accessed via a command register that is assigned to the DBR area. Erasing write/read of flash memory is performed by a JEDEC standard command. After typing in the command, write and erase will automatically be performed.

Command register

Address High:	CADRH	($0F81_H$)	Write Only
Address Low:	CADRL	($0F80_H$)	Write Only
Write data:	CWDATA	($0F82_H$)	Write Only
Read data:	CRDATA	($0F82_H$)	Read Only
Status monitor:	FSTATUS	($0F83_H$)	Read Only
Command register:	CCMD	($0F83_H$)	Write Only

- To transmit command data:

1. Set the address (CADRH/L).
2. Set the data to be transmitted (CWDATA)
3. By setting the rewrite command in Command register (CCMD), data is transmitted to the flash memory. (The command sequence is transmitted to the flash memory by using this method.)

* While the automatic algorithm is being executed, the RY/BY status is read into the DBR status register ($0F32_H$), FSTATUS. Verify that the write is completed before writing the next data.

Table 6.1 Command sequence

Command sequence	Cycle	1 st bus write cycle		2 nd bus write cycle		3rd bus write cycle		4 th bus write cycle		5 th bus write cycle		6 th bus write cycle	
		address	data	address	data	address	data	address	data	address	data	address	data
Read / Reset	1	$xxxx_H$	$F0_H$	–	–	–	–	–	–	–	–	–	–
	3	$AAAA_H$	AA_H	5555_H	55_H	$AAAA_H$	$F0_H$	RA	RD	–	–	–	–
Program	3	$AAAA_H$	AA_H	5555_H	55_H	$AAAA_H$	$A0_H$	PA	PD	–	–	–	–
Chip erase	6	$AAAA_H$	AA_H	5555_H	55_H	$AAAA_H$	80_H	$AAAA_H$	AA_H	5555_H	55_H	$AAAA_H$	10_H
Sector erase	6	$AAAA_H$	AA_H	5555_H	55_H	$AAAA_H$	80_H	$AAAA_H$	AA_H	5555_H	55_H	SA	30_H
Sector erase temporary stop		Input of ADDr(Add. = "H" or "L") and Data($B0_H$) temporarily stops erase operation in sector erase.											
Sector erase resume		Input of ADDr(Add. = "H" or "L") and Data(30_H) resumes erase operation after temporary sector erase stop.											

*RA: Read Address、RD: Read Data
*PA: Program Address、PD: Program Data
*SA: Erase Address (Select sectors by combination of A15,14,13,12)

6.4 Flash Memory Control Registers

- Flash memory setting address

	7	6	5	4	3	2	1	0	
CADRL	A7	A6	A5	A4	A3	A2	A1	A0	(Initial value: 0000 0000)

Address: SFR $0F80_H$

	7	6	5	4	3	2	1	0	
CADRH	A15	A14	A13	A12	A11	A10	A9	A8	(Initial value: 0000 0000)

Address: SFR $0F81_H$

A15 to A0	Addresses set by Flash ROM	Write

- Flash memory write data

	7	6	5	4	3	2	1	0	
CWDATA	CWD7	CWD6	CWD5	CWD4	CWD3	CWD2	CWD1	CWD0	(Initial value: 1111 1111)

Address: SFR $0F82_H$

CWD7 to CWD0	Flash ROM write data	Write

- Flash memory read data

	7	6	5	4	3	2	1	0	
CRDATA	CRD7	CRD6	CRD5	CRD4	CRD3	CRD2	CRD1	CRD0	(Initial value: 1111 1111)

Address: SFR $0F82_H$

CRD7 to CRD0	Flash ROM read data	Read

- Executing setting to flash memory (Command register)

	7	6	5	4	3	2	1	0	
CCMD	–	–	–	–	–	–	–	CCMD	(Initial value: **** ***0)

Address: DBR $0F83_H$

CCMD	Execute data setting to Flash ROM	0: execute data read from Flash ROM 1: execute data write to Flash ROM	Write

- RY/BY pin monitor (Status monitor)

	7	6	5	4	3	2	1	0	
FSTATUS	–	–	–	–	–	–	–	RYBY	(Initial value: **** ***1)

Address: DBR $0F83_H$

RYBY	bus READY or BUSY	0: BUSY 1: READY	Read

- Example of Write Program

  An example of a 1-byte write program is shown below.

  * Example program (to write 66_H in 1000_H)

```
LD    HL, 0F80H      ;  Address setting adderss
LDW   (HL), AAAAH    ;  Address (AAAAH)
LD    (0F82H), AAH   ;  Data (AAH)
LD    (0F83H), 01H   ;  Execute write
LDW   (HL), 5555H    ;  Address (5555H)
LD    (0F82H), 55H   ;  Data (55H)
LD    (0F83H), 01H   ;  Execute write
LDW   (HL), AAAAH    ;  Address (AAAAH)
LD    (0F82H), A0H   ;  Data (A0H)
LD    (0F83H), 01H   ;  Execute write

LDW   (HL), 1000H    ;  Write address (1000H)
LD    (0F82H), 66H   ;  Write data (A0H)
LD    (0F83H), 01H   ;  Execute write

LOOPW:               ;  Wait for write complete status
      TEST (0F83H).0 ;  JF? (x).b (0: BUSY, 1: READY)
      JRS  T, LOOPW  ;  if JF=1 then PC?PC+d
```

- Example of Read Program

  An example of a 1-byte read program is shown below.

  * Example program (read data in 1000_H into A register)

```
LOOPR1:              ;  Check to see if it is not busy
TEST (0F83H).0       ;  JF? (x).b (0: BUSY, 1: READY)
JRS  T, LOOPR1       ;  if JF=1 then PC?PC+d

LD    HL, 0F80H      ;  Address setting address
LDW   (HL), AAAAH    ;  Address (AAAAH)
LD    (0F82H), AAH   ;  Data (AAH)
LD    (0F83H), 01H   ;  Execute write
LDW   (HL), 5555H    ;  Address (5555H)
LD    (0F82H), 55H   ;  Data (55H)
LD    (0F83H), 01H   ;  Execute write
LDW   (HL), AAAAH    ;  Address (AAAAH)
LD    (0F82H), F0H   ;  Data (F0H)
LD    (0F83H), 01H   ;  Execute write

LDW   (HL), 1000H    ;  Read address (1000H)
LD    (0F83H), 00H   ;  Execute read
LDA, (0F82H)         ;  Read data (address 1000H)
```

Electrical Characteristics

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter	Symbol	Pins	Ratings	Unit
Supply Voltage	V_{DD}		− 0.3 to 6.5	V
Input Voltage	V_{IN}		− 0.3 to V_{DD} + 0.3	
Output Voltage	V_{OUT}		− 0.3 to V_{DD} + 0.3	
Output Current (Per 1 pin)	I_{OUT1}	P0, P1, P3, P4, P5, P6, P7 Port	− 3.2	mA
	I_{OUT2}	P0, P1, P2, P3, P4, P6, P7 Port	3.2	
	I_{OUT3}	P5 Port	30	
Output Current (Total)	ΣI_{OUT1}	P0, P1, P2, P3, P4, P6, P7 Port	80	
	ΣI_{OUT2}	P5 Port	120	
Power Dissipation (Topr = 70°C)	PD		700	mW
Soldering Temperature (time)	Tsld		260 (10 s)	°C
Storage Temperature	Tstg		− 55 to 125	
Operating Temperature	Topr		− 20 to 70	

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Condition (V_{SS} = 0 V, Topr = − 20 to 70°C)

Parameter	Symbol	Pins	Condition	Min	Max	Unit
Supply Voltage	V_{DD}		fc = 1 to 16 MHz fs = 32.768 kHz (NORMAL1,2 mode IDLE 0,1,2 mode SLEEP 0,1,2 mode SLOW1,2 mode STOP mode)	4.5	5.5	V
Input high Level	V_{IH1}	Except Hysterisis, TTL input	$V_{DD} \geqq$ 4.5 V	$V_{DD} \times 0.70$	V_{DD}	
	V_{IH2}	Hysteresis input		$V_{DD} \times 0.75$		
Input low Level	V_{IL1}	Except Hysterisis, TTL input	$V_{DD} \geqq$ 4.5 V	0	$V_{DD} \times 0.30$	
	V_{IL2}	Hysteresis input			$V_{DD} \times 0.25$	
Clock Frequency	fc	XIN, XOUT		1.0	16.0	MHz
	fs	XTIN, XTOUT		30.0	34.0	kHz

Note: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

D.C. Characteristics

(V_{SS} = 0 V, Topr = − 20 to 70°C)

Parameter	Symbol	Pins	Condition	Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis inputs		–	0.9	–	V
Input Current	I_{IN1}	TEST	V_{DD} = 5.5 V V_{IN} = 5.5 V / 0 V	–	–	± 2	μA
	I_{IN2}	Sink Open Drain, Tri-st Port					
	I_{IN3}	$\overline{RESET}$					
Input Resistance	R_{IN}	$\overline{RESET}$		100	220	450	kΩ
Osec. Feedback Resistance	Rfx	XIN-XOUT		–	1.2	–	MΩ
	Rfxt	XTIN-XTOUT		–	6	–	
Output Leakage Current	I_{LO1}	Sink Open Drain Port	V_{DD} = 5.5 V, V_{OUT} = 5.5 V	–	–	2	μA
	I_{LO2}	Tri-st Port	V_{DD} = 5.5 V, V_{OUT} = 5.5 V / 0V	–	–	± 2	
Output High Voltage	V_{OH}	Tri-st Port	V_{DD} = 4.5 V, I_{OH} = − 0.7 mA	4.1	–	–	V
Output Low Voltage	V_{OH3}	P5	V_{DD} = 4.5 V, I_{OL} = 1.6 mA	–	–	0.4	V
Output Low Current	I_{OL1}	Except P5	V_{DD} = 4.5 V, V_{OL} = 0.4 V	–	1.6	–	mA
	I_{OL3}	P5 (High Current Output port)	V_{DD} = 4.5 V, V_{OL} = 1.0 V	–	20	–	
Supply Current in NORMAL 1, 2 mode	I_{DD}		V_{DD} = 5.5 V V_{IN} = 5.3 V / 0.2 V fc = 16 MHz fs = 32.768 kHz	–	30	40	mA
Supply Current in IDLE 1, 2 mode				–	9	13	mA
Supply Current in SLOW 1 mode			V_{DD} = 5.5 V V_{IN} = 5.3 V / 0.2 V fs = 32.768 kHz	–	11	16.5	mA
Supply Current in SLEEP 0, 1 mode				–	28	55	μA
Supply Current in STOP mode			V_{DD} = 5.5 V V_{IN} = 5.3 V / 0.2 V	–	200	400	μA

Note 1: Typical values show those at Topr = 25°C, V_{DD} = 5 V

Note 2: Input current (I_{IN1}, I_{IN4}); The current through pull-up or pull-down resistor is not included.

AD Conversion Characteristics (V_{SS} = 0 V, Topr = – 20 to 70°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{AREF}		V_{DD} – 1.5	–	V_{DD}	V
	A_{VDD}		V_{DD}			
	A_{VSS}		V_{SS}			
Analog Reference Voltage Range	ΔV_{AREF}	V_{AREF} – A_{VSS}	2.5	–	–	V
Analog Input Voltage	V_{AIN}		V_{SS}	–	V_{AREF}	V
Power Supply Current of Analog Reference Voltage	I_{REF}	V_{DD} = A_{VDD} = V_{AREF} = 5.5 V VSS = A_{VSS} = 0.0 V	–	0.6	1.0	mA
Non linearity Error		V_{DD} = 4.5 to 5.5 V V_{SS} = 0.0 V A_{VDD} = V_{AREF} = VDD A_{VSS} = 0.0 V	–	–	±2	LSB
Zero Point Error			–	–	±2	
Full Scale Error			–	–	±2	
Total Error			–	–	±4	

Note 1: Total errors includes all errors, except quantization error.
Note 2: Conversion time is different in recommended value by power supply voltage.
About conversion time, please refer to "2.10.2 Register Framing".
Note 3: Please use input voltage to AIN input Pin in limit of V_{AREF} - V_{SS}.
When voltage of range outside is input, conversion value becomes unsettled and gives affect to other channel conversion value.