E1Fx8 Device
8-Channel E1 Framer
TXC-03109

DATA SHEET
PRELIMINARY

FEATURES

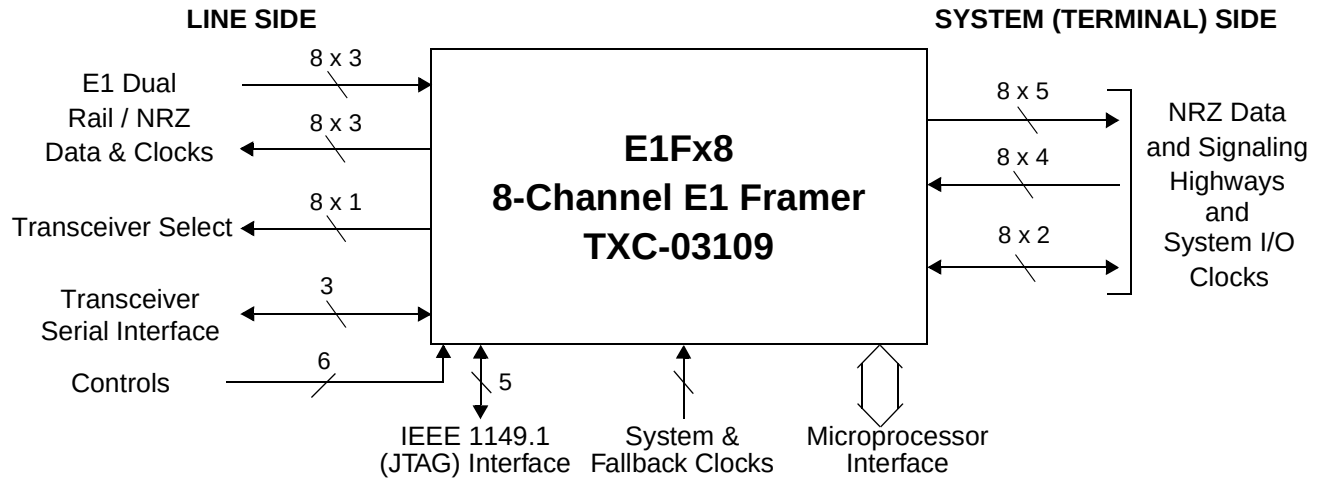
- Eight-channel offline framer supports standard and frame hold-off frame alignment with CRC-4 multiframe check, selectable out of frame criteria and change of frame alignment alarm, plus transparent non-framing mode
- Frame alignment detection and loss of frame declaration comply with ITU-T G.706 /ETS 300 011
- Dual unipolar (HDB3/AMI) or NRZ line interface
- Fractional E1; gapped clock or marker and aux. Tx Input
- Clock, data, and frame pulse can be monitored for any E1
- Two-frame slip buffers in both receive and transmit directions with delay measurements
- Supports Time Slot 16 CCS/CAS signaling (CAS debounced /processor-forced on a per time slot basis)
- Detects and forces Time Slots 0 and 16 RAI and AIS; detects LOS, OOF, OOMF, OOMF16, and AUX pattern
- Detects, counts and forces line code errors (BPVs and excess zeros), CRC-4 errors, frame word errors, and CRC errors (E-bits, 2 Sa6 code counters)
- Motorola/Intel-compatible microprocessor interface
- Auxiliary port with TSI for ITU-T G.964/5 (V5.1/2)
- One-second interrupt input latches counter values and line events into shadow registers
- Local, line remote, payload remote and time slot loopbacks with ANSI T1.231 Fractional T1 compatible loopback support
- Per framer PRBS/code word generator and analyzer for E1 and N x time slot testing
- Four system interface options: Transmission, Data, MVIP, and H-MVIP/H.100 plus dual reference clock outputs
- ETS 300 011, 300 233 and ITU-T I.431 ISDN support
- Boundary scan capability (IEEE 1149.1)
- Single +3.3V power supply; 5 volt tolerant TTL inputs
- 208-lead or 256-lead plastic ball grid array package

DESCRIPTION

The E1Fx8 is an eight-channel E1 (2048 kbit/s) framer designed with extended features for voice and data communications applications. AMI and HDB3 line codes are supported with full alarm detection and generation per ITU-T G.703, G.775 and I.431. Integral receive dual unipolar rail dejitter buffers (ITU-T G.735-739 and G.823) are provided. The transmit and receive sections of each of the eight framers are independent, including framing, with individual slip buffers to allow operation in a wide range of switching and transmission products. Framing algorithm support for ITU-T G.704, G.706 and ETS 300 011 is included. Access and control for signaling and data are provided via a Motorola/Intel-compatible microprocessor interface. For HDLC link applications, each framer supplies a full duplex HDLC controller with dual 128-byte FIFOs (for Sa4-Sa8 access) in addition to onboard latching of all performance parameters, requiring minimal software overhead. Word-wide National bit read/write access is provided, with full Sa6 code support. Diagnostic, test, and maintenance functions are integrated, including E1 and per time slot local and remote loopback modes, per channel PRBS/code word generator/analyzer and boundary scan (IEEE 1149.1).

APPLICATIONS

- SDH terminal or add/drop multiplexers supporting E1 byte-synchronous operation or E1 monitoring with G.706 annex C
- DCS, digital central office or remote digital terminals (exchange terminations and access nodes)
- E1 multiplexers
- E1 and fractional E1 CSUs
- ATM products with integrated E1 interfaces
- LAN routers with integrated E1 interfaces
- Multichannel E1 test equipment
- Internet access equipment with E1 and Fractional E1 ports



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OVERVIEW

The E1Fx8 provides the features of two QE1F-*Plus* devices complemented by independent per time slot local or remote loopbacks, a gapped clock/marker system interface option, a per-channel PRBS/code word generator analyzer, a per-channel time slot inband loopback activate/deactivate detector/generator (compatible with the T1Fx8 and ANSI T1.231), an internal selection option for the one-second clock, and frame pulse monitoring added to the E1 monitor function. The receive line interfaces are enhanced with dejitter buffers for loop timed applications and direct multiplexer interface applications. In addition, an intact mode for slip buffering unframed E1s, an auxiliary input for fractional E1 and CCS or ISDN D channel access, and independent transmit or receive framing have been incorporated. For multichannel ISDN or V5.1/V5.2 applications an Auxiliary E1 rate port is provided that can directly connect to a multichannel HDLC controller for access to any user time slots from any of the channels for a maximum of 32 total. Signaling debounce and a signaling change of state interrupt are incorporated along with certain alarms mapped to and from Time Slot 16 CAS codes to automatically support ITU-T G.732 alarm propagation. The HDLC FIFOs have been expanded to 128 bytes for each transmit and receive channel as well as being able to support back-to-back frames. A delay value register was added to the slip buffers and digital A-law or mu-law digital milliwatt or a programmable idle code is available per time slot. The System Interface options are the same as those of the T1Fx8 with both separate signaling, alternate data bit and full data inversion capability. The E1Fx8 is available in the same 208-lead and 256-lead plastic ball grid array packages as the T1Fx8. The E1Fx8 packages have the same power, ground and signal lead configurations as the corresponding T1Fx8 packages, except that some leads which are no-connect spares on the T1Fx8 are used for additional power, ground and signal functions on the E1Fx8. Reduced power consumption is an added benefit of the E1Fx8, which is powered from a 3.3 volt supply, but is still tolerant of inputs from 5 volt parts.

The E1Fx8 supports multiple applications, including SDH/PDH networks and data applications where multiple framing functions are required in a single board. The E1Fx8 contains many features which allow it to be used in SDH Add/Drop multiplexers, E1 multiplexers, E1 and fractional E1 CSUs, PBXs, ATM products, LAN routers with integrated E1 interfaces, E1 Internet access equipment, Primary Rate ISDN interfaces, multichannel E1 test equipment, repeaters, access nodes and switches. In addition, the E1Fx8 includes many advanced diagnostic, test, and maintenance features, including boundary scan (IEEE 1149.1) and both E1 and time slot level loopbacks. The E1Fx8 is well suited for embedded CSU/DSU functions in routers and bridges and for test instruments needing a high degree of data manipulation.

The E1Fx8 supports TS0/CRC-4 and TS16/Signaling Multiframes operating in an offine mode. Either Common Channel Signaling (CCS) or Channel Associated Signaling (CAS) is supported. The transmit and receive sections of each of the eight framers are independent, with individual slip buffers and independent framed or unframed operation to allow use in a wide range of switching and transmission products.

Each framer supplies a full duplex HDLC message controller with onboard transmit and receive FIFOs, and TS0 National bit access, in addition to onboard latching of all required performance parameters, requiring minimal software overhead and microprocessor bandwidth to support HDLC protocols. The HDLC controller is enhanced to include deep FIFOs (128 bytes each way) and a back-to-back capability where a single flag can separate frames. When not used for HDLC functions, the National bits are accessible to transmit and receive code words, with full Sa6 bit functionality supporting ETS 300 233 for ISDN applications.

The E1 digital line interface port is extremely flexible, allowing the device to connect to any industry standard line interface device with no external glue logic. AMI, HDB3, and NRZ line codes are supported with full alarm detection and generation. An optional 64-bit dual rail dejitter buffer meeting ITU-T G.823 for jitter tolerance, G.735 and G.736 for jitter generation, and G.735/6/8/9 for jitter transfer is provided. Optional frame pulse or drive bit output is available in the NRZ mode. The NRZ mode allows the E1Fx8 to count externally detected code violations or to incorporate an external loss of clock/signal detector. The interface contains a serial port, which can directly control the external line interface unit and other components using the industry standard 'host' mode for device control.

The framer provides a microprocessor interface that is compatible with either Motorola or Intel processors. It is designed to act as an 8-bit peripheral using asynchronous bus transfers. Polling or interrupt support and latching of critical events are provided to accelerate interrupt processing and reduce the burden on the attached microprocessor. Individual alarm masks are available to ignore certain alarms or to operate different channels in different modes. Direct access to the slip buffers is provided for time slots and the signaling RAMs, which makes sending special signaling or time slot codes possible with low overhead. Scanning for signaling is facilitated with signaling debounce and interrupt on signaling change of state.

The framer supports a wide variety of individual and multiplexed system interface options to permit seamless interfacing to many types of time slot-based devices. Both MVIP and HMVIP/H.100 interfaces are provided for operation with many different system buses and devices. For maintenance support the E1Fx8 incorporates a per E1 PRBS code word generator/analyzer that provides 2^{11}-1, 2^{15}-1, QRSS (2^{20}-1) and 2^{23}-1 codes in addition to a programmable 32-bit code word. In addition, a per E1 time slot loopback activate and deactivate function compatible with the T1Fx8 and ANSI T1.403-1998 Fractional T1 Loopback are provided. Error forcing and diagnostic access are also provided.

To support monitoring functions, the E1Fx8 provides a bypass mode in which a received E1 signal is monitored and looped back to the transmitter. In this mode the Sa4 through Sa8 bits may be individually replaced and the CRC-4 is updated to reflect only the changed bits, retaining end to end performance monitoring per ITU-T G.706 Annex C.

Although many advanced features are included, the device is optimized for the multichannel application. System I/O is minimized, and peripheral functions requiring significant logic or I/O have been reduced or eliminated. This device is well suited to systems requiring many E1 interfaces where real estate is at a premium.

FEATURES

The following features are supported by the E1Fx8:

FRAMING MODES AND OPTIONS

- Offline framer (data passes uninterrupted from line to system even in loss of frame)
- Follows ITU-T G.706 (‘88 or ‘91) frame alignment detection and loss of alignment declaration
- Thirty-two 64 kbit/s time slots basic frame structure
- TS0/CRC-4 multiframe
  - Two FAS selectable algorithms (standard and frame hold-off; G.704/G.706)
  - CRC-4 generation/check
  - CRC-4 and non CRC-4 multiframing automatic interworking(G.706 and TBR 04 versions)
  - Reframe on excessive CRC errors (>914 per second)
- TS16/signaling multiframe synchronization and alarm
  - Two MAS selectable algorithms (standard and enhanced)
- Programmable out of frame control
  - 3 or 4 FAS in error, 3 FAS/3 NFAS, or
  - 4 FAS/4 NFAS in error
- Programmable frame synchronization
  - Transparent, CRC-4 disabled, CRC-4 enabled, CRC-4 enabled with E-bit alarms
  - Microprocessor resync option
- Full ETS 300 011 compliant automatic alarm generation
- Full ETS 300 233 compliant National bit support
- Independent transmit and receive transparent modes
- Automatic CRC-4/non CRC-4 interworking per ITU-T G.706-1991 appendix B or optionally per TBR-4 ITAAB note: 075
- ITU-T G.706 Annex C compliant special loopback mode with update capabilities for National bits Sa4-Sa8

LINE CODES AND OPTIONS

- NRZ (unipolar)
- Rail (HDB3 or AMI line codes)
  - LOS detector with programmable recovery interval and ones density threshold covering ITU-T G.775 and I.431 plus ETS 300 233
  - 16-bit BPV counters
  - Wandel and Goltermann or TTC T-BERD BPV options plus an excessive zeros option
- NRZ (unipolar) option
  - External BPV or LOS (sense option) using RNEGn lead or
  - Fast sync on receive (2 ms) option on RNEGn lead
  - Spare drive lead using TNEGn lead or
  - Transmit framing pulse option, 2 ms or 125 µs using TNEGn lead
  - Clock polarity clock in/out selection
  - NRZ data inversion option
- Force transmit leads to 0, 1, or 3-state

SIGNALING METHODS SUPPORTED

- Common Channel Signaling (CCS)
  - Time Slot 16
  - Marker/gapped clock option with auxiliary input for external HDLC
- Channel Associated Signaling (CAS) in Time Slot 16
  - with inversion option of transmit or receive
  - 0000 substitution option to prevent mimics of TS16 multiframe pattern
- CEPT IRSM Signaling
  - CAS with E signal bit in Sa4-Sa8 bytes
  - Available on signaling highway in transmission mode only

SIGNALING ACCESS AND PROCESSING OPTIONS

- Dedicated signaling bus
- Data stream embedded (Time Slot 16)
- Directly addressable internal registers (microprocessor interface)
- Per time slot individual signaling freeze option
  - With microprocessor rewrite capability for trunk conditioning
  - Receive and transmit independent control
- E1 signaling freeze on LOS, LO16MF, OOF and Line AIS
- Signaling debounce option (programmable number of multiframes)
- Signaling change of state interrupt and activity register indication

FOUR SYSTEM INTERFACE OPTIONS

- Separate transmit and receive paths for both data and signaling for all four modes
- Per device programmable sync start position for transmit (1 of 256) and receive (different 1 of 256)
- Separate signaling bit inversion and data (time slot) inversion
- 2048 kbit/s transmission
  - 2 ms multiframe rate
  - Defined signaling highway format; signaling for pair of time slots per frame plus alarms (AIS and RAI), National bits (Sa4-Sa8) and International bits (Si)
  - Receive system frame and clock are outputs when slip buffers bypassed
  - Receive system frame and clock are inputs when slip buffers enabled
  - Gapped clock/marker option with auxiliary input for fractional E1 and ISDN support
- 2048 kbit/s data
  - 125 µs frame rate
  - all ABCD signaling bits available per time slot every frame
  - 32 time slots
  - Receive system frame and clock are outputs when slip buffers bypassed
  - Receive system frame and clock are inputs when slip buffers enabled
  - Gapped clock/marker option with auxiliary input for fractional E1 and ISDN support
- 2048 kbit/s MVIP
  - 125 µs frame rate
  - all ABCD signaling bits available per time slot every frame
  - 32 time slots
  - Receive system frame and clock are inputs; slip buffers always enabled
- 8 Mbit/s H-MVIP/H.100
  - Four E1 MVIP formats byte-interleaved with 128 time slots
  - 125 µs frame rate
  - Receive system frame and clock are inputs; slip buffers always enabled
  - H.100 compliant timing

TRANSMIT AND RECEIVE SLIP BUFFERS

- System transmission and data interfaces
- Full frame (30 or 31 time slots depending on CAS or CCS operation plus Time Slot 0 FAS and NFAS storage)
- Bypass option
- Framed slips with Time Slots 0 through 31 repeated or skipped as a block
- E1 intact mode (slip buffering of an unframed E1 for all 32 time slots)
- MVIP and H-MVIP interfaces
  - Slip buffers always enabled
  - 31 time slots
- Features and options
  - Current delay (0.5 µs resolution) plus read and write pointer registers
  - Microprocessor toggle option
  - E1 freeze option for microprocessor write option to individual time slots
  - Time Slot 0 freeze option with microprocessor rewrite capability
  - Slip buffer status with common interrupt on slip of transmit or receive buffer

RECEIVE DEJITTER BUFFERS

- 64-bit dual rail or single rail with bypass option
- Meets ITU-T G.823 jitter tolerance, G.735/6 for jitter generation, and G.735/6/8/9 for jitter transfer and attenuation
- Operates from a standard 2048 kbit/s backplane reference oscillator or 64512 kHz reference

FRACTIONAL E1 SUPPORT

- Programmable receive gapped clock or enable pulse output per framer per time slot
- Programmable transmit gapped clock or enable pulse output per framer per time slot
- Fractional E1 data channel auxiliary input that multiplexes data into frame

MICROPROCESSOR INTERFACE

- Directly addressable control and status registers
- All interrupts are maskable
- Motorola split address/data
- Intel split address/data
- Global alarm indications
  - with separate channel activity pointers for line events, Time Slot 16 events and HDLC events
- Global interrupt mask bits
- Interrupt on alarms
  - Positive transition
  - Negative transition
  - Both transitions
- Hardware interrupt polarity selection
- Hardware and software resets

EXTERNAL LINE INTERFACE UNIT PORT

- Serial port for the control of external line interface components using ‘host’ mode
- Individual chip select and interrupt signals for each transceiver
- Integration of line interface unit alarms
- Microprocessor registers for read/write of line interface components
- Broadcast capability to initialize all line interface components

MAINTENANCE FUNCTIONS

- Loopbacks
  - Local with AIS to transmit line option
  - Line remote (all time slots)
  - Payload remote (Time Slots 1 to 31)
  - Per time slot (single or multiple) remote (from receive line to transmit line)
  - Per time slot (single or multiple) local (from system interface to system interface)
- Pattern generation/detection per E1
  - PRBS/Code word generator/analyzer: 2^{11}-1, 2^{15}-1, QRSS (2^{20}-1), 2^{23}-1 pseudo-random patterns or 32-bit code word
  - Full E1 framed or unframed (PRBS only)
  - Two insertion options: input to receive slip buffer or in place of transmit slip buffer input
  - Two monitoring options: at line decoder output or at transmit slip buffer input
  - A-law or mu-law digital milliwatt in place of data for any time slot
  - Programmable idle code insertion in place of data for any time slot
  - Force programmable code in any time slot via slip buffer access
  - Monitor for codes via read of the slip buffer RAM or code word analyzer
- Error and alarm insertion capability
  - BPV
  - CRC-4
  - FAS/NFAS
  - LOS
  - AIS
  - AUXP
- Data link access
  - Full duplex onboard HDLC message controller supporting back-to-back frames
  - 8-bit access via microprocessor interface
  - Transmit from HDLC controller or system side (trans. mode; bypass National bits)
  - FIFO status bits
  - Zero stuffing/destuffing
  - Flag detection/generation, abort message detection/CRC-16
  - 4 kbit/s to 20 kbit/s data link using any combination of the TS0 National spare bits
  - A 128-byte message buffer per transmit and receive directions per E1
- E1 monitor access for multiplexed applications
  - Select any E1 transmit or receive direction
  - Receive line side
  - Receive terminal side with frame pulse output
  - Transmit side with frame pulse output
  - Clock, NRZ data and frame pulse brought to tristate leads for multiple E1Fx8s on a bus
- Per National bit byte code read and write synchronized to a multiframe
- Time slot loopback activate/deactivate generation/detection per E1
  - PRBS generator/analyzer (2^7-1, 2^7-1 inverted) pseudorandom patterns
  - Any group of time slots
  - Compatible with T1Fx8 and ANSI T1.231/ T1.403
- IEEE 1149.1 boundary scan
- High impedance on all leads for board testing
- SDH byte-synchronous mapper support
  - Direct interface
  - RAI and AIS support to and from signaling highway
  - TS AIS generation to transmit line TS16 (all channels) on SDH alarms
  - TS AIS generation to signaling highway (all channels) on E1 alarms
  - TS RAI generation to signaling highway (all channels) on E1 RAI alarm

ALARM INDICATIONS

- Full ETS 300 011 compliant automatic alarm generation
- Programmable alarm generation and consequent actions
- LOS, loss of signal with programmable detect and recovery periods (ITU-T G.775 and I.431)
- OOF, out of frame
- LOSMF, loss of signaling multiframe (Time Slot 16)
- LCRCMF, loss of CRC multiframe (Time Slot 0)
- RAI, remote frame alarm
- MFRAI, remote multiframe alarm (Time Slot 16)
- Line AIS, all ones received, selectable thresholds to meet ITU-T G.775 or I.431
- TS16 AIS detection
- COFA, change of frame alignment
- Signal multiframe error
- Slip alarm for transmit or receive slip event
- Line code violation counter with excessive zeros option
- Far end block error (E-bit) counter
- Far end block error for ISDN TE (Sa6 code 0010) counter
- Far end block error for ISDN T interface (Sa6 code 0001) counter
- Sa6 code detectors for ISDN
- Auxiliary pattern detector (continuous 01 pattern on line) for ISDN applications
- Frame alignment word error counter
- CRC-4 multiframe error counter
- PRBS/code word error counter

PERFORMANCE AND FAULT MONITORING

- LOS, line AIS, TS16 AIS, OOF, LOSMF, LCRCMF, CFA, AUXP, Tx slip, Rx slip, signaling change, MFRAI, and RAI are latched and shadowed (TS16 alarms optionally included with TS0 alarms)
- One-second update via selected line clock, one-second clock input, or 2048 kHz backplane clock
- Any change is recorded in a performance shadow register every second
- Any fault that persists uninterrupted is recorded in a fault shadow register every second
- Error counter roll-over generates a maskable processor interrupt
- One-second input will latch counter values into shadow registers

AUXILIARY PORT

- Full duplex 2048 kbit/s port timed from backplane oscillator, synchronization selections or an input
- Any Time Slot (1 - 31) from any of the 8 channels (system or line side) may be assigned to any of the 32 output slots
- Any Time Slot (1 - 31) of any of the 8 channels (system or line side) may be assigned from any of the 32 input slots
- Supports V5.1 or ISDN PRI or BRI via the TranSwitch MCHDLC device

CLOCKS

- Flexible receive and transmit clock selection
  - System clock
  - Line clock before or after dejitter buffer
  - Backplane reference clock
- Two external clock inputs (2048 kHz and optional 1 Hz)
- 1 Hz reference can be derived from either 2048 kHz external clock or 1 of 8 line clocks before or after dejitter buffer and can be provided as an output
- Dual reference outputs at 2048 kHz or 8 kHz
  - Select any E1 framer for reference 1 (before or after dejitter buffer)
  - Select any E1 framer for reference 2 (before or after dejitter buffer)
  - Select 2048 kHz or 8 kHz (optionally synchronized to start of frame)

POWER, PACKAGE AND ENVIRONMENT

- 3.3 volt ± 5% single supply with 5.0 volt tolerant inputs
- Power dissipation < 780 mW with all channels operational
- 17 x 17 mm 208-lead (1 mm ball pitch) PBGA and
  27 x 27 mm 256-lead (1.27mm ball pitch) PBGA
- Operating ambient air temperature range of -40 to +85 ^{o}C

E1Fx8 FEATURE ENHANCEMENTS AND DIFFERENCES VERSUS THE QE1F-*Plus*

- Twice the channel count of the QE1F-*Plus* with more than the functionality of the QE1F-*Plus* but:
  - Less power than that of a single QE1F-*Plus* by using 3.3V 0.35 micron technology
  - Less board space than that of a single QE1F-*Plus* by using PBGA technology
- Framing pulse monitor and selection of pre or post synchronizer monitor access
- Deeper HDLC FIFOs (128-byte transmit and receive per E1 vs. 16-byte) and back-to-back messages
- Loopbacks per time slot or group of time slots, both local and remote
- Signaling debounce and signaling change of state interrupt
- One-second clock from one of eight receive lines or local oscillator with optional output
- PRBS generator/analyzer per E1 for E1 or time slot(s) testing using 2^{11}-1, 2^{15}-1, QRSS (2^{20}-1), 2^{23}-1 pseudorandom test patterns plus 32-bit code word
- Fractional E1 support providing gapped clocks and enable pulses for assigned time slots (transmit and receive independent assignments) versus QE1F-*Plus* gapped clock
- Transmit and receive slip buffer delay value in registers for microprocessor wander control
- Independent transmit and receive framing bypass with unframed slip buffering option
- Byte-wide access for reception and transmission of each National bit plus code detectors and counters per ETS 300 233 for Sa6
- Independent data (time slot), alternate bit (even or odd) and signaling inversions
- ISDN features (ITU-T I.431 and ETS 300 233) with LOS, AIS, and National bit compliant operation plus AUXP alarm
- Auxiliary data input lead for fractional E1 or ISDN D channel access
- Programmable idle code, A-law or mu-law digital milliwatt per time slot
- SDH or ITU-T G.732 alarm mapping to or from Time Slot 16 CAS and Time Slot 0 alarms
- QE1F-*Plus* PCM highway mode and 8 or 16 Mbit/s transmission modes not supported
- RNEGn is programmable for BPV counting, fast synch. or external LOS in NRZ mode; QE1F-*Plus* supplies a separate LINTn lead for external LOS
- The frame pulse output option on the E1Fx8 TNEGn lead is programmable to 2.0 ms or 125 µs; on the QE1F-*Plus* it is only 2.0 ms
- Separate latched, shadowed and activity registers for Time Slot 16 and miscellaneous events (excessive CRC, one-second interrupt, signaling change of state, TS16 AIS and out of signaling multiframe)
- Separate auxiliary port for direct MCHDLC access of 32 time slots for ISDN and V5.1
- ANSI T1.231/ T1.403 compatible N x time slot loopback activate and deactivate generation and detection for compatibility with North American fractional T1 equipment
- Bypass CRC mode for monitoring and insertion of new National bits while maintaining performance

E1Fx8 FEATURE DIFFERENCES VERSUS THE T1Fx8

- E1Fx8 provides both per time slot remote and per time slot local loopbacks; T1Fx8 only provides per time slot remote loopback.
- E1Fx8 allows the slip buffer recentering to toggle; T1Fx8 only recenters to least delay.
- E1Fx8 allows the PRBS generator or analyzer to be connected to either transmit or receive path; T1Fx8 is fixed so the generator is on the transmit path and the analyzer is on the receive path.
- E1Fx8 has an auxiliary port for direct MCHDLC access of 32 time slots for ISDN and V5.1.
- E1Fx8 has per E1 receive dejitter buffers.
- E1Fx8 permits an internally generated one-second clock to be an output; T1Fx8 it is only an input.
- E1Fx8 has no equivalent of Automatic Performance Report Message generation.
- E1Fx8 has no equivalent of N x 56 kbit/s time slots.

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- ITU-T G.735 Characteristics of Primary PCM Multiplex Equipment Operating at 2048 kbit/s and Offering Synchronous Digital Access at 384 kbit/s and/or 64 kbit/s.
- ITU-T G.736 Characteristics of a Synchronous Digital Multiplex Equipment Operating at 2048 kbit/s.
- ITU-T G.738 Characteristics of Primary PCM Multiplex Equipment Operating at 2048 kbit/s and Offering Synchronous Digital Access at 320 kbit/s and/or 64 kbit/s.
- ITU-T G.739 Characteristics of an External Access Equipment Operating at 2048 kbit/s and Offering Synchronous Digital Access at 320 kbit/s and/or 64 kbit/s.
- ITU-T G.775 Loss of Signal (LOS) and Alarm Indication Signal (AIS) Defect Detection and Clearance Criteria.
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- ITU-T O.152 Error Performance Measuring Equipment for 64 kbit/s paths. 10/92.
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- IEEE 1149.1 Standard Test Access Port and Boundary-Scan Architecture, May 1990.
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- Enterprise Computer Telephony Forum, H.100 Rev. 1.0 Hardware Compatibility Spec. CT Bus
- ANSI T1.231 -1997
- ANSI T1.403-CORE and -ROB; Draft for letter ballot Sept. 1998
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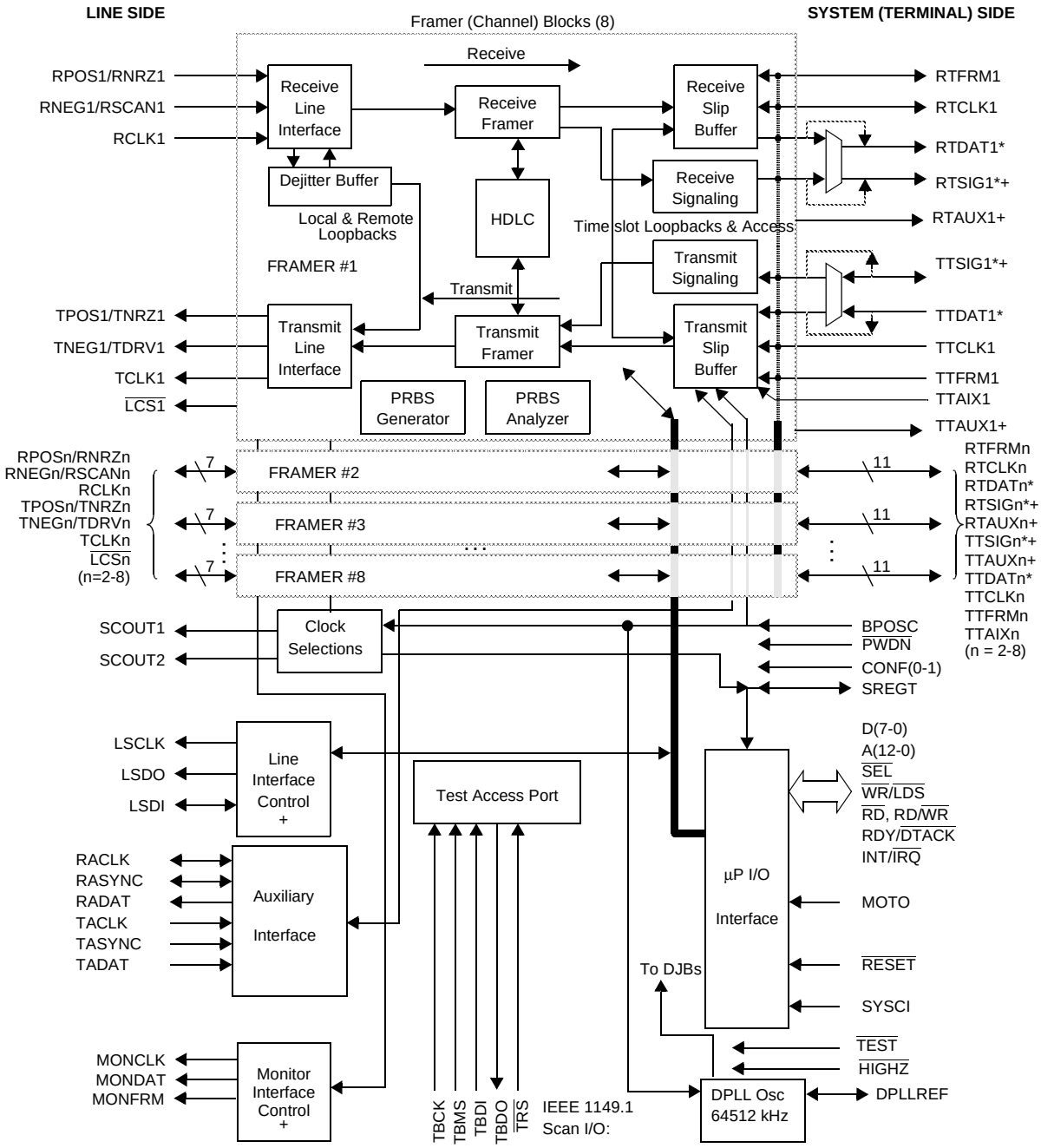
BLOCK DIAGRAM



* Note: Signaling and data for each group of four framers is multiplexed on framer 1 and 5 signaling and data leads for HMVIP/ H.100 Mode.
\+ Note: For 208-lead PBGA Line Interface Control and Monitor Interface Control share leads, and TTSIGn/RTSIGn share leads with TTAUXn/RTAUXn.
RTAUXn can also be used to externally monitor PRBS out of lock.

Figure 1. E1Fx8 TXC-03109 Block Diagram

BLOCK DIAGRAM DESCRIPTION

A simplified block diagram of the 8-Channel E1 Framer (E1Fx8) is shown in Figure 1. The E1Fx8 consists of the following major blocks: eight Framer blocks, Line Interface Control, Clock Selections, Microprocessor Input/Output Interface, Auxiliary Interface, Monitor Interface Control, DPLL Oscillator and Test Access Port.

Line Interface

Each of the eight identical framer blocks consists of the following sub-blocks: Receive and Transmit Line Interface blocks, Receive and Transmit Framer blocks, HDLC block, Receive and Transmit Slip Buffer blocks, PRBS Generator, PRBS Analyzer, and Receive and Transmit Signaling blocks.

The Receive and Transmit Line Interface blocks connect each of the eight framers to an external line interface transceiver, which performs the LIU and clock recovery functions. The interface to the external line interface transceiver can be configured for two interface modes: a dual unipolar (rail) interface or a NRZ interface.

When the dual unipolar interface mode is selected, input data from the external line interface transceiver is clocked into the E1Fx8 on leads RPOSn and RNEGn using the recovered receive clock present on the RCLKn input lead (where n=1-8 identifies one of the eight framers). In the transmit direction, unipolar data is clocked out of the E1Fx8 on leads TPOSn and TNEGn by the transmit line clock present on the TCLKn output lead. For reduced power dissipation in protection switching applications, the TCLKn, TPOSn, and TNEGn leads for the eight framers may be forced low, by per channel control bits as well as a power-down lead ($\overline{\text{PWDN}}$) which affects all eight framers. Control bits are provided in the memory map which enable the unipolar data to be clocked in and out of the E1Fx8 on either edge of the clocks. For the dual unipolar interface mode, the E1Fx8 provides either a High Density Bipolar of order 3 (HDB3), or an Alternate Mark Inversion (AMI), coder and decoder function, and Loss Of Signal detection. The Loss Of Signal detector is programmable to meet the requirements specified in the ITU-T Recommendation G.775, I.431 or ETS 300 233. A 16-bit performance counter is provided for each framer, for counting HDB3 or AMI coding violation errors with an option to include excessive zeros (blocks of four contiguous zeros in HDB3 and blocks of sixteen contiguous zeros in AMI).

When the NRZ interface mode is selected, NRZ data is clocked in at the RNRZn lead by the recovered received clock present on the RCLKn lead. The NRZ data is clocked out of the E1Fx8 on the TNRZn lead by the transmit clock present on the TCLKn lead. Control bits are provided in the memory map which enable the NRZ data to be inverted in and out of the E1Fx8 or to be clocked in and out of the E1Fx8 on either edge of the clocks. In NRZ interface mode, the HDB3 or AMI coder and decoder functions are bypassed. However, bipolar violations which are detected in the external line interface transceiver may be clocked into the E1Fx8 on the RNEGn/RSCANn lead and counted in the associated 16-bit coding violation performance counter. The RNEGn/RSCANn lead may be used to bring in external LOS indications in place of code violation counts or to force frame synchronization. In NRZ mode the TNEGn/TDRVn lead may be used to provide a fixed drive signal or it can output a 2 ms or 125 µs frame sync pulse. The Remote Line Loopback function for each framer is implemented in the Line Interface blocks.

A 64-bit dejitter buffer is provided to remove line, demapping or demultiplexing jitter when an external dejitter buffer is not provided by a LIU or other device and when receive slip buffer usage is not practical for a given application. Both RPOSn/RNRZn and RNEGn are dejittered using a digitally controlled oscillator and 64-bit FIFO. The transfer function is that of a single pole low pass filter with the pole at 9 to 11 Hz; wander is passed through but jitter is attenuated. Remote loopbacks also go through the dejitter buffer and clock reference selections are taken from the dejittered clock outputs when it is enabled. The onboard DPLL runs at 64512 kHz to operate the dejitter buffers. The signal may be output, or the DPLL may be disabled and the dejitter buffers may be operated from an external clock via lead DPLLREF.

Receive Framer

The Receive Framer block for each framer performs two basic functions: frame synchronization and Channel Associated Signaling (CAS) multiframe alignment. The frame synchronization circuit has two framing options: frame synchronization based on the frame alignment signal (FAS) carried in Time Slot 0, or frame synchronization based on the frame alignment signal and validation by the CRC-4 multiframe alignment signal. The frame synchronizing circuit meets the framing requirements specified in ITU-T Recommendations G.704 and G.732 as well as ETS 300 011 and TBR 4 with ITAAB note 75 supported optionally for automatic CRC-4/non CRC-4 interworking. The frame synchronization Out Of Frame alarm criteria are programmable to use 3 or 4 framing words in error, with or without validation by the CRC-4 multiframe alignment signal and with or without NFAS. Framing word errors and CRC-4 errors are counted in performance counters. The Receive Framer block monitors and detects a remote alarm A-bit (bit 3) in Time Slot 0 as specified in ITU-T Recommendation G.704 and G.732, counts E-bit errors (which represent far end performance), and counts CRC-4 errors (which represent near end performance). Detectors for AIS, the Auxiliary pattern, and loss of multiframe alignment via excessive CRC-4 errors are provided. A non-framing mode is enabled individually for the receive path when the E1Fx8 is configured in the Transmission or Data Modes. The non-framing mode bypasses the Receive Framer block, but the Receive Slip Buffer may be included optionally to provide an intact mode, which slip buffers the entire E1 signal with a random start position.

When frame alignment is acquired, the CAS multiframe pattern in Time Slot 16 is detected for alignment. After multiframe alignment is established, the signaling bits are forwarded to the Receive Signaling block for buffering, debouncing, microprocessor access, and formatting into the signaling highway data stream.

Per Sa4-Sa8 (National bits) byte-wide registers are provided to store the entire multiframe content of each individual Sa4-Sa8 bit stream. This implementation supports a wide variety of options like ISDN access, CEPT IRSM and ITU-T G.704 Synchronization Status Messages. In addition, Sa6 is provided with code detectors and debounce circuitry plus 10-bit counters for two specific codes in support of ETS 300 233 (ISDN far end block errors). Sa5 and Sa7 codes are also supported.

The E1Fx8 complies with the G.706 ITU-T Recommendation, which specifies the frame alignment and CRC procedures relating to basic frame structures defined in Recommendation G.704.

Receive Slip Buffer

Each Receive Slip Buffer controls time slot access and retiming for a framer by using a two-frame receive buffer that can be optionally bypassed in the 2 Mbit/s Transmission and Data Modes. The Receive Slip Buffer is always enabled in MVIP and HMVIP/H.100 modes. When the receive slip buffer is enabled, received time slots are written into the buffer by recovered receive clock RCLKn, and read out as data (RTDATn) from the slip buffer by the system input clock RTCLKn. A phase shift between the two clocks is detected in this block and a deletion or repetition of one frame of data (32 time slots for intact mode, 31 time slots for CCS or ISDN, or 30 time slots if Time Slot 16 is assigned for signaling) is provided when the buffer reaches an almost full or almost empty condition, respectively. Microprocessor access is provided to the delay register indicating delay in 0.5 µs increments (a measurement is made of delay in single bit increments) as well as the read and write pointers. Channel 0 and channel 16 (when channel 16 is assigned for Channel Associated Signaling) are not affected by a slip in the framed mode of operation. Buffer alarm indications of slip repeat, slip skip and slip error are provided. The slip buffer may be toggled by the microprocessor, or automatically recentered as described above. Individual time slots are accessible by the microprocessor for the insertion of system idle or out of service codes. When the receive slip buffer is bypassed, the receive clock (RTCLKn) and data (RTDATn) are provided as outputs, along with a receive sync signal (RTFRMn), all derived from RCLKn or from BPOSC if an LOS condition is present.

For maintenance purposes, a transmit time slot from the Transmit Slip Buffer or Data Highway may selectively replace a time slot from the Receive Line Interface. One bit per time slot is provided for this purpose in the Microprocessor Interface for Time Slots 0 through 31.

Receive Signaling

For Channel Associated Signaling (in Time Slot 16), a multiple 120-bit signaling buffer is used to store the signaling bits which have been extracted by the Receive Framer (one main buffer that contains the current or debounced ABCD bits, a temporary buffer that contains the current and previous multiframe ABCD bits used for debouncing, and a count buffer indicating the number of frames in a row that match). The signaling bits are stored sequentially in the signaling buffer in the order that they were received. The main signaling buffer may be read, frozen, and written to by the microprocessor. If signaling is to be disabled for a particular channel, the ABCD signaling bits for that time slot are frozen in their present states and these frozen values are repeatedly sent to the System Interface Receive Signaling Highway (RTSIGn); since the microprocessor is able to overwrite the frozen values, special signaling states may be substituted for received signaling. When a loss of signal, Line AIS, loss of multiframe alignment, or an out of frame condition is detected, the signaling bits are automatically frozen in their present states. The signaling bit states are held and repeated to the Receive Signaling Highway (RTSIGn) until framing has been recovered.

When signaling debounce is provided, the main 120-bit buffer is used to store the debounced signaling bits; this buffer is updated if, in the current multiframe, the signaling bits received in Time Slot 16 match the signaling bits received in the previous multiframes (the number is programmable). The signaling bits are debounced as a nibble. The main signaling buffer, and hence the Receive Signaling Highway (RTSIGn), are not updated unless the signaling bits match for N consecutive multiframes. If a change occurs, an optional interrupt is generated to the microprocessor indicating a Change of Signaling State.

For cross connect and ITU-T G.732 applications, particular ABCD codes can be used to indicate Line RAI or Line AIS. When Line AIS, loss of multiframe alignment, loss of signal, or out of frame occurs, a programmable ABCD code can be sent to the System Interface Signaling Highway, RTSIGn, in place of a frozen signaling code. For Line RAI (Time Slot 0 A-bit) or the Multiframe alarm (Y-bit in Time Slot 16) a different programmable ABCD code can be sent to the System Interface Signaling Highway (RTSIGn).

System Interface

On the terminal side, the System Interface interconnects the eight framers with the system. For each framer there is a separate Receive and Transmit Highway for the 2 Mbit/s Transmission, Data, and MVIP interface modes of operation. The Receive Highway consists of a data bus (RTDATn), a signaling bus (RTSIGn), a clock (RTCLKn), a gapped clock/enable signal (RTAUXn), and a synchronization signal (RTFRMn). The Transmit Highway consists of a data bus (TTDATn), a signaling bus (TTSIGn), a clock (TTCLKn), a gapped clock/enable signal (TTAUXn), an auxiliary data bus (TTAIXn), and a synchronization signal (TTFRMn). When RTFRMn is an input, and for TTFRMn, the frame start position is programmable independently for transmit or receive (all transmitters are programmed to one of 256 values and all receivers are programmed to either the same one of 256 values or a different value).

Transmit Slip Buffer

A Transmit Slip Buffer is provided to absorb low speed jitter in the transmit data. Each Transmit Slip Buffer block controls time slot access and retiming for the framer by using a two-frame buffer that can be optionally bypassed in the Transmission and Data Modes. When the transmit buffer is enabled, transmit time slots are written into the buffer by the transmit system clock (TTCLKn), and they are read out from the buffer by the receive clock (RCLKn), local oscillator (BPOSC), or transmit system clock (TTCLKn). A phase shift between the two clocks is detected in this block, and a deletion or repetition of one frame of data (i.e., 31 time slots, or 30 time slots if Time Slot 16 is assigned for signaling) is provided when the buffer reaches an almost full or almost empty condition, respectively. Microprocessor access is provided to a delay register which indicates the delay through the slip buffer in increments of 0.5 µs as well as the read and write pointers. Buffer alarm indications of slip repeat, slip skip and slip error are provided. The slip buffer may be recentered or toggled by the microprocessor, or automatically as described above. Individual time slots can be accessed by the microprocessor for the insertion of system idle or out of service codes or for reading to detect special codes or test patterns.

Transmit Framer

The Transmit Framer block forms the frame (with or without the CRC multiframe) with time slots read from the Transmit Slip Buffer block, or the Data Highway if the slip buffer is bypassed, and signaling information from the Transmit Signaling block. The International bits from the Signaling Highway are inserted into Time Slot 0 via a buffer when the framing mode is selected. The National bits in Time Slot 0 can be inserted from the HDLC block, from the System Interface or via a byte-deep buffer per National bit position. The CRC-4 is calculated as specified in ITU-T Recommendation G.704 and inserted in Time Slot 0. The Remote Alarm Indication for Time Slot 0 is inserted as a result of a receiver loss of frame alignment alarm, or by the microprocessor, or via the Signaling Highway (TTSIGn); both G.706 and I.431 algorithms can be selected. The E-bits are updated to indicate the sub-multiframes received with bad CRC-4. A single frame bit error, or CRC-4 error, can be generated for test purposes. The Transmit Framer and Transmit Slip Buffer can be bypassed if the unframed mode of operation is selected in the 2 Mbit/s Transmission Mode.

For maintenance purposes the Transmit Framer may selectively replace a time slot from the Slip Buffer or Data Highway with a time slot received by the E1Fx8 Receive Line Interface. One bit per time slot is provided for this purpose in the Microprocessor Interface for Time Slots 1 through 31; Time Slot 0 is not looped back.

Per Sa4-Sa8 (National bits) byte-wide registers are provided to transmit the entire multiframe content of each individual Sa4-Sa8 bit stream as a code. This is particularly useful in ISDN applications.

Transmit Signaling

For Channel Associated Signaling (in Time Slot 16), a 120-bit signaling buffer is used to store the signaling bits which have been input on the Transmit Signaling Highway (TTSIGn). The signaling bits are stored sequentially in the signaling buffer in the order that they were received. The signaling buffer may be read, frozen, and written to by the microprocessor. If signaling is to be disabled for a particular channel, the ABCD signaling bits for that time slot are frozen in their present states and repeatedly sent in channel 16. The microprocessor has the ability to write to the signaling buffer when signaling is disabled for the purpose of direct control of Channel Associated Signaling for one or more time slots providing call control or trunk conditioning functions.

FDL HDLC Controller

Each framer has a full duplex HDLC block. The HDLC block is configurable to send and receive messages using any of the five spare bits reserved for National use (Sa bits) in Time Slot 0 in alternating frames. A 128-byte FIFO is provided in each direction. Interrupt and status alarm support is provided to facilitate FIFO servicing for long messages. The HDLC controller supports zero bit stuffing/destuffing, ITU-T CRC-16 generation/checking, flag generation/detection, abort generation/detection, start of frame detection, end of frame detection, and FIFO underflows and overflows. A separate message length register is provided in addition to a byte count register to permit the reception of back-to-back FDL messages. The FDL function may be bypassed.

Line Interface Control

The Line Interface Control block provides a serial port for communicating with an external line interface transceiver that has the ‘host mode’ feature. This allows the system microprocessor to control the transceiver through the E1Fx8 without any external glue logic. The interface consists of a data output lead (LSDO), clock output lead (LSCLK), and a data input lead (LSDI). These signals are shared between all of the transceivers. Each transceiver is selected by the E1Fx8, using individual chip select output signals ($\overline{\text{LCSn}}$). Address, received data, and transmit data registers are provided to read or write individual registers in each line interface transceiver as well as to provide a broadcast mode to ease redundancy or initialization.

Monitor Interface Control

For system applications that do not have direct E1 line access (e.g., E123MUX or QE1M devices), the MONCLK, MONDAT and MONFRM leads can be configured to provide an E1 monitoring of any transmit or receive E1 line. These leads are tristateable to allow bussing of multiple E1Fx8s. Monitoring of the received side can take place prior to or after frame synchronization, with the latter supplying a signal on MONFRM; the transmit side monitoring always supplies the frame synchronization signal MONFRM.

Test Access Port

The Test Access Port block includes a five-lead Test Access Port (TAP) that conforms to the IEEE 1149.1 standard. This Test Access Port block provides for external boundary scan to read and write the E1Fx8 input and output leads from the TAP for board and component testing. In addition, a four-byte read-only memory location is provided for reading the JEDEC manufacturer ID, E1Fx8 part number, and version number of the device as part of the Microprocessor Interface.

Maintenance: PRBS Generator and Analyzer Blocks, Loopbacks

To assist in testing, built-in Pseudo-Random Binary Sequence (PRBS) Generator and Analyzer blocks are provided on a per E1 basis, framed or unframed. The PRBS Generator and Analyzer supports the 2^{15}-1 bit pseudo-random binary sequence which is specified in the ITU-T Recommendation O.151. In addition to the O.151 a 2^{20}-1 (QRSS), 2^{11}-1 (O.152), and a 2^{23}-1 pseudo-random binary sequence are provided. An optional 32-bit code word may be substituted for the PRBS in framed mode only. Each E1 framer may select where the PRBS Generator and Analyzer are connected so that both line testing (Generator on the transmit side and Analyzer on the receive side) and system testing (Generator on the receive side and Analyzer on the transmit side) can be supported. The output of the Analyzer is provided in a per channel register as well as counted in a 16-bit out of lock counter. The PRBS may operate in a framed or unframed mode for the entire E1 channel or it may operate over a single time slot or group of time slots to support fractional E1 and per time slot maintenance.

The E1Fx8 provides local loopback (transmit framer looped to receive framer), remote line loopback (receive line signal looped to transmit line), and payload loopback (Time Slots 1 through 31 from receive line looped back but with a locally generated Time Slot 0) options for each E1 channel. In addition, any one or more received time slot (except Time Slot 0) may be selected and looped back, and transmitted in place of the time slot input from the data highway, or any one of the transmit time slots may be substituted for a received time slot.

The E1Fx8 provides time slot loopback activate and deactivate code detection and generation in support of the ANSI T1.231/T1.403-CORE standard, permitting single-ended transatlantic loopback testing of fractional T1s/E1s using the E1Fx8.

Microprocessor Interface

The E1Fx8 can be configured to operate with either Intel- or Motorola-compatible microprocessors via the Microprocessor Input/Output Interface block. Interrupt capability is provided with global and individual framer mask bits. Global event and polling registers are provided to indicate the type of alarms present and on which E1 channels these alarms or events are taking place. One-second error counters, performance monitors and fault monitors are supported by shadow registers. These shadow registers permit performance and fault statistics to be gathered on one-second intervals with minimal microprocessor overhead. An option is provided which permits the interrupt polarity to be inverted. An external system clock (SYSCI) of 19 to 25 MHz is used to run the internal state machines. This section of the design is the same as the T1Fx8 except for the fact that the Signaling Activity Register and the SA6 Status Register are read to clear registers.

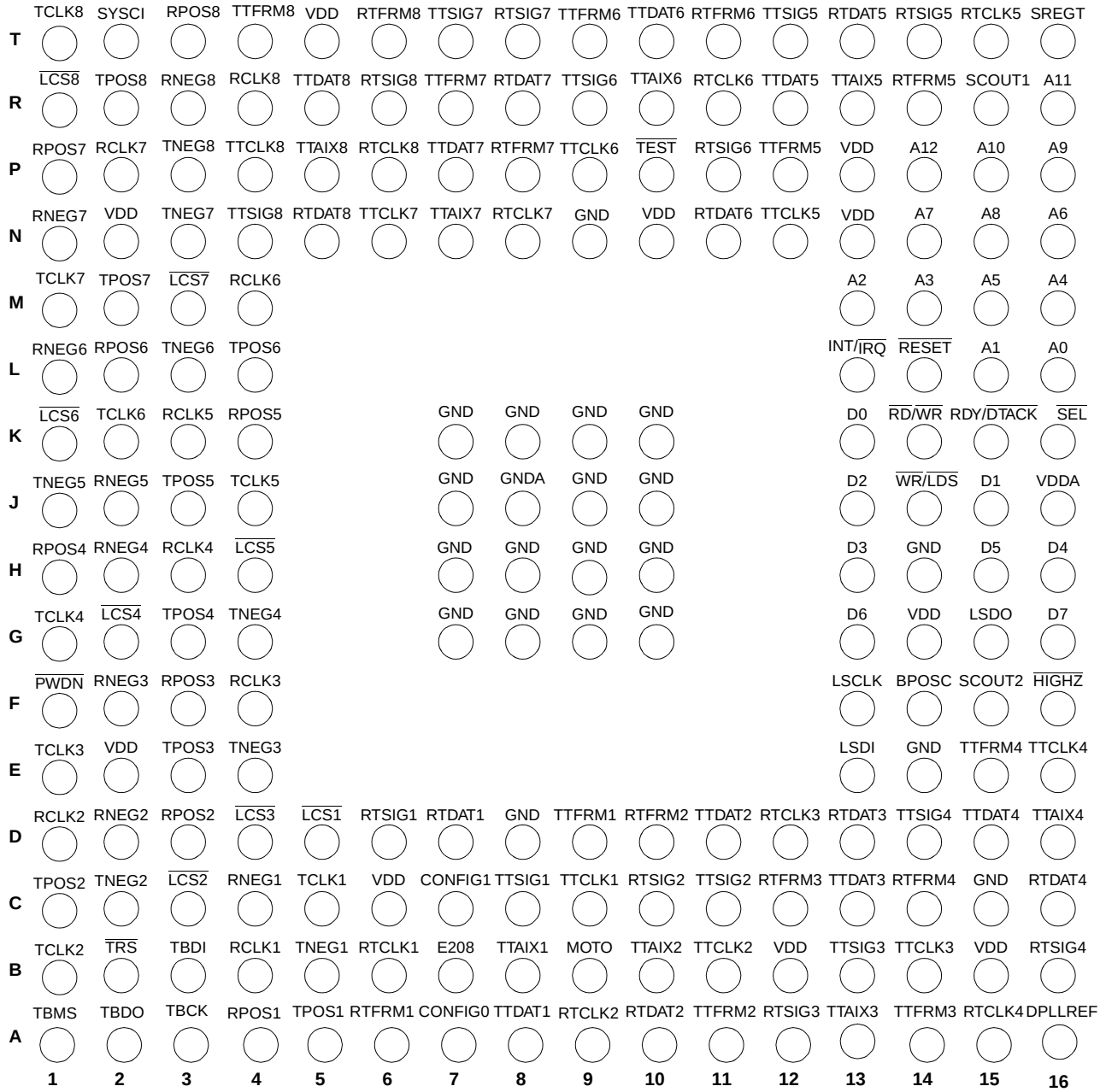
Clock Selections

The E1Fx8 provides a pair of reference clock outputs which are each selected from one of the eight RCLKn inputs after the dejitter buffer, if it is enabled. If not selected, the output is tristated to allow multiple E1Fx8s to share a single bus. If a selected channel experiences a LOS, the output is forced low. One-second performance monitoring can be triggered by an external 1 Hz clock (SREGT) as an input, or it can be triggered by counting the 2048 kHz local oscillator (BPOSC) input or a selected received line clock (RCLKn). When the one-second clock is derived internally, SREGT is an output to synchronize additional E1Fx8 and/or other devices; this is the only difference outside of divide ratios between the T1Fx8 and the E1Fx8. BPOSC is used to substitute for RCLKn when the receive line clock is selected for the system side output and LOS occurs.

Auxiliary Port Interface

For system applications that need to support ISDN PRI, ISDN BRI (multiplexed) or ITU G.964/5 V5.1/2 functionality, an auxiliary port is provided with 32 transmit and 32 receive 64 kbit/s time slots, each individually programmable to any receive or any transmit Time Slot (1 to 31) to or from any of the eight E1 framer channels, either line or system side. No broadcast or concatenation functionality is provided as all applications are 64 kbit/s or subrates of 64 kbit/s. Each connection is passed through a FIFO function with independent depth control to account for line side or system side clock differences from the auxiliary port clock. Thus buffering is provided by this block to match this block's clock with the 16 transmit E1 and the 16 receive E1 line clock domains. For data output from this port on the RADAT lead, the clock and frame reference signals, RACLK and RASYNC, may each be an input or an output which is either derived from the BPOSC lead or from either of the reference clock selection outputs. Control bits determine the direction of the RACLK and RASYNC signals and whether BPOSC or a selected receive line is used as a clock source when these signals are outputs. Input data, clock and frame are provided by input leads TADAT, TACLK, and TASYNC. Control bits determine the direction of the TACLK and TASYNC signals and whether BPOSC or a selected receive line is used as a clock source when these signals are outputs.

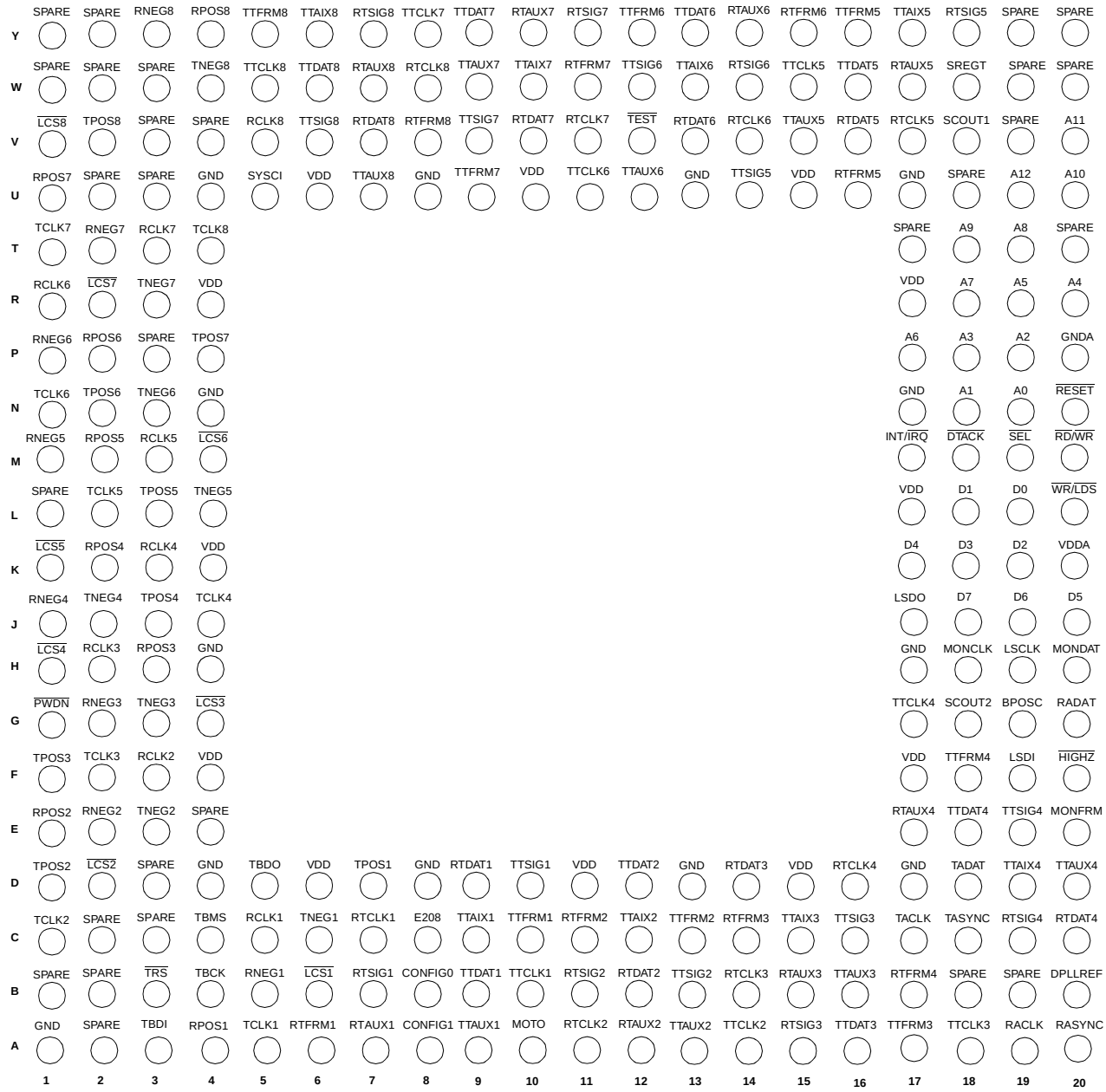
LEAD DIAGRAM FOR 208-LEAD PBGA PACKAGE



Notes: This is the bottom view. The leads are solder balls. See Figure 67 for package information. Some signal Symbols have been abbreviated to fit the space available. The 'A' designation for VDD and GND indicate 'Analog'.

Figure 2. E1Fx8 TXC-03109 Lead Diagram for the 208-lead PBGA Package

LEAD DIAGRAM FOR 256-LEAD PBGA PACKAGE



Notes: This is the bottom view. The leads are solder balls. See Figure 68 for package information. Some signal Symbols have been abbreviated to fit the space available. The 'A' designation for VDD and GND indicate 'Analog'.

Figure 3. E1Fx8 TXC-03109 Lead Diagram for the 256-lead PBGA Package

LEAD DESCRIPTIONS

The interface signal leads are TTL inputs and CMOS 2 mA outputs, unless otherwise noted. Also, the high Impedance test mode requires all output leads to operate as tristate outputs, however, the leads are not specified as such. The use of internal pull-up resistors is noted for input leads by use of the Type suffix “p” as required. The E1Fx8 is packaged in a 256-lead Plastic Ball Grid Array with a 1.27 mm ball pitch and a 208-lead small outline Plastic Ball Grid Array with a 1.00 mm ball pitch. A ‘T’ designation in the ‘I/O/P’ column indicates tristate. Symbol and lead number listings are in the same order in the table rows below.

Power Supply, Ground and Spares

Symbol	208-Lead PBGA Lead No.	256-Lead PBGA Lead No.	I/O/P*	Name/Function
VDD	B12, B15, C6, E2, G14, N2, N10, N13, P13, and T5	D6, D11, D15, F4, F17, K4, L17, R4, R17, U6, U10, and U15	P	**Digital VDD:** + 3.3 volt supply ± 5%
VDDA	J16	K20	P	**Analog VDD:** + 3.3 volt supply ± 5%
GND	C15, D8, E14, G7, G8, G9, G10, H7, H8, H9, H10, H14, J7, J9, J10, K7, K8, K9, K10, and N9	A1, D4, D8, D13, D17, H4, H17, N4, N17, U4, U8, U13, and U17	P	**Digital Ground:** 0 volt reference
GNDA	J8	P20	P	**Analog Ground:** 0 volt reference
SPARE	None	A2, B1, B2, B18, B19, C2, C3, D3, E4, L1, P3, T17, T20, U2, U3, U18, V3, V4, V19, W1, W2, W3, W19, W20, Y1, Y2, Y19, and Y20	-	Spare leads. These leads must not be connected to each other, to ground, or to any external circuit. Connection could impair performance or cause damage.

* Note: I = Input; O = Output; P = Power; T = Tristate; NA = Not Available.

Line Interface Signals

Symbol	208 PBGA Lead No.	256 PBGA Lead No.	I/O/P	Type*	Name/Function
RPOSn/ RNRZn (n=1-8)	A4, D3, F3, H1, K4, L2, P1, T3	A4, E1, H3, K2, M2, P2, U1, Y4	I	TTL	**Receive Unipolar Positive Signal Input:** When control bit RAIL (bit 7 in register X+00H) is a 1, the dual unipolar line interface is selected, and the RPOSn lead carries the receive positive rail input signal. RPOSn is high whenever a positive pulse is received. **Receive Line NRZ Data Input:** When control bit RAIL (bit 7 in register X+00H) is a 0, the NRZ line interface mode is selected and this lead carries the E1 data.
RCLKn (n=1-8)	B4, D1, F4, H3, K3, M4, P2, R4	C5, F3, H2, K3, M3, R1, T3, V5	I	TTL	**Receive Line Clock Input:** The 2048 kHz recovered clock input. Control bit RXCP (bit 5 in register X+00H) determines the edge on which the positive/negative rail and NRZ signals are to be clocked in on (RXCP = 1 for positive clock edge).

* Note: See Input, Output and I/O Parameters section for Type definitions.
TTL_P is a TTL input with a pull-up

<table>
<tr><th>Symbol</th><th>208 PBGA Lead No.</th><th>256 PBGA Lead No.</th><th>I/O/P</th><th>Type*</th><th>Name/Function</th></tr>
<tr><td>RNEGn/ RSCANn (n=1-8)</td><td>C4, D2, F2, H2, J2, L1, N1, R3</td><td>B5, E2, G2, J1, M1, P1, T2, Y3</td><td>I</td><td>TTL</td><td>Receive Unipolar Negative Signal Input: When control bit RAIL (bit 7 in register X+00H) is a 1, the dual unipolar line interface is selected, and the RNEGn lead carries the receive negative rail input signal. RNEGn is high whenever a positive pulse is received.

Receive Scan Input: When control bit RAIL (bit 7 in register X+00H) is a 0 and the fast sync option is not selected (control bit RXFS, bit 1 in register X+1FFH, is a 0), the RSCANn lead provides an input for indications of external bipolar violations or loss of signal detected in the external line interface transceiver as selected by control bit EXLOS (bit 3 in register X+00H). For code violations, a high indicates a bipolar violation and increments the internal 16-bit coding violation counter. For loss of signal the active level is programmable using control bit ELOSN (bit 2 in register X+00H). The control selections are as follows (where X=don’t care):

<table>
<tr><th>RXFS</th><th>EXLOS</th><th>ELOSN</th><th>Lead Function</th></tr>
<tr><td>0</td><td>0</td><td>X</td><td>A high = one coding violation</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>LOS true when lead high</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>LOS true when lead low</td></tr>
<tr><td>1</td><td>0</td><td>X</td><td>A high = last bit of multiframe</td></tr>
<tr><td>1</td><td>1</td><td>X</td><td>Do not use.</td></tr>
</table>

All inputs are clocked in on the active edge of the receive line clock RCLKn. If unused, ground this lead.</td></tr>
<tr><td>TPOSn/ TNRZn (n=1-8)</td><td>A5, C1, E3, G3, J3, L4, M2, R2</td><td>D7, D1, F1, J3, L3, N2, P4, V2</td><td>O</td><td>CMOS 2mA</td><td>Transmit Unipolar Positive Signal Output: When control bit RAIL (bit 7 in register X+00H) is a 1, the dual unipolar mode is selected, and the TPOSn lead carries the transmit positive rail output signal. TPOSn is high whenever a positive pulse is to be transmitted by the external line interface transceiver.

Transmit Line (NRZ) Data Output: When control bit RAIL (bit 7 in register X+00H) is a 0, the NRZ mode is selected, and the TNRZn lead carries the transmit NRZ data output signal. TNRZn is normally active high whenever a positive or negative pulse is to be transmitted by the external line interface transceiver. When control bit TXNRZ (bit 2 in register X+05H) is a 1, the data output TNRZn is inverted and it is active low.</td></tr>
</table>

Symbol	208 PBGA Lead No.	256 PBGA Lead No.	I/O/P	Type*	Name/Function
TCLKn (n=1-8)	C5, B1, E1, G1, J4, K2, M1, T1	A5, C1, F2, J4, L2, N1, T1, T4	O	CMOS 2 mA	**Transmit Line Clock:** A 2048 kHz clock output. The transmit 2048 kHz line clock can be derived from a back-plane oscillator input (lead BPOSC), receive line clock (lead RCLKn), or system clock (TTCLKn). Control bit TXCP (bit 3 in register X+05H) determines the clock edge on which the transmit line signals TPOSn/TNEGn and TNRZn are clocked out (TXCP is set to a 1 for rising edge).
TNEGn/ TDRVn (n=1-8)	B5, C2, E4, G4, J1, L3, N3, P3	C6, E3, G3, J2, L4, N3, R3, W4	O	CMOS 2 mA	**Transmit Unipolar Negative Signal Output:** When control bit RAIL (bit 7 in register X+00H) is a 1, the dual unipolar mode is selected, and the TNEGn lead carries the transmit negative rail output signal. TNEGn is high whenever a negative pulse is to be transmitted by the external line interface transceiver. **Transmit Mode General Purpose Drive Output:** When control bit RAIL (bit 7 in register X+00H) is a 0 and control bit TDFME (bit 7 of register X+07H) is a 0, the state written into control bit TXDRV (bit 6 in register X+07H) is clocked out on active edges of the transmit line clock TCLKn. **Transmit Fast Sync:** When control bit RAIL (bit 7 in register X+00H) is a 0 and the fast sync mode is selected by control bit TDFME (bit 7 in register X+07H) set to a 1, this lead is used for a fast sync feature providing a sync pulse every frame or multiframe one TCLKn clock cycle wide coincident with the first bit of a frame or multiframe (the frame bit) as determined by control bit TLMF (bit 5 of register X+07H). See the table below (where X=don't care).

TDFME	TLMF	TXDRV	Lead Function
0	X	0	Drive Low
0	X	1	Drive High
1	1	X	2.0 ms Multiframe Pulse
1	0	X	125 µs Frame Pulse

Line Interface Control Signals

Symbol	208 PBGA Lead No.	256 PBGA Lead No.	I/O/P	Type	Name/Function
LSDI	E13 (see MONFRM below)	F19	I/O	TTL/ CMOS 2 mA	**Line Interface Transceiver Data Input Signal:** This lead provides an input data signal shared by all the LIUs controlled by the E1Fx8. When using the 208-lead package this lead is used by MONFRM output when control bit ESPBMON (bit 5 in register 01DH) is set to a 1.
LSDO	G15 (see MONDAT below)	J17	O	CMOS 4 mA	**Line Interface Transceiver Data Output Signal:** This lead provides an output data signal shared with all the LIUs controlled by the E1Fx8. When using the 208-lead package this lead is used by MONDAT when control bit ESPBMON (bit 5 in register 01DH) is set to a 1.
$\overline{\text{LCSn}}$ (n=1-8)	D5, C3, D4, G2, H4, K1, M3, R1	B6, D2, G4, H1, K1, M4, R2, V1	O	CMOS 2 mA	**Line Interface Transceiver Chip Select Output:** An active low signal on a chip select lead indicates that the corresponding transceiver has been selected for communications between the transceiver and E1Fx8.
LSCLK	F13 (see MONCLK below)	H19	O	CMOS 4 mA	**Line Interface Transceiver Clock Output:** This clock is used to clock input and output data between the E1Fx8 and the external transceivers. This clock and the other timing signals for the LIU interface are derived from the BPOSC signal. When using the 208-lead package this lead is used by MONCLK when control bit ESPBMON (bit 5 in register 01DH) is set to a 1.

Monitor Interface Signals

Symbol	208 PBGA Lead No.	256 PBGA Lead No.	I/O/P	Type	Name/Function
MONCLK	F13 Shares LSCLK lead when global control bit ESPBMON = 1	H18	O	CMOS 2 mA	**Monitor Clock Output:** This clock is used to clock out one of the 8 receive or transmit channels selected. The 2048 kHz clock is derived from either receive line clock or system transmit clock. The monitored data and framing pulse are clocked out on rising edges of this clock. This lead is tristated if a 1 is written to control bit MONTR (bit 5 in register 022H).
MONFRM	E13 Shares LSDI lead when global control bit ESPBMON = 1	E20	O	CMOS 2 mA	**Monitor Framing Pulse Output:** A one clock cycle wide positive framing pulse that represents the location of the framing bit, when the input or output of the receive or output of the transmit framer is selected by writing a 1 to control bits MONRF and MONRX (bits 6 and 7 in register 022H) or ia 0 to control bit MONRX. This lead is also tristated when control bit MONTR (bit 5 in register 022H) is written with a 1. For test purposes the internally generated one-second clock can be brought out on this lead if control bit OBT1SI (bit 2 in register 0FFH) is set to a 1.
MONDAT	G15 Shares LSDO lead when global control bit ESPBMON = 1	H20	O	CMOS 2 mA	**Monitor Data Output:** The data on this lead is either from the input to the receive framer, the output from the receive framer, or from the output of the transmit framer, prior to the codec. A 0 written to control bit MONRX (bit 7 in register 022H) selects the transmit side. A 1 written to control bit MONRX selects the receive side. A 1 written to control bit MONRF (bit 6 in register 022H) selects the receive framer output. This lead is also tristated when control bit MONTR (bit 5 in register 022H) is written with a 1.

Reference Clock Input Signals

Symbol	208 PBGA Lead No.	256 PBGA Lead No.	I/O/P	Type	Name/Function
BPOSC	F14	G19	I	TTL	**Back Plane External Transmit Clock/Clock Substitution/LIU Input Signal:** This lead is used to input an independent transmit 2048 kHz ± 50 ppm clock. This clock is used for internal transmit frame timing, clocking data/signaling out of the buffers, and a transmit clock. The Transmit Clock feature is enabled when control bits TXC1,0 (bits 7 and 6 in register X+11CH) are set to 00. This clock, when enabled by control bit S1CIEN (bit 7 in register 00CH) set to a 1, is used for receive line clock substitution or for one-second clock source when a loss of signal alarm is detected on the receive line clock being used. This clock is used for deriving the timing signals needed for the external LIU transceivers; It becomes LSCLK. This clock can also be used to derive the one-second shadow register timing in place of SREGT lead. Global control bits S1SEXTB and S1SINT (bits 4 and 3 in register 024H) set to 10 are used to select this lead as the source. This clock is required to operate the DPLL for the dejitter buffers.
SREGT	T16	W18	I/O	TTL/ CMOS 2 mA	**One-second Shadow Register Input/Output:** A positive one-second pulse (± 50 ppm when used for performance monitoring) can be applied to this lead when the shadow register feature or the ANSI T1.403 DS0 remote loopback feature is enabled. Global control bit S1SEXTB (bit 4 in register 024H) set to 0 is used to select this input for one-second timing. When control bit S1SEXTB is set to a 1, this lead becomes a one-second output signal.
DPLLREF	A16	B20	I/O	TTLp/ CMOS 8 mA	**DPLL Reference Input/Output:** When the internal DPLL is shut off (control bit DISECKSYN (bit 4) in register 0FEH is set to a 1), this lead is used to input a 64512 kHz ± 100 ppm (40 to 60% duty cycle) signal. This signal is used to operate the receive dejitter buffers. When the internal DPLL is enabled (control bit DISECKSYN is set to a 0), this lead is used to output the 64512 kHz (45 to 55% duty cycle) DPLL reference clock signal which may be used to drive other E1Fx8 devices. This clock is 31.5 times the frequency present at lead BPOSC and is used to operate the receive dejitter buffers. This lead has an internal pull-up resistor.

Synchronization Clock Output Signals

Symbol	208 PBGA Lead No.	256 PBGA Lead No.	I/O/P	Type	Name/Function
SCOUT1	R15	V18	O (T)	CMOS 2 mA	**Synchronization Clock Output No. 1:** A 2048 kHz clock or an 8 kHz signal (positive single 2048 kHz clock cycle wide pulse, occurring every 125 µs) which is derived from the receive clock framer input, for one of the 8 framers. Control bits S1YNC2-S1YNC0 (bits 2 - 0 in register 024H) select the specific receive line clock. Control bit S18KHZ (bit 7 in register 024H) when set to a 1 selects the 8 kHz reference. An option is provided for enabling the 8 kHz to be synchronous with the line framing bit, but delayed by the decoder. Control bit SYNLF (bit 6 in register 00CH) when set to a 1 synchronizes this signal with the received framing bit position as the first bit of a frame in NRZ mode for control bit RXCP (bit 5) in register X+00H set to 0; in AMI or HDB3 it is the fourth bit of the frame. If RXCP is set to 1, this signal is aligned to the center of the last bit of the frame in NRZ mode and the center of the third bit of the frame in AMI or HDB3 mode. The alignments are delayed by 29.5 clock cycles with the dejitter buffers enabled. This lead is tristated when control bit S1CTRI (bit 6 in register 024H) is set to 1. When a LOS occurs on the selected framer input this signal goes low if control bit S1YNCEN (bit 5 in register 024H) is set to a 1. The source selected by control bits S1YNC2-S1YNC0 can also be used to derive the one-second shadow register timing in place of SREGT. Global control bits S1SEXTB and S1SINT (bits 4 and 3 in register 024H) select the source.
SCOUT2	F15	G18	O (T)	CMOS 2 mA	**Synchronization Clock Output No. 2:** A 2048 kHz clock or an 8 kHz signal (positive single 2048 kHz clock cycle wide pulse, occurring every 125 µs) which is derived from the receive clock framer input, for one of the 8 framers. Control bits S2YNC2-S2YNC0 (bits 2 - 0 in register 025H) select the specific receive line clock. Control bit S28KHZ (bit 7 in register 025H) when set to a 1 selects the 8 kHz reference. An option is provided for enabling the 8 kHz to be synchronous with the line framing bit, but delayed by the decoder. Control bit SYNLF (bit 6 in register 00CH) when set to a 1 synchronizes this signal with the received framing bit position as the first bit of a frame in NRZ mode for control bit RXCP (bit 5) in register X+00H set to 0; in AMI or HDB3 it is the fourth bit of the frame. If RXCP is set to 1, this signal is aligned to the center of the last bit of the frame in NRZ mode and the center of the third bit of the frame in AMI or HDB3 mode. The alignments are delayed by 29.5 clock cycles with the dejitter buffers enabled. This lead is tristated when control bit S2CTRI (bit 6 in register 025H) is set to 1. When a LOS occurs on the selected framer input this signal goes low if control bit S2YNCEN (bit 5 in register 025H) is set to a 1.

System Interface Signals

<table>
<tr><th>Symbol</th><th>208 PBGA Lead No.</th><th>256 PBGA Lead No.</th><th>I/O/P</th><th>Type</th><th>Name/Function</th></tr>
<tr><td>RTDATn (n=1-8)</td><td>D7, A10, D13, C16, T13, N11, R8, N5</td><td>D9, B12, D14, C20, V16, V13, V10, V7</td><td>O</td><td>CMOS 2 mA; 8 mA for n=1,5</td><td>Receive System Data Highway Output: This lead outputs the E1 received data. The following table is a summary of the receive data highway interface.
<table>
<tr><th>Interface</th><th>Format</th></tr>
<tr><td>2.048 Mbit/s Transmission</td><td>E1 multiframe format (32 channels, 16 frames).</td></tr>
<tr><td>2 Mbit/s MVIP</td><td>E1 frame carried in 31 time slots in a 32 time slot format.</td></tr>
<tr><td>8 Mbit/s H-MVIP/H.100</td><td>Four E1 frames carried in four MVIP frame formats that are byte-interleaved (n = 1, 5).</td></tr>
<tr><td>2.048 Mbit/s Data</td><td>E1 frame format (32 channels)</td></tr>
</table></td></tr>
<tr><td>RTFRMn (n=1-8)</td><td>A6, D10, C12, C14, R14, T11, P8, T6</td><td>A6, C11, C14, B17, U16, Y15, W11, V8</td><td>I/O</td><td>TTL/ CMOS 2 mA</td><td>Receive System Framing Pulse Input/Output: This signal is used for frame and multiframe synchronization input. The following table summarizes the frame pulse characteristics used for the system side interfaces. Leads CONF0 and CONF1 determine the modes.
<table>
<tr><th>Interface</th><th>Width</th><th>Polarity</th><th>Period</th><th>Lead used</th></tr>
<tr><td>2.048 Mbit/s Transmission</td><td>1 clk cyc.</td><td>Pos.</td><td>2 ms</td><td>RTFRMn</td></tr>
<tr><td>2 Mbit/s MVIP</td><td>1 clk cyc.</td><td>Neg.</td><td>125 µs</td><td>RTFRMn</td></tr>
<tr><td>8 Mbit/s H-MVIP/H.100</td><td>2,4 clk cyc</td><td>Neg.</td><td>125 µs</td><td>RTFRM1,5</td></tr>
<tr><td>2.048 Mbit/s Data</td><td>1 clk cyc.</td><td>Pos.</td><td>125 µs</td><td>RTFRMn</td></tr>
</table>
The E1Fx8 can also be configured to source the clock and framing pulse for the transmission and data interfaces only. Control bit RXCKE (bit 7 in register X+11BH) when set to a 1 causes the E1Fx8 to source RTFRMn.</td></tr>
</table>

<table>
<tr><th>Symbol</th><th>208 PBGA Lead No.</th><th>256 PBGA Lead No.</th><th>I/O/P</th><th>Type</th><th>Name/Function</th></tr>
<tr><td>RTCLKn (n=1-8)</td><td>B6, A9, D12, A15, T15, R11, N8, P6</td><td>C7, A11, B14, D16, V17, V14, V11, W8</td><td>I/O</td><td>TTL/ CMOS 2 mA</td><td>Receive System Clock Input/Output: A 2048/ 16384 kHz clock that is clock for the received data, signaling, auxiliary, and framing pulse. The following table is a summary of the clock rates and transitions used for clocking data, signaling, RTAUXn signal and framing pulse (when sourced).

<table>
<tr><th>Interface</th><th>Rate</th><th>Clk Out</th><th>Clk In</th><th>Lead used</th></tr>
<tr><td>2.048 Mbit/s Transmission</td><td>2.048MHz.</td><td>Neg.</td><td>Neg.</td><td>RTCLKn</td></tr>
<tr><td>2 Mbit/s MVIP</td><td>2.048 MHz</td><td>-</td><td>Pos.</td><td>RTCLKn</td></tr>
<tr><td>8 Mbit/s H-MVIP/H.100</td><td>16.384 MHz</td><td>-</td><td>Neg.</td><td>RTCLK1,5</td></tr>
<tr><td>2.048 Mbit/s Data</td><td>2.048 MHz</td><td>Neg.</td><td>Neg.</td><td>RTCLKn</td></tr>
</table>

The E1Fx8 can also be configured to source the clock and framing pulse for the transmission and data interfaces only. Control bit RXCKE (bit 7 in register X+11BH) when set to a 1 causes the E1Fx8 to source RTCLKn.</td></tr>
<tr><td>RTSIGn (n=1-8)</td><td>D6, C10, A12, B16, T14, P11, T8, R6 (see RTAUXn below)</td><td>B7, B11, A15, C19, Y18, W14, Y11, Y7</td><td>O</td><td>CMOS 2 mA; 8 mA for n=1,5</td><td>Receive Signaling Highway Output: This lead carries the E1 signaling states for data time slots. The following table provides information about the format of this signal.

<table>
<tr><th>Interface</th><th>Format</th></tr>
<tr><td>2.048 Mbit/s Transmission</td><td>Time Slot 1 carries FAS and NFAS framing including RAI; Time Slot 2 carries signaling for two data time slots; 30 time slots carry an AIS indication; a 16 frame structure covers 120 signaling bits.</td></tr>
<tr><td>2 Mbit/s MVIP</td><td>Signaling per data time slot carried in the lower nibble of 30 time slots in a 32-time slot format each frame plus optional FAS/NFAS framing carried in Time Slot 0.</td></tr>
<tr><td>8 Mbit/s H-MVIP/H.100</td><td>Same as a MVIP, except four signaling highways are byte-interleaved (n = 1, 5).</td></tr>
<tr><td>2.048 Mbit/s Data</td><td>Signaling per data time slot carried in 30 time slots each frame plus optional FAS/NFAS framing carried in Time Slot 0.</td></tr>
</table>

When using the 208-lead package this lead is used by RTAUXn when control bit FE1M (bit 4 in register X+07H) is set to a 1.</td></tr>
</table>

<table>
<tr><th>Symbol</th><th>208 PBGA Lead No.</th><th>256 PBGA Lead No.</th><th>I/O/P</th><th>Type</th><th>Name/Function</th></tr>
<tr><td>RTAUXn (n=1-8)</td><td>D6, C10, A12, B16, T14, P11, T8, R6 Shares RTSIGn lead when control bit FE1M (bit 4, reg. X+07H) = 1</td><td>A7, A12, B15, E17, W17, Y14, Y10, W7</td><td>O</td><td>CMOS 2 mA</td><td>Receive System Auxiliary Output: This lead is enabled for the transmission and data interfaces only. This signal lead can be programmed to provide a gapped clock or channel marker for one or more fractional time slots; see control bits RFCH1-32 (registers X+1BH, X+1CH, X+1DH and X+1EH) and RCHMK (bit 7 in register X+1AH).
For testing purposes this lead can be selected by setting control bit OBLOL (bit 2 in register X+1FFH) to a 1 to output the state of the PRBS analyzer (status bit TPLOL = 1 indicates out of lock and this lead will go high on a out of lock).</td></tr>
<tr><td>TTDATn (n=1-8)</td><td>A8, D11, C13, D15, R12, T10, P7, R5</td><td>B9, D12, A16, E18, W16, Y13, Y9, W6</td><td>I</td><td>TTL</td><td>Transmit System Data Input: This lead inputs the E1 system side data for transmission on the E1 line. The following table is a summary of the transmit data interface.
<table>
<tr><th>Interface</th><th>Format</th></tr>
<tr><td>2.048 Mbit/s Transmission</td><td>E1 multiframe format (32 channels, 16 frames).</td></tr>
<tr><td>2 Mbit/s MVIP</td><td>E1 frame carried in 31 time slots in a 32 time slot format.</td></tr>
<tr><td>8 Mbit/s H-MVIP/H.100</td><td>Four E1 frames carried in four MVIP frame formats that are byte-interleaved (n = 1, 5).</td></tr>
<tr><td>2.048 Mbit/s Data</td><td>E1 frame format (32 channels)</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Symbol</th><th>208 PBGA Lead No.</th><th>256 PBGA Lead No.</th><th>I/O/P</th><th>Type</th><th>Name/Function</th></tr>
<tr><td>TTSIGn (n =1-8)</td><td>C8, C11, B13, D14, T12, R9, T7, N4 (see TTAUXn below)</td><td>D10, B13, C16, E19, U14, W12, V9, V6</td><td>I/O</td><td>TTL/ CMOS 2 mA</td><td>Transmit Signaling Highway Input: This lead carries the E1 signaling states for data time slots into the E1Fx8. The following table provides information about the format of this signal.

<table><tr><th>Interface</th><th>Format</th></tr><tr><td>2.048 Mbit/s Transmission</td><td>Time Slot 1 carries FAS and NFAS framing including RAI; Time Slot 2 carries signaling for two data time slots; 30 time slots carry an AIS indication; a 16 frame structure covers 120 signaling bits.</td></tr><tr><td>2 Mbit/s MVIP</td><td>Signaling per data time slot carried in the lower nibble of 30 time slots in a 32 time slot format each frame plus optional FAS/NFAS framing carried in Time Slot 0.</td></tr><tr><td>8 Mbit/s H-MVIP/H.100</td><td>Same as a MVIP, except four signaling highways are byte-interleaved (n = 1, 5).</td></tr><tr><td>2.048 Mbit/s Data</td><td>Signaling per data time slot carried in 30 time slots each frame plus optional FAS/NFAS framing carried in Time Slot 0.</td></tr></table>
When using the 208-lead package this lead is used by TTAUXn when control bit FE1M (bit 4 in register X+07H) is set to a 1.
When used as TTAUXn, this lead is an output.</td></tr>
<tr><td>TTFRMn (n=1-8)</td><td>D9, A11, A14, E15, P12, T9, R7, T4</td><td>C10, C13, A17, F18, Y16, Y12, U9, Y5</td><td>I</td><td>TTL</td><td>Transmit System Framing Pulse Input: This signal is used for frame and multiframe synchronization. The following table is a summary of the frame pulse characteristics used for the various system side interfaces.

<table><tr><th>Interface</th><th>Width</th><th>Polarity</th><th>Period</th><th>Lead used</th></tr><tr><td>2.048 Mbit/s Transmission</td><td>1 clk cyc.</td><td>Pos.</td><td>2 ms</td><td>TTFRMn</td></tr><tr><td>2 Mbit/s MVIP</td><td>1 clk cyc.</td><td>Neg.</td><td>125 µs</td><td>TTFRMn</td></tr><tr><td>8 Mbit/s H-MVIP/H.100</td><td>2,4 clk cyc</td><td>Neg.</td><td>125 µs</td><td>TTFRM1,5</td></tr><tr><td>2.048 Mbit/s Data</td><td>1 clk cyc.</td><td>Pos.</td><td>125 µs</td><td>TTFRMn</td></tr></table></td></tr>
</table>

<table>
<tr><th>Symbol</th><th>208 PBGA Lead No.</th><th>256 PBGA Lead No.</th><th>I/O/P</th><th>Type</th><th>Name/Function</th></tr>
<tr><td>TTCLKn (n=1-8)</td><td>C9, B11, B14, E16, N12, P9, N6, P4</td><td>B10, A14, A18, G17, W15, U11, Y8, W5</td><td>I</td><td>TTL</td><td>Transmit System Clock Input: A 2048/16384 kHz clock that is clock for the data, signaling, auxiliary, and framing pulse. This clock is also used to clock out the gapped clock or channel marker for fractional E1 channels. The following table is a summary of the clock rates and transitions used for clocking in data, signaling, and framing pulse or clocking out the TTAUXn signal.
<table>
<tr><th>Interface</th><th>Rate</th><th>GapOut</th><th>Clk In</th><th>Lead used</th></tr>
<tr><td>2.048 Mbit/s Transmission</td><td>2.048 MHz</td><td>Pos.</td><td>Pos.</td><td>RTCLKn</td></tr>
<tr><td>2 Mbit/s MVIP</td><td>2.048 MHz</td><td>-</td><td>Neg.</td><td>RTCLKn</td></tr>
<tr><td>8 Mbit/s H-MVIP/H.100</td><td>16.384 MHz</td><td>-</td><td>Pos.</td><td>RTCLK1,5</td></tr>
<tr><td>2.048 Mbit/s Data</td><td>2.048 MHz</td><td>Pos.</td><td>Pos.</td><td>RTCLKn</td></tr>
</table>
The gapped clock or channel marker (TTAUXn) for selected E1 channels is clocked out on the listed transitions of this clock, one clock cycle earlier than the bit time required.</td></tr>
<tr><td>TTAUXn (n=1-8)</td><td>C8, C11, B13, D14, T12, R9, T7, N4 Shares TTSIGn lead when control bit FE1M (bit 4, reg. X+07H) =1</td><td>A9, A13, B16, D20, V15, U12, W9, U7</td><td>O</td><td>CMOS 2 mA</td><td>Transmit System Auxiliary Output: This lead is enabled for the transmission and data interfaces only. This signal lead can be programmed to provide a gapped clock or channel marker for one or more fractional E1 time slots; see control bits TC0C0-TC0C31 (even bits of registers X+111H - X+118H), TC1C0-TC1C31 (odd bits of registers X+111H - X+118H) and TCHMK (bit 7 of register X+110H).</td></tr>
<tr><td>TTAIXn (n=1-8)</td><td>B8, B10, A13, D16, R13, R10, N7, P5</td><td>C9, C12, C15, D19, Y17, W13, W10, Y6</td><td>I</td><td>TTL</td><td>Transmit System Auxiliary Input: A signal input lead for multiplexing in the data from one or more fractional E1 time slots. It behaves like TTDATn but each time slot on this lead replaces the time slot (c = 0 - 31) on TTDATn if control bits TC1Cc, TC0Cc (registers X+111H - X+118H) are set to 01.</td></tr>
</table>

Other Control Signals

Symbol	208 PBGA Lead No.	256 PBGA Lead No.	I/O/P	Type	Name/Function
$\overline{\text{HIGHZ}}$	F16	F20	I	TTLp	**High Impedance Select Input:** A low forces all output leads (except TBDO) to the high impedance state for board testing purposes. This lead must be held high for normal operation. This lead has an internal pull-up resistor.
$\overline{\text{TEST}}$	P10	V12	I	TTLp	**TranSwitch Test Select Input:** Used for manufacturing test purposes only. This lead must be tied high for normal operation. This lead has an internal pull-up resistor.
$\overline{\text{RESET}}$	L14	N20	I	TTL	**Reset:** An active low signal for resetting and initializing the internal counters and logic circuits for all 8 framers to their preset values. The reset must be applied only after power is applied and the clocks are stable for a minimum of 10 SYSCI pulses.
$\overline{\text{PWDN}}$	F1	G1	I	TTLp	**Power Down:** An activate low on this lead forces the transmit line clocks (TCLKn), and the transmit line interface leads (TPOSn/TNEGn or TNRZn/TDRVn) to the active low state. The active low overrides the software power down control bits. This lead must be held high during power up of the E1Fx8. This lead has an internal pull-up resistor.
CONF0 CONF1	A7, C7	B8, A8	I	TTL	**System Side Configuration Selection:** Selects the E1Fx8 System side interface configuration according to the following table (where X=don't care): **System Interface** / **CONF1** / **CONF0** / **DINTF** 2Mbit/s Transmission / L / L / 0 2 Mbit/s MVIP / L / H / X 8 Mbit/s H-MVIP / H / L / 0 8 Mbit/s H.100 / H / L / 1 2 Mbit/s Data / L / L / 1 Not Used / H / H / X Control bit DINTF is bit 1 in register 00BH.

Symbol	208 PBGA Lead No.	256 PBGA Lead No.	I/O/P	Type	Name/Function
E208	B7 (VDD)	C8 (GND)	I	TTL	**Enable Small Package Input:** An active low on this lead selects the 256-lead version of the E1Fx8; it must be tied to a ground lead with this package. Control bits FE1M (bit 4 in register X+07H) and ESPBMON (bit 5 in register 01DH) have no effect on the function of leads RTSIGn, TTSIGn, LSCLK, LSDI, or LSDO. An active high signal on this lead selects the 208-lead version of the E1Fx8 enabling the control bits FE1M (which selects between signaling or gapped clock operation on leads RTSIGn and TTSIGn) and ESPBMON (which selects between the Line Interface Control option and the Monitor mode function on leads LSCLK, LSDI and LSDO). When common control bit ESPBMON is set to a 1, the Monitor mode function is selected. When per framer control bit FE1M is set to a 1, the marker/gapped clock function is selected for that particular framer.

Boundary Scan

Symbol	208 PBGA Lead No.	256 PBGA Lead No.	I/O/P	Type	Name/Function
TBCK	A3	B4	I	TTL	**IEEE 1149.1 Test Port Serial Scan Clock Input:** The input clock for boundary scan testing. The TBDI and TBMS states are clocked into the on rising edges. The maximum clock frequency is 10 MHz.
TBDI	B3	A3	I	TTLp	**IEEE 1149.1 Test Port Serial Scan Data Input:** Serial test instructions and data are clocked in on the rising edges of TBCK. This lead has an internal pull-up resistor.
TBDO	A2	D5	O/(T)	CMOS 4 mA	**IEEE 1149.1 Test Port Serial Scan Data Output:** Serial data output whose information is clocked out on falling edges of TBCK. When inactive this output is forced to the high impedance state.
TBMS	A1	C4	I	TTLp	**IEEE 1149.1 Test Port Mode Select Input:** This signal is clocked in on rising edges of TBCK and is used to place the Test Access Port Controller into various states as defined in the IEEE 1149.1 standard. This lead must be set high for normal framer operation. This lead has an internal pull-up resistor.
$\overline{\text{TRS}}$	B2	B3	I	TTLp	**IEEE 1149.1 Test Port Reset Input:** An active low signal that provides for synchronization of the Test Access Port (TAP) controller. This lead is to be held low, asserted low or pulsed low to reset the TAP controller on E1Fx8 power up. This lead has an internal pull-up resistor.

Microprocessor Interface

Symbol	208 PBGA Lead No.	256 PBGA Lead No.	I/O/P	Type	Name/Function
MOTO	B9	A10	I	TTL	**Motorola/Intel Microprocessor Select:** A high selects a Motorola (M Mode) microprocessor compatible bus interface. A low selects the Intel (I Mode) microprocessor compatible bus interface.
A(12-0)	P14,R16, P15, P16, N15, N14, N16, M15, M16, M14, M13, L15, L16	U19, V20, U20, T18, T19, R18, P17, R19, R20, P18, P19, N18, N19	I	TTL	**Address Bus (Motorola/Intel Buses) Input:** These are active high address line inputs that are used by the microprocessor for accessing a memory location for a read/write cycle. A12 is the most significant bit.
D(7-0)	G16, G13, H15, H16, H13, J13, J15, K13	J18, J19, J20, K17, K18, K19, L18, L19	I/O	TTL/ CMOS 8 mA	**Data Bus:** Bi-directional data lines used for transferring data between the E1Fx8 and the microprocessor. D7 is the most significant bit.
$\overline{SEL}$	K16	M19	I	TTLp	**Select.** A low enables data transfers between the microprocessor and the E1Fx8 during a read/ write cycle.This lead has an internal pull-up resistor.
$\overline{RD}$ RD/$\overline{WR}$	K14	M20	I	TTL	**Read (I Mode) or Read/Write (M Mode):** Intel Mode - An active low signal generated by the microprocessor for reading the memory locations. Motorola Mode - An active high signal generated by the microprocessor for reading the 8-channel memory locations. An active low signal is used to write to the memory locations.
$\overline{WR}$/ $\overline{LDS}$	J14	L20	I	TTL	**Write (I Mode) or Data Strobe (M Mode):** Intel Mode - An active low signal generated by the microprocessor for writing to the E1Fx8. Motorola Mode - An active low DS signal for Motorola 68302 operation. This input can be grounded.
RDY/ $\overline{DTACK}$	K15	M18	O/(T)	CMOS 8 mA	**Ready (I Mode) or Data Transfer Acknowledge (M Mode):** Intel Mode - A high is an acknowledgment from the addressed RAM location that the transfer can be completed. A low indicates that the device cannot complete the transfer cycle, and microprocessor wait states must be generated. Motorola Mode - During a read bus cycle, a low signal indicates the information on the data bus is valid. During a write bus cycle, a low signal acknowledges the acceptance of data.
INT/ $\overline{IRQ}$	L13	M17	O	CMOS 4 mA	**Interrupt:** Intel Mode - A high on this output lead signals an interrupt request to the microprocessor. Motorola Mode - A low on this lead signals an interrupt request to the microprocessor.

<table>
<tr><th>Symbol</th><th>208 PBGA Lead No.</th><th>256 PBGA Lead No.</th><th>I/O/P</th><th>Type</th><th>Name/Function</th></tr>
<tr><td>SYSCI</td><td>T2</td><td>U5</td><td>I</td><td>TTL</td><td>System Clock Input: Asynchronous clock input used for internal functions. This clock is usually connected to the microprocessor clock, and should be capable of operating between 19 and 25 MHz with a 40 to 60% duty cycle. This clock is not required to be synchronous with other clocks. This frequency range will provide correct operation with an E1 signal that complies with the frequency range and jitter as specified in ITU-T G.703 and G.823. When the E1Fx8 is used in a gapped clock situation (e.g. a direct connection to the TXC-03361, E123MUX E1 ports), SYSCI minimum frequency must guarantee that at least 9 rising edges of SYSCI occur between any two rising or falling edges of any particular RCLKn. The following table can be used to determine SYSCI frequency:
<table>
<tr><th>RCLKn Minimum t_{CYC} (ns)</th><th>SYSCI Minimum Frequency (MHz)</th></tr>
<tr><td>480</td><td>19</td></tr>
<tr><td>456</td><td>20</td></tr>
<tr><td>435</td><td>21</td></tr>
</table>
</td></tr>
</table>

Auxiliary Port

Symbol	208 PBGA Lead No.	256 PBGA Lead No.	I/O/P	Type	Name/Function
RACLK	NA	A19	I/O	TTLp/ CMOS 2 mA	**Receive Auxiliary Clock I/O:** A 2.048 MHz clock signal used to clock out the data on lead RADAT. This clock may be derived from one of the 8 RCLK leads, lead BPOSC or it may be selected as an input under direction of control bits RACKSEL and RADIRSEL (bits 1 and 0) in register 037H as shown in the table (where X=don't care): **RACKSEL / RADIRSEL / RACLK (RASYNC)** X / 0 / Input: 2.048 MHz (125 µs.) 1 / 1 / Output: from BPOSC 0 / 1 / Output: from RCLKn; S1YNC2-S1YNC0 selects the received line clock When RACLK is an output it clocks out RASYNC. This lead has an internal pull-up resistor.
RASYNC	NA	A20	I/O	TTLp/ CMOS 2 mA	**Receive Auxiliary Frame Synchronization:** A 125 microsecond synchronization positive pulse signal for a single RACLK clock cycle coincident with the first bit of the first time slot on RADAT. Control bits RACKSEL and RADIRSEL (bits 1 and 0) in register 037H as shown in the table for RACLK control the source and directionality of this signal. This lead has an internal pull-up resistor.
RADAT	NA	G20	O	CMOS 2 mA	**Receive Auxiliary Data Output:** A data highway with 32 64 kbit/s time slots repeated at a 125 microsecond rate. Each time slot may come from any one of 8 receive line ports (any time slot) or from any one of 8 transmit system interface ports (any time slot). Control bits RDIR31-0 in registers 038H through 03BH determine the source port side for each time slot; for RDIRc set to 0 the source port side is the receive line (RPOSn/RNRZn and RNEGn); for RDIRc set to 1 the source port side is the transmit system (TTDATn) where n = 1 to 8 and c = 0 to 31. The individual time slot source is determined by control bits RAFRSELc(2-0) and RATSSELc(5-0) in registers 040H through 05FH. RAFRSELc(2-0) selects ports 1 through 8 (000 selects framer port 1 and 111 selects framer port 8) and RATSSELc(4-0) selects time slots 0 through 31 (00000 selects Time Slot 0 and 11111 selects Time Slot 31) on the selected port.

<table>
<tr><th>Symbol</th><th>208 PBGA Lead No.</th><th>256 PBGA Lead No.</th><th>I/O/P</th><th>Type</th><th>Name/Function</th></tr>
<tr><td>TACLK</td><td>NA</td><td>C17</td><td>I/O</td><td>TTLp/ CMOS 2 mA</td><td>Transmit Auxiliary Clock I/O: A 2.048 MHz clock signal used to clock in the data on lead TADAT. This clock may be derived from one of the 8 RCLK leads, lead BPOSC or it may be selected as an input under direction of control bits TACKSEL and TADIRSEL (bits 3 and 2) in register 037H as shown in the table (where X=don’t care):

<table>
<tr><th>TACKSEL</th><th>TADIRSEL</th><th>TACLK (TASYNC)</th></tr>
<tr><td>X</td><td>0</td><td>Input: 2.048 MHz (125 µs.)</td></tr>
<tr><td>1</td><td>1</td><td>Output: from BPOSC</td></tr>
<tr><td>0</td><td>1</td><td>Output: from RCLKn; S1YNC2-S1YNC0 selects the received line clock</td></tr>
</table>

When TACLK is an output it clocks out TASYNC. This lead has an internal pull-up resistor.</td></tr>
<tr><td>TASYNC</td><td>NA</td><td>C18</td><td>I/O</td><td>TTLp/ CMOS 2 mA</td><td>Transmit Auxiliary Frame Synchronization: A 125 microsecond synchronization positive pulse signal for a single TACLK clock cycle coincident with the first bit of the first time slot on TADAT. Control bits TACKSEL and TADIRSEL (bits 3 and 2) in register 037H as shown in the table for TACLK control the source and directionality of this signal. This lead has an internal pull-up resistor.</td></tr>
<tr><td>TADAT</td><td>NA</td><td>D18</td><td>I</td><td>TTL_P</td><td>Transmit Auxiliary Data Input. A data highway with 32 64 kbit/s time slots repeated at a 125 microsecond rate. Each time slot may go to any one of 8 transmit line ports any time slot or to any one of 8 receive system interface ports any time slot. Control bits TDIR31-0 in registers 03CH through 03FH determine the destination port side for each time slot; for TDIRc set to 0 the destination port side is the transmit line (TPOSn/TNRZn and TNEGn); for TDIRc set to 1 the destination port side is the receive system (RTDATn) where n = 1 to 8 and c = 0 to 31. The individual time slot destination is determined by control bits TAFRSELc(2-0) and TATSSELc(5-0) in registers 060H through 07FH. TAFRSELc(2-0) selects ports 1 through 8 (000 selects framer port 1 and 111 selects framer port 8) and TATSSELc(4-0) selects time slots 0 through 31 (00000 selects Time Slot 0 and 11111 selects Time Slot 31) on the selected port. This lead has an internal pull-up resistor.</td></tr>
</table>

ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

Parameter	Symbol	Min	Max	Unit	Conditions
Supply voltage	V_{DD}	-0.3	+3.9	V	Note 1
DC input voltage	V_{IN}	-0.5	+5.5	V	Note 1
Storage temperature range	T_S	-55	+150	^oC	Note 1
Ambient Operating Temperature	T_A	-40	+85	^oC	0 ft/min linear airflow
Moisture Exposure Level	ME	5		Level	per EIA/JEDEC JESD22-A112-A
Relative Humidity, during assembly	RH	30	60	%	Note 2
Relative Humidity, in-circuit	RH		100	%	non-condensing
ESD Classification	ESD	absolute value 2000		V	Note 3

Notes:

1. Conditions exceeding the Min or Max values may cause permanent failure. Exposure to conditions near the Min or Max values for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the "CAUTION" label on the drypack bag in which devices are supplied.
3. Test method for ESD per MIL-STD-883D, Method 3015.7.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
208-lead PBGA thermal resistance: junction to ambient			38.0	$^oC/W$	0 ft/min linear airflow
256-lead PBGA thermal resistance: junction to ambient			25.0	$^oC/W$	0 ft/min linear airflow

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	3.15	3.30	3.45	V	
I_{DD} (outputs loaded)	148[3]	163[1]	225[2]	mA	1. All channels operating. Output load 30 pF. SYSCI at 20 MHz. Transmission, Data or MVIP Mode. 2. All channels operating. Output load 30 pF. SYSCI at 25 MHz. H-MVIP Mode @ 85 ^oC. 3. Same as 1, except SYSCI at 19 MHz.
P_{DD} (outputs loaded)	470[3]	540[1]	776[2]	mW	
I_{DD} (outputs loaded)		152		mA	All channels powered down (lead $\overline{PWDN}$ low). Output load 30 pF. SYSCI at 19 MHz.
P_{DD} (outputs loaded)		500		mW	

INPUT, OUTPUT AND INPUT/OUTPUT PARAMETERS

Input Parameters For TTL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.15 \leq V_{DD} \leq 3.45$
V_{IL}			0.8	V	$3.15 \leq V_{DD} \leq 3.45$
Input leakage current	-10		+10	µA	0 to 5.25 V input
Input capacitance		5		pF	

Input Parameters For TTLp

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.15 \leq V_{DD} \leq 3.45$
V_{IL}			0.8	V	$3.15 \leq V_{DD} \leq 3.45$
Input leakage current	-30	-100	-500	µA	0 to 5.25 V input
Input capacitance		5		pF	

Output Parameters For CMOS 2mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	$V_{DD} = 3.15$; $I_{OH} = -2.0$
V_{OL}			0.4	V	$V_{DD} = 3.15$; $I_{OL} = 2.0$
I_{OL}			2.0	mA	
I_{OH}			-2.0	mA	
t_{RISE}			10	ns	$C_{LOAD} = 15$ pF
t_{FALL}			10	ns	$C_{LOAD} = 15$ pF
Leakage tristate	-10		+10	µA	0 to 5.25 V input
Output capacitance		7.5		pF	

Output Parameters For CMOS 4mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	$V_{DD} = 3.15$; $I_{OH} = -4.0$
V_{OL}			0.4	V	$V_{DD} = 3.15$; $I_{OL} = 4.0$
I_{OL}			4.0	mA	
I_{OH}			-4.0	mA	
t_{RISE}			10	ns	$C_{LOAD} = 15$ pF
t_{FALL}			10	ns	$C_{LOAD} = 15$ pF
Leakage tristate	-10		+10	µA	0 to 5.25 V input
Output capacitance		7.5		pF	

Output Parameters For CMOS 8mA (slew rate controlled)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 3.15; I_{OH} = -8.0
V_{OL}			0.4	V	V_{DD} = 3.15; I_{OL} = 8.0
I_{OL}			8.0	mA	
I_{OH}			-8.0	mA	
t_{RISE}			10	ns	C_{LOAD} = 25 pF
t_{FALL}			5	ns	C_{LOAD} = 25 pF
Leakage tristate	-10		+10	µA	0 to 5.25 V input
Output capacitance		7.5		pF	

Input/Output Parameters For TTL/CMOS 2mA and TTLp/CMOS 2mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.15 \leq V_{DD} \leq 3.45$
V_{IL}			0.8	V	$3.15 \leq V_{DD} \leq 3.45$
Input leakage current TTL	-10		+10	µA	0 to 5.25 V input
Input leakage current TTLp	-30	-100	-500	µA	0 to 5.25 V input
Input capacitance		7.5		pF	
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 3.15; I_{OH} = -2.0
V_{OL}			0.4	V	V_{DD} = 3.15; I_{OL} = 2.0
I_{OL}			2.0	mA	
I_{OH}			-2.0	mA	
t_{RISE}			10	ns	C_{LOAD} = 15 pF
t_{FALL}			10	ns	C_{LOAD} = 15 pF

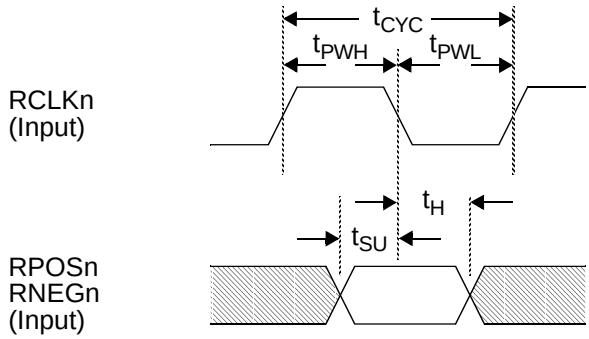
Input/Output Parameters For TTL/CMOS 8mA and TTLp/CMOS 8mA (slew rate controlled)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.15 \leq V_{DD} \leq 3.45$
V_{IL}			0.8	V	$3.15 \leq V_{DD} \leq 3.45$
Input leakage current TTL	-10		+10	µA	0 to 5.25 V input
Input leakage current TTLp	-30	-100	-500	µA	0 to 5.25 V input
Input capacitance		7.0		pF	
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 3.15; I_{OH} = -8.0
V_{OL}			0.4	V	V_{DD} = 3.15; I_{OL} = 8.0
I_{OL}			8.0	mA	
I_{OH}			-8.0	mA	
t_{RISE}			10	ns	C_{LOAD} = 25 pF
t_{FALL}			5	ns	C_{LOAD} = 25 pF

TIMING CHARACTERISTICS

Detailed timing diagrams for the E1Fx8 are illustrated in Figures 4 through 37, with values of the timing intervals tabulated below the waveform diagrams in each figure. All output times are measured with a maximum 25 pF load capacitance. Timing parameters are measured at voltage levels of $(V_{IH} + V_{IL})/2$ for input signals or $(V_{OH} + V_{OL})/2$ for output signals, unless otherwise indicated.

Figure 4. Dual Unipolar (RAIL) Receive Interface Timing



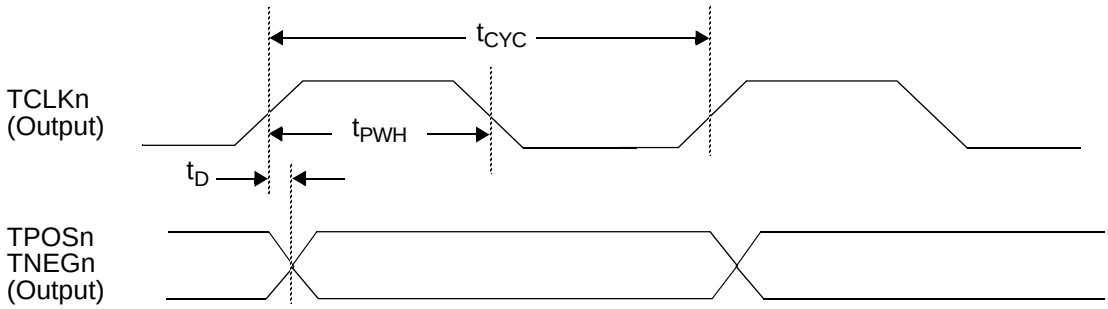
Note: n=1- 8

Parameter	Symbol	Min	Typ	Max	Unit
RCLKn clock period (see Note 2)	t_{CYC}	435	488.3		ns
RCLKn high time	t_{PWH}	180	0.5 x t_{CYC}		ns
RCLKn low time	t_{PWL}	180	0.5 x t_{CYC}		ns
RPOSn/RNEGn setup time to RCLKn↓	t_{SU}	5.0			ns
RPOSn/RNEGn hold time after RCLKn↓	t_H	15			ns

Notes:

1. RCLKn is shown for control bit RXCP (bit 5) in register X+00H set to 0. Data (RPOSn/RNEGn) is clocked in on the rising edges of RCLKn when control bit RXCP is a 1.
2. The minimum frequency of SYSCI must guarantee that at least 9 rising edges of SYSCI occur between any two consecutive rising or falling edges of any particular RCLKn.

Figure 5. Dual Unipolar (RAIL) Transmit Interface Timing

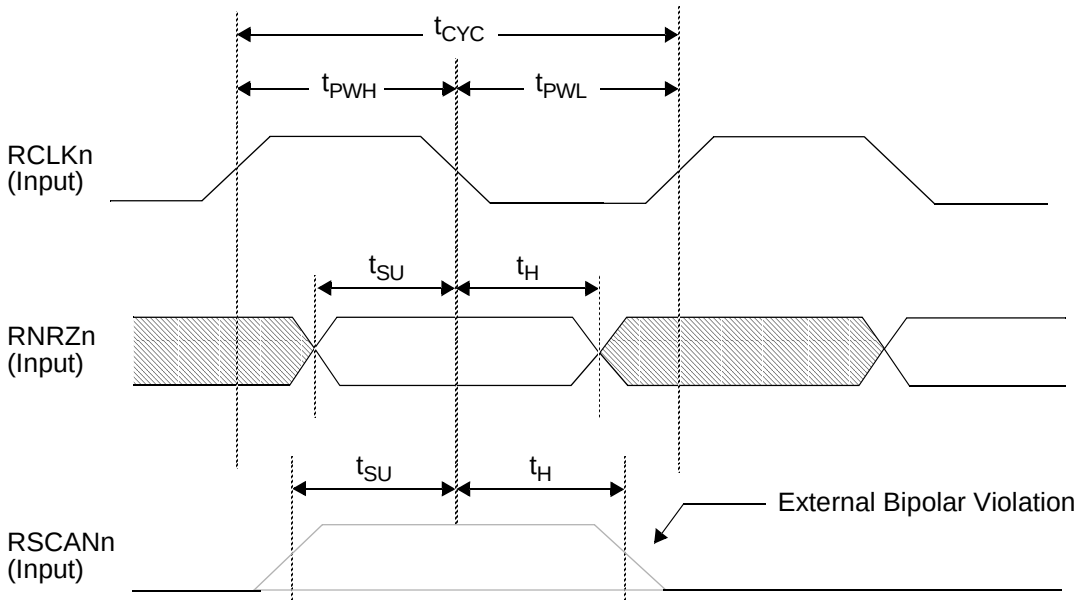


Note: n=1- 8

Parameter	Symbol	Min	Typ	Max	Unit
TCLKn clock period	t_{CYC}		488.3		ns
TCLKn duty cycle (t_{PWH}/t_{CYC})	--	45	50	55	%
TPOSn/TNEGn delay after TCLKn↑	t_D	0	5.0	10	ns

Note: TCLKn is shown for control bit TXCP (bit 3) in register X+05H set to 1. Data is clocked out on falling edges of TCLKn when control bit TXCP is a 0.

Figure 6. NRZ Receive Interface Timing (External Transceiver)



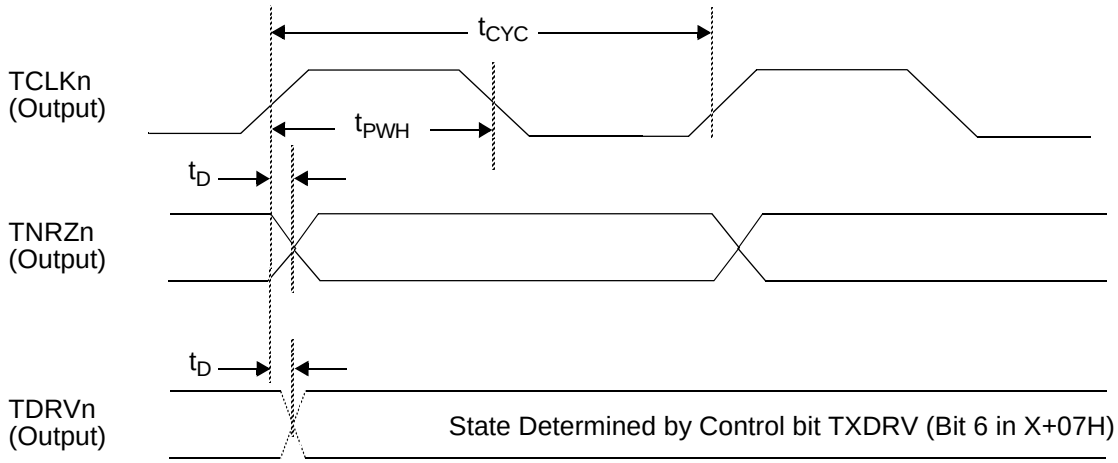
Note: n=1 - 8

Parameter	Symbol	Min	Typ	Max	Unit
RCLKn clock period (see Note 2)	t_{CYC}	435	488.3		ns
RCLKn high time	t_{PWH}	180	0.5 x t_{CYC}		ns
RCLKn low time	t_{PWL}	180	0.5 x t_{CYC}		ns
RNRZn/RSCANn setup time to RCLKn↓	t_{SU}	5.0			ns
RNRZn/RSCANn hold time after RCLKn↓	t_H	15			ns

Notes:

1. The above figure is valid when control bit RAIL (bit 7 in register X+00H) is set to a 0.
2. RCLKn is shown for control bit RXCP (bit 5 in register X+00H) set to 0. RNRZn and RSCANn are clocked in on rising edges of RCLKn when control bit RXCP is a 1. The E1Fx8 accepts an inverted RNRZn signal when control bit RXNRZ (bit 4 in register X+00H) is a 1. Control bit RXFS (bit 1 in register X+1FFH) must be set to 0 to use the RSCANn input for code violation counting.
3. The minimum frequency of SYSCI must guarantee that at least 9 rising edges of SYSCI occur between any two consecutive rising or falling edges of any particular RCLKn.

Figure 7. NRZ Transmit Interface Timing (External Transceiver)



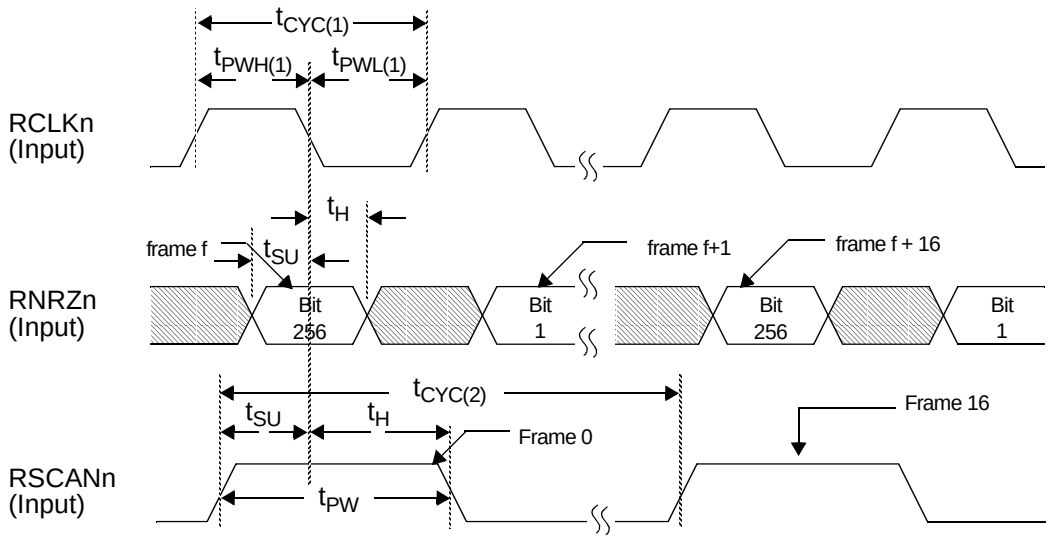
Note: n=1 - 8

Parameter	Symbol	Min	Typ	Max	Unit
TCLKn clock period	t_{CYC}		488.3		ns
TCLKn duty cycle (t_{PWH}/t_{CYC})	--	45	50	55	%
TNRZn/TDRVn delay after TCLKn↑	t_D	0	5.0	10	ns

Notes:

1. The above figure is valid when control bit RAIL (bit 7 in register X+00H) is set to a 0.
2. TCLKn is shown for control bit TXCP (bit 3 in register X+05H) set to 1. TNRZn and TDRVn are clocked out on falling edges of TCLKn when control bit TXCP is a 0. The E1Fx8 provides an inverted TNRZn signal when control bit TXNRZ (bit 2 in register X+05H) is a 1.
3. Control bit TDFME (bit 6 in register X+07H) must be set to 0 to obtain the TDRVn output shown.

Figure 8. NRZ Receive Interface Timing (Fast Sync Mode)

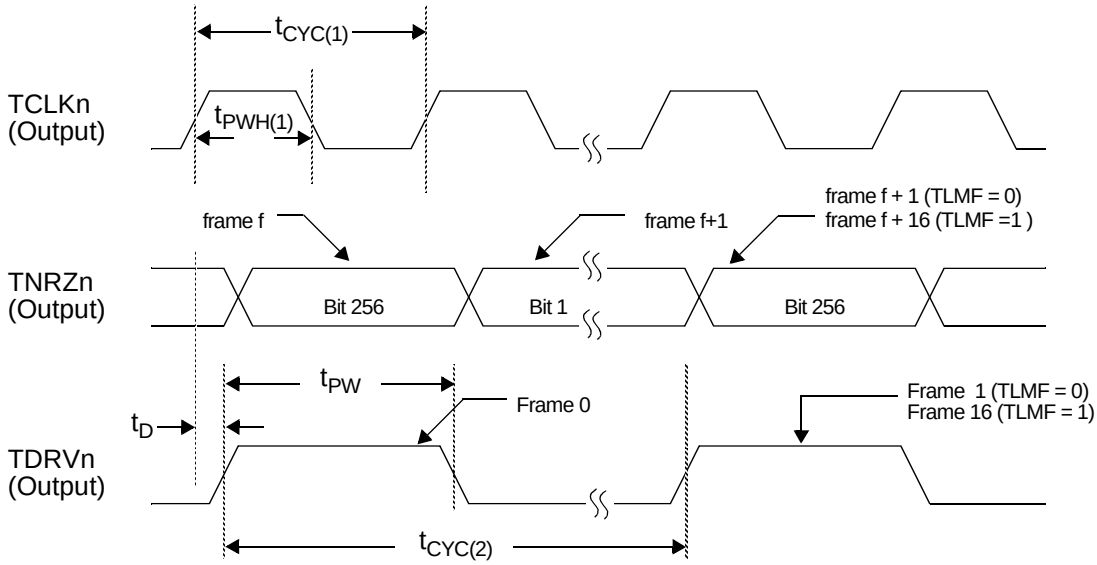


Note: n=1 - 8

Parameter	Symbol	Min	Typ	Max	Unit
RCLKn clock period	$t_{CYC(1)}$	435	488.3		ns
RCLKn high time	$t_{PWH(1)}$	180	0.5 x $t_{CYC(1)}$		ns
RCLKn low time	$t_{PWL(1)}$	180	0.5 x $t_{CYC(1)}$		ns
RNRZn/RSCANn setup time to RCLKn↓	t_{SU}	15			ns
RNRZn/RSCANn hold time after RCLKn↓	t_H	15			ns
RSCANn period	$t_{CYC(2)}$		256 x 16 x $t_{CYC(1)}$		ns
RSCANn pulse width high time	t_{PW}	0.5 x $t_{CYC(1)}$	1 × $t_{CYC(1)}$	1.5 x $t_{CYC(1)}$	ns

Notes:
1. The above figure is valid when control bit RAIL (bit 7 in register X+00H) is set to a 0.
2. RCLKn is shown for control bit RXCP (bit 5 in register X+00H) set to 0. Data is clocked in on rising edges when control bit RXCP is a 1. The E1Fx8 will accept an inverted RNRZn signal when a 1 is written to control bit RXNRZ (bit 4) in register X+00H).
3. The fast sync mode is selected by writing a 1 to control bit RXFS (bit 1 in register X+1FFH).

Figure 9. NRZ Transmit Interface Timing (Fast Sync Mode)



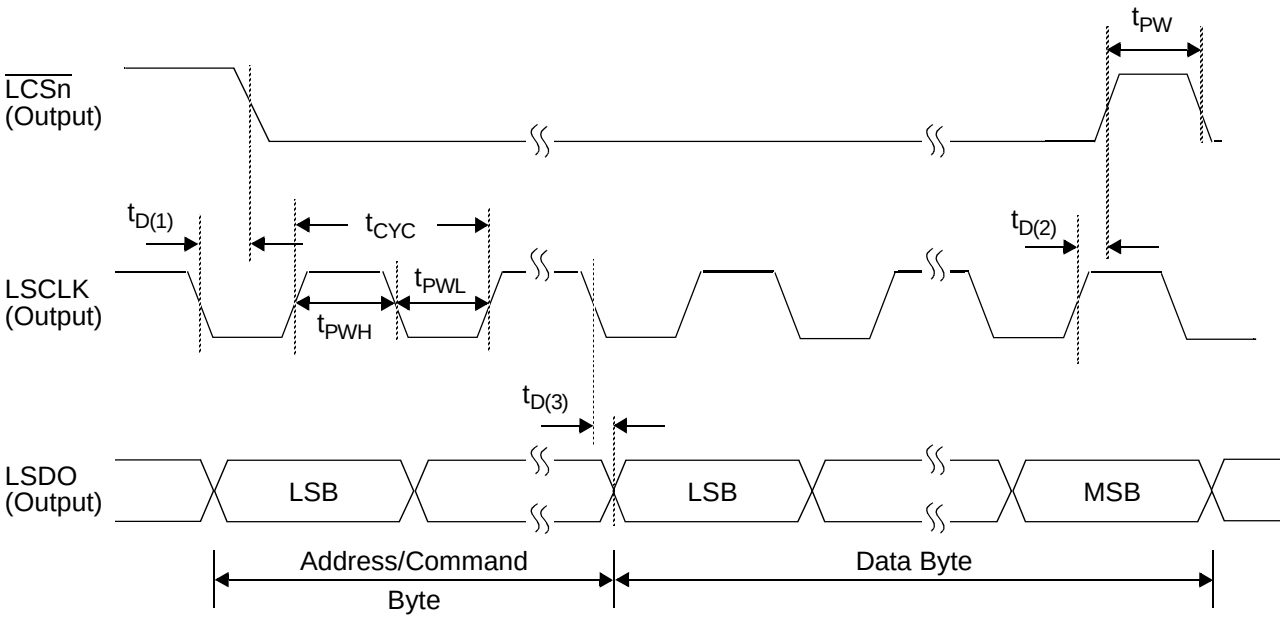
Note: n=1 - 8

Parameter	Symbol	Min	Typ	Max	Unit
TCLKn clock period	$t_{CYC(1)}$		488.3		ns
TCLKn duty cycle $t_{PWH(1)}/t_{CYC(1)}$		45	50	55	%
TDRVn delay after TCLKn↑	t_D	0		10	ns
TDRVn pulse width high time	t_{PW}		$1 \times t_{CYC(1)}$		ns
TDRVn period control bit TLMF = 0	$t_{CYC(2)}$		256 x $t_{CYC(1)}$		ns
TDRVn period control bits TLMF =1	$t_{CYC(2)}$		256 x 16 x $t_{CYC(1)}$		ns

Notes:

1. The above figure is valid when control bit RAIL (bit 7 in register X+00H) is set to a 0.
2. TCLKn is shown for control bit TXCP (bit 3 in register X+05H) set to 1. TNRZn/TDRVn is clocked out on falling edges of LTCLKn when control bit TXCP is set to 0. The E1Fx8 will output an inverted TNRZn signal when control bit TXNRZ (bit 2 in register X+05H) is a 1.
3. The fast sync mode is selected by writing a 1 to control bit TDFME (bit 7 in register X+07H).

Figure 10. Serial Port Write Timing



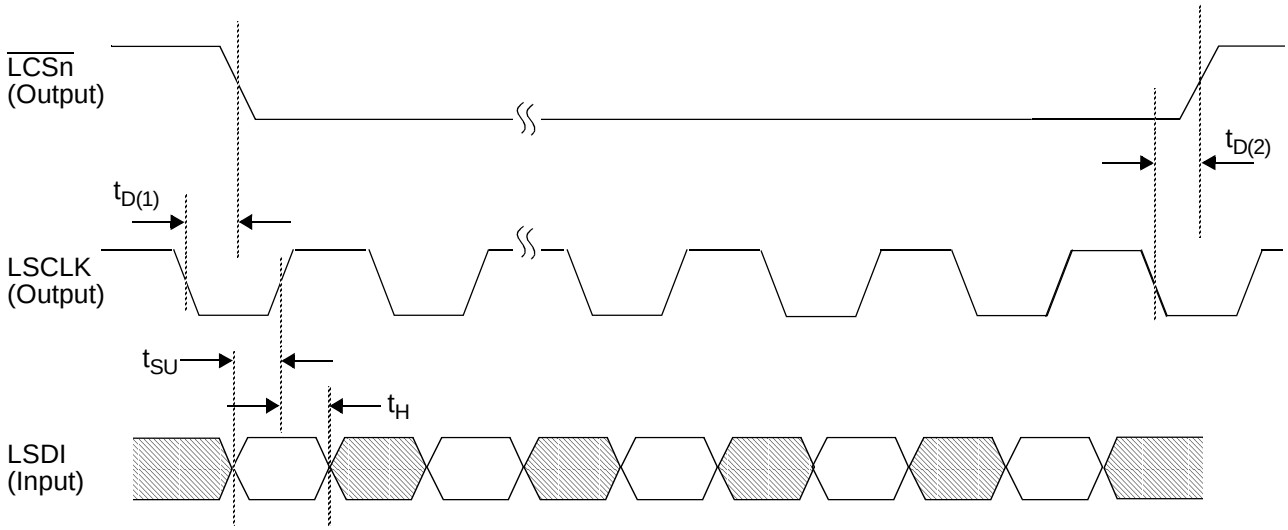
Note: n=1 - 8

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{\text{LCSn}}$ pulse width high time	t_{PW}	300			ns
LSCLK clock period (see Note 2)	t_{CYC}	480	488.3		ns
LSCLK high time	t_{PWH}	190	0.5 x t_{CYC}		ns
LSCLK low time	t_{PWL}	190	0.5 x t_{CYC}		ns
$\overline{\text{LCSn}}$ delay after LSCLK↓	$t_{D(1)}$	0	5.0	12	ns
LSDO delay after LSCLK↓	$t_{D(3)}$	0	5.0	10	ns
$\overline{\text{LCSn}}$ delay after LSCLK↑	$t_{D(2)}$	0	5.0	10	ns

Notes:

1. The serial port interface for the line interface transceiver is selected in the 208-lead package when control bit ESPBMON (bit 5 in register 01DH) is set to 0.
2. The clock period for LSCLK is the same as that of the signal provided on the BPOSC input lead because LSCLK is derived from the signal at BPOSC.

Figure 11. Serial Port Read Timing

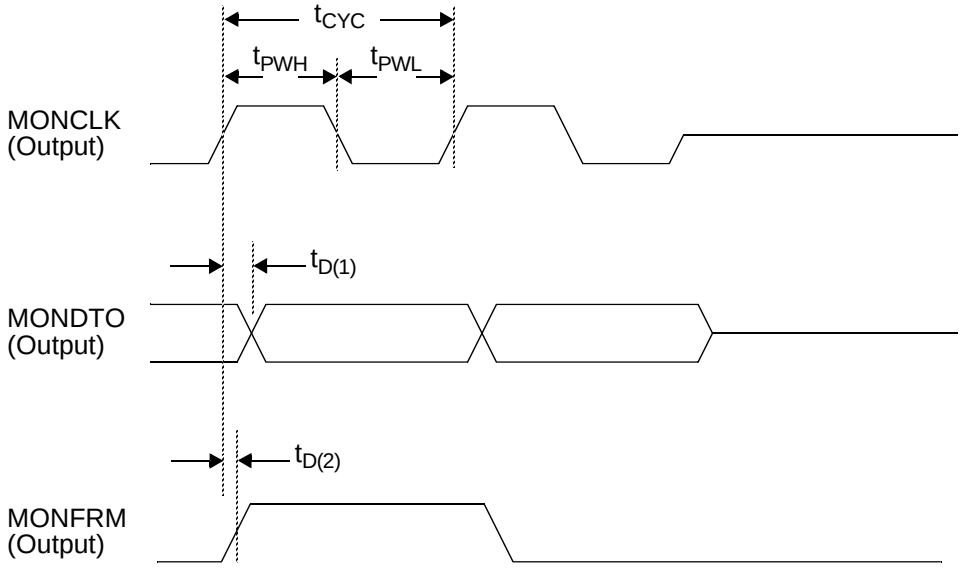


Parameter	Symbol	Min	Typ	Max	Unit
LSDI setup time to LSCLK↑	t_{SU}	10			ns
LSDI hold time after LSCLK↑	t_H	10			ns
$\overline{LCSn}$↓ delay after LSCLK↓	$t_{D(1)}$	0	5.0	10	ns
$\overline{LCSn}$↑ delay after LSCLK↓	$t_{D(2)}$	0	5.0	10	ns

Notes:

1. The serial port interface for the line interface transceiver is selected in the 208-lead package when control bit ESPBMON (bit 5 in register 01DH) is set to 0.
2. The clock period for LSCLK is the same as that of the signal provided on the BPOSC input lead because LSCLK is derived from the signal at BPOSC.

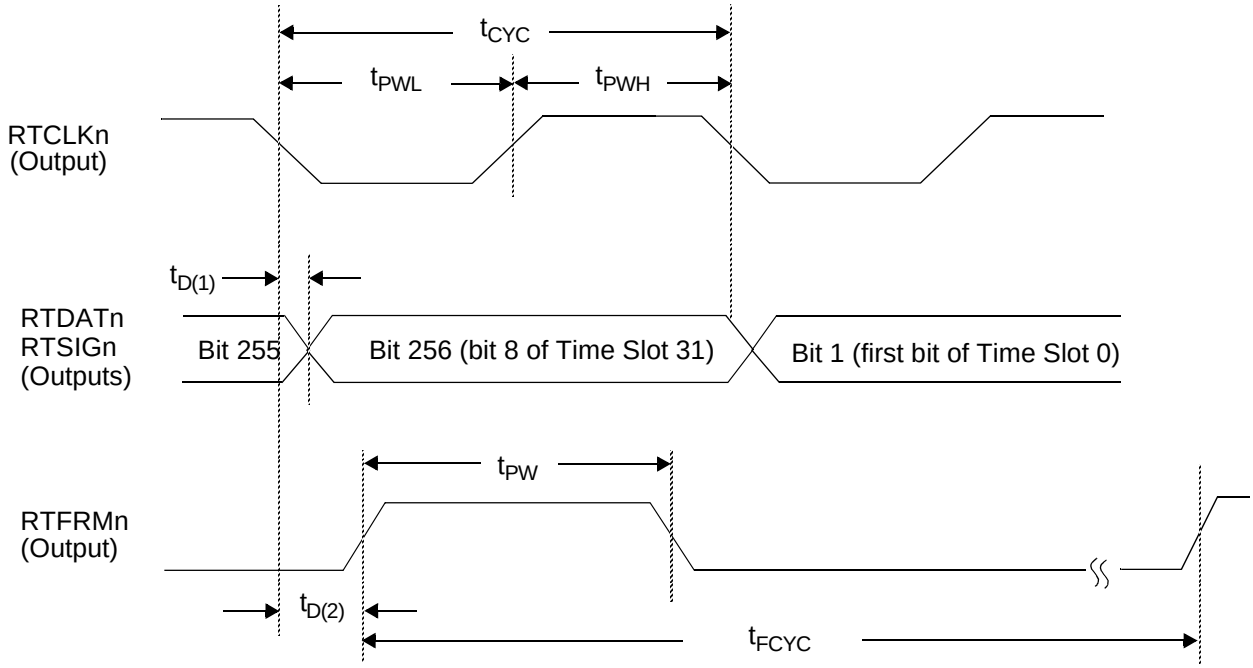
Figure 12. Monitor Mode Timing



Parameter	Symbol	Min	Typ	Max	Unit
MONCLK clock period	t_{CYC}		488.3		ns
MONCLK high time	t_{PWH}		0.5 x t_{CYC}		ns
MONCLK low time	t_{PWL}		0.5 x t_{CYC}		ns
MONDTO delay after MONCLK↑	$t_{D(1)}$	-1.0		5.0	ns
MONFRM delay after MONCLK↑	$t_{D(2)}$	-1.0		5.0	ns

Note: When control bit MONTR (bit 5 in control register 022H) is set to a 1 the MONCLK, MONDTO and MONFRM leads are tristated. When MONTR is set to 0 the monitor function in the E1Fx8 is enabled; for the 208-lead package control bit ESPBMON (bit 5 in register 01DH) must be set to 1 also. Control bits MFR2 - MFR0 (bits 2 - 0 in register 022H) select the channel to be monitored. Control bit MONRX (bit 7 in register 022H) selects either the receive side or transmit side to be monitored; when MONRX is set to a 0 the transmit framer output is monitored. Writing a 1 to control bit MONRX and a 0 to control bit MONRF (bit 6 in register 022H) monitors the receive signal at the input to the receive framer. Writing a 1 to both control bits MONRF and MONRX monitors the receive signal at the output of the receive framer.

Figure 13. Receive Highway Timing - Transmission Mode (Recovered Receive Line Clock)

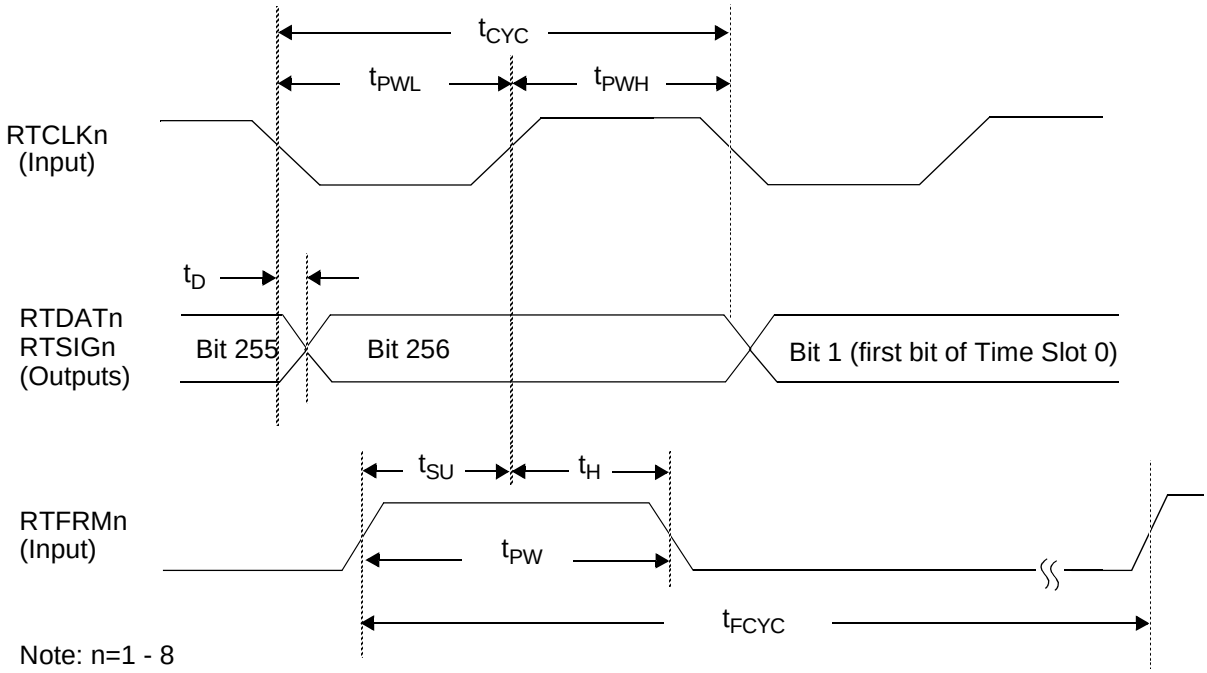


Note: n=1- 8

Parameter	Symbol	Min	Typ	Max	Unit
RTCLKn clock period	t_{CYC}	435	488.3		ns
RTCLKn low time	t_{PWL}	180	0.5 x t_{CYC}		ns
RTCLKn high time	t_{PWH}	180	0.5 x t_{CYC}		ns
RTDATn/RTSIGn delay after RTCLKn↓	$t_{D(1)}$	2.0	8.0	17	ns
RTFRMn delay after RTCLKn↓	$t_{D(2)}$	1.0	10	14	ns
RTFRMn pulse width	t_{PW}	435	488.3		ns
RTFRMn period	t_{FCYC}		256 x 16 x t_{CYC}		ns

Note: The Transmission Mode is selected when a low is placed on both CONF0 and CONF1 leads with control bit DINTF (bit 1 in register 00BH) set to a 0. The recovered receive line clock (RCLKn) and an internal sync pulse are used to clock out data (RTDATn), signaling (RTSIGn), and the sync pulse (RTFRMn) to the system, when control bit RXCKE (bit 7 in register X+11BH) is set to a 1. Control bit RXCKE selects the clock source, while RXSBE (bit 5 in register X+11BH) enables/disables the receive slip buffer. The position of RTFRMn with respect to the RTDATn/RTSIGn signals can be offset. The values written to control bits RFRM7 - RFRM0 (register 02EH) will determine the offset. RTFRMn is shown for an offset value equal to zero.

Figure 14. Receive Highway Timing - Transmission Mode (System Clock)

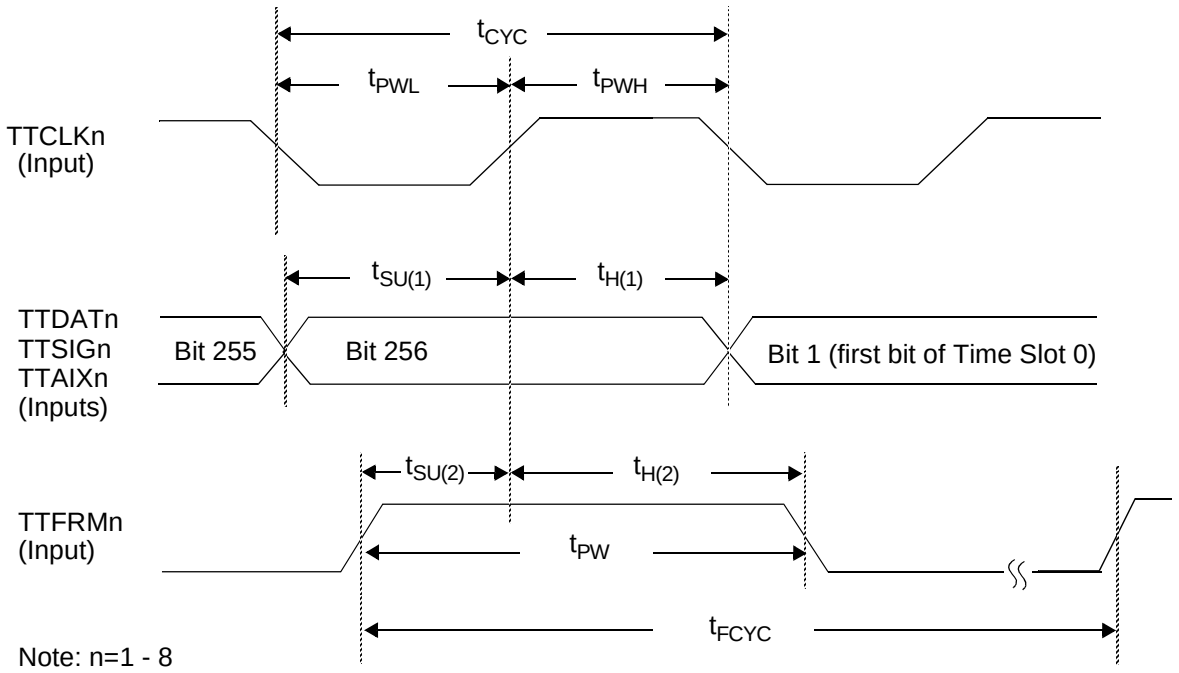


Parameter	Symbol	Min	Typ	Max	Unit
RTCLKn clock period	t_{CYC}	465	488.3		ns
RTCLKn low time	t_{PWL}	233	0.5 x t_{CYC}		ns
RTCLKn high time	t_{PWH}	233	0.5 x t_{CYC}		ns
RTDATn/RTSIGn delay after RTCLKn↓	t_D	5.0	15	28	ns
RTFRMn setup time to RTCLKn↑	t_{SU}	10			ns
RTFRMn hold time after RTCLKn↑	t_H	15			ns
RTFRMn pulse width (see Note 2)	t_{PW}		1 x t_{CYC}		ns
RTFRMn period	t_{FCYC}		256 x 16 x t_{CYC}		ns

Notes:

1. The Transmission Mode is selected when a low is placed on both CONF0 and CONF1 leads with control bit DINTF (bit 1 in register 00BH) set to a 0. A system side clock (RTCLKn) and a sync pulse (RTFRMn) are used to clock out data (RTDATn) and signaling (RTSIGn) to the system, when control bit RXCKE (bit 7 in register X+11BH) is set to a 0. Control bit RXCKE selects the clock source, while RXSBE (bit 5 in register X+11BH) set to 1 enables the receive slip buffer. The position of RTFRMn with respect to the RTDATn/RTSIGn signals can be offset. The values written to control bits RFRM7 - RFRM0 (register 02EH) will determine the offset. RTFRMn is shown for an offset value equal to zero.
2. Only one rising edge of RTCLKn may occur during the time interval (t_{PW}) of the positive pulse for the RTFRMn input.

Figure 15. Transmit Highway Timing - Transmission Mode

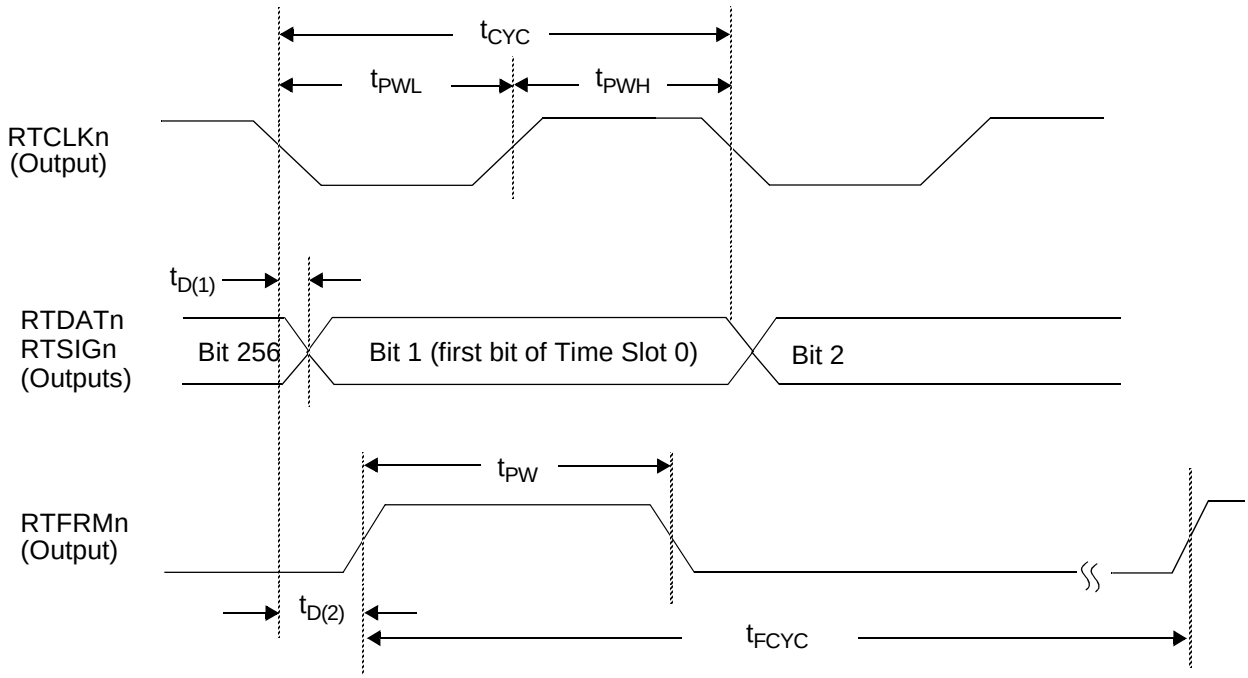


Parameter	Symbol	Min	Typ	Max	Unit
TTCLKn clock period	t_{CYC}	435	488.3		ns
TTCLKn low time	t_{PWL}	180	0.5 x t_{CYC}		ns
TTCLKn high time	t_{PWH}	180	0.5 x t_{CYC}		ns
TTDATn/TTSIGn/TTAIXn setup time to TTCLKn↑	$t_{SU(1)}$	12			ns
TTDATn/TTSIGn/TTAIXn hold time after TTCLKn↑	$t_{H(1)}$	12			ns
TTFRMn setup time to TTCLKn↑	$t_{SU(2)}$	12			ns
TTFRMn hold time after TTCLKn↑	$t_{H(2)}$	12			ns
TTFRMn pulse width (see Note 2)	t_{PW}		1 x t_{CYC}		ns
TTFRMn period	t_{FCYC}		256 x 16 x t_{CYC}		ns

Notes:

1. The Transmission Mode is selected when a low is placed on both CONF0 and CONF1 leads with control bit DINTF (bit 1 in register 00BH) set to a 0. The position of TTFRMn with respect to the TTDATn/TTSIGn/TTAIXn signals can be offset. The values written to control bits TFRM7-TFRM0 (register 02FH) will determine the offset. TTFRMn is shown for an offset value equal to zero.
2. Only one rising edge of TTCLKn may occur during the time interval (t_{PW}) of the positive pulse for the TTFRMn input.

Figure 16. Receive Highway Timing - Data Mode (Recovered Receive Line Clock)

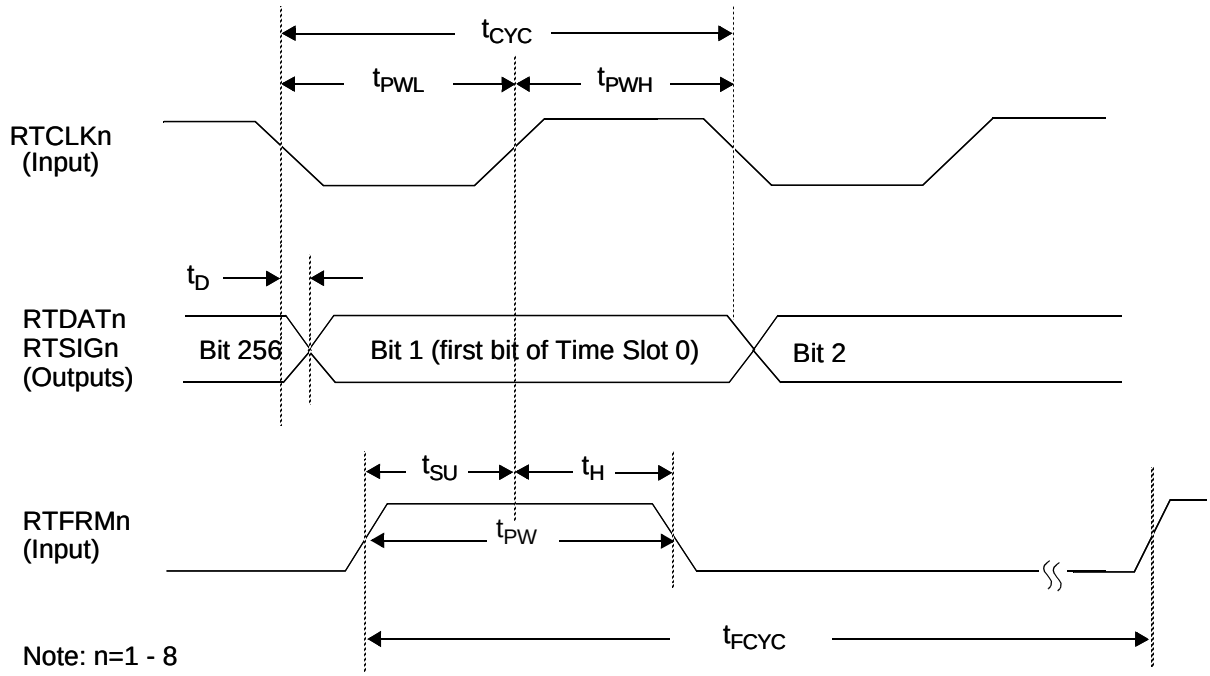


Note: n=1- 8

Parameter	Symbol	Min	Typ	Max	Unit
RTCLKn clock period	t_{CYC}	435	488.3		ns
RTCLKn low time	t_{PWL}	180	0.5 x t_{CYC}		ns
RTCLKn high time	t_{PWH}	180	0.5 x t_{CYC}		ns
RTDATn/RTSIGn delay after RTCLKn↓	$t_{D(1)}$	2.0	8.0	17	ns
RTFRMn delay after RTCLKn↓	$t_{D(2)}$	1.0	8.0	14	ns
RTFRMn pulse width	t_{PW}	435	488.3		ns
RTFRMn period	t_{FCYC}		256 x t_{CYC}		ns

Note: The Data Mode is selected when a low is placed on both CONF0 and CONF1 leads with control bit DINTF (bit 1 in register 00BH) set to a 1. The recovered receive line clock (RCLKn) and an internal sync pulse are used to clock out data (RTDATn), signaling (RTSIGn), and the sync pulse (RTFRMn) to the system, when control bit RXCKE (bit 7 in register X+11BH) is set to a 1. Control bit RXCKE selects the clock source, while RXSBE (bit 5 in register X+11BH) enables/disables the receive slip buffer. The position of RTFRMn with respect to the RTDATn/RTSIGn signals can be offset. The values written to control bits RFRM7 - RFRM0 (register 02EH) will determine the offset. RTFRMn is shown for an offset value equal to zero.

Figure 17. Receive Highway Timing - Data Mode (System Clock)

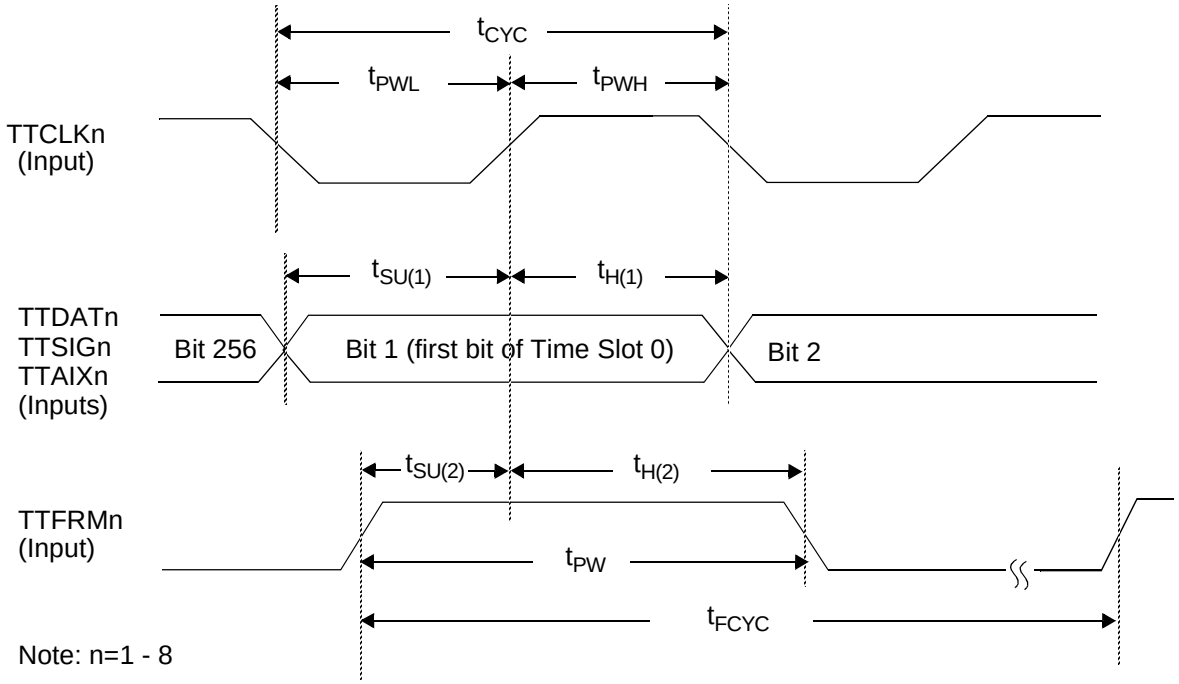


Parameter	Symbol	Min	Typ	Max	Unit
RTCLKn clock period	t_{CYC}	465	488.3		ns
RTCLKn low time	t_{PWL}	233	0.5 x t_{CYC}		ns
RTCLKn high time	t_{PWH}	233	0.5 x t_{CYC}		ns
RTDATn/RSTIGn delay after RTCLKn↓	t_D	5.0	15	28	ns
RTFRMn setup time to RTCLKn↑	t_{SU}	10			ns
RTFRMn hold time after RTCLKn↑	t_H	15			ns
RTFRMn pulse width (see Note 2)	t_{PW}		1 x t_{CYC}		ns
RTFRMn period	t_{FCYC}		256 x t_{CYC}		ns

Notes:

1. The Data Mode is selected when a low is placed on both CONF0 and CONF1 leads with control bit DINTF (bit 1 in register 00BH) set to a 1. A system side clock (RTCLKn) and a sync pulse (RTFRMn) are used to clock out data (RTDATn) and signaling (RTSIGn) to the system, when control bit RXCKE (bit 7 in register X+11BH) is set to a 0. Control bit RXCKE selects the clock source, while RXSBE (bit 5 in register X+11BH) set to 1 enables the receive slip buffer. The position of RTFRMn with respect to the RTDATn/RTSIGn signals can be offset. The values written to control bits RFRM7-RFRM0 (register 02EH) will determine the offset. RTFRMn is shown for an offset value equal to zero.
2. Only one rising edge of RTCLKn may occur during the time interval (t_{PW}) of the positive pulse for the RTFRMn input.

Figure 18. Transmit Highway Timing - Data Mode

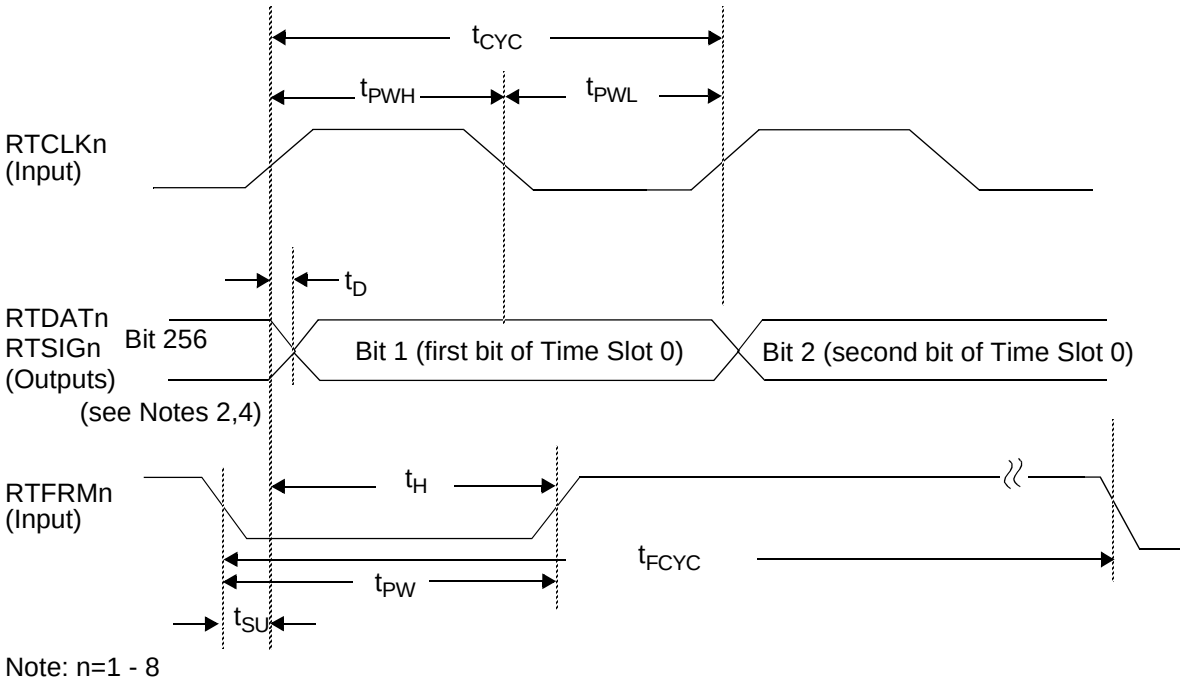


Parameter	Symbol	Min	Typ	Max	Unit
TTCLKn clock period	t_{CYC}	435	488.3		ns
TTCLKn low time	t_{PWL}	180	0.5 x t_{CYC}		ns
TTCLKn high time	t_{PWH}	180	0.5 x t_{CYC}		ns
TTDATn/TTSIGn/TTAIXn setup time to TTCLKn↑	$t_{SU(1)}$	12			ns
TTDATn/TTSIGn/TTAIXn hold time after TTCLKn↑	$t_{H(1)}$	12			ns
TTFRMn setup time to TTCLKn↑	$t_{SU(2)}$	12			ns
TTFRMn hold time after TTCLKn↑	$t_{H(2)}$	12			ns
TTFRMn pulse width (see Note 2)	t_{PW}		1 x t_{CYC}		ns
TTFRMn period	t_{FCYC}		256 x t_{CYC}		ns

Notes:

1. The Data Mode is selected when a low is placed on both CONF0 and CONF1 leads with control bit DINTF (bit 1 in register 00BH) set to a 1. The position of TTFRMn with respect to the TTDATn/TTSIGn/TTAIXn signals can be offset. The values written to control bits TFRM7-TFRM0 (register 02FH) will determine the offset. TTFRMn is shown for an offset value equal to zero.
2. Only one rising edge of TTCLKn may occur during the time interval (t_{PW}) of the positive pulse for the TTFRMn input.

Figure 19. Receive Highway Timing - MVIP Mode



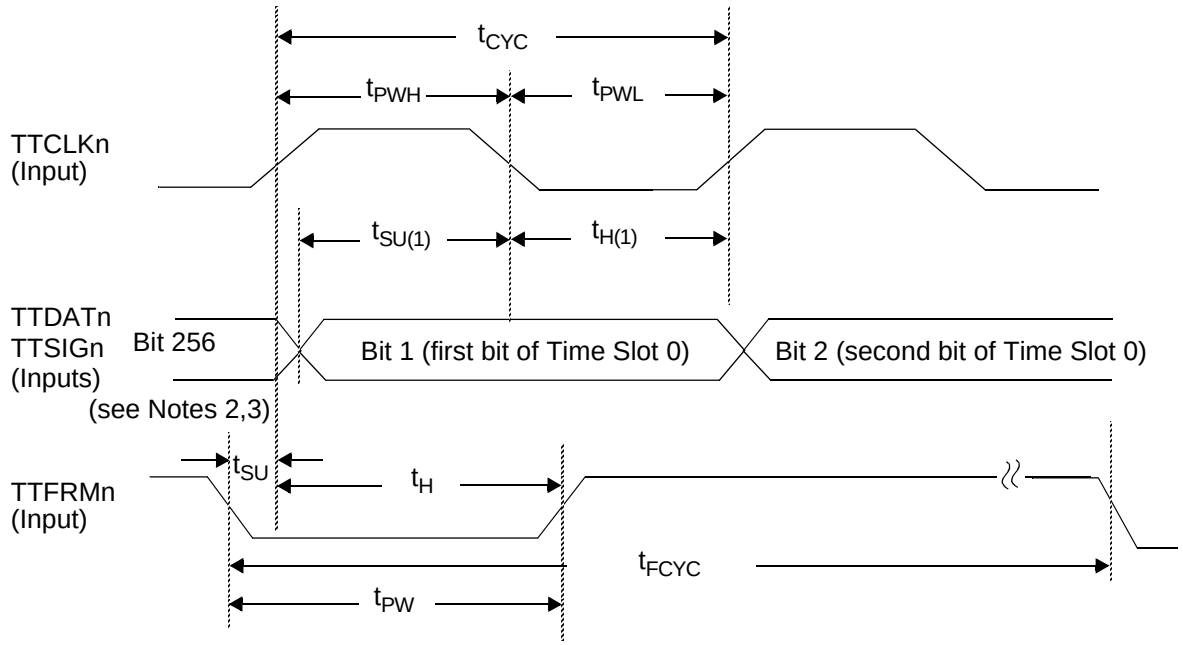
Note: n=1 - 8

Parameter	Symbol	Min	Typ	Max	Unit
RTCLKn clock period	t_{CYC}	465	488.3	513	ns
RTCLKn low time	t_{PWL}	220	0.5 x t_{CYC}	268	ns
RTCLKn high time	t_{PWH}	220	0.5 x t_{CYC}	268	ns
RTDATn/RTSIGn delay after RTCLKn↑	t_D	5.0	10	20	ns
RTFRMn setup time to RTCLKn↑	t_{SU}	10			ns
RTFRMn hold time after RTCLKn↑	t_H	15			ns
RTFRMn pulse width low time; (see Note 3)	t_{PW}	200	488	500	ns
RTFRMn period	t_{FCYC}		256 x t_{CYC}		ns

Notes:

1. The MVIP Mode is selected when a high is placed on CONF0 lead and a low is placed on CONF1 lead. A system side clock (RTCLKn) and a sync pulse (RTFRMn) are used to clock out data (RTDATn) and signaling (RTSIGn) to the system, when control bit RXCKE (bit 7 in register X+11BH) is set to a 0. Control bit RXCKE selects the clock source, while RXSBE (bit 5 in register X+11BH) set to 1 enables the receive slip buffer. The position of RTFRMn with respect to the RTDATn/RTSIGn signals can be offset. The values written to control bits RFRM7 - RFRM0 (register 02EH) will determine the offset. RTFRMn is shown for an offset value equal to zero.
2. On RTDATn bit 256 is bit 8 of Time Slot 31. On RTSIGn bit 256 is the D signaling bit of Time Slot 31.
3. RTFRMn should not be held low for more than 10 RTCLKn clock cycles under any circumstances.
4. When referring to MVIP standards, bit 256 is bit 0 of Time Slot 31 (channel 31). Bit 1 of the frame is bit 7 of Time Slot 0 (channel 0) and bit 2 of the frame is bit 6 of Time Slot 0 (channel 0).

Figure 20. Transmit Highway Timing - MVIP Mode



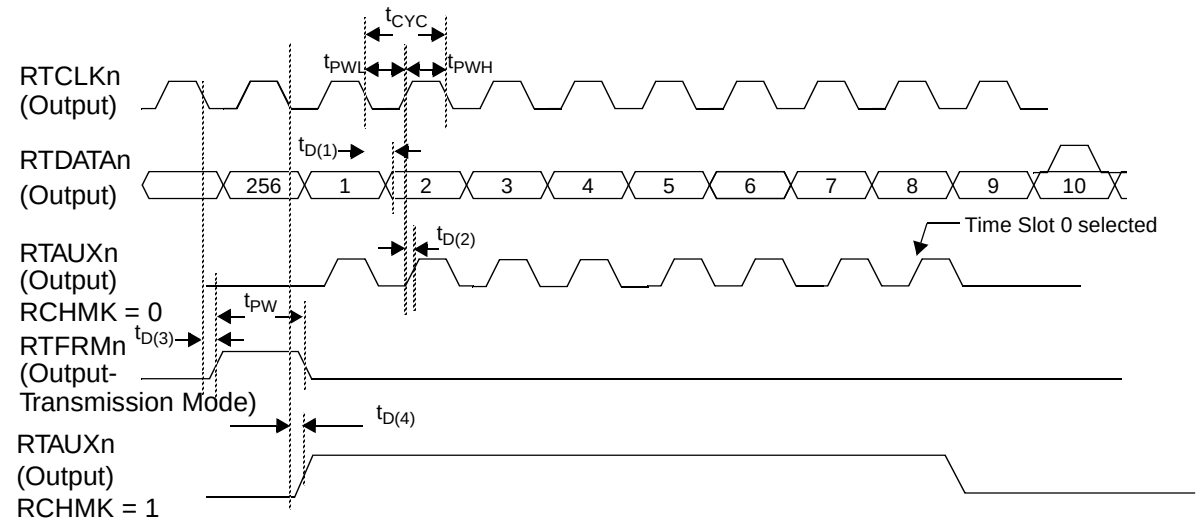
Note: n=1 - 8

Parameter	Symbol	Min	Typ	Max	Unit
TTCLKn clock period	t_{CYC}	480	488.3	497	ns
TTCLKn low time	t_{PWL}	220	0.5 x t_{CYC}	268	ns
TTCLKn high time	t_{PWH}	220	0.5 x t_{CYC}	268	ns
TTDATn/TTSIGn setup time to TTCLKn↓	$t_{SU(1)}$	12			ns
TTDATn/TTSIGn hold time after TTCLKn↓	$t_{H(1)}$	12			ns
TTFRMn setup time to TTCLKn↑	t_{SU}	10			ns
TTFRMn hold time after TTCLKn↑	t_{H}	10			ns
TTFRMn pulse width low time; (see Note 3)	t_{PW}	200	488	500	ns
TTFRMn period	t_{FCYC}		256 x t_{CYC}		ns

Notes:

1. The MVIP Mode is selected when a high is placed on CONF0 lead and a low is placed on CONF1 lead. The transmit slip buffer is always enabled in this mode by setting control bit TXSBE (bit 5 in register X+11CH) to a 1. The position of TTFRMn with respect to the TTDATn/TTSIGn signals can be offset. The values written to control bits TFRM7 - TFRM0 (register 02FH) will determine the offset. TTFRMn is shown for an offset value equal to zero.
2. On TTDATn bit 256 is bit 8 of Time Slot 31. On TTSIGn bit 256 is the D signaling bit of Time Slot 31.
3. TTFRMn should not be held low for more than 10 TTCLKn clock cycles under any circumstances.
4. When referring to MVIP standards, bit 256 is bit 0 of Time Slot 31 (channel 31). Bit 1 of the frame is bit 7 of Time Slot 0 (channel 0) and bit 2 of the frame is bit 6 of Time Slot 0 (channel 0).

Figure 21. Receive Highway Timing - Fractional E1 Gapped Clock (Rec. Line Clock Transmission & Data Modes)

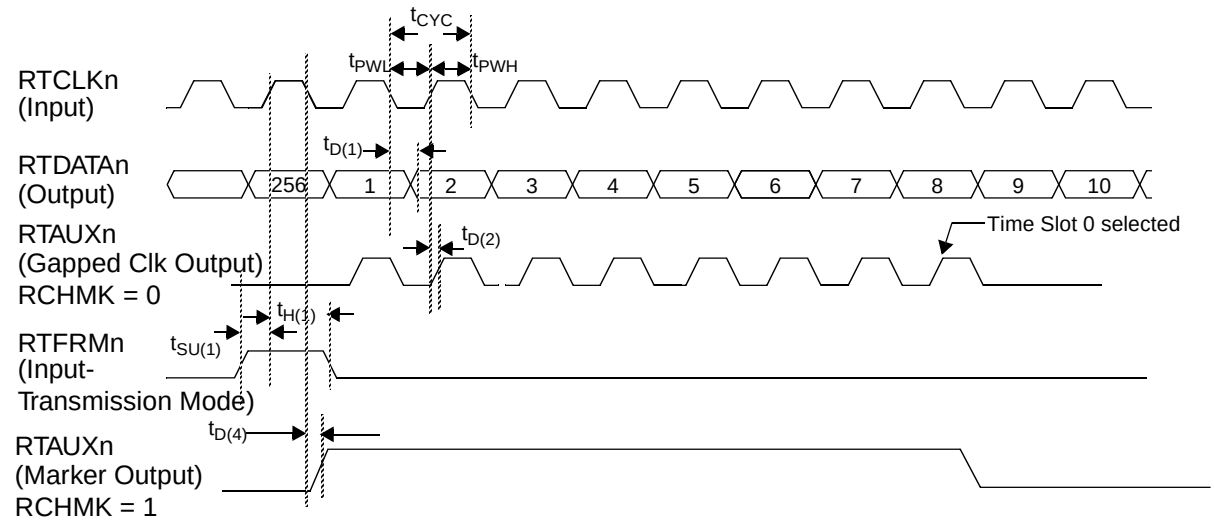


Note: n=1 - 8

Parameter	Symbol	Min	Typ	Max	Unit
RTCLKn clock period	t_{CYC}	435	488.3		ns
RTCLKn low time	t_{PWL}	180	0.5 x t_{CYC}		ns
RTCLKn high time	t_{PWH}	180	0.5 x t_{CYC}		ns
RTDATn delay after RTCLKn↓	$t_{D(1)}$	2.0	8.0	12	ns
RTAUXn↑ gapped clock delay after RTCLKn↑	$t_{D(2)}$	1.0		8.0	ns
RTFRMn delay after RTCLKn↓	$t_{D(3)}$	1.0	6.0	10	ns
RTAUXn↑ marker delay after RTCLKn↓	$t_{D(4)}$	3.0		15	ns
RTFRMn pulse width	t_{PW}	435	488.3		ns

Note: The fractional E1 gapped clock or marker feature is enabled when a low is placed on both CONF0 and CONF1 leads with control bit DINTF (bit 1 in register 00BH) set to a 1 for Data Mode or set to a 0 for Transmission Mode and control bit FE1M (bit 4 in register X+07H) is written with a 1 when the 208-lead version is used. One or more time slots may be selected by writing a 1 to one or more control bits RFCH1-RFCH32 (in registers X+1BH-X+1EH). If control bit RCHMK (bit 7 in register X+1AH) is set to a 1 a marker signal is provided in place of a gapped clock.

Figure 22. Receive Highway Timing - Fractional E1 Gapped Clock (System Clock Transmission & Data Modes)

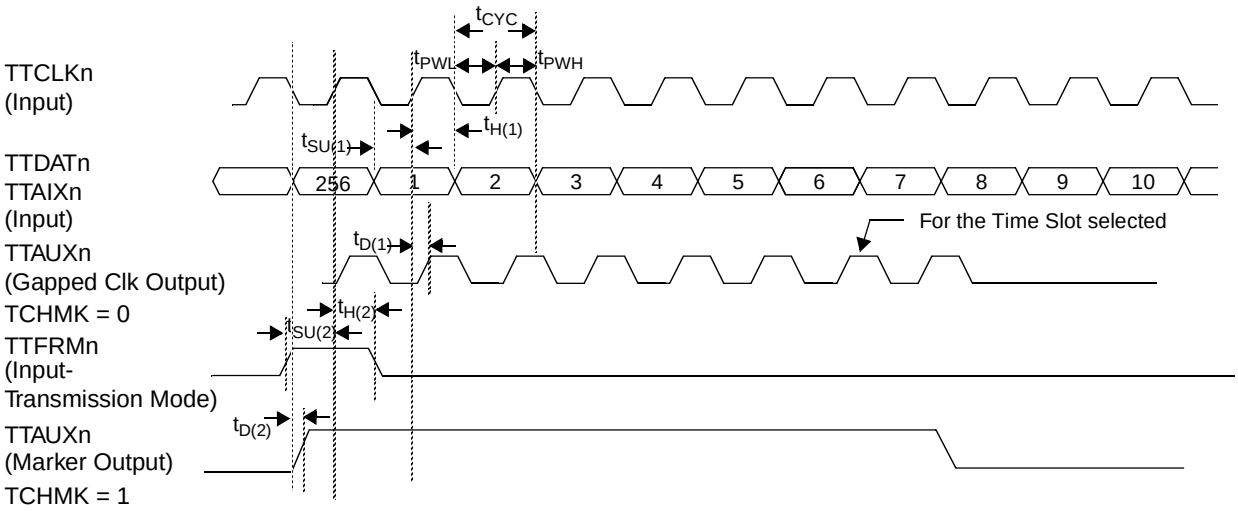


Note: n=1 - 8

Parameter	Symbol	Min	Typ	Max	Unit
RTCLKn clock period	t_{CYC}	465	488.3		ns
RTCLKn low time	t_{PWL}	180	0.5 x t_{CYC}		ns
RTCLKn high time	t_{PWH}	180	0.5 x t_{CYC}		ns
RTDATn delay after RTCLKn↓	$t_{D(1)}$	5.0		20	ns
RTAUXn↑ gapped clock delay after RTCLKn↑	$t_{D(2)}$	5.0		20	ns
RTFRMn hold after RTCLKn↑	$t_{SU(1)}$	15			ns
RTAUXn↑ marker delay after RTCLKn↓	$t_{D(4)}$	5.0		25	ns
RTFRMn setup before RTCLKn↑	$t_{H(1)}$	10			ns

Note: The fractional E1 gapped clock or marker feature is enabled when a low is placed on both CONF0 and CONF1 leads with control bit DINTF (bit 1 in register 00BH) set to a 1 for Data Mode or set to a 0 for Transmission Mode and control bit FE1M (bit 4 in register X+07H) is written with a 1 when the 208-lead version is used. One or more time slots may be selected by writing a 1 to one or more control bits RFCH1-RFCH32 (in registers X+1BH-X+1EH). If control bit RCHMK (bit 7 in register X+1AH) is set to a 1 a marker signal is provided in place of a gapped clock.

Figure 23. Transmit Highway Timing - Fractional E1 Gapped Clock (Transmission & Data Modes)

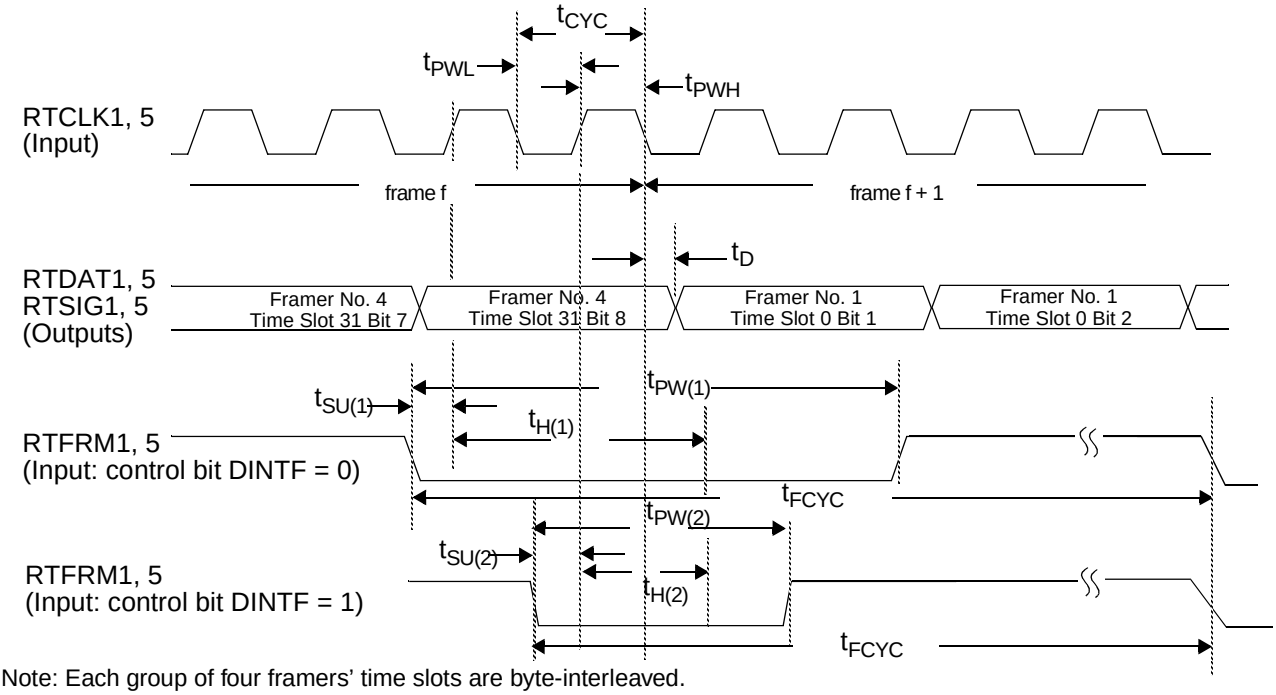


Note: n=1 - 8

Parameter	Symbol	Min	Typ	Max	Unit
TTCLKn clock period	t_{CYC}	422	488.3		ns
TTCLKn low time	t_{PWL}	190	0.5 x t_{CYC}		ns
TTCLKn high time	t_{PWH}	190	0.5 x t_{CYC}		ns
TTDATn/TTAIXn setup time to TTCLKn↑	$t_{SU(1)}$	12			ns
TTDATn/TTAIXn hold time after TTCLKn↑	$t_{H(1)}$	12			ns
TTFRMn setup time to TTCLKn↑	$t_{SU(2)}$	12			ns
TTFRMn hold time after TTCLKn↑	$t_{H(2)}$	12			ns
TTAUXn gapped clock output delay from TTCLKn↑	$t_{D(1)}$	5.0	10	25	ns
TTAUXn marker output delay from TTCLKn↓	$t_{D(2)}$	5.0	10	25	ns

Note: The fractional E1 gapped clock or marker feature is enabled when a low is placed on both CONF0 and CONF1 leads with control bit DINTF (bit 1 in register 00BH) set to a 1 for Data Mode or set to a 0 for Transmission Mode and control bit FE1M (bit 4 in register X+07H) is written with a 1 when the 208-lead version is used. One or more time slots may be selected by writing a 01 to one or more control bit pairs TC1C0/TC0C0-TC1C31/TC0C31 (in registers X+111H-X+118H). If control bit TCHMK (bit 7 in register X+110H) is set to a 1 a marker signal is provided in place of a gapped clock. Inputs from the TTAIXn lead replace time slots from the TTDATn lead for gapped clock or marker selections when control bit pairs TC1C0/TC0C0-TC1C31/TC0C31 are set to a 01.

Figure 24. Receive Highway Timing - 8 Mbit/s H-MVIP/ H.100 Mode



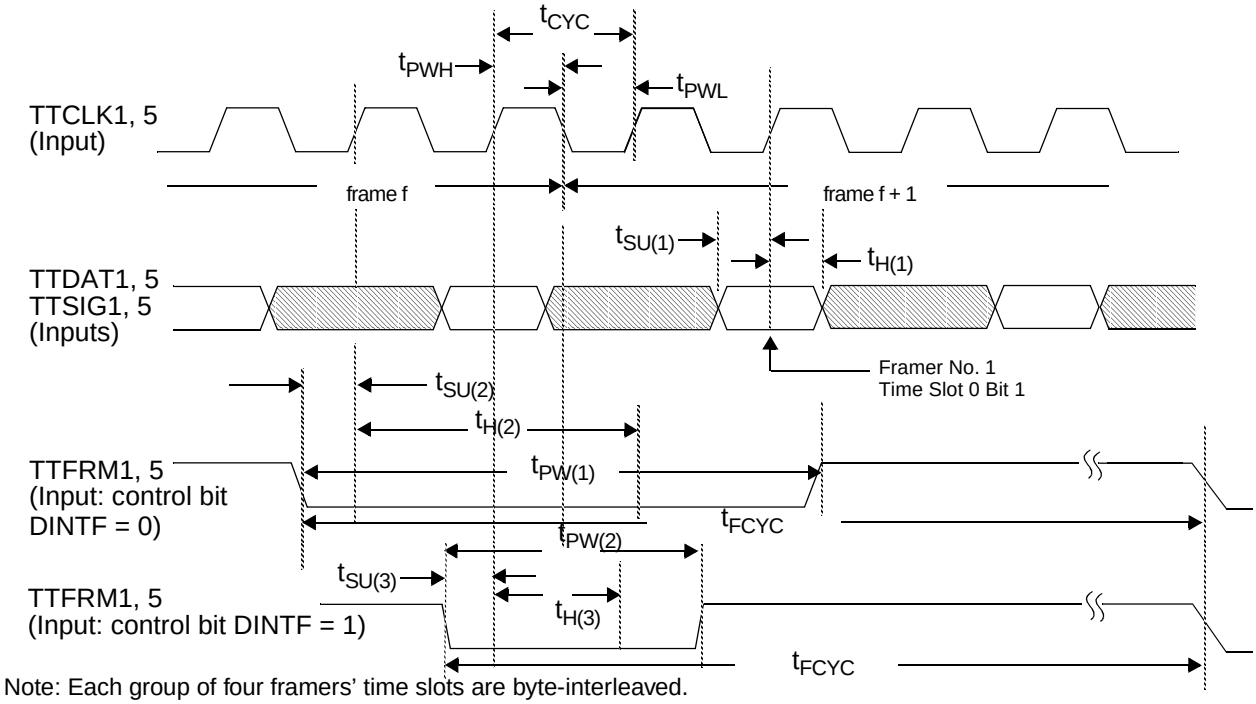
Note: Each group of four framers' time slots are byte-interleaved.

Parameter	Symbol	Min	Typ	Max	Unit
RTCLK1, 5 clock period	t_{CYC}	60	61		ns
RTCLK1, 5 low time	t_{PWL}	30	0.5 x t_{CYC}		ns
RTCLK1, 5high time	t_{PWH}	30	0.5 x t_{CYC}		ns
RTDAT1, 5/RTSIG1, 5 delay after RCLK1, 5↓	t_D	5.0	15	20	ns
RTFRM1, 5 setup time to RCLK1, 5↑; HMVIP	$t_{SU(1)}$	10			ns
RTFRM1, 5 hold time after RCLK1, 5↑; HMVIP	$t_{H(1)}$	10			ns
RTFRM1, 5 pulse width low time; HMVIP (see Note 3)	$t_{PW(1)}$	4 x t_{CYC}	4 x t_{CYC}	<5 x t_{CYC}	ns
RTFRM1, 5 setup time to RCLK1, 5↑; H.100	$t_{SU(2)}$	10			ns
RTFRM1, 5 hold time after RCLK1, 5↑; H.100	$t_{H(2)}$	10			ns
RTFRM1, 5 pulse width low time; H.100 (see Note 4)	$t_{PW(2)}$	2 x t_{CYC}	2 x t_{CYC}	<3 x t_{CYC}	ns
RTFRM1, 5 period	t_{FCYC}		2048 x t_{CYC}		ns

Notes:

1. The 8 Mbit/s H-MVIP/H.100 Mode is selected when a low is placed on the CONF0 lead and a high is placed on the CONF1 lead. Control bit DINTF (bit 1 in register 00BH) is set to a 1 for H.100 Mode or set to a 0 for H-MVIP Mode. A system side 16.384 MHz clock (RTCLK1, 5) and a 125 microsecond sync pulse (RTFRM1, 5) are used to clock out data (RTDAT1, 5) and signaling (RTSIG1, 5) to the system, when control bit RXCKE (bit 7 in register X+11BH) is set to a 0. Control bit RXCKE selects the clock source, while RXSBE (bit 5 in register X+11BH) set to 1 enables the receive slip buffer. The position of RTFRM1, 5 with respect to the RTDAT1, 5/RTSIG1, 5 signals can be offset in 8-clock cycle increments. The values written to control bits RFRM7 - RFRM0 (register 02EH) will determine the offset. RTFRMn is shown for an offset value equal to zero.
2. RTFRMn should not be held low for more than 10 RTCLKn clock cycles under any circumstances.
3. RTFRM1, 5 pulse widths may be wider than 4 x t_{CYC} as long as no more than 4 rising edges of RTCLK1, 5 occur while RTFRM1, 5 is low.
4. RTFRM1, 5 pulse widths may be wider than 2 x t_{CYC} as long as no more than 2 rising edges of RTCLK1, 5 occur while RTFRM1, 5 is low.

Figure 25. Transmit Highway Timing - 8 Mbit/s H-MVIP/ H.100 Mode



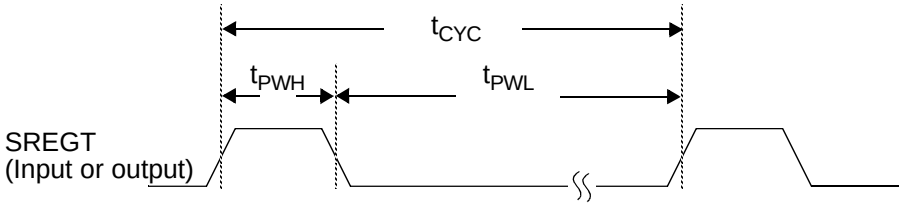
Note: Each group of four framers' time slots are byte-interleaved.

Parameter	Symbol	Min	Typ	Max	Unit
TTCLK1, 5 clock period	t_{CYC}	60	61		ns
TTCLK1, 5low time	t_{PWL}	30	0.5 x t_{CYC}		ns
TTCLK1, 5high time	t_{PWH}	30	0.5 x t_{CYC}		ns
TTDAT1, 5/TTSIG1, 5 setup time to TCLK1, 5↑	$t_{SU(1)}$	15			ns
TTDAT1, 5/TTSIG1, 5 hold time after TCLK1, 5↑	$t_{H(1)}$	5.0			ns
TTFRM1, 5 setup time to TCLK1, 5↑; HMVIP	$t_{SU(2)}$	15			ns
TTFRM1, 5 hold time after TCLK1, 5↑; HMVIP	$t_{H(2)}$	5.0			ns
TTFRM1, 5 pulse width low time; HMVIP (see Note 3)	$t_{PW(1)}$	4 x t_{CYC}	4 x t_{CYC}	<5 x t_{CYC}	ns
TTFRM1, 5 setup time to TCLK1, 5↑; H100	$t_{SU(3)}$	15			ns
TTFRM1, 5 hold time after TCLK1, 5↑; H100	$t_{H(3)}$	5.0			ns
TTFRM1, 5 pulse width low time; H100 (see Note 4)	$t_{PW(2)}$	2 x t_{CYC}	2 x t_{CYC}	<3 x t_{CYC}	ns
TTFRM1, 5 period	t_{FCYC}		2048 x t_{CYC}		ns

Notes:

1. The 8 Mbit/s H-MVIP/H.100 Mode is selected when a low is placed on the CONF0 lead and a high is placed on the CONF1 lead. Control bit DINTF (bit 1 in register 00BH) is set to a 1 for H.100 Mode or set to a 0 for H-MVIP Mode. A system side 16.384 MHz clock TTCLK1, 5) and a 125 microsecond sync pulse (TTFRM1, 5) are used to clock in data (TTDAT1, 5) and signaling (TTSIG1, 5) to the system. Control bit TXSBE (bit 5 in register X+11CH) always set to 1 enables the transmit slip buffer. The position of TTFRM1, 5 with respect to the TTDAT1, 5/TTSIG1, 5 signals can be offset in 8-clock cycle increments. The values written to control bits TFRM7-TFRM0 (register 02FH) will determine the offset. TTFRMn is shown for an offset value equal to zero.
2. TTFRMn should not be held low for more than 10 TTCLKn clock cycles under any circumstances.
3. TTFRM1, 5 pulse widths may be wider than 4 x t_{CYC} as long as no more than 4 rising edges of TTCLK1, 5 occur while RTFRM1, 5 is low.
4. TTFRM1, 5 pulse widths may be wider than 2 x t_{CYC} as long as no more than 2 rising edges of TTCLK1, 5 occur while RTFRM1, 5 is low.

Figure 26. Shadow Register Timing

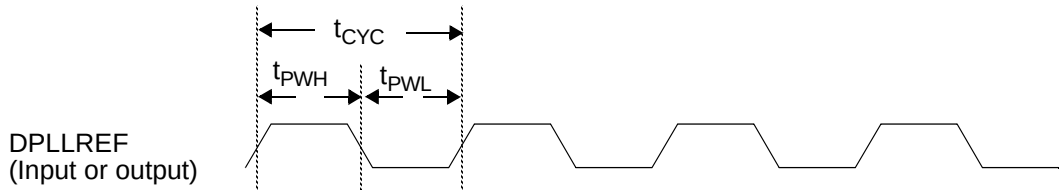


Parameter	Symbol	Min	Typ	Max	Unit
SREGT clock period (see Notes 2,4)	t_{CYC}		1.0		s
SREGT (Input) pulse width high	t_{PWH}	435			ns
SREGT (Input) pulse width low (see Note 3)	t_{PWL}			1020	ms
SREGT (Output) pulse width high	t_{PWH}		488.3		ns
SREGT (Output) pulse width low (see Note 4)	t_{PWL}		1000		ms

Notes:

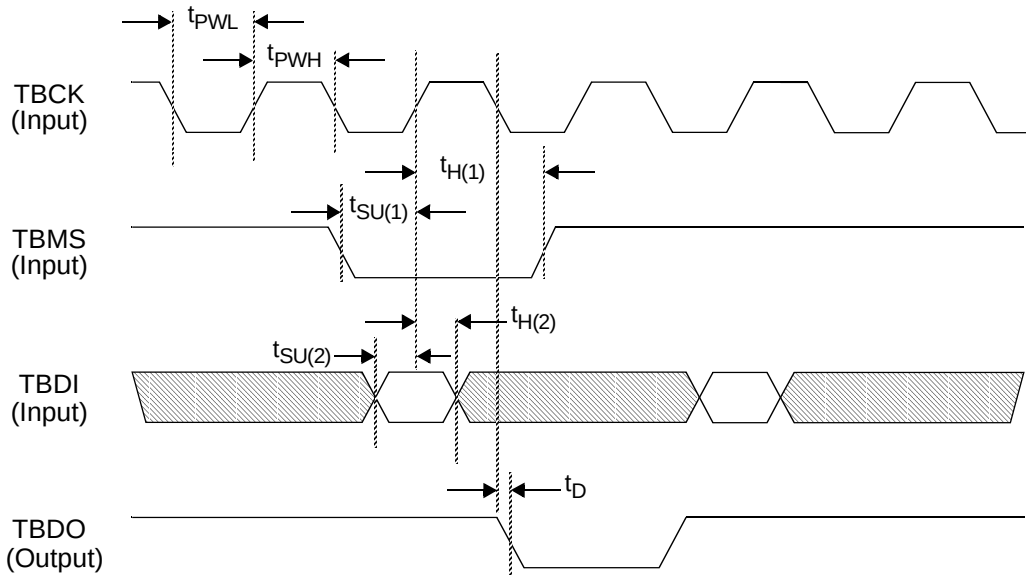
1. The shadow register feature and this input are enabled when a 1 is written to control bit SRGEN (bit 3 in register 00BH). This signal is selected when control bit S1SEXTB (bit 4 in register 024H) is set to a 0.
2. To meet ITU-T G.823 requirements this clock must be 1.0 Hz ± 50 ppm when used for performance monitoring.
3. SREGT pulse width low can exceed this maximum value with a risk of overflow on the E-bit, CRC-4 and Sa6 code counters.
4. The actual cycle for SREGT as an output is a function of the accuracy of the selected clock source.

Figure 27. DPLL Reference Input/Output Timing



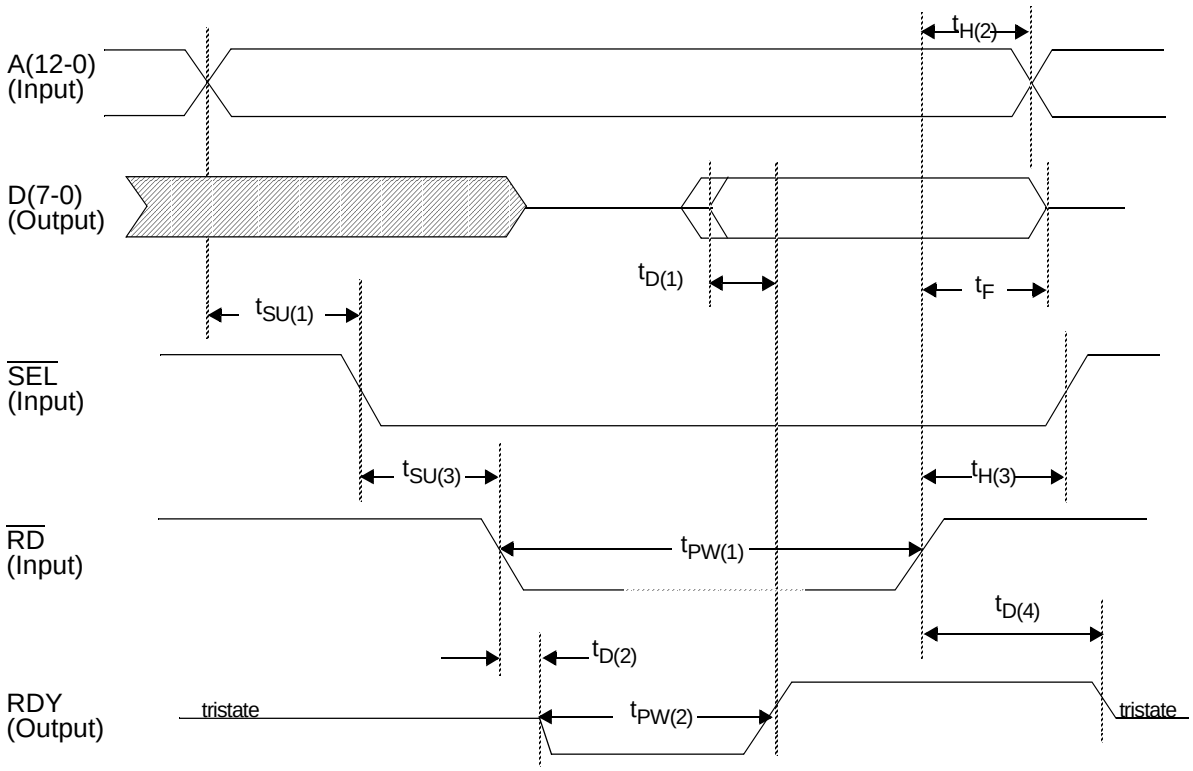
Parameter	Symbol	Min	Typ	Max	Unit
DPLLREF clock period	t_{CYC}		15.5		ns
DPLLREF (Input) pulse width high	t_{PWH}	6.2			ns
DPLLREF (Input) pulse width low	t_{PWL}	6.2			ns
DPLLREF (Output) pulse width high	t_{PWH}	7.0			ns
DPLLREF (Output) pulse width low	t_{PWL}	7.0			ns

Figure 28. Boundary Scan Timing



Parameter	Symbol	Min	Max	Unit
TBCK clock high time	t_{PWH}	50		ns
TBCK clock low time	t_{PWL}	50		ns
TBMS setup time to TBCK↑	$t_{SU(1)}$	3.0	-	ns
TBMS hold time after TBCK↑	$t_{H(1)}$	2.0	-	ns
TBDI setup time to TBCK↑	$t_{SU(2)}$	5.0	-	ns
TBDI hold time after TBCK↑	$t_{H(2)}$	7.0	-	ns
TBDO delay from TBCK↓	t_D	3.0	15	ns

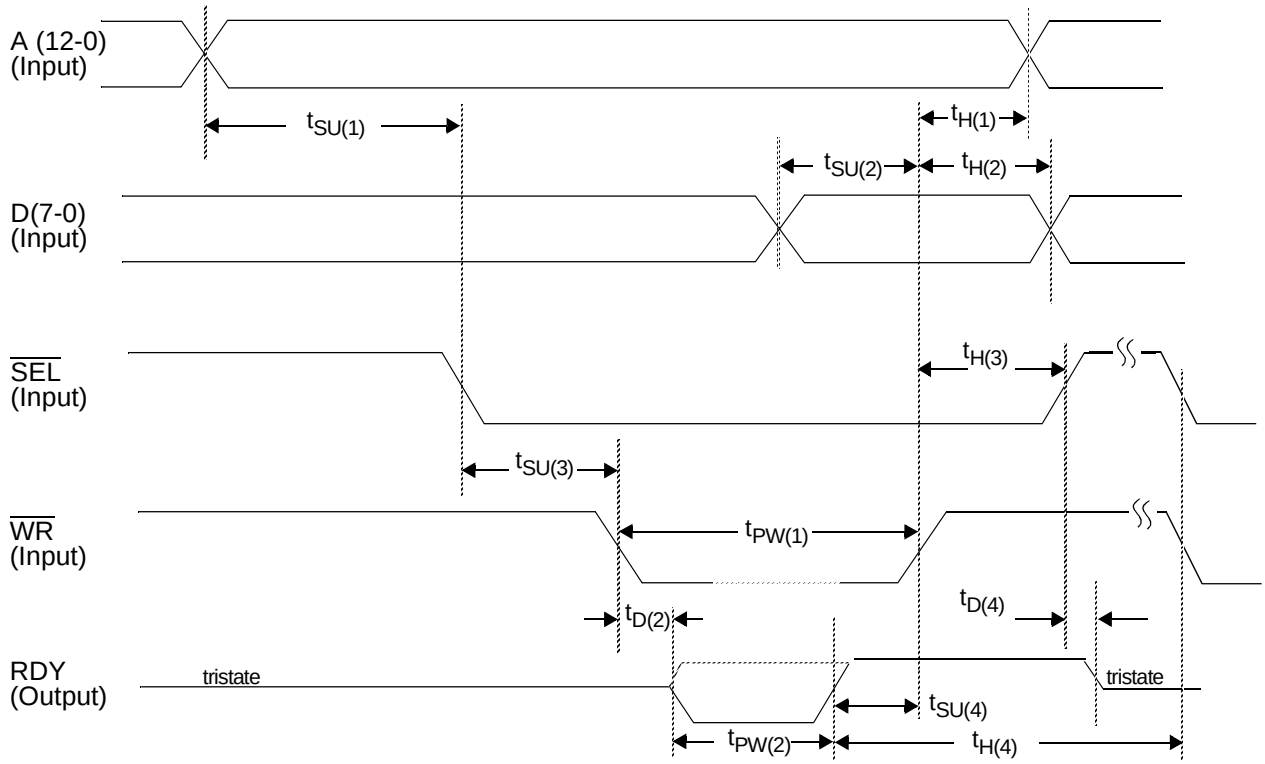
Figure 29. Intel Microprocessor Read Cycle Timing



Parameter	Symbol	Min	Typ	Max	Unit
A(12-0) valid setup time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	5.0			ns
D(7-0) valid delay before RDY$\uparrow$	$t_{D(1)}$	10			ns
D(7-0) float time after $\overline{RD}\uparrow$	t_F	2.0		15	ns
$\overline{SEL}$ setup time to $\overline{RD}\downarrow$	$t_{SU(3)}$	5.0			ns
$\overline{SEL}$ hold time after $\overline{RD}\uparrow$	$t_{H(3)}$	7			ns
$\overline{RD}$ pulse width low time	$t_{PW(1)}$	50			ns
RDY$\downarrow$ delay after $\overline{RD}\downarrow$	$t_{D(2)}$	3.0		17	ns
RDY pulse width low time (see Note 2)	$t_{PW(2)}$	1 cycle of SYSCI	2 cycles of SYSCI	10 cycles of SYSCI	ns
A(12-0) hold time after $\overline{RD}\uparrow$	$t_{H(2)}$	7			ns
RDY high to tristate delay after $\overline{RD}\uparrow$	$t_{D(4)}$	4.0		15	ns

Notes:
1. The Intel microprocessor bus is selected by placing a low on the MOTO lead.
2. The system clock (SYSCI) has a nominal frequency of 19-25 MHz.

Figure 30. Intel Microprocessor Write Cycle Timing

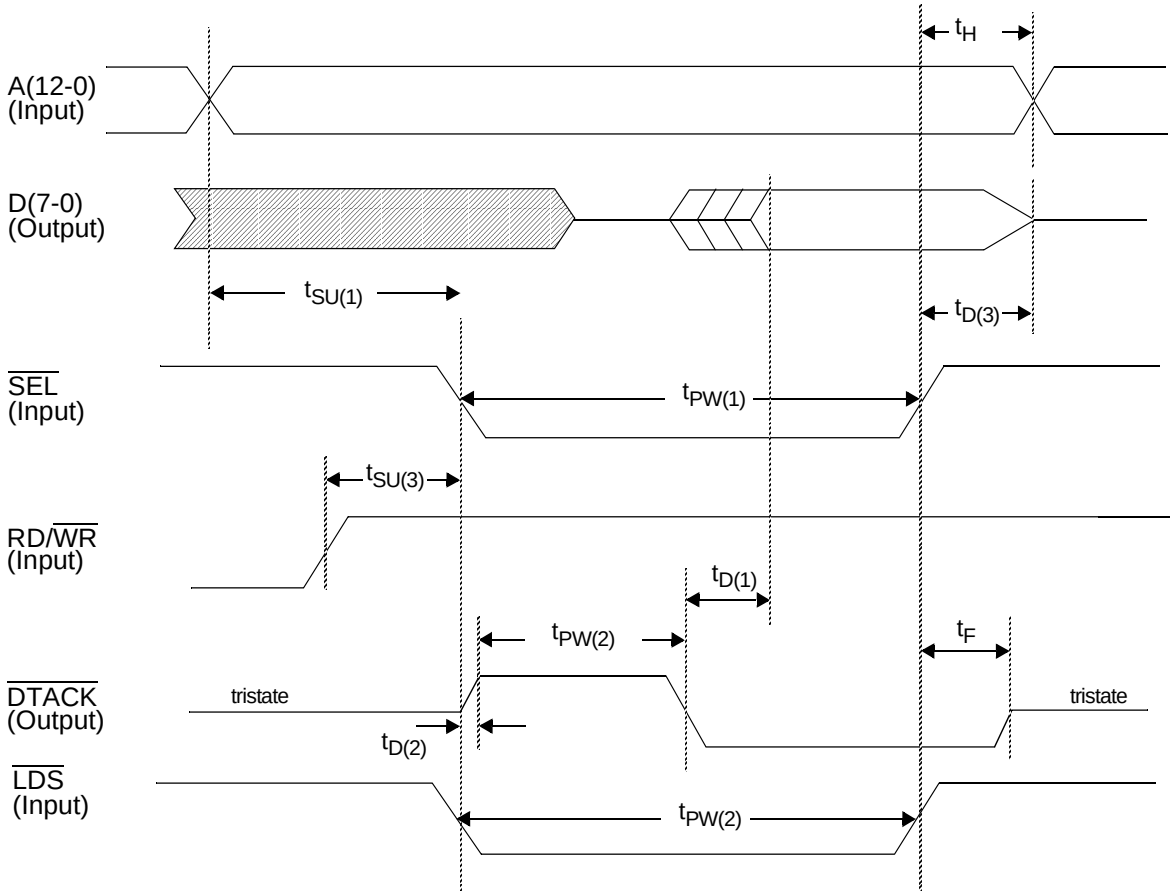


Parameter	Symbol	Min	Typ	Max	Unit
A(12-0) valid setup time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	5.0			ns
A(12-0) hold time after $\overline{WR}\uparrow$, $\overline{SEL}\uparrow$ (see Note 4)	$t_{H(1)}$	7.0			ns
D(7-0) valid setup time to $\overline{WR}\uparrow$, $\overline{SEL}\uparrow$ (see Note 4)	$t_{SU(2)}$	10			ns
D(7-0) hold time after $\overline{WR}\uparrow$, $\overline{SEL}\uparrow$ (see Note 4)	$t_{H(2)}$	7.0			ns
$\overline{SEL}$ setup time to $\overline{WR}\downarrow$	$t_{SU(3)}$	5.0			ns
$\overline{WR}$ pulse width low time/ $\overline{SEL}$ pulse width low time	$t_{PW(1)}$	50			ns
RDY delay after $\overline{WR}\downarrow$	$t_{D(2)}$	3.0		17	ns
RDY pulse width low time (see Notes 2, 3)	$t_{PW(2)}$	0 cycles of SYSCI	7 cycles of SYSCI	10 cycles of SYSCI	ns
RDY high to tristate delay after earliest of $\overline{WR}\uparrow$ or $\overline{SEL}\uparrow$	$t_{D(4)}$	17		35	ns
RDY high to $\overline{WR}\uparrow$, $\overline{SEL}\uparrow$ (see Note 4)	$t_{SU(4)}$	0.0			ns
$\overline{SEL}$ hold time after $\overline{WR}\uparrow$	$t_{H(3)}$	7.0			ns
RDY$\uparrow$ hold time after $\overline{WR}\downarrow$ or $\overline{SEL}\downarrow$ (see Note 5)	$t_{H(4)}$	2 cycles of SYSCI			ns

Notes:

1. The Intel microprocessor bus is selected by placing a low on the MOTO lead.
2. The system clock (SYSCI) has a nominal frequency of 19-25 MHz.
3. Wait states only occur if a write cycle immediately follows a previous read/write cycle (e.g., read modify write or word wide write).
4. The timing is with respect to the earliest of $\overline{WR}\uparrow$ or $\overline{SEL}\uparrow$.
5. When writing to address X+127H (FDL Transmit FIFO) only, allow a minimum of 2 cycles of SYSCI between RDY$\uparrow$ and $\overline{SEL}\downarrow$ or $\overline{WR}\downarrow$

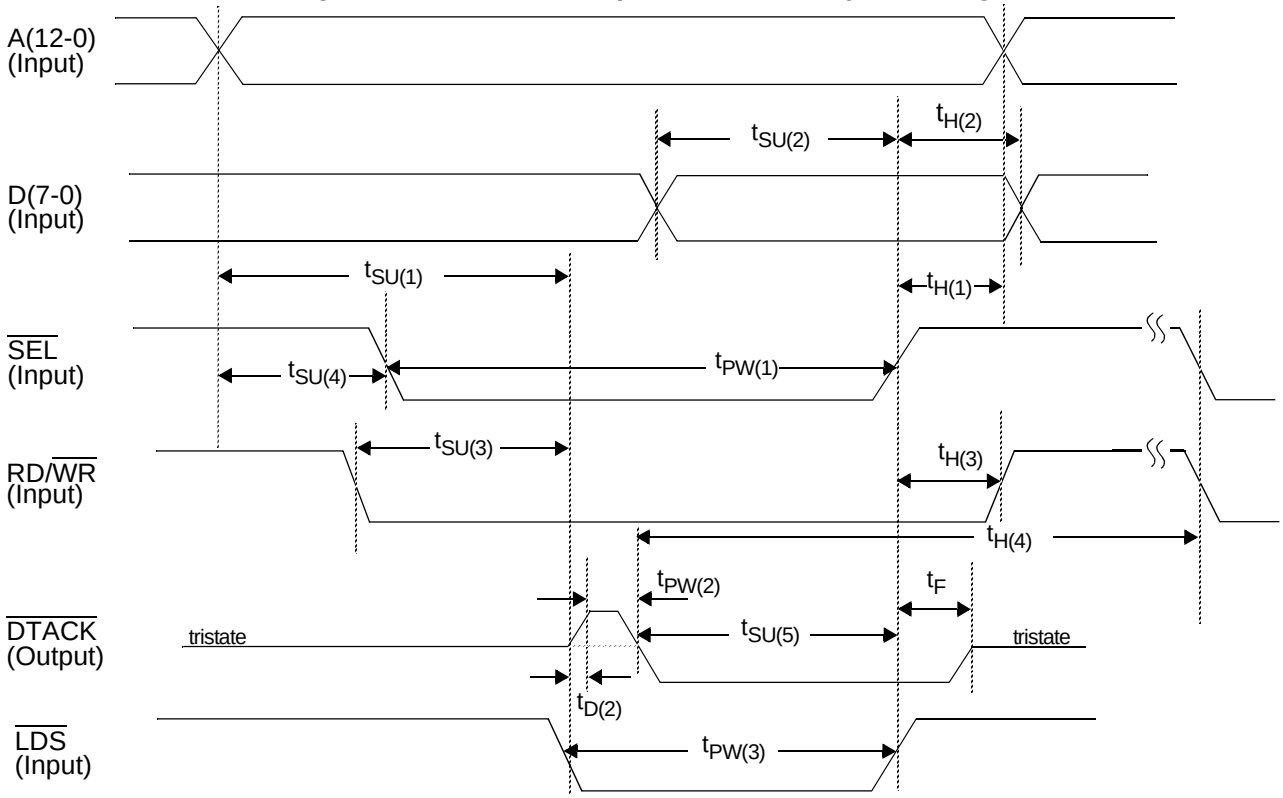
Figure 31. Motorola Microprocessor Read Cycle Timing



Parameter	Symbol	Min	Typ	Max	Unit
A(12-0) valid setup time to $\overline{SEL}/\overline{LDS}\downarrow$ (see Note 3)	$t_{SU(1)}$	10			ns
A(12-0) hold time to $\overline{SEL}/\overline{LDS}\uparrow$ (see Note 3)	t_H	7.0			ns
D(7-0) delay to tristate after $\overline{SEL}/\overline{LDS}\uparrow$ (see Note 3)	$t_{D(3)}$	3.0		15	ns
D(7-0) valid output delay after $\overline{DTACK}\downarrow$ (see Note 2)	$t_{D(1)}$	-1 cycle of SYSCI		-1/4 cycle of SYSCI	ns
$\overline{SEL}$ or $\overline{LDS}$ pulse width low time	$t_{PW(1)}$, $t_{PW(2)}$	50			ns
RD/$\overline{WR}$ setup time to $\overline{SEL}/\overline{LDS}\downarrow$ (see Note 3)	$t_{SU(3)}$	10			ns
$\overline{DTACK}$ pulse width high time (see Note 2)	$t_{PW(2)}$	2 cycles of SYSCI		10 cycles of SYSCI	ns
$\overline{DTACK}$ float time after $\overline{SEL}/\overline{LDS}\uparrow$ (see Note 3)	t_F	4.0		12	ns
$\overline{DTACK}$ delay after $\overline{SEL}/\overline{LDS}\downarrow$ (see Note 3)	$t_{D(2)}$	4.0		15	ns

Notes:
1. The Motorola microprocessor bus is selected by placing a high on the MOTO lead.
2. The system clock (SYSCI) has a nominal frequency of 19-25 MHz.
3. Setup time $t_{SU(1)}$ / $t_{SU(3)}$/$t_{D(2)}$ min. is the latter of $\overline{LDS}$ or $\overline{SEL}$ $\downarrow$; delay to tristate $t_{D(3)}$/t_F is the earlier of $\overline{LDS}$ or $\overline{SEL}$ $\uparrow$.

Figure 32. Motorola Microprocessor Write Cycle Timing

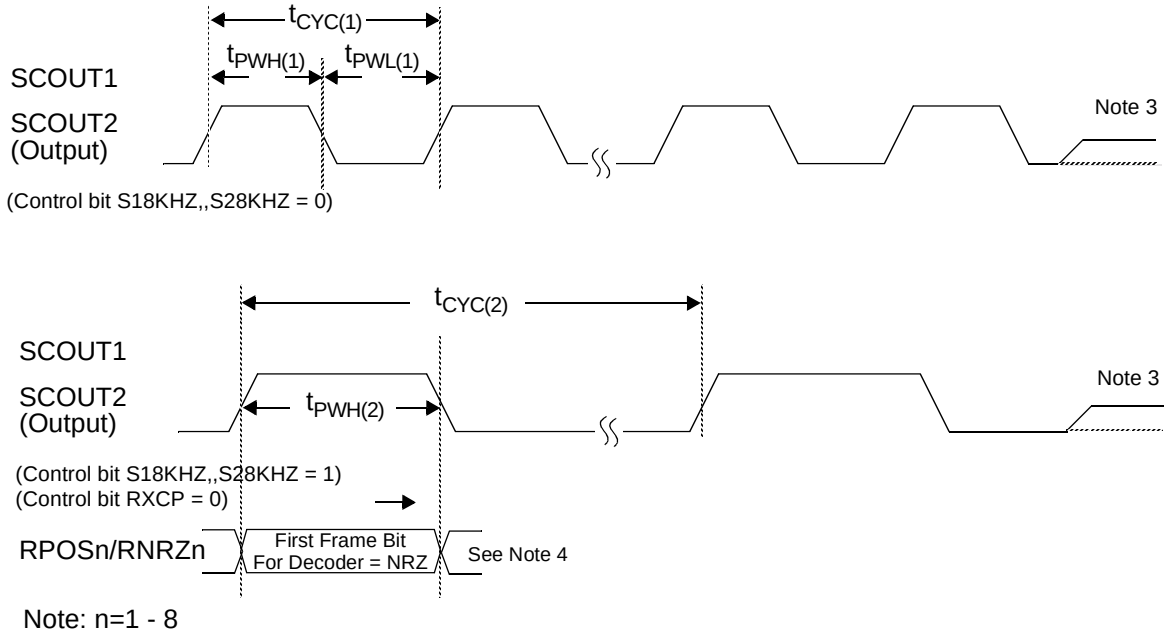


Parameter	Symbol	Min	Typ	Max	Unit
A(12-0) valid setup time to $\overline{LDS}\downarrow$, $\overline{SEL}\downarrow$ (see Note 4)	$t_{SU(1)}$/ $t_{SU(4)}$	10			ns
A(12-0) hold time after $\overline{LDS}\uparrow$, $\overline{SEL}\uparrow$ (see Note 5)	$t_{H(1)}$	7.0			ns
D(7-0) valid setup time to $\overline{LDS}\uparrow$, $\overline{SEL}\uparrow$ (see Note 5)	$t_{SU(2)}$	10			ns
$\overline{SEL}$ pulse width low time	$t_{PW(1)}$	50			ns
D(7-0) hold time after $\overline{LDS}\uparrow$, $\overline{SEL}\uparrow$ (see Note 5)	$t_{H(2)}$	7.0			ns
RD/$\overline{WR}$ setup time to $\overline{LDS}\downarrow$, $\overline{SEL}\downarrow$ (see Note 4)	$t_{SU(3)}$	10			ns
$\overline{DTACK}$ pulse width high time (see Notes 2, 3)	$t_{PW(2)}$	0 cycles of SYSCI		10 cycles of SYSCI	ns
$\overline{DTACK}$ float time after $\overline{LDS}\uparrow$, $\overline{SEL}\uparrow$ (see Note 5)	t_F	3.0		15	ns
$\overline{DTACK}\uparrow$ delay after $\overline{LDS}\downarrow$, $\overline{SEL}\downarrow$ (see Note 4)	$t_{D(2)}$	4.0		17	ns
RD/$\overline{WR}$ hold time to $\overline{LDS}\uparrow$, $\overline{SEL}\uparrow$ (see Note 4)	$t_{H(3)}$	10			ns
$\overline{LDS}$ pulse width low time	$t_{PW(3)}$	50			ns
$\overline{DTACK}$ low to $\overline{LDS}\uparrow$, $\overline{SEL}\uparrow$ (see Note 5)	$t_{SU(5)}$	0.0			ns
$\overline{DTACK}\downarrow$ to $\overline{SEL}\downarrow$ or RD/$\overline{WR}\downarrow$ (see Note 6)	$t_{H(4)}$	2 cycles of SYSCI			ns

Notes:

1. The Motorola microprocessor bus is selected by placing a high on the MOTO lead.
2. The system clock (SYSCI) has a nominal frequency of 19-25 MHz.
3. Wait states only occur if a write cycle immediately follows a previous read/write cycle (e.g., read modify write or word wide write).
4. Measured with respect to the latter of $\overline{\text{LDS}}$ or $\overline{\text{SEL}}$ falling edge.
5. Measured with respect to the earlier of $\overline{\text{SEL}}$ or $\overline{\text{LDS}}$ rising edge.
6. When writing to address X+127H (FDL Transmit FIFO) only, allow a minimum of 2 cycles of SYSCI between $\overline{\text{DTACK}}\downarrow$ and $\overline{\text{SEL}}\downarrow$ or RD/$\overline{\text{WR}}\downarrow$

Figure 33. Clock Reference Timing



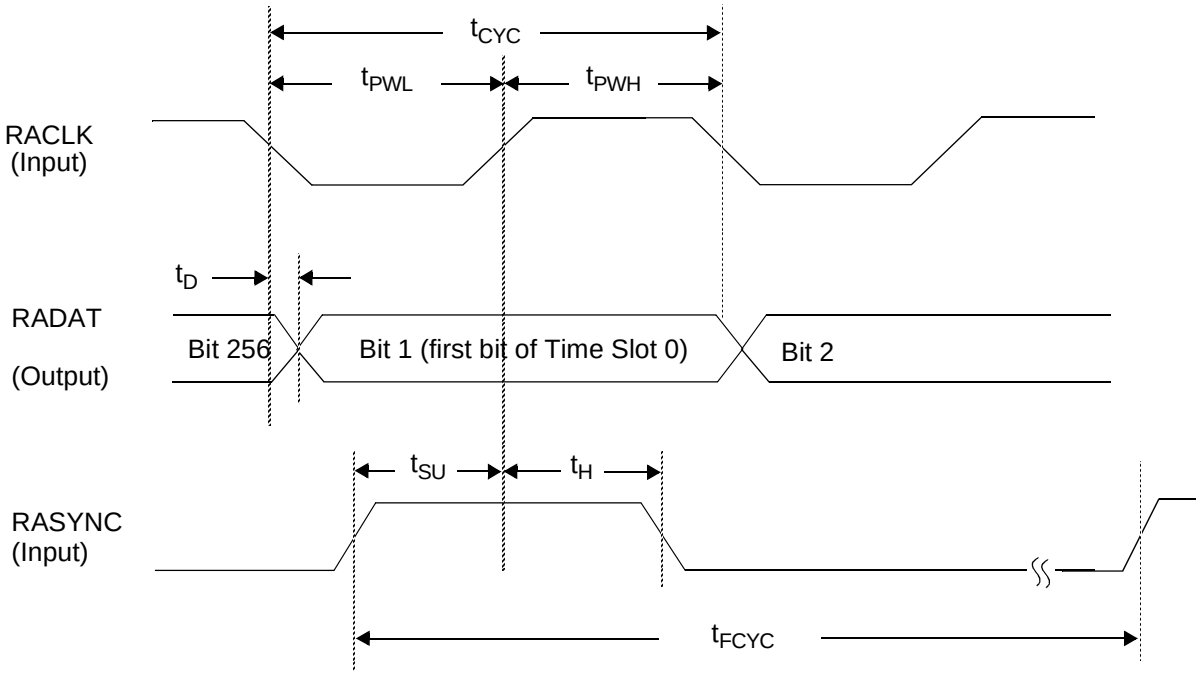
Note: n=1 - 8

Parameter (see note 2)	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
SCOUT1,2 clock period when control bit S18KHZ, S28KHZ = 0	$t_{CYC(1)}$	465	488.3		ns
SCOUT1,2 high time when control bit S18KHZ, S28KHZ = 0	$t_{PWH(1)}$		0.5 x $t_{CYC(1)}$		ns
SCOUT1,2 low time when control bit S18KHZ, S28KHZ = 0	$t_{PWL(1)}$		0.5 x $t_{CYC(1)}$		ns
SCOUT1,2 clock period when control bit S18KHZ, S28KHZ = 1	$t_{CYC(2)}$		256 x $t_{CYC(1)}$		ns
SCOUT1,2 high time when control bit S18KHZ, S28KHZ = 1	$t_{PWH(2)}$	465	488.3		ns

Notes

1. SCOUT1 and SCOUT2 output leads are controlled by registers 024H and 025H respectively. Control bit S18KHZ (bit 7 in register 024H) selects either a direct clock output for SCOUT1 when set to 0 or via a divide by 256 circuit when set to 1. Control bit S28KHZ (bit 7 in register 025H) selects either a direct clock output for SCOUT2 when set to 0 or via a divide by 256 circuit when set to 1. Control bits S1CTRI (bit 6 in register 024H) and S2CTRI (bit 6 in register 025H) enables output leads SCOUT1 and SCOUT2 when set to 0; when S1CTRI and S2CTRI are set to 1 SCOUT1 and SCOUT2 are tristated. The particular receive clock RCLKn used as a reference is selected by control bits S1YNC2 - S1YNC0 (bits 2-0 in register 024H) for SCOUT1 and control bits S2YNC2 - S2YNC0 (bits 2-0 in register 025H) for SCOUT2.
2. The actual clock period and high or low times are a function of the selected clock RCLKn.
3. A fault detected (LOS or RSCANn lead active if enabled by control bit EXLOS (bit 3 in register X+00H) set to a 1) by the particular channel selected for the reference clock will cause SCOUT1 to stay low if control bit S1YNCEN (bit 5 in register 024H) is set to 1. A fault detected (LOS or RSCANn lead active if enabled by control bit EXLOS set to a 1) by the particular channel selected for the reference clock will cause SCOUT2 to stay low if control bit S2YNCEN (bit 5 in register 025H) is set to 1. The output only goes to tristate only if control bit S1CTRI or S2CTRI is set to 1.
4. For a NRZ setting of the Line Decoder by control bit RAIL (bit 7 in register X+00H) set to 0 and control bit RXCP (bit 5 in register X+00H) set to 0 the 8 kHz pulse on SCOUT1 and SCOUT2 is coincident with the first bit of a frame if control bit SYNLF (bit 6 in register 00CH) is set to a 1; for RXCP set to 1 the pulse is coincident with the center of the last bit of a frame. For AMI or HDB3 mode (RAIL set to 1) the pulse is coincident with the fourth bit of a frame for RXCP set to 0; for RXCP set to 1 the pulse is coincident with the center of the third bit of a frame. This feature works in framed modes only.
5. The above measurements are with the dejitter buffers disabled. A delay of 29.5 clock cycles is added with the dejitter buffers enabled.

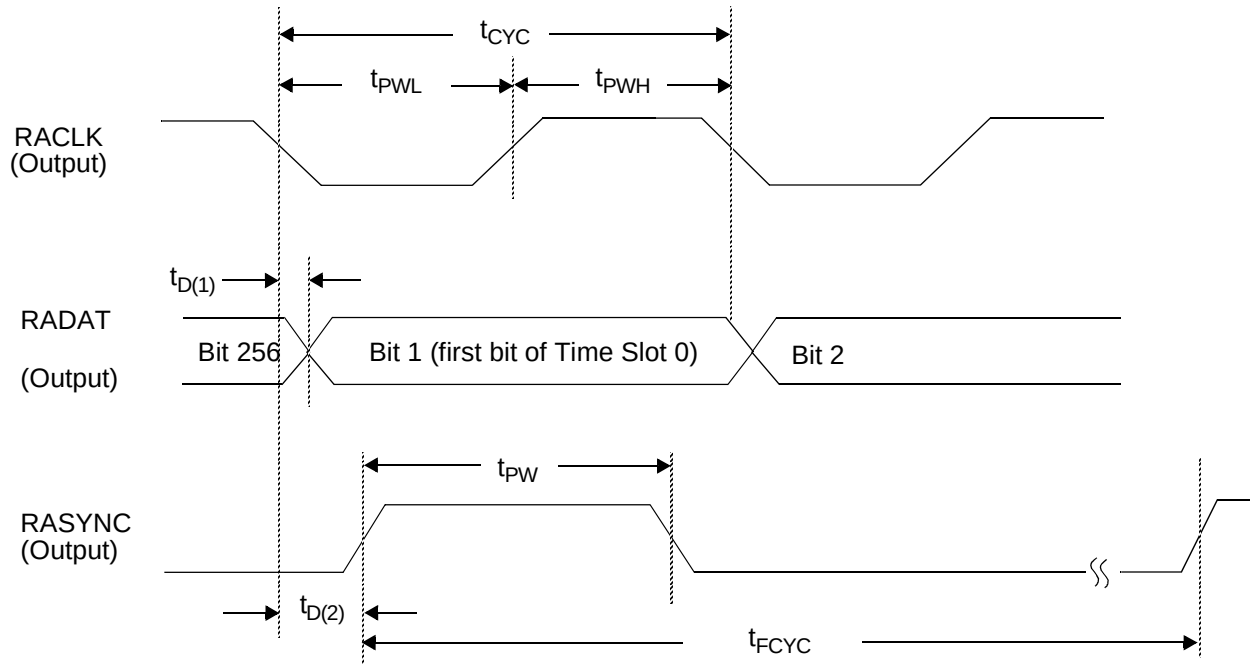
Figure 34. Auxiliary Port Receive Timing (Clock Slave)



Parameter	Symbol	Min	Typ	Max	Unit
RACLK clock period	t_{CYC}	465	488.3		ns
RACLK low time	t_{PWL}	233	0.5 x t_{CYC}		ns
RACLK high time	t_{PWH}	233	0.5 x t_{CYC}		ns
RADAT delay after RACLK↓	t_D	5.0	15	28	ns
RASYNC setup time to RACLK↑	t_{SU}	10			ns
RASYNC hold time after RACLK↑	t_H	15			ns
RASYNC period	t_{FCYC}	465	256 x t_{CYC}		ns

Note: When control bit RADIRSEL (bit 0) in register 037H is set to a 0, RACLK and RASYNC are inputs.

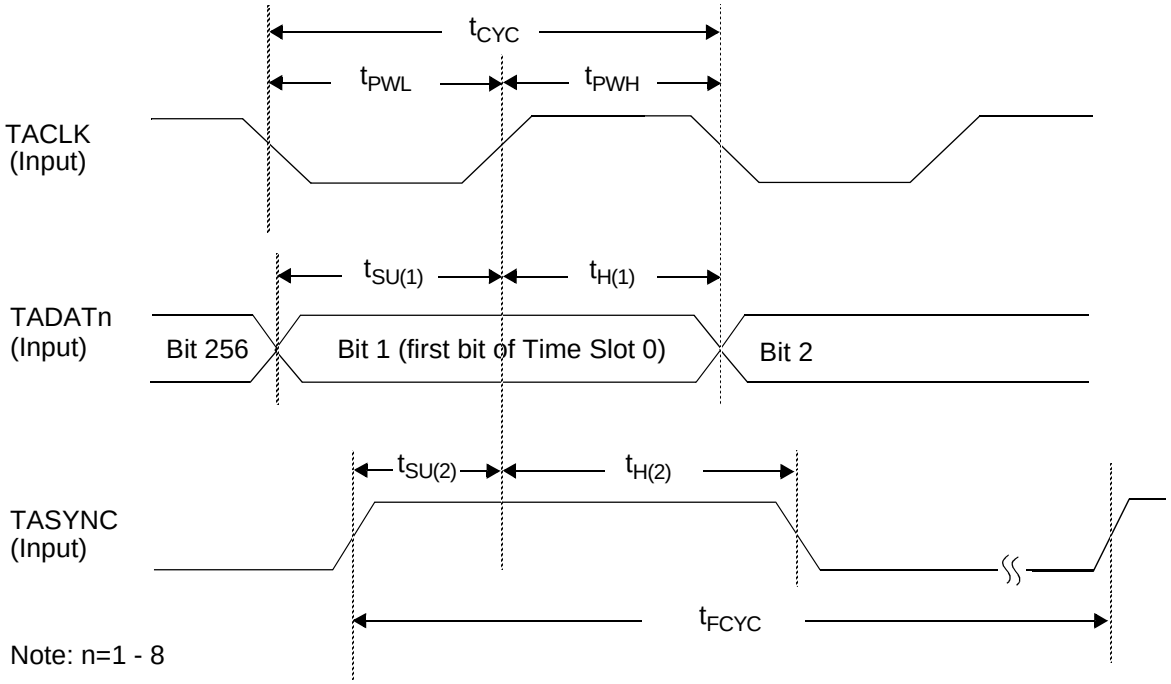
Figure 35. Auxiliary Port Receive Timing (Clock Master)



Parameter	Symbol	Min	Typ	Max	Unit
RACLK clock period	t_{CYC}	435	488.3		ns
RACLK low time	t_{PWL}	180	0.5 x t_{CYC}		ns
RACLK high time	t_{PWH}	180	0.5 x t_{CYC}		ns
RADAT delay after RACLK↓	$t_{D(1)}$	2.0	8.0	17	ns
RASYNC delay after RACLK↓	$t_{D(2)}$	1.0	10	14	ns
RASYNC pulse width	t_{PW}	435	488.3		ns
RASYNC period	t_{FCYC}		256 x t_{CYC}		ns

Note: When control bit RADIRSEL (bit 0) in register 037H is set to a 1, RACLK and RASYNC are outputs. Control bit RACKSEL (bit 1) in register 037H when set to 1 selects BPOSC as the source of RACLK and RASYNC. When RACKSEL is set to 0, control bits S1YNC2 - S1YNC0 (bits 2-0) in register 024H select the receive line clock RCLKn as the source of RACLK and RASYNC.

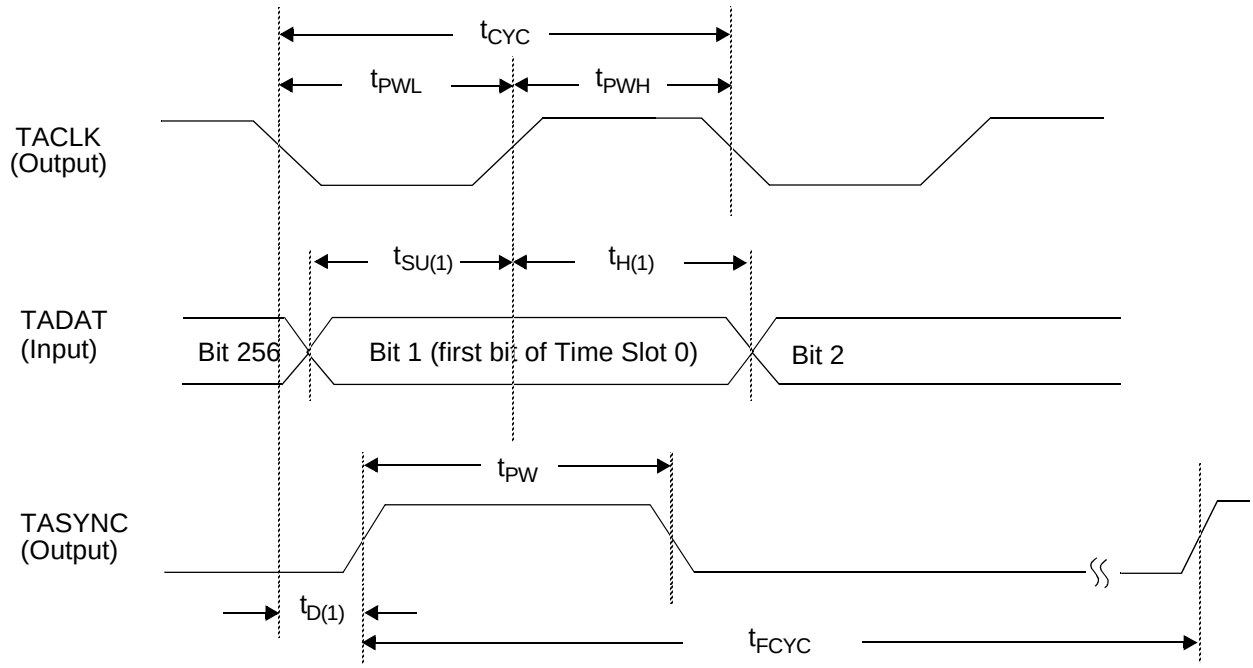
Figure 36. Auxiliary Port Transmit Timing (Clock Slave)



Parameter	Symbol	Min	Typ	Max	Unit
TACLK clock period	t_{CYC}	435	488.3		ns
TACLK low time	t_{PWL}	180	0.5 x t_{CYC}		ns
TACLK high time	t_{PWH}	180	0.5 x t_{CYC}		ns
TADATn setup time to TACLK↑	$t_{SU(1)}$	12			ns
TADATn hold time after TACLK↑	$t_{H(1)}$	12			ns
TASYNC setup time to TACLK↑	$t_{SU(2)}$	12			ns
TASYNC hold time after TACLK↑	$t_{H(2)}$	12			ns
TASYNC period	t_{FCYC}		256 x t_{CYC}		ns

Note: When control bit TADIRSEL (bit 2) in register 037H is set to a 0, TACLK and TASYNC are inputs.

Figure 37. Auxiliary Port Transmit Timing (Clock Master)



Parameter	Symbol	Min	Typ	Max	Unit
TACLK clock period	t_{CYC}	435	488.3		ns
TACLK low time	t_{PWL}	180	0.5 x t_{CYC}		ns
TACLK high time	t_{PWH}	180	0.5 x t_{CYC}		ns
TADAT setup time to TACLK↑	$t_{SU(1)}$	12			ns
TADAT hold time after TACLK↑	$t_{H(1)}$	12			ns
TASYNC delay after TACLK↓	$t_{D(1)}$	1.0	10	14	ns
TASYNC pulse width	t_{PW}	435	488.3		ns
TASYNC period	t_{FCYC}		256 x t_{CYC}		ns

Note: When control bit TADIRSEL (bit 2) in register 037H is set to a 1, TACLK and TASYNC are outputs. Control bit TACKSEL (bit 3) in register 037H when set to 1 selects BPOSC as the source of TACLK and TASYNC. When TACKSEL is set to 0, control bits S1YNC2 - S1YNC0 (bits 2-0) in register 024H select the receive line clock RCLKn as the source of TACLK and TASYNC.

OPERATION

The following sections detail the internal operation of the E1Fx8.

LINE INTERFACE SELECTION

Each of the eight framers in the E1Fx8 can be programmed to provide either a dual unipolar interface or a NRZ interface. The dual unipolar interface is selected when a 1 is written into control bit RAIL (bit 7) in the Framer Configuration register located at address X+00H in the memory map. The X stands for the framer selected, and will be equal to the value shown in the Per Channel Control and Status Indication Registers section (X= 0200H for framer 1, X=0400H for framer 2, etc.). The HDB3 line or AMI coder/decoder (codec) feature can be selected for the dual unipolar interface. The HDB3 codec is selected by writing a 1 to control bit BE (bit 6) in the Framer Configuration register X+00H. A 0 will select an AMI codec. The HDB3 stands for High Density Bipolar of order 3, which is described in ITU-T G.703 - 1993 Annex A.

The clock polarity of the input and output line clocks is selectable by writing the sense required to control bits TXCP (bit 3) in the Framer Configuration register X+05H and RXCP (bit 5) in the Framer Configuration register X+00H. When a framer is configured for the dual unipolar mode, the line signal is monitored for loss of signal (LOS). LOS is detected if no transitions are present on either RPOSn or RNEGn as defined by control bits LOSI7-LOSI0 in register 02AH, and ENLOSI in register 02BH. The binary value written to LOSI7-LOSI0 determines the number of consecutive missing pulses to detect LOS. When ENLOSI is set to 1, the binary value in LOSI7-LOSI0 is multiplied by 16. To comply with ITU-T G.775 set ENLOSI to a 0 and LOSI7-LOSI0 may be set in the range of 0AH to FFH (10 to 255 pulse periods). For ISDN applications ITU-T I.431 or ETS 300 233 compliance may be met by setting ENLOSI to a 1 and LOSI7-LOSI0 to 7FH (2048 pulse positions or 1.0 millisecond of no pulses). Recovery occurs when a ones density as determined by control bits OND5-OND0 in register 02BH is met; the binary value of pulses in the interval set by LOSI7-LOSI0 must equal or exceed the value written to OND5-OND0. A Loss of Signal alarm will be indicated in status bit LOS (bit 7) in register X+10H. An associated mask bit MLOS, a latched event bit LLOS, a performance value PLOS and a fault value FLOS are all bit 7 of registers X+14H, X+11H, X+12H and X+13H respectively. The connections between a E1Fx8 framer and external line interface transceivers are shown in Figure 38 below for dual unipolar mode.

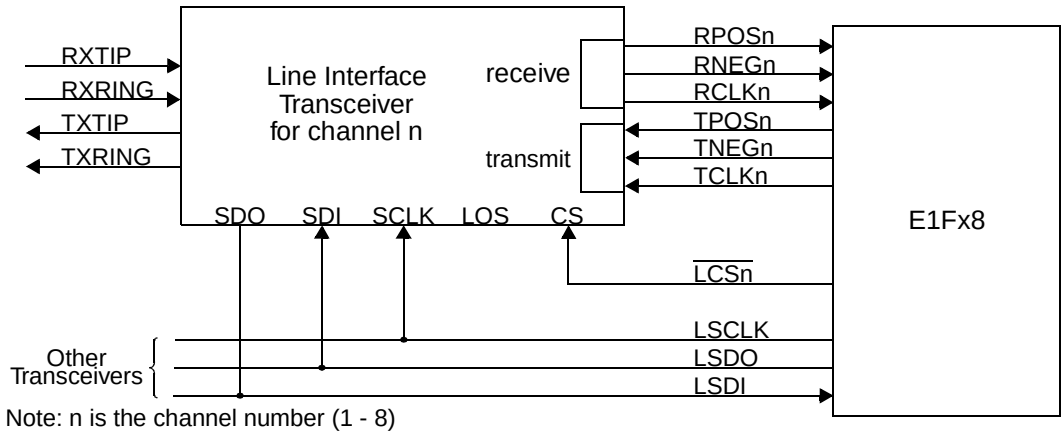


Figure 38. Line Interface For Dual Unipolar Mode

A coding violation counting function is provided in AMI and HDB3 modes. Control bit ENZC (bit 1) in register X+00H when set to a 1 counts a string of 4 zeros as a coding violation in HDB3 mode and 16 zeros as a coding violation in AMI mode. A 16 bit coding violation counter CV15- CV0 is located at X+F8H and X+F7H in the memory map with overflow bit CVO (bit 7) in register X+F9H. A shadow register of the counter and overflow bit LCV15-LCV0 and LCVO are located at X+F5H, X+F4H and X+F6H.

The NRZ interface is selected when a 0 is written into control bit RAIL (bit 7) in register X+00H. The clock polarity of the line input and output clocks is selectable by writing the sense required to control bits TXCP (bit 3) in the Framer Configuration register X+05H and RXCP (bit 5) in the Framer Configuration register X+00H. Options are provided for inverting the polarity of the transmit and receive data leads. A 1 written to control bit TXNRZ (bit 2) in register X+05H inverts the polarity of the transmit data signal, TNRZn, while a 1 written to control bit RXNRZ (bit 4) in register X+00H inverts the polarity of the receive data signal RNRZn. In NRZ mode, the RNEGn lead also designated RSCANn may be used to input an external indication of coding violations, loss of signal, or a fast sync pulse for testing purposes. The following table summarizes the line interface options (where X=don't care).

RAIL	BE	EXLOS	RXFS	E1 Receive Line Input Action
0	X	1	0	NRZ interface selected. RNEGn lead may be used to input an external LOS.
0	X	0	1	NRZ interface selected. RNEGn lead may be used to input a Nx2.0 ms sync pulse.
0	X	0	0	NRZ interface selected. RNEGn lead may be used to input a BPV count.
0	X	1	1	Not used.
1	0	X	X	RAIL interface selected. AMI line coding selected.
1	1	X	X	RAIL interface selected. HDB3 line coding selected.

External coding violations are counted in the same 16-bit performance counter used in Dual Unipolar mode when control bit EXLOS (bit 3) in register X+00H is a 0. Coding violations are counted when the input on RSCANn is high for active edges of the line clock RCLKn. When control bit RXFS (bit 1) in register X+1FF is a 1, the RSCANn lead is used for inputting a receive fast sync pulse. A single RCLKn clock period high pulse will force the framer to interpret the next bit on RNRZn as the first bit of a multiframe. Proper Time Slot 0 FAS and NFAS patterns are necessary to remain in sync. When control bit EXLOS is set to a 1, RSCANn may be used to input loss of signal or loss of clock from an external detector. The active level is set by control bit ELOSN (bit 2) in register X+00H. When control bit ELOSN is a 1, the input sense is active low (i.e. active low is a loss of signal indication). When the control bit is a 0, the alarm sense is active high. The following is a summary of the actions taken by the two control bits (where X=don't care).

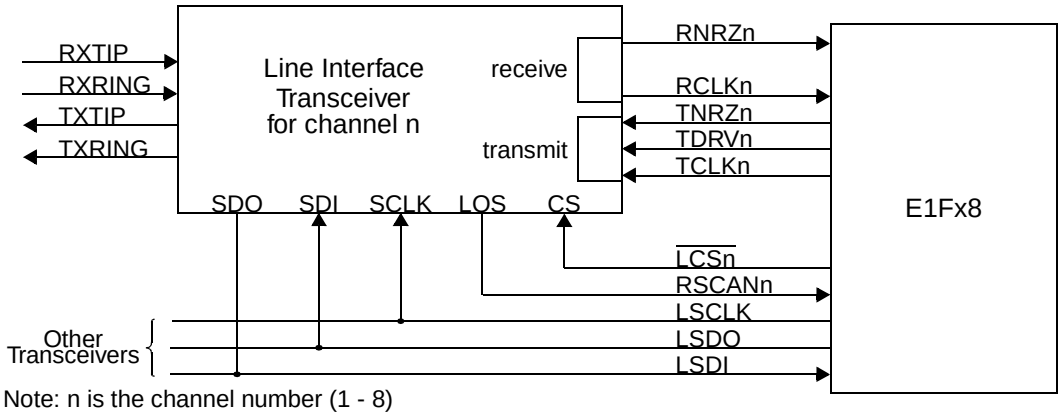
EXLOS	ELOSN	E1 Receive Line Input Action
0	X	NRZ interface selected. The RNEGn lead may be used to input an external bipolar coding violation. External LOS alarm indication is disabled.
1	0	NRZ interface selected. The RNEGn lead may be used to input an external loss of signal indication. The input state to indicate an external loss of signal is active high. Access to the counter via the external lead is disabled.
1	1	NRZ interface selected. The RNEGn lead may be used to input an external loss of signal indication. The input state to indicate an external loss of signal is active low. Access to the counter via the external lead is disabled.

In the Dual Unipolar Mode, a single coding violation can be transmitted to verify receiving equipment operation. Setting control bit BPVE (bit 5) in register X+106H to a 1 will cause a single coding violation to be generated. BPVE must be set to a 0 before another coding violation can be sent. In HDB3 mode a coding violation may mimic a zero substitution and not be recorded as an error by the receiving equipment; e.g. a '1001' which would normally be sent as a 'B00B' could be triggered to become a 'B00V' (validly decoded as 0000 not as a code violation) if control bit BPVE were set to a 1 in the middle of transmitting 'B00B'. 'B' is a normal bipolar pulse (alternate polarity to the previous pulse) and 'V' is a bipolar violation (same polarity as the previous pulse).

In the transmit direction, when the NRZ mode is selected, the TNEGn lead becomes a TDRVn lead. The lead may be used to output a fast sync pulse on a frame or superframe basis, or it may be used as a general purpose output lead. When control bit TDFME (bit 7) in register X+07H is a 1, a fast sync output pulse is provided on this lead. The control bit TLMF (bit 5) in the same register determines if the output pulse is every 125 microseconds or occurs at the superframe rate of every 1.5 or 3 milliseconds. When control bit TDFME is a 0, the TDRVn lead can be used as a general purpose output lead whose level is determined by control bit TXDRV (bit 6) in the same register. The following table summarizes the transmit options (where X=don't care).

RAIL	TDFME	TLMF	Action
1	X	X	Rail Interface, B8ZS or AMI line coding
0	0	X	NRZ interface. Control bit TXDRV determines the state of the TDRVn lead.
0	1	0	NRZ interface. The TDRVn lead provides a one clock cycle wide framing pulse that occurs at a 125 µs rate except in transparent mode (control bit TTFM is a 1).
0	1	1	NRZ interface. The TDRVn lead provides a one clock cycle wide framing pulse that occurs at a 2.0 ms rate except in transparent mode (control bit TTFM is a 1).

A typical interface between a framer in the E1Fx8 and an external line transceiver is shown in Figure 39 below for the NRZ mode.



Note: n is the channel number (1 - 8)

Figure 39. Line Interface For NRZ Mode

RECEIVE DEJITTER BUFFER

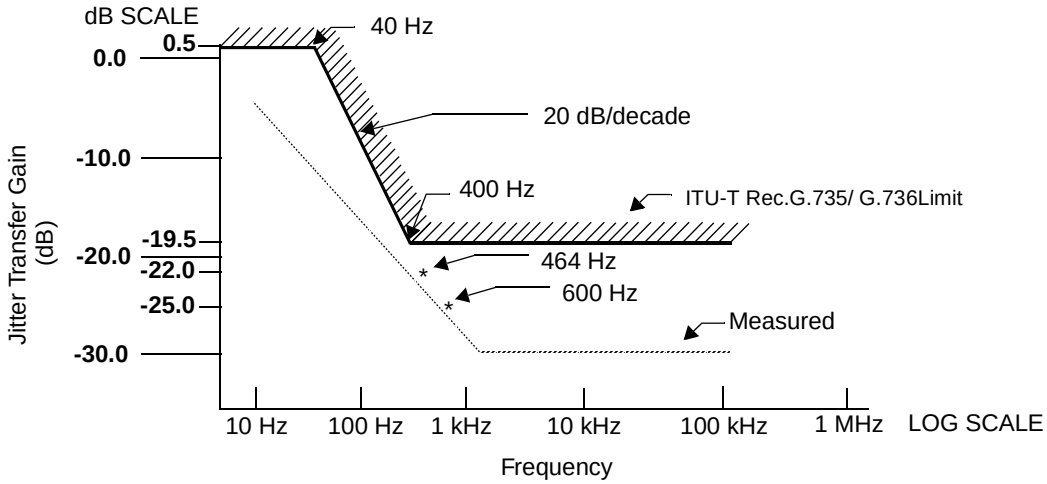
A 64-bit dejitter buffer is provided to remove line, de-mapping or de-multiplexing jitter when an external dejitter buffer is not provided by an LIU or other device and when receive slip buffer usage is not practical for a given application. Both RPOSn/RNRZn and RNEGn are dejittered using a digitally controlled oscillator and 64-bit FIFO. The transfer function is that of a single pole low pass filter with the pole at approximately 10 Hz; wander passes through but jitter is attenuated. A remote loopback (control bits RLP (bit 5) and LLP (bit 7) in register X+107H are set to 1 and 0 respectively) also goes through the dejitter buffer and clock reference selections are taken from the dejittered clock outputs when it is enabled. The on board DPLL runs at 64512 kHz to operate the dejitter buffers. The DPLL signal may be input on lead DPLLREF and the DPLL may be disabled if control bit DISECKSYN (bit 4) in register 0FEH is set to a 1. When DISECKSYN is set to a 0, lead DPLLREF is an output. Each dejitter buffer may be recentered or bypassed by per framer control bits RECENTER and BYPASS respectively (bits 1 and 0) in register X+161H. Setting RECENTER to a 1 will recenter the dejitter buffer once. Setting BYPASS to a 0 will cause the dejitter buffer to be bypassed. To completely shut down the dejitter buffer to conserve power, set BYPASS to a 0, DISECKSYN to a 1 and RESECKSYN to a 1 simultaneously. The BYPASS set to 0 disables the dejitter buffer and clock synthesis, DISECKSYN set to a 1 keeps the high frequency generator in power down and RESECKSYN set to a 1 keeps the counter in the high frequency block

reset. Each dejitter buffer can be made to recenter automatically on overflow or underflow or to pass the jitter through if the overflow or underflow limits are reached. Control bit ATTNLM (bit 2) in register X+161H when set to a 1 allows the dejitter buffer to automatically recenter; this will cause a loss or repetition of data. Since the dejitter buffer has much more head room than required by the standards, the input signal needs to be substantially out of specification to cause an underflow or overflow. When ATTNLM is set to a 0, no data is lost but the jitter present on the input is passed through until the dejitter buffer can recover.

The requirements for the dejitter buffer are listed below:

DEJITTER BUFFER SPECIFICATION	
Format:	Single or Dual Rail
Depth:	64 bits (x2 wide) total
Normal Location:	Between the RPOSn and RNEGn inputs and the codec.
Test Location:	When enabled, it is in the Remote Loopback path
Internal connections for clocks:	When enabled its output clock is used for SCOUT1,2 (S1EXTB, S1SINT = 11), Monitor output, RTCLKn (RXCKE = 1) and TCLKn (TXC1, TXC0 = 10)
Nominal frequency range:	2048 kHz ± 50 ppm
Nominal output jitter with jitter free reference:	<0.05 UIp-p 20 Hz to 100 kHz (G.735/G.736)
Maximum output jitter with jitter free reference:	0.10 UIp-p 20 Hz to 100 kHz (G.735/G.736)
Minimum jitter attenuation at 10 Hz:	0 dB to tolerance limit of G.823
Minimum jitter attenuation at 400 Hz:	=20 dB to tolerance limit of G.823 (G.735/G.736)
Minimum jitter tolerance (G.823 - 1993):	1.2×10^{-5} Hz to 4.88×10^{-3} Hz = 36.9 UIp-p 0.01 Hz to 1.667 Hz = 18 UIp-p 20 Hz to 2.4 kHz = 1.5 UIp-p 18 kHz to 100 kHz = 0.2 UIp-p Curves between ranges is 20 dB/decade roll off.
Overflow or Underflow operation:	When control bit ATTNLM is set to a 0 and the dejitter buffer reaches limit of storage, jitter is passed through rather than dropping data. When control bit ATTNLM is set to a 1 and the dejitter buffer reaches limit of storage, the dejitter buffer is recentered causing a loss or repetition of data.

The jitter transfer characteristics of the E1Fx8 with the dejitter buffer enabled are shown in Figure 40. The jitter transfer gain is well below the -19.5 dB for frequencies above 400 Hz (meets requirements of G.735 and G.736).



Test conditions: V_{DD} = 3.3 V, T_A = 25 °C

Frequency	Jitter Transfer Gain	Frequency	Jitter Transfer Gain
15.0 Hz	-4.7 dB	2.4 kHz	-30.0 dB
40.0 Hz	-11.4 dB	4.8 kHz	-30.0 dB
200.0 Hz	-21.3 dB	18.0 kHz	-30.0 dB
464.0 Hz	-22.0 dB	36.0 kHz	-30.0 dB
600.0 Hz	-25.0 dB	72.0 kHz	-30.0 dB
800.0 Hz	-27.2 dB	100.0 kHz	-30.0 dB

Note: Narrow isolated spikes occur at 464 Hz and 600 Hz, magnitude as shown, but well below the requirements of the ITU-T specifications.

Figure 40. E1Fx8 Jitter Transfer Characteristics

LINE INTERFACE CONTROL

This interface permits the microprocessor to have complete control of the eight external line interface transceivers through the E1Fx8. This interface is selected by setting global control bit ESPBMON (bit 5) in register 01DH to a 0 for the 208-lead package; this interface is always available in the 256-lead package. The line interface control leads are common to all eight framers and comprise a data input lead (LSDI), a data output lead (LSDO), and a clock output lead (LSCLK). The clock signal LSCLK is derived from the signal at the BPOSC lead; it is the same frequency as the signal applied to the BPOSC lead. Individual chip select leads ($\overline{\text{LCSn}}$) are used between the E1Fx8 and the external transceivers to determine which of the eight external transceivers is to be accessed through the E1Fx8. Typical interfaces between the E1Fx8 and external line interface transceivers using the line interface control leads are shown in Figure 38 and 39, for the dual unipolar and NRZ interface modes, respectively.

Data to be written to the external transceiver is formatted as a two-byte message. The first byte is an address/command byte and the second byte contains the data to be written or read. Figure 41 illustrates the message and control formats associated with the transceiver serial I/O timing.

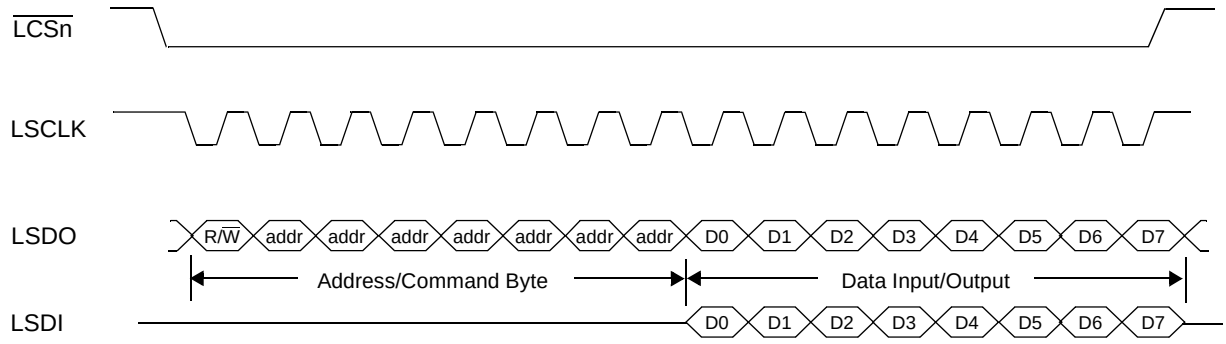


Figure 41. Transceiver Serial I/O Timing

The format of the address/command byte depends upon the external transceiver being controlled. Please refer to the transceiver's data sheet for the command/data formats. The interface for controlling the external transceiver operates in the following way. The external transceiver selection (via $\overline{\text{LCSn}}$) is determined by the value written to three bits E1CHS2, E1CHS1, and E1CHS0 (bits 2 - 0) in register 01DH. For example, a 000 value selects the transceiver for framer 1 while a 111 value selects the transceiver for framer 8. The microprocessor writes the command byte to LCB7-LCB0 in the Line Interface Control register 01EH. This is followed by writing the data byte to LDO7-LDO0 in Line Interface Control register 01FH. The serial message is sent on LSDO when a 1 is written to replace the 0 in the ESP bit (bit 6) in register 01DH. The ESP bit must be first written with a 0, followed by a 1, before another transfer can take place between the E1Fx8 and the external transceiver selected. Broadcast capability to all transceivers is enabled when the control bit BDCST (bit 7) in register 01DH is written with a 1.

For a read operation, the read command is sent on lead LSDO as described above. Eight clock cycles later, the selected transceiver will respond by sending serial data on the LSDI input lead. The data is shifted in LSB first to LDI7-LDI0 in the Serial Port Data Input Register 020H.

MONITOR MODE

The monitor mode interface permits the E1Fx8 to provide an external receive or transmit NRZ signal from one of the framers to an external device. This interface is selected by setting global control bit ESPBMON (bit 5) in register 01DH to a 1 for the 208-lead package; this interface is always available in the 256-lead package. Please note that the leads for this mode are shared with the line control interface in the 208-lead package, and if the monitor mode is selected, these leads cannot be used to provide a serial interface between the external transceivers and the E1Fx8. In addition, a 0 must be written into the MONTR control bit (bit 5) in the Global Configuration register 022H to enable the monitor mode interface output leads. A 1 written into MONTR control bit causes these data, frame, and clock leads to be tristated, permitting multiple E1Fx8 devices to share an external line driver.

A 1 written to control bit MONRX (bit 7) in register 022H selects the receive side, while a 0 selects the transmit side. For the receive side the data stream may be monitored before or after the receive framer selected by control bit MONRF (bit 6) in register 022H. The framer to be monitored is selected by the value written into the MFR2, MFR1 and MFR0 control bits (bits 2-0) in register 022H. For example, a value of 000 selects framer 1, and a value of 111 selects framer 8. The selected framer NRZ signal is provided on output lead MONDAT and the frame pulse is provided on output lead MONFRM. The NRZ receive or transmit data is clocked out on rising edges of the MONCLK clock lead signal. If LOS, AIS or OOF is detected while monitoring the receive side (i.e., while control bit MONRX is set to 1), the frame pulse will cease to be present on lead MONFRM. However, detection of LOS, AIS or OOF will not affect the frame pulse output on lead MONFRM while monitoring the transmit side (i.e., while MONRX is set to 0).

MONRX	MONRF	MONTR	Action
X	X	1	The monitor data lead (MONDAT), clock lead (MONCLK), and framing pulse lead (MONFRM) are tristated to allow other E1Fx8s to share a bus.
0	X	0	Transmit monitoring selected. Framer selected is determined by control bits MFR2-MFR0, where 000 is framer 1. The monitor data lead (MONDAT), clock lead (MONCLK), and framing pulse lead (MONFRM) are provided as outputs.
1	0	0	Receive monitoring selected. Data stream monitored before the input to the receive framer. The Framer whose input is selected is determined by control bits MFR2-MFR0, where 000 is framer 1. The monitor data lead (MONDAT), clock lead (MONCLK), and framing pulse lead (MONFRM) are provided as outputs.
1	1	0	Receive monitoring selected. Data stream monitored after the receive framer. The Framer whose output is selected is determined by control bits MFR2-MFR0, where 000 is framer 1. The monitor data lead (MONDAT), clock lead (MONCLK), and framing pulse lead (MONFRM) are provided as outputs.

Note: X=don’t care

SYSTEM INTERFACE

The system interface connects each of the eight framers within the E1Fx8 to and from the system. The system interface is selected by the CONF0 and CONF1 input leads and control bit DINTF (bit 1) in global register 00BH according to the table shown below (where X=don't care).

DINTF	CONF1	CONF0	Configuration Selected
0	Low	Low	Transmission Interface
1	Low	Low	Data Interface
X	Low	High	MVIP Interface
0	High	Low	H-MVIP
1	High	Low	H-MVIP with H.100 frame pulse width option
X	High	High	Not Used

For the Transmission and Data Modes each framer has separate transmit and receive interfaces that are referred to as receive and transmit highways. Each highway consists of a serial data bus (i.e., data highway) RTDATn/TTDATn, a serial signaling bus (i.e., signaling highway) RTSIGn/TTSIGn, a clock RTCLKn/TTCLKn, a separate gapped clock or marker output for transmit and receive RTAUXn/TTAUXn, a serial auxiliary transmit data input TTAIXn for fractional E1, and frame synchronization signal RTFRMn/TTFRMn. In the receive direction, clock and frame synchronization are outputs or inputs (slip buffer required if the receive clock and frame are inputs). For the MVIP Mode, each framer has separate transmit and receive interfaces that are referred to as receive and transmit highways. Each highway consists of a serial data bus (i.e., data highway) RTDATn/TTDATn, a serial signaling bus (i.e., signaling highway) RTSIGn/TTSIGn, a clock RTCLKn/TTCLKn, and a synchronization signal RTFRMn/TTFRMn. In the receive direction, clock and frame synchronization are inputs (slip buffer required). For the H-MVIP and H.100 Modes, four framers (i.e., 1-4 and 5-8) share transmit and receive interfaces that are referred to as receive and transmit highways. Each highway consists of a byte-interleaved serial data bus (i.e., data highway) RTDAT1,5/TTDAT1,5, a byte-interleaved serial signaling bus (i.e., signaling highway) RTSIG1,5/TTSIG1,5, a clock RTCLK1,5/TTCLK1,5, and a synchronization signal RTFRM1,5/TTFRM1,5. In the receive direction, clock and frame synchronization are inputs (slip buffer required). Internally, each data bus is connected to a two-frame slip buffer per framer, and each signaling bus is connected to a 120-bit signaling buffer per framer. Two additional active receive signaling buffers are also provided per framer for signaling debounce. Please note that control bits are provided which enable the slip buffers to be bypassed when the Transmission or Data Modes are selected. For the MVIP, H-MVIP and H.100 Modes, the receive and transmit slip buffers must be enabled by setting control bits RXSBE (bit 5) in register X+11BH to a 1, and TXSBE (bit 5) in register X+11CH to a 1.

The System Interface has a wide variety of options, not all of which are available in all interface Modes. The table below lists the options available in each Mode. Unless restricted by a lead signal, all features are available in all Modes In the 208-lead package RTAUXn and RTSIGn share a lead as do TTAUXn and TTSIGn. Control bit FE1M (bit 4) in register X+07H when set to a 1 selects RTAUXn and TTAUXn; when set to a 0 RTSIGn and TTSIGn is selected.

Function	Transmission Mode	Data Mode	MVIP Mode	H-MVIP/H.100
No. of Time Slots on R/TTDATn	32	32	32	128 (R/TTDAT1,5)
RTCLKn	2.048 MHz in & out	2.048 MHz in & out	2.048 MHz in only	16.384 MHz in only
TTCLKn	2.048 MHz in only	2.048 MHz in only	2.048 MHz in only	16.384 MHz in only
RTFRMn	2.0 ms in & out	125 µs in & out	125 µs in	125 µs in

Function	Transmission Mode	Data Mode	MVIP Mode	H-MVIP/H.100
TTFRMn	2.0 ms in	125 µs in	125 µs in	125 µs in
R/TTSIGn	8 bits/125 µs	120 bits/125 µs	120 bits/125 µs	480 bits/125 µs
R/TAUXn	64 kbit/s gapped clock or marker	64 kbit/s gapped clock or marker	Not Available; forced to zero	Not Available; forced to zero
No. of Time Slots from TTAIXn	Up to 31	Up to 31	Not Available	Not Available
Alarms on R/TTSIGn	AIS & RAI in/out	Not Available	Not Available	Not Available
Time Slot 0 National and International Bits	In & out on R/TTSIGn & R/TTDATn	In & out on R/TTSIGn & R/TTDATn	In & out on R/TTSIGn & R/TTDATn	In & out on R/TTSIGn & R/TTDATn
Unframed mode	Yes; with or without slip buffering	Yes; with or without slip buffering	Not Available	Not Available

TRANSMISSION MODE

The Transmission Mode is enabled when a low is placed on both the CONF0 and CONF1 leads and control bit DINTF (bit 1) in register 00BH is set to 0.

Transmit Highway with Fractional E1 Support

When the Transmission Mode is selected, the transmit highway carries information from the system to the E1Fx8 for each framer. The highway is subdivided into two time division multiplexed buses, one for data (TTDATn), and the other one for signaling, alarms and selected bits that may be multiplexed into Time Slot 0 (TTSIGn). The n in the TTDATn and TTSIGn signals represents one of the eight framers. The two buses are synchronous with respect to the highway clock (TTCLKn), which has a clock rate of 2048 kHz. The data highway is a single bit-serial bus organized into 256-bit groups called frames, with the bits in each group numbered 1 through 256. Each frame consists of 32 time slots numbered from 0 to 31, as shown in Figure 42. Time Slot 0 carries the frame synchronization pattern, multiframe pattern for the CRC-4 multiframe option which uses the International bits, RAI bits and Sa4 through Sa8 National bits. Also note that 16 frames form a multiframe for the CRC-4 option, with the beginning of each multiframe identified by an active high synchronization pulse (TTFRMn), one (TTCLKn) clock cycle wide, which occurs every 2 ms, normally at the end of frame 16. Each multiframe carries two Sub-multiframes. Each sub-multiframe carries a CRC-4 calculated over the previous Sub-multiframe. Every second Sub-multiframe carries two far end error bits (E-bits) for the current and the previous sub-multiframes. The position of the TTFRMn pulse is programmable to any bit position within the data bus frame using control bits TFRM7-TFRM0 in register 02FH. The synchronization pulse is aligned to bit 8 in Time Slot 31 in frame 15 when a value of 00H is written into this register. Data from the data highway may be enabled on a per time slot basis for transmission to the E1 line. Control bits TDE1 through TDE31 in control registers X+E4H, X+E5H, X+E6H and X+E7H when set to a 1 enable the time slot data to the line for the selected time slots.

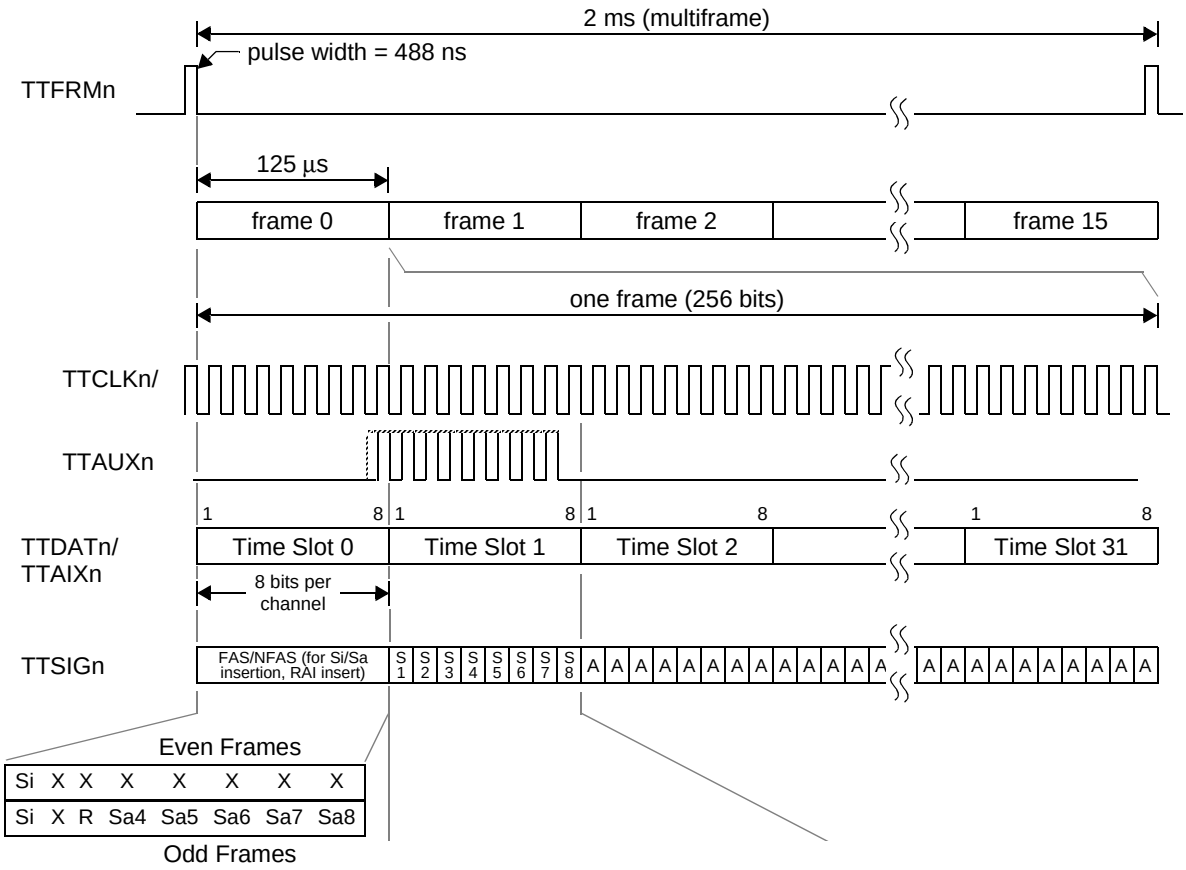
The signaling bus (TTSIGn) is also divided into 256-bit frames. Each signaling frame consists of 256-bits of signaling and alarm information for the 30 telephone channels, numbered from 1 to 30, that are carried on the data bus occupying time slots 1 through 15 and 17 through 31. The first time slot (Time Slot 0) in the signaling highway is assigned to carry the two International bits in bit 1 of alternate frames (bit Si), and the five National bits in bits 4 through 8 and the Remote Alarm Indication bit (A-bit) in bit 3 of alternate (NFAS) frames. The positions of the Time Slot 0 bits in this frame are the same as found in Time Slot 0 of the E1 frame format. It is not

required that the Time Slot 0 bits from the signaling highway carry the frame alignment pattern in FAS frames or have bit 2 in NFAS frames set to a 1. As an option, the International bits and the National bits may be sourced from TTSIGn; when control bit BNAL (bit 5) in register X+122H is set to a 1, control bits TSA4S through TSA8S (bits 4-0) in register X+E3H set to a 1 select the National bits to be sourced from Time Slot 0 of TTSIGn. Control bit TSIS (bit 7) in register X+E3H when set to a 1 selects the International bits to be sourced from Time Slot 0 of TTSIGn if control bits CRCMD1,0 equal 01 which corresponds to CRC-4 disabled.

Time Slot 1 in the signaling highway carries the Channel Associated Signaling (CAS) multiframe format. Like Time Slot 0 multiframe, this multiframe is repeated every 16 frames. The multiframe alignment pattern (0000), and the spare and multiframe alarm bits (X0, Y, X1, X2) occur in frame 0, followed by the ABCD signaling bits for telephone channels 1 through 30 (starting with telephone channels 1 and 16 in frame 1 and ending with telephone channels 15 and 30 in frame 15). The remaining bits are marked “A” in time slots 2 through 31 and carry an AIS indication, when set to 1, on the system side. Status bit TABIT (bit 5) in register X+17H indicates the state of these A-bits. If control bit EXTAIS (bit 5) in register X+06H is set to a 1 and the A-bits on TTSIGn are set to 1, an unframed all ones (AIS) will be transmitted by the E1Fx8. Likewise, if control bit EXTRAI (bit 4) in register X+06H is set to a 1 and the R-bit (bit 3) in Time Slot 0 of odd frames is set to a 1 indicating a system side RAI, the A-bit (bit 3) of the transmitted Time Slot 0 in NFAS frames will be set to a 1 indicating RAI. The status of the R-bit on the signaling highway is indicated in status bit TYBIT (bit 4) in register X+17H. It is not necessary to place a multiframe alignment pattern in Time Slot 1 frame 1. Time Slot 16 spare bits may be sourced from TTSIGn by setting control bits TX2S, TX1S and TX0S (bits 2-0) in register X+E2H to 1 for each spare bit selected. In Figure 42 below the S1 through S8 bits represent the ABCD signaling states associated with each pair of telephone channels. The E1Fx8 inserts the signaling bits from the signaling highway into the transmitted Time Slot 16 if enabled by control bits TSE1 through TSE30 in registers X+ECH, X+EDH, X+EEH and X+EFH.

Figure 40 shows the operation of the gapped clock or marker output TTAUXn as well as the auxiliary input TTAIXn. TTAUXn is shown with a gapped clock output for Time Slot 1. The 32 control bit pairs TC1Cc/TC0Cc in registers X+112H through X+118H determine the source of each transmitted time slot (c = 0 - 31); it can come from the TTDATn, TTAIXn, the Idle Code Insertion register (X+119H) or a Digital Milliwatt generator. Control bit TCHMK (bits 7) in register X+110H controls the TTAUXn signal. TCHMK set to 1 selects a channel marker (TTAUXn high for 8 clock periods of selected time slot). Control bit ULAW (bit 2) in register X+06H selects the coding law used to generate the digital milliwatt. The table below shows the options described (where X= don’t care). These features are generally available in all System Interface Modes unless the lead is not supported in that Mode. For example, if TC1Cc and TC0Cc are set to 01, fractional E1 functions are available, except that gapped clocks on TTAUXn or inputs from TTAIXn are not available in MVIP or H-MVIP/H.100 Modes.

TC1Cc	TC0Cc	TCHMK	ULAW	Action for the Selected Time Slot
0	0	X	X	Normal Operation. The Time Slot (c= 1 - 31) is transmitted intact from the data highway, TTDATn. The TTAIXn lead is disabled.
0	1	0	X	Fractional E1 Service. 64 kbit/s gapped Clock provided on the TTAUXn lead, and data from TTAIXn lead is multiplexed into transmit bit stream.
0	1	1	X	Fractional E1 Service. Channel marker provided on the TTAUXn lead, and data from TTAIXn lead is multiplexed into transmit bit stream.
1	0	X	X	Insert microprocessor-written Idle Code value from register X+119H. No gapped clock or channel marker generation on the TTAUXn lead. The TTAIXn lead is disabled.
1	1	X	0	A-law Digital Milliwatt generated for the Time Slot selected. No gapped clock or marker channel generation on TTAUXn lead. The TTAIXn lead is disabled.
1	1	X	1	mu-law Digital Milliwatt generated for the Time Slot selected. No gapped clock or marker channel generation on TTAUXn lead. The TTAIXn lead is disabled.



Frame	RTSIG; S1 - S8
0	0, 0, 0, 0, X0, Y, X1, X2,
1	A1, B1, C1, D1, A16, B16, C16, D16
2	A2, B2, C2, D2, A17, B17, C17, D17
3	A3, B3, C3, D3, A18, B18, C18, D18
4	A4, B4, C4, D4, A19, B19, C19, D19
5	A5, B5, C5, D5, A20, B20, C20, D20
6	A6, B6, C6, D6, A21, B21, C21, D21
7	A7, B7, C7, D7, A22, B22, C22, D22
8	A8, B8, C8, D8, A23, B23, C23, D23
9	A9, B9, C9, D9, A24, B24, C24, D24
10	A10, B10, C10, D10, A25, B25, C25, D25
11	A11, B11, C11, D11, A26, B26, C26, D26
12	A12, B12, C12, D12, A27, B27, C27, D27
13	A13, B13, C13, D13, A28, B28, C28, D28
14	A14, B14, C14, D14, A29, B29, C29, D29
15	A15, B15, C15, D15, A30, B30, C30, D30

Notes:
Si = International Bits
R = Remote Alarm Indication (RAI) bit, known as TS0 A-bit
San = National bits (n = 4-8)
Xb = Spare bits (b = 0-2)
Y = Multiframe Alarm
Ac Bc Cc Dc = ABCD signal bits for channel c (1-30)
A = Alarm Bits (AIS)
Gapped clock TTAUXn is shown for Time Slot 1 (the marker is a single 8 bit wide pulse) comes out one clock cycle earlier relative to TTDATn in the transmit direction.

Figure 42. Transmit Highway - Transmission Mode

Receive Highway with Fractional E1 Support

In the Transmission Mode, the receive highway for each framer carries information from the E1Fx8 to the system. Like the transmit path, the receive highway is also subdivided into two time division multiplexed buses, one for data (RTDATn), and one for signaling and alarms (RTSIGn), where n represents one of the eight framers. The two buses are synchronous with the highway clock (RTCLKn), which has a clock rate of 2048 kHz. The clock (RTCLKn) is either an output to the system or an input from the system. The system clock (RTCLKn) or the line clock (RCLKn) may be the input clock source for the slip buffer when it is enabled. Usually the system clock (RTCLKn) is used. The E1Fx8 must be set to source the clock (RTCLKn) as an output when the slip buffer is bypassed. The receive slip buffer for a framer is disabled when a 0 is written to the RXSBE bit (bit 5) in the register X+11BH. The clock source selection is determined by the RXCKE bit (bit 7) in register X+11BH. A 0 written into this bit position selects the system clock (RTCLKn) as the source clock. In addition to controlling the source of the clock, control bit RXCKE also controls the source of the synchronization pulse.

The data bus is a single bit-serial bus organized into 256-bit groups called frames, as shown in Figure 43, with the bits in each group numbered 1 through 256. Each frame consists of 32 time slots numbered from 0 to 31, as shown in Figure 43. Time Slot 0 carries the frame synchronization pattern, multiframe pattern for the CRC-4 multiframe option which uses the International bits, RAI bit and Sa4 through Sa8 National bits. Also note that 16 frames form a multiframe for the CRC-4 option, with the beginning of each multiframe identified by an active high synchronization pulse (RTFRMn), one (RTCLKn) clock cycle wide, which occurs every 2 ms, normally at the end of frame 16. Each multiframe carries two Sub- multiframes. Each Sub-multiframe carries a CRC-4 calculated over the previous Sub-multiframe. Every second Sub-multiframe carries two far end error bits (E-bits) for the current and the previous Sub-multiframes. The position of the RTFRMn pulse is programmable to any bit position within the data bus frame using control bits RFRM7-RFRM0 in register 02EH. The synchronization pulse is aligned to bit 8 in Time Slot 31 in frame 15 when a value of 00H is written into this register. Data from the E1 line may be enabled on a per time slot basis for insertion on the Data Highway. Control bits RDE1 through RDE31 in control registers X+3CH, X+3DH, X+3EH and X+3FH when set to a 1 enable the time slot data to RTDATn for the selected time slots.

The signaling bus (RTSIGn) is also divided into 256-bit frames. Each signaling frame consists of 256-bits of signaling and alarm information for the 30 telephone channels, numbered from 1 to 30, that are carried on the data bus occupying time slots 1 through 15 and 17 through 31. The first time slot (Time Slot 0) in the signaling highway is assigned to carry the two International bits in bit 1 of alternate frames (bit Si), and the five National bits in bits 4 through 8 and the Remote Alarm Indication bit (A-bit) in bit 3 of alternate (NFAS) frames. The positions of the Time Slot 0 bits in this frame are the same as found in Time Slot 0 of the E1 frame format. Time Slot 0 on RTSIGn is Time Slot 0 received from the E1 line but not subject to slip buffering.

Time Slot 1 in the signaling highway carries the Channel Associated Signaling (CAS) multiframe format. Like Time Slot 0 multiframe, this multiframe is repeated every 16 frames. Time Slot 16 multiframe alignment may or may not be aligned with Time Slot 0 multiframe on the E1 received signal. However, the internal signaling buffer provides alignment such that both multiframes are aligned on RTSIGn. The Time Slot 16 multiframe alignment pattern (0000), and the spare and multiframe alarm bits (X0, Y, X1, X2) occur in frame 0, followed by the ABCD signaling bits for telephone channels 1 through 30 (starting with telephone channels 1 and 16 in frame 1 and ending with telephone channels 15 and 30 in frame 15) as shown in Figure 43 below. The remaining bits are marked “A” in time slots 2 through 31 and carry an AIS indication to the system side. The “A” bits are set to 1 if the E1Fx8 if control bit ENABIT (bit 4) in register X+02H is set to a 1 and either AIS, OOF or LOS is detected and enabled by control bits ENAIS, ENOOF or ENLOS (bits 7-5) in register X+02H to set the “A” bits. The “A” bits may be forced to a 1 by setting control bit RTAIS (bit 2) in register X+02H to a 1 with control bit ENABIT set to a 1. AIS (all ones) on RTDATn may also be forced under the same line conditions (ENAIS, ENOOF and ENLOS plus the associated alarm or RTAIS is set to a 1) if control bit ENDBIT (bit 3) in register X+02H is set to a 1. Likewise, if control bit ENRAI (bit 1) in register X+02H is set to a 1 the “R” bit (bit 3) in Time Slot 0 of odd frames is set to a 1 if a line RAI, the A-bit (bit 3) of the received Time Slot 0 in NFAS, has been set to a 1 for four or more consecutive times indicating RAI. The “R” bit on the signaling highway may also be forced to a 1 by setting control bit RTRAI (bit 0) in register X+02H to a 1. In Figure 43 below the S1 through S8 bits represent the ABCD signaling states associated with each pair of telephone channels. The E1Fx8 inserts

the signaling bits into the signaling highway from the received E1 Time Slot 16 after processing as described below if enabled by control bits RSE1 through RSE30 in registers X+E8H, X+E9H, X+EAH and X+EBH. Control bits RX2S, RX1S and RX0S (bits 2-0) in register X+3AH when set to 1 enable the spare bits received on the E1 line Time Slot 16 to be placed on the signaling highway. Control bits RSIS (bit 7) and RSA4S- RSA8S in register X+3BH when set to 1 enable the International and National bits received on the E1 line to be placed on the signaling highway.

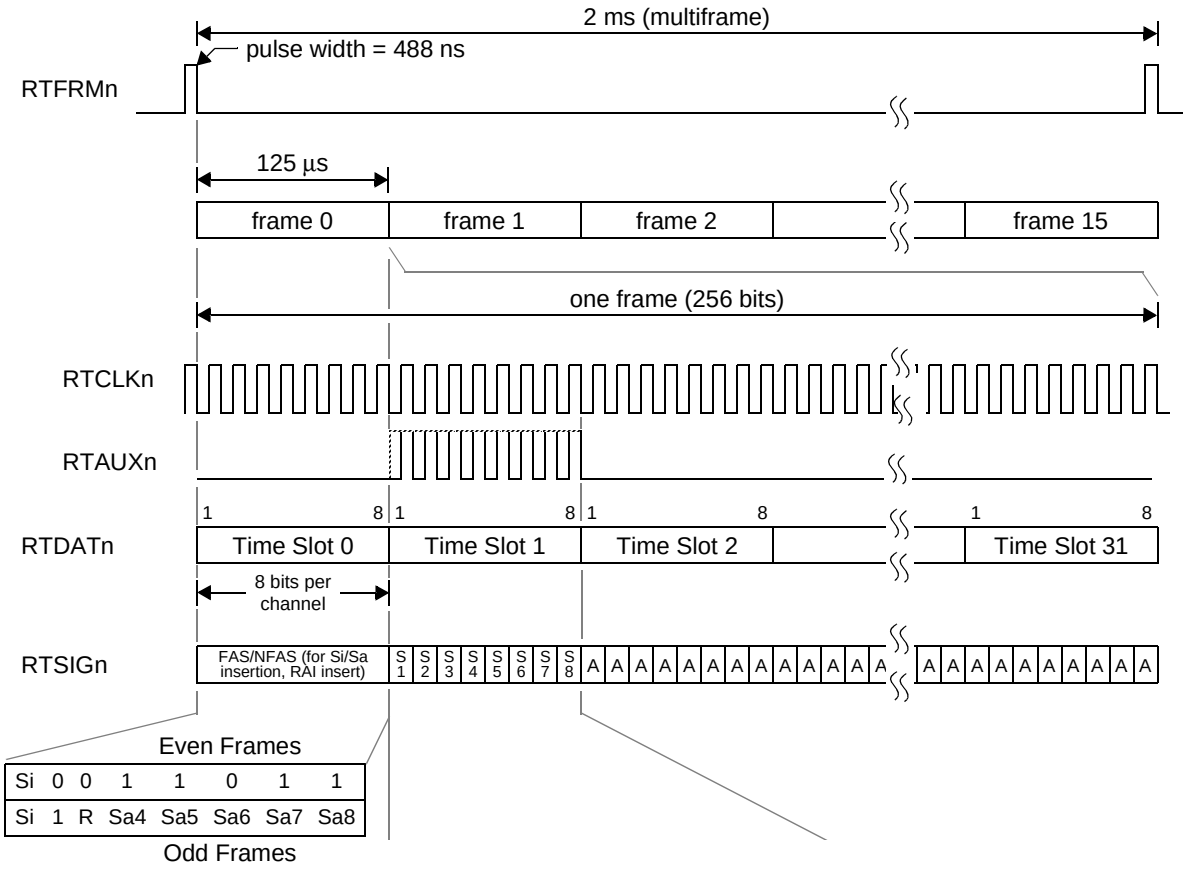
Figure 43 shows the operation of the gapped clock or marker output RTAUXn. RTAUXn is shown with a gapped clock output for Time Slot 1. The 32 control bits RFCHc in registers X+1BH through X+1EH determine the signal on RTAUXn. Control bit RCHMK (bits 7) in register X+1AH controls the selected RTAUXn signal. RCHMK set to 1 selects a channel marker (RTAUXn high for 8 clock periods of selected time slot). The table below shows the options described (where X=don't care).

RFCHc	RCHMK	Action for the Selected Time Slot
0	X	Normal Operation. Channel not selected for fractional E1 service. RTAUXn lead low.
1	0	Fractional E1 Service. 64 kbit/s gapped clock provided on the RTAUXn lead.
1	1	Fractional E1 Service. 64 kbit/s channel marker provided on the RTAUXn lead.

Data and Signaling Inversion

To accommodate different system applications either the Data (time slots) or the Signaling (ABCD) may be inverted to or from the System Interface. Alternate digit inversion (either odd or even bits) is also provided. This feature is available per E1. FAS bits, NFAS bits, spare bits, National bits and International bits and alarm bits are not inverted or altered by these control bits. Control bits RDINV and RSINV (bits 7 and 6) in register X+04H, when set to 1, invert the time slot data to output lead RTDATn and the signaling bits to output lead RTSIGn, respectively. Control bits TDINV and TSINV (bits 5 and 4) in register X+04H, when set to 1, invert the time slot data input from leads TTDATn and TTAIXn and the signaling bits input from lead TTSIGn, respectively. Control bit RDADI and TDADI (bits 3 and 2) in register X+04H invert the even bits of RTDATn and TTDATn respectively if set to 1 after inversion if any by RDINV or TDINV. The table below indicates the options (where X=don't care).

RDINV	RDADI	RSINV	TDINV	TDADI	TSINV	Action Taken on Highways
0	0	0	X	X	X	Received data, Si bits, Sa4 - Sa8 bits, Spare bits and signaling not inverted from line to RTDATn/RTSIGn.
0	0	1	X	X	X	Signaling bits only on RTSIGn inverted (frames 2 - 16).
1	0	0	X	X	X	RTDATn inverted (time slots 1 through 31).
0	1	0	X	X	X	Even bits on RTDATn time slots 1 through 31 inverted.
1	1	0	X	X	X	Odd bits on RTDATn time slots 1 through 31 inverted.
1	0	1	X	X	X	Even bits on RTDATn time slots 1 through 31 inverted; Signaling bits only on RTSIGn inverted (frames 2 - 16).
1	1	1	X	X	X	Odd bits on RTDATn time slots 1 through 31 inverted; Signaling bits only on RTSIGn inverted (frames 2 - 16).
X	X	X	0	0	0	Data, signaling, Si bits, Sa4 - Sa8 bits and Spare bits selected to be transmitted as received on TTDATn/TTSIGn.
X	X	X	0	0	1	Signaling bits only from TTSIGn inverted (frames 2 - 16)
X	X	X	1	0	0	TTDATn inverted (time slots 1 through 31).
X	X	X	0	1	0	Even bits from TTDATn time slots 1 through 31 inverted.
X	X	X	1	1	0	Odd bits from TTDATn time slots 1 through 31 inverted.
X	X	X	1	0	1	Even bits from TTDATn time slots 1 through 31 inverted; Signaling bits only from TTSIGn inverted (frames 2 - 16).
X	X	X	1	1	1	Odd bits from TTDATn time slots 1 through 31 inverted; Signaling bits only from TTSIGn inverted (frames 2 - 16).



Frame	RTSIG; S1 - S8
0	0, 0, 0, 0, X0, Y, X1, X2,
1	A1, B1, C1, D1, A16, B16, C16, D16
2	A2, B2, C2, D2, A17, B17, C17, D17
3	A3, B3, C3, D3, A18, B18, C18, D18
4	A4, B4, C4, D4, A19, B19, C19, D19
5	A5, B5, C5, D5, A20, B20, C20, D20
6	A6, B6, C6, D6, A21, B21, C21, D21
7	A7, B7, C7, D7, A22, B22, C22, D22
8	A8, B8, C8, D8, A23, B23, C23, D23
9	A9, B9, C9, D9, A24, B24, C24, D24
10	A10, B10, C10, D10, A25, B25, C25, D25
11	A11, B11, C11, D11, A26, B26, C26, D26
12	A12, B12, C12, D12, A27, B27, C27, D27
13	A13, B13, C13, D13, A28, B28, C28, D28
14	A14, B14, C14, D14, A29, B29, C29, D29
15	A15, B15, C15, D15, A30, B30, C30, D30

Notes:
Si = International Bits
R = Remote Alarm Indication (RAI) bit, known as TS0 A-bit
San = National bits (n = 4-8)
Xb = Spare bits (b = 0-2)
Y = Multiframe Alarm
Ac Bc Cc Dc = ABCD signal bits for channel c (1-30)
A = Alarm Bits (AIS)
Gapped clock RTAUXn shown for Time Slot 1 (the marker is a single 8 bit wide pulse) Bit TS0FZ (bit 5) reg. X+134H=0

Figure 43. Receive Highway - Transmission Mode

DATA MODE

The Data Mode is enabled when a low is placed on both the CONF0 and CONF1 leads and control bit DINTF (bit 1) in register 00BH is set to 1.

Transmit Highway with Fractional E1 Support

When the Data Mode is selected, the transmit highway carries information from the system to the E1Fx8 for each framer. The highway is subdivided into two time division multiplexed buses, one for data (TTDATn), and the other one for signaling (TTSIGn). The n in the TTDATn and TTSIGn signals represents one of the eight framers. The two buses are synchronous with respect to the highway clock (TTCLKn), which has a clock rate of 2048 kHz. The data highway is a single bit-serial bus organized into 256-bit groups called frames, with the bits in each group numbered 1 through 256. Each frame consists of 32 time slots numbered from 0 to 31, as shown in Figure 44. Time Slot 0 carries the frame synchronization pattern, multiframe pattern for the CRC-4 multiframe option which uses the International bits, RAI bits and Sa4 through Sa8 National bits. Also note that the beginning of each frame is identified by an active high synchronization pulse (TTFRMn), one (TTCLKn) clock cycle wide, which occurs every 125 µs, normally at the beginning of each frame. The position of the TTFRMn pulse is programmable to any bit position within the data bus frame using control bits TFRM7-TFRM0 in register 02FH. The synchronization pulse is aligned to bit 1 in Time Slot 0 in every frame when a value of 00H is written into this register. Data from the data highway may be enabled on a per time slot basis for transmission to the E1 line. Control bits TDE1 through TDE31 in control registers X+E4H, X+E5H, X+E6H and X+E7H when set to a 1 enable the time slot data to the line for the selected time slots.

The signaling bus (TTSIGn) is also divided into 256-bit frames. Each signaling frame consists of 120-bits of signaling information for the 30 telephone channels, numbered from 1 to 30, that are carried on the data bus occupying time slots 1 through 15 and 17 through 31. The first time slot (Time Slot 0) in the signaling highway is assigned to carry the two International bits in bit 1 of alternate frames (bit Si), and the five National bits in bits 4 through 8 and the Remote Alarm Indication bit (A-bit) in bit 3 of alternate (NFAS) frames. The positions of the Time Slot 0 bits in this frame are the same as found in Time Slot 0 of the E1 frame format. It is not required that the Time Slot 0 bits from the signaling highway carry the frame alignment pattern in FAS frames or have bit 2 in NFAS frames set to a 1. The E1Fx8 generates a new Time Slot 0 and does not use any of the information from TTSIGn. The sync pulse (TTFRMn) determines the start of each frame.

In Figure 44 below the ABCD signaling states associated with each of the time slots are carried in the last four bits of each signaling bus time slot. Thus, signaling is available for all telephone channels every frame. The first four bits in each signaling bus time slot may be set to zero. The E1Fx8 inserts the signaling bits from the signaling highway into the corresponding Time Slot 16 positions for transmission on the E1 line if enabled by control bits TSE1 through TSE30 in registers X+ECH, X+EDH, X+EEH and X+EFH.

Figure 44 shows the operation of the gapped clock or marker output TTAUXn as well as the auxiliary input TTAIXn. TTAUXn is shown with a marker output for Time Slot 0. The 32 control bit pairs TC1Cc/TC0Cc in registers X+112H through X+118H determine the source of each transmitted time slot (c = 0 - 31); it can come from the TTDATn, TTAIXn, the Idle Code Insertion register (X+119H) or a Digital Milliwatt generator. Control bit TCHMK (bits 7) in register X+110H controls the TTAUXn signal. TCHMK set to 1 selects a channel marker (TTAUXn high for 8 clock periods of selected time slot). Control bit ULAW (bit 2) in register X+06H selects the coding law used to generate the digital milliwatt. The table below shows the options described (where X=don't care).

TC1Cc	TC0Cc	TCHMK	ULAW	Action for the Selected Time Slot
0	0	X	X	Normal Operation. The Time Slot (c= 1 - 31) is transmitted intact from the data highway, TTDATn. The TTAIXn lead is disabled.
0	1	0	X	Fractional E1 Service. 64 kbit/s gapped Clock provided on the TTAUXn lead, and data from TTAIXn lead is multiplexed into transmit bit stream.
0	1	1	X	Fractional E1 Service. Channel marker provided on the TTAUXn lead, and data from TTAIXn lead is multiplexed into transmit bit stream.
1	0	X	X	Insert microprocessor-written Idle Code value from register X+119H. No gapped clock or channel marker generation on the TTAUXn lead. The TTAIXn lead is disabled.
1	1	X	0	A-law Digital Milliwatt generated for the Time Slot selected. No gapped clock or marker channel generation on TTAUXn lead. The TTAIXn lead is disabled.
1	1	X	1	mu-law Digital Milliwatt generated for the Time Slot selected. No gapped clock or marker channel generation on TTAUXn lead. The TTAIXn lead is disabled.

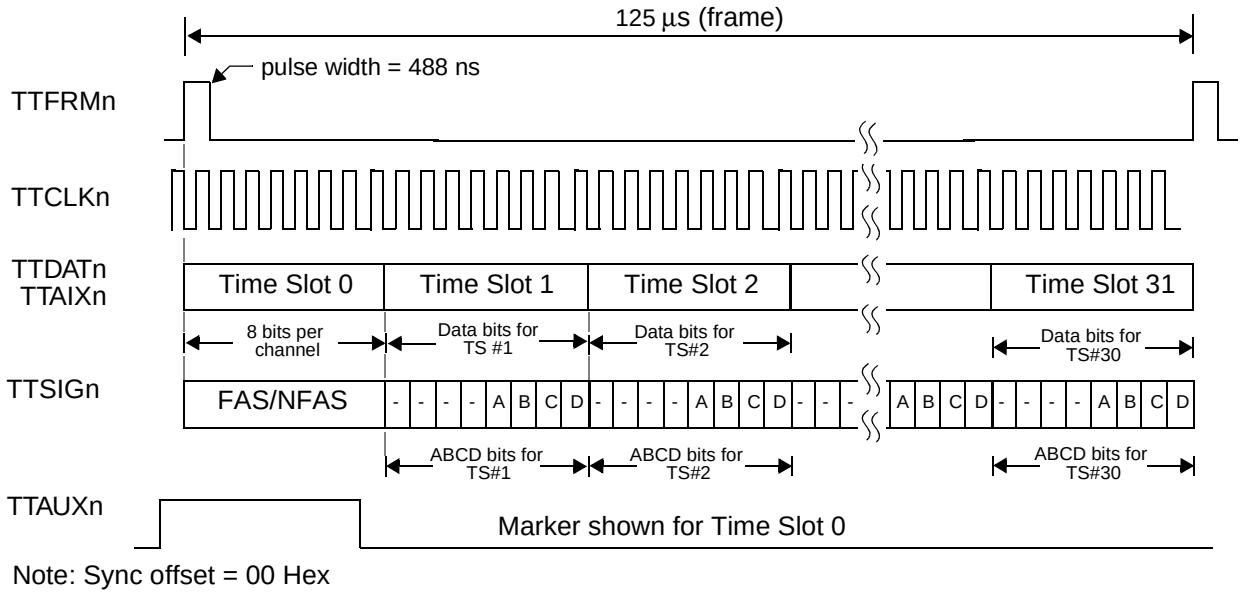


Figure 44. Transmit Highway - Data Mode

Receive Highway with Fractional E1 Support

In the Data Mode, the receive highway for each framer carries information from the E1Fx8 to the system. Like the transmit path, the receive highway is also subdivided into two time division multiplexed buses, one for data (RTDATn), and one for signaling (RTSIGn), where n represents one of the eight framers. The two buses are synchronous with the highway clock (RTCLKn), which has a clock rate of 2048 kHz. The clock (RTCLKn) is either an output to the system or an input from the system. The system clock (RTCLKn) or the line clock (RCLKn) may be the input clock source for the slip buffer when it is enabled. Usually the system clock (RTCLKn) is used. The E1Fx8 must be set to source the clock (RTCLKn) as an output when the slip buffer is bypassed. The receive slip buffer for a framer is disabled when a 0 is written to the RXSBE bit (bit 5) in the register X+11BH. The clock source selection is determined by the RXCKE bit (bit 7) in register X+11BH. A 0 written into this bit position selects the system clock (RTCLKn) as the source clock. In addition to controlling the source of the clock, control bit RXCKE also controls the source of the synchronization pulse.

The data highway is a single bit-serial bus organized into 256-bit groups called frames, with the bits in each group numbered 1 through 256. Each frame consists of 32 time slots numbered from 0 to 31, as shown in Figure 45. Time Slot 0 carries the frame synchronization pattern, multiframe pattern for the CRC-4 multiframe option which uses the International bits, RAI bits and Sa4 through Sa8 National bits. Time Slot 0 is output on RTDATn as it is received from the E1 line. Also note that the beginning of each frame is identified by an active high synchronization pulse (RTFRMn), one (RTCLKn) clock cycle wide, which occurs every 125 µs, normally at the beginning of each frame. The position of the RTFRMn pulse is programmable to any bit position within the data bus frame using control bits RFRM7-RFRM0 in register 02EH. The synchronization pulse is aligned to bit 1 in Time Slot 0 in every frame when a value of 00H is written into this register. Data to the data highway may be enabled on a per time slot basis from the E1 line. Control bits RDE1 through RDE31 in control registers X+3CH, X+3DH, X+3EH and X+3FH when set to a 1 enable the time slot data from the line for the selected time slots.

The signaling bus (RTSIGn) is also divided into 256-bit frames. Each signaling frame consists of 120-bits of signaling information for the 30 telephone channels, numbered from 1 to 30, that are carried on the data bus occupying time slots 1 through 15 and 17 through 31. The first time slot (Time Slot 0) in the signaling highway is assigned to carry the two International bits in bit 1 of alternate frames (bit Si), and the five National bits in bits 4 through 8 and the Remote Alarm Indication bit (A-bit) in bit 3 of alternate (NFAS) frames. The content of the Time Slot 0 bits in each frame are the same as found in Time Slot 0 of the received E1 frame. The sync pulse (RTFRMn) determines the start of each frame.

In Figure 45 below the ABCD signaling states associated with each of the data time slots are carried in the last four bits of a signaling bus time slot. The first four bits in each signaling bus time slot are set to zero. The E1Fx8 inserts the signaling bits from the line onto the signaling highway if enabled by control bits RSE1 through RSE30 in registers X+E8H, X+E9H, X+EAH and X+EBH (after debouncing the signal, if debouncing is selected) every frame.

Figure 45 shows the operation of the gapped clock or marker output RTAUXn. RTAUXn is shown with a marker output for Time Slot 0. The 32 control bits RFCHc in registers X+1BH through X+1EH determine the signal on RTAUXn. Control bit RCHMK (bits 7) in register X+1AH controls the selected RTAUXn signal. RCHMK set to 1 selects a channel marker (RTAUXn high for 8 clock periods of selected time slot). The table below shows the options described (where X=don't care).

RFCHc	RCHMK	Action for the Selected Time Slot
0	X	Normal Operation. Channel not selected for fractional E1 service. RTAUXn lead low.
1	0	Fractional E1 Service. 64 kbit/s gapped clock provided on the RTAUXn lead.
1	1	Fractional E1 Service. 64 kbit/s channel marker provided on the RTAUXn lead.

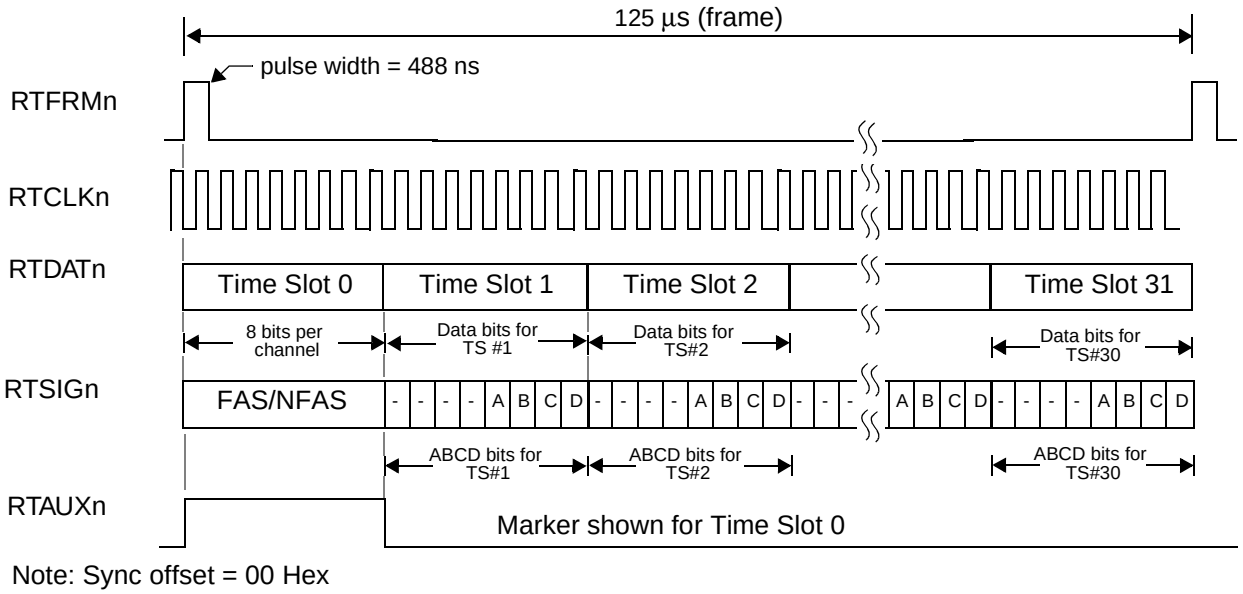


Figure 45. Receive Highway - Data Mode

Data and Signaling Inversion

To accommodate different system applications either the Data (time slots) or the Signaling (ABCD) may be inverted to or from the System Interface. Alternate digit inversion (either odd or even bits) is also provided. This feature is available per E1. Time Slot 0 is not inverted or altered by these control bits. Control bits RDINV and RSINV (bits 7 and 6) in register X+04H, when set to 1, invert the time slot data to output lead RTDATn and the signaling bits to output lead RTSIGn, respectively. Control bits TDINV and TSINV (bits 5 and 4) in register X+04H, when set to 1, invert the time slot data input from leads TTDATn and TTAIXn and the signaling bits input from lead TTSIGn, respectively. Control bit RDADI and TDADI (bits 3 and 2) in register X+04H invert the even bits of RTDATn and TTDATn respectively if set to 1 after inversion if any by RDINV or TDINV. The table below indicates the options (where X=don't care).

RDINV	RDADI	RSINV	TDINV	TDADI	TSINV	Action Taken on Highways
0	0	0	X	X	X	Received data, and signaling not inverted from line to RTDATn/RTSIGn.
0	0	1	X	X	X	Signaling bits only on RTSIGn inverted (time slots 1 through 31).
1	0	0	X	X	X	RTDATn inverted (time slots 1 through 31).
0	1	0	X	X	X	Even bits on RTDATn time slots 1 through 31 inverted.
1	1	0	X	X	X	Odd bits on RTDATn time slots 1 through 31 inverted.
1	0	1	X	X	X	Even bits on RTDATn time slots 1 through 31 inverted. Signaling bits only on RTSIGn inverted (time slots 1 through 31).
1	1	1	X	X	X	Odd bits on RTDATn time slots 1 through 31 inverted; Signaling bits only on RTSIGn inverted (time slots 1 through 31).
X	X	X	0	0	0	Data to be transmitted as received on TTDATn/TTSIGn.

RDINV	RDADI	RSINV	TDINV	TDADI	TSINV	Action Taken on Highways
X	X	X	0	0	1	Signaling bits only from TTSIGn inverted (time slots 1 through 31)
X	X	X	1	0	0	TTDATn inverted (time slots 1 through 31).
X	X	X	0	1	0	Even bits from TTDATn time slots 1 through 31 inverted.
X	X	X	1	1	0	Odd bits from TTDATn time slots 1 through 31 inverted.
X	X	X	1	0	1	Even bits from TTDATn time slots 1 through 31 inverted; Signaling bits only from TTSIGn inverted (time slots 1 through 31).
X	X	X	1	1	1	Odd bits from TTDATn time slots 1 through 31 inverted. Signaling bits only from TTSIGn inverted (time slots 1 through 31).

MVIP MODE

The MVIP Mode is enabled when a high is placed on the CONF0 lead and a low is placed on the CONF1 lead.

Transmit Highway

In the MVIP Mode, the transmit highway for each framer in the E1Fx8 carries input information from the system. The highway for framer n is subdivided into two time division multiplexed buses, one for data (TTDATn), and one for signaling (TTSIGn). The two buses are synchronous with the highway clock (TTCLKn), which has a clock rate of 2048 kHz. The data bus is a single bit-serial bus organized into 256-bit groups called frames. Each frame consists of thirty-two time slots corresponding to the time slots on a framed E1 line.

The frame start is identified by an active low synchronization pulse (TTFRMn), which is one (TTCLKn) clock cycle wide and occurs every 125 microseconds. The position of the TTFRMn pulse is programmable to any bit position within the frame using control bits TFRM7 - TFRM0 in register 02FH. The synchronization pulse is aligned to bit 1 in Time Slot 0 when a value of 00H is written into this register.

The signaling bus (TTSIGn) is also divided into 256-bit frames. Each signaling frame consists of 32 time slots, of which 30 time slots carry the ABCD signaling bits associated with the 30 telephone channels. Time Slots 0 and 16 do not carry signaling information. The first time slot (Time Slot 0) in the signaling highway is assigned to carry the two International bits in bit 1 of alternate frames (bit Si), and the five National bits in bits 4 through 8 and the Remote Alarm Indication bit (A-bit) in bit 3 of alternate (NFAS) frames. The positions of the Time Slot 0 bits in this frame are the same as found in Time Slot 0 of the E1 frame format. It is not required that the Time Slot 0 bits from the signaling highway carry the frame alignment pattern in FAS frames or have bit 2 in NFAS frames set to a 1. The E1Fx8 generates a new Time Slot 0 and does not use any of the information from TTSIGn. The signaling information (ABCD) is carried in the last four bits of a signaling bus time slot. The signaling buffer is updated every other frame. The line signaling states are updated once every sixteen frames per the Time Slot 16 signaling positions. In Figure 46 below the ABCD signaling states associated with each of the telephone channels is carried in the last four bits of a signaling bus time slot. The first four bits in each signaling bus time slot may be set to zero. The E1Fx8 inserts the signaling bits from the signaling highway into time Slot 16 positions if enabled by control bits TSE1 through TSE30 in registers X+ECH, X+EDH, X+EEH and X+EFH.

Figure 46 shows the basic operation in MVIP Mode. The transmit slip buffer must always be enabled by control bit TXSBE (bit 5) in register X+11CH being set to a 1 to provide clock rate adjustment between the 2.048 MHz backplane and the 2.048 MHz line.

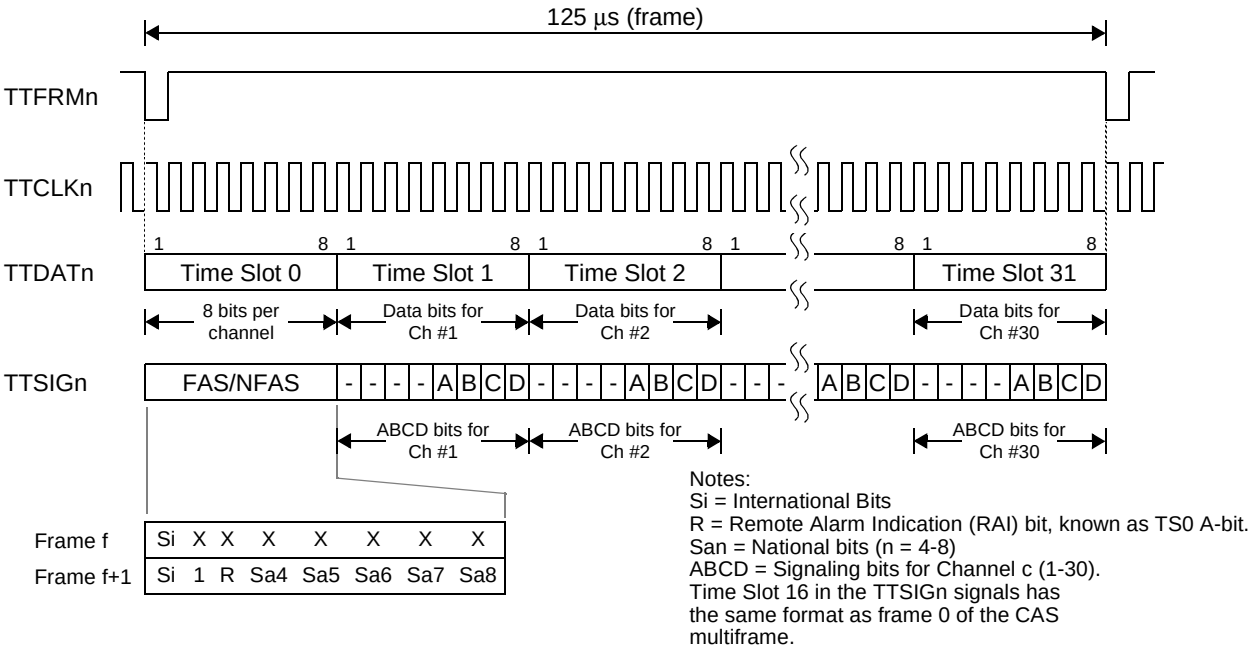


Figure 46. Transmit Highway - MVIP Mode

Receive Highway

In the MVIP Mode, the receive highway for each framer carries output information from the E1Fx8 to the system. The highway for framer n is subdivided into two time division multiplexed buses, one for data (RTDATn), and one for signaling (RTSIGn). The two buses are synchronous with the highway clock (RTCLKn), which has a clock rate of 2048 kHz. The data bus is a single bit-serial bus organized into 256-bit groups called frames. Each frame consists of thirty-two time slots corresponding to the time slots from the framed E1 line.

The frame start is identified by an active low synchronization pulse (RTFRMn), which is one (RTCLKn) clock cycle wide and occurs every 125 microseconds. The position of the RTFRMn pulse is programmable by setting the values of the control bits RFRM7 - RFRM0 in register 02EH. The synchronization pulse is aligned to bit 1 in Time Slot 0 when a value of 00H is written into this register.

The signaling bus (RTSIGn) is also divided into 256-bit frames. Each signaling frame consists of 32 time slots, of which 30 time slots carry the ABCD signaling bits associated with the 30 telephone channels. Time Slots 0 and 16 do not carry signaling information. Time Slot 0 carries the received Time Slot 0 from the E1 line and Time Slot 16 carries the signals from Time Slot 16 frame 1 (0000 X0,Y,X1,X2). The signaling information (ABCD) is carried in the last four bits of a signaling bus time slot. The first four bits in each time slot are 0000. In Figure 47 below, the ABCD signaling states associated with each of the telephone channels are carried in the last four bits of a signaling bus time slot. The E1Fx8 inserts the signaling bits from the signaling buffer into the signaling highway bit positions; if enabled by control bits RSE1 through RSE30 in registers X+E8H, X+E9H, X+EAH and X+EBH, the signaling bits from the Time Slot 16 positions from the line side are inserted into the signaling buffer. The signaling highway is updated from the signaling buffer every frame. The signaling buffer is updated by the line every sixteen frames.

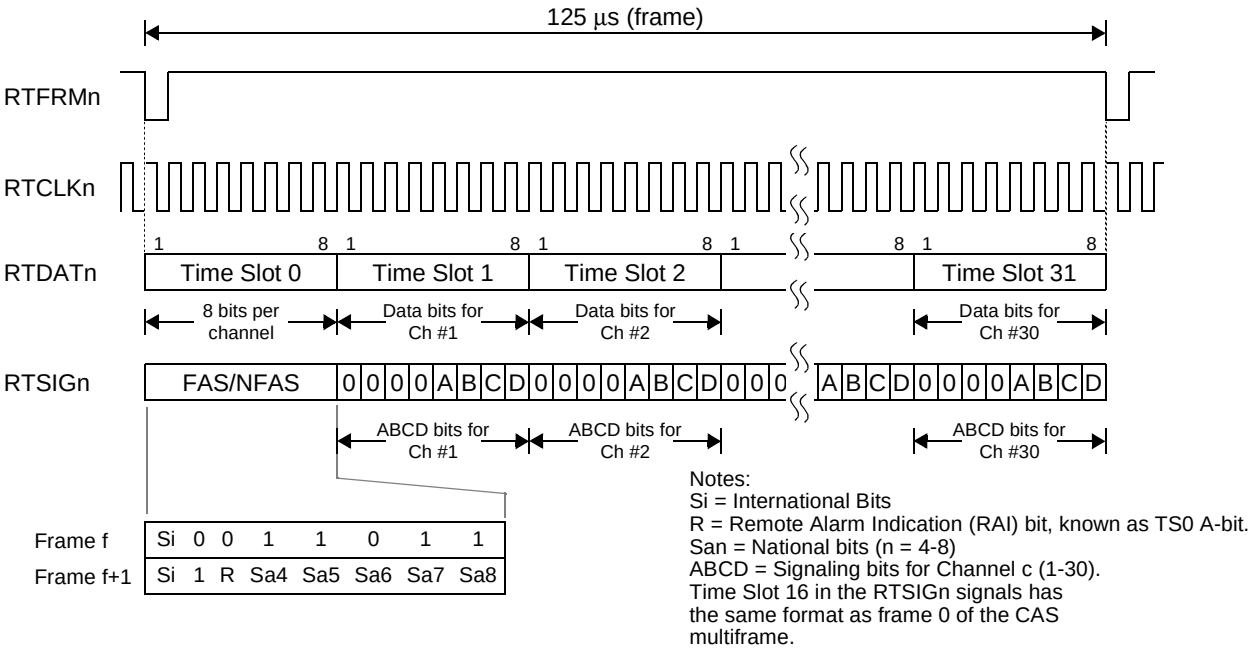


Figure 47. Receive Highway - MVIP Mode

Data and Signaling Inversion

To accommodate different system applications either the Data (time slots) or the Signaling (ABCD) may be inverted to or from the System Interface. Alternate digit inversion (either odd or even bits) is also provided. This feature is available per E1. Time Slot 0 is not inverted or altered by these control bits. Control bits RDINV and RSINV (bits 7 and 6) in register X+04H, when set to 1, invert the time slot data to output lead RTDATn and the signaling bits to output lead RTSIGn, respectively. Control bits TDINV and TSINV (bits 5 and 4) in register X+04H, when set to 1, invert the time slot data input from leads TTDATn and TTAIXn and the signaling bits input from lead TTSIGn, respectively. Control bit RDADI and TDADI (bits 3 and 2) in register X+04H invert the even bits of RTDATn and TTDATn respectively if set to 1 after inversion if any by RDINV or TDINV. The table below indicates the options (where X=don't care).

RDINV	RDADI	RSINV	TDINV	TDADI	TSINV	Action Taken on Highways
0	0	0	X	X	X	Received data, and signaling not inverted from line to RTDATn/RTSIGn.
0	0	1	X	X	X	Signaling bits only on RTSIGn inverted (time slots 1 through 31).
1	0	0	X	X	X	RTDATn inverted (time slots 1 through 31).
0	1	0	X	X	X	Even bits on RTDATn time slots 1 through 31 inverted.
1	1	0	X	X	X	Odd bits on RTDATn time slots 1 through 31 inverted.
1	0	1	X	X	X	Even bits on RTDATn time slots 1 through 31 inverted; Signaling bits only on RTSIGn inverted (time slots 1 through 31).
1	1	1	X	X	X	Odd bits on RTDATn time slots 1 through 31 inverted; Signaling bits only on RTSIGn inverted (time slots 1 through 31).
X	X	X	0	0	0	Data to be transmitted as received on TTDATn/TTSIGn.

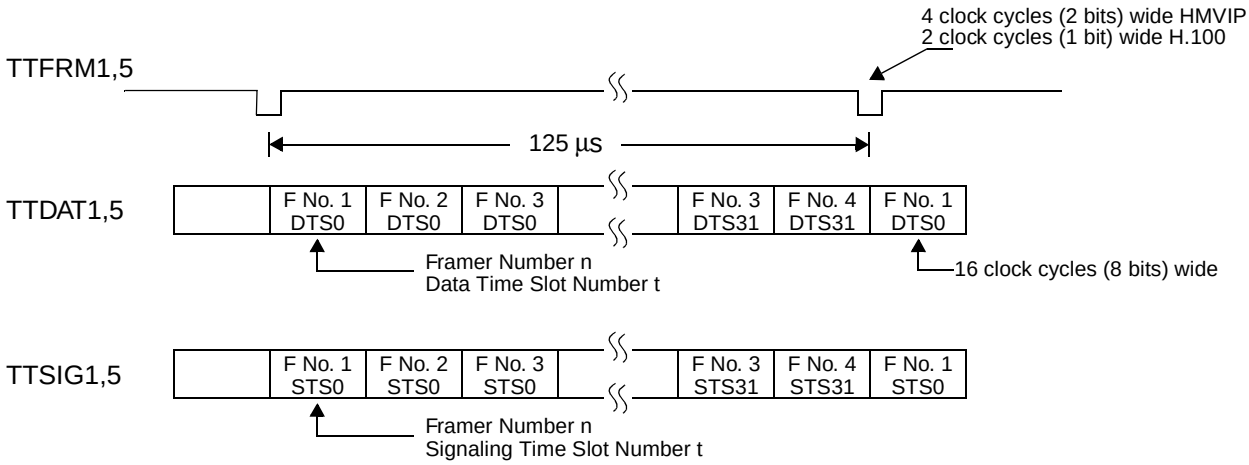
RDINV	RDADI	RSINV	TDINV	TDADI	TSINV	Action Taken on Highways
X	X	X	0	0	1	Signaling bits only from TTSIGn inverted (time slots 1 through 31)
X	X	X	1	0	0	TTDATn inverted (time slots 1 through 31).
X	X	X	0	1	0	Even bits from TTDATn time slots 1 through 31 inverted.
X	X	X	1	1	0	Odd bits from TTDATn time slots 1 through 31 inverted.
X	X	X	1	0	1	Even bits from TTDATn time slots 1 through 31 inverted; Signaling bits only from TTSIGn inverted (time slots 1 through 31).
X	X	X	1	1	1	Odd bits from TTDATn time slots 1 through 31 inverted; Signaling bits only from TTSIGn inverted (time slots 1 through 31).

H-MVIP/H.100 MODE

The H-MVIP Mode is enabled when a low is placed on the CONF0 lead and a high is placed on the CONF1 lead with control bit DINTF (bit 1) in register 00BH set to a 0. H.100 Mode is enabled when a low is placed on the CONF0 lead and a high is placed on the CONF1 lead with control bit DINTF (bit 1) in register 00BH set to a 1. Operationally, the two Modes are the same except the width of TTRFM1,5 and RTFRM1,5 is two clock cycles wide in H.100 Mode and four clock cycles wide in H-MVIP Mode. H.100 PCI level drivers and receivers are not supplied in the H.100 mode.

Transmit Highway

The 8 Mbit/s H-MVIP/H.100 Mode provides dual Transmit Highways, each of which is shared by a group of four framers (1-4 and 5-8). Each Transmit Highway consists of a data bus (TTDAT1, 5), a signaling bus (TTSIG1, 5), a clock (TTCLK1, 5), and a synchronization signal (TTFRM1, 5), with an H.100 option for pulse width. The data and signaling time slots for each of the four framers are byte-interleaved on the Data and Signaling Highways, starting with framer 1 (or 5) bit 1 of Time Slot 0, followed by framer 1 (or 5) bits 2 through 8 of Time Slot 0, then framer 2 (or 6) bits 1 through 8 of Time Slot 0, and so on, ending with framer 4 (or 8) bits 1 through 8 of Time Slot 31. In this Mode, the separate Data and Signaling Highways operate at 8.192 Mbit/s. However, the clock rate is 16.384 MHz. The Transmit System Interface is synchronized by pulses that occur at 125-microsecond intervals. The transmit slip buffer must be enabled in each of the framers. Auxiliary inputs and gapped clocks are not provided in this Mode. Figure 48 below shows the general structure for the framer group n=1-4.



Note: The data and signaling frame formats for each framer are the same as found in the 2 Mbit/s MVIP Mode.

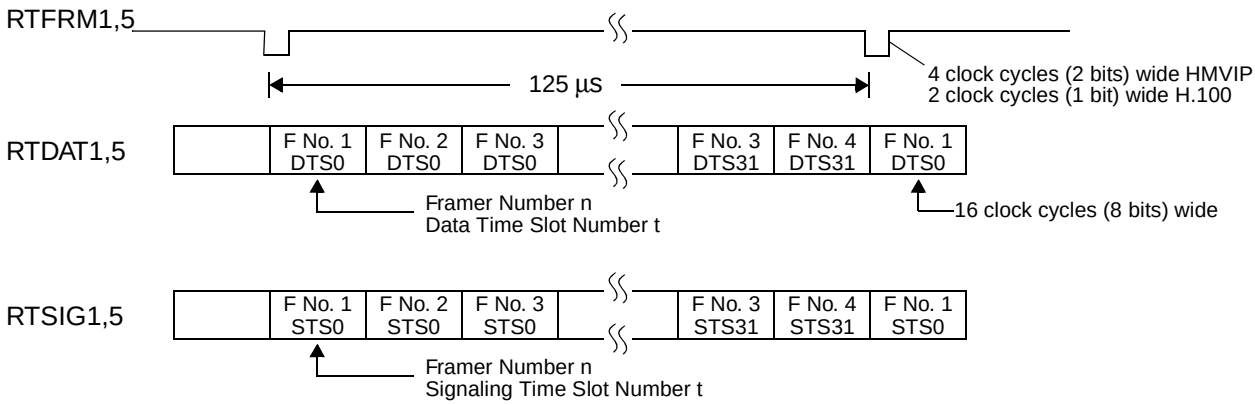
Figure 48. Transmit Data and Signaling Highways - 8 Mbit/s H-MVIP/H.100 Modes

The frame start is identified by an active low synchronization pulse (TTFRM1,5), which is either two (H.100) or four (H-MVIP) TTCLK1,5 clock cycles wide and occurs every 125 microseconds. The position of the TTFRM1,5 pulse is programmable to any of 256 positions within the frame using control bits TFRM7 - TFRM0 in register 02FH. The synchronization pulse is aligned to straddle bit 8 of Time Slot 31 of framer No. 4 (or 8) and bit 1 in Time Slot 0 of framer No. 1 (or 5) when a value of 00H is written into this register. Each value of 01H added to this register shifts the synchronization pulse 8 TTCLK1,5 clock cycles earlier.

Receive Highway

The 8 Mbit/s H-MVIP/H.100 Mode provides dual Receive Highways, each of which is shared by a group of four framers (1-4 and 5-8). Each Receive Highway consists of a data bus (RTDAT1, 5), a signaling bus (RTSIG1, 5), a clock (RTCLK1, 5), and a synchronization signal (RTFRM1, 5), with an H.100 option for pulse width. The data and signaling time slots for each of the four framers are byte-interleaved on the Data and Signaling Highways, starting with framer 1 (or 5) bit 1 of Time Slot 0, followed by framer 1 (or 5) bits 2 through 8 of Time Slot 0, then framer 2 (or 6) bits 1 through 8 of Time Slot 0, and so on, ending with framer 4 (or 8) bits 1 through 8 of Time Slot 31. In this Mode, the separate Data and Signaling Highways operate at 8.192 Mbit/s. However, the clock rate is 16.384 MHz. The Receive System Interface is synchronized by pulses that occur at 125-microsecond intervals. The receive slip buffer must be enabled in each of the framers. Auxiliary inputs and gapped clocks are not provided in this Mode. Figure 49 below shows the general structure for the framer group n=1-4.

The frame start is identified by an active low synchronization pulse (RTFRM1,5), which is either two (H.100) or four (H-MVIP) RTCLK1,5 clock cycles wide and occurs every 125 microseconds. The position of the RTFRM1,5 pulse is programmable to any of 256 positions within the frame using control bits RFRM7-RFRM0 in register 02EH. The synchronization pulse is aligned to straddle bit 8 of Time Slot 31 of framer No. 4 (or 8) and bit 1 in Time Slot 0 of framer No. 1 (or 5) when a value of 00H is written into this register. Each value of 01H added to this register shifts the synchronization pulse 8 RTCLK1,5 clock cycles earlier.



Note: The data and signaling frame formats for each framer are the same as found in the 2 Mbit/s MVIP Mode.

Figure 49. Receive Data and Signaling Highways - 8 Mbit/s H-MVIP/H.100 Modes

Data and Signaling Inversion

To accommodate different system applications either the Data (time slots) or the Signaling (ABCD) may be inverted to or from the System Interface. Alternate digit inversion (either odd or even bits) is also provided. This feature is available per E1. Time Slot 0 is not inverted or altered by these control bits. Control bits RDINV and RSINV (bits 7 and 6) in register X+04H, when set to 1, invert the time slot data to output lead RTDATn and the signaling bits to output lead RTSIGn, respectively. Control bits TDINV and TSINV (bits 5 and 4) in register X+04H, when set to 1, invert the time slot data input from leads TTDATn and TTAIXn and the signaling bits

input from lead TTSIGn, respectively. Control bit RDADI and TDADI (bits 3 and 2) in register X+04H invert the even bits of RTDATn and TTDATn respectively if set to 1 after inversion if any by RDINV or TDINV. The table below indicates the options (where X=don't care). Since RDINV, RDADI, RSINV, TDINV, TDADI and TSINV are controls per E1, the actions taken are per framer, not on the entire highway.

RDINV	RDADI	RSINV	TDINV	TDADI	TSINV	Action Taken per Framer
0	0	0	X	X	X	Received data and signaling not inverted from line to system
0	0	1	X	X	X	Signaling bits on RTSIG1,5 selected time slots inverted.
1	0	0	X	X	X	RTDAT1,5 selected time slots inverted.
0	1	0	X	X	X	Even bits on RTDAT1,5 selected time slots inverted.
1	1	0	X	X	X	Odd bits on RTDAT1,5 selected time slots inverted.
1	0	1	X	X	X	Even bits on RTDAT1,5 selected time slots inverted. Signaling bits on RTSIGn selected time slots inverted.
1	1	1	X	X	X	Odd bits on RTDAT1,5 selected time slots inverted. Signaling bits on RTSIGn selected time slots inverted.
X	X	X	0	0	0	Data to be transmitted as received on TTDAT1,5/TTSIG1,5.
X	X	X	0	0	1	Signaling bits on TTSIG1,5 selected time slots inverted.
X	X	X	1	0	0	TTDAT1,5 selected time slots inverted.
X	X	X	0	1	0	Even bits from TTDAT1,5 selected time slots inverted.
X	X	X	1	1	0	Odd bits from TTDAT1,5 selected time slots inverted.
X	X	X	1	0	1	Even bits on TTDAT1,5 selected time slots inverted. Signaling bits on TTSIGn selected time slots inverted.
X	X	X	1	1	1	Odd bits on TTDAT1,5 selected time slots inverted. Signaling bits on TTSIGn selected time slots inverted.

FRAMING

Frame Structure

The basic frame structure of the 2048 kbit/s E1 signal consists of thirty-two 8-bit time slots, or 256 bits, and has a duration of 125 microseconds (8,000 frames per second). Each time slot provides a 64 kbit/s channel. The thirty-two time slots are numbered 0 to 31, and the time slot bits are numbered 1 to 8. The first bit in a time slot to be received and transmitted is bit 1. Framing information is carried in Time Slot 0, and signaling information, if it is assigned for Channel Associated Signaling (CAS), is carried in Time Slot 16.

Framing information for aligning the E1 frame is carried in Time Slot 0, using a two-frame sequence that alternates for consecutive frames. Time Slot 0 in the first frame carries the frame alignment pattern of X0011011. The second frame carries the pattern of X1XXXXXX, so that bit 2 identifies the first and second frames. The other bits in Time Slot 0, which are designated as X and are not used for frame alignment, are assigned for national, alarm and international use. The following table illustrates the framing pattern and bit assignment for Time Slot 0 when assigned to carry the basic framing format.

Frame	Type	Bit 1	2	3	4	5	6	7	8
1	FAS	Si (#1)	0	0	1	1	0	1	1
2	NFAS	Si (#2)	1	RAI	Sa4	Sa5	Sa6	Sa7	Sa8

Where: Si is reserved for international use.
RAI is defined as a Remote Alarm Indication A-bit (true state is equal to 1)
Sa4-Sa8 bits are reserved for national use.

To provide end to end performance monitoring and additional framing protection against the emulation of a frame alignment pattern in the data stream, Time Slot 0 can be assigned to carry a 16-frame multiframe. The 16-frame multiframe carries a 001011 multiframe alignment pattern, CRC-4 check, and two E-bits in the bit 1 position of two sub-multiframes designated as SF I and SF II, as shown below:

Sub-F	Frame	Type	Bit 1	2	3	4	5	6	7	8
SF I	0	FAS	C1	0	0	1	1	0	1	1
	1	NFAS	0	1	RAI	Sa4	Sa5	Sa6	Sa7	Sa8
	2	FAS	C2	0	0	1	1	0	1	1
	3	NFAS	0	1	RAI	Sa4	Sa5	Sa6	Sa7	Sa8
	4	FAS	C3	0	0	1	1	0	1	1
	5	NFAS	1	1	RAI	Sa4	Sa5	Sa6	Sa7	Sa8
	6	FAS	C4	0	0	1	1	0	1	1
	7	NFAS	0	1	RAI	Sa4	Sa5	Sa6	Sa7	Sa8
SF II	8	FAS	C1	0	0	1	1	0	1	1
	9	NFAS	1	1	RAI	Sa4	Sa5	Sa6	Sa7	Sa8
	10	FAS	C2	0	0	1	1	0	1	1
	11	NFAS	1	1	RAI	Sa4	Sa5	Sa6	Sa7	Sa8
	12	FAS	C3	0	0	1	1	0	1	1
	13	NFAS	E	1	RAI	Sa4	Sa5	Sa6	Sa7	Sa8
	14	FAS	C4	0	0	1	1	0	1	1
	15	NFAS	E	1	RAI	Sa4	Sa5	Sa6	Sa7	Sa8

Where: C1-C4 are the CRC-4 bits.
RAI is defined as a Remote Alarm Indication A-bit (true state is equal to 1)
Sa4-Sa8 are reserved for national use.
E-bits are used for a CRC-4 error indication to or from far end (far end block error)
FAS is the frame alignment signal
NFAS is the non frame alignment signal

FRAME ALIGNMENT

The E1Fx8 supports two frame alignment operating modes in each framer: basic frame alignment detection, and frame alignment detection with a CRC-4 validation. The receive framer circuit also employs an offline framing algorithm, where the payload is sent to the terminal side output even during loss of frame (together with RTFRMn and RTCLKn, if these are framer outputs). This is advantageous, since re-framing usually occurs at the same frame position.

Frame alignment and framing pattern generation may be optionally applied to the receive path or the transmit path of the E1Fx8 as shown in the table below.

RTFM X+01H:7	TTFM X+01H:6	Framing Actions taken by E1Fx8
0	0	The receive path is set to detect frame alignment and the transmit path generates Time Slot 0 as determined by control bits CRCMD1,0, BFAA, CRCA, AAGS and AIW.

RTFM X+01H:7	TTFM X+01H:6	Framing Actions taken by E1Fx8
0	1	The receive path is set to detect frame alignment as determined by control bits CRCMD1,0, BFAA, CRCA, AAGS and AIW. The transmit path is transparent; Data is passed through from TTDATn directly or via the transmit slip buffer unaltered; TTFRMn has no influence. Slip buffer slips affect a group of 256 bits uniformly (skipped or repeated).
1	0	The transmit path generates Time Slot 0 as determined by control bits CRCMD1,0, BFAA, CRCA, AAGS and AIW. The receive path is transparent. Every 256 line bits are passed through to RTDATn directly or via the receive slip buffer unaltered; RTFRMn has no relationship to Time Slot 0. Slip buffer slips affect a group of 256 bits uniformly (skipped or repeated).
1	1	The receive and transmit paths are transparent. Every 256 line bits are passed through to RTDATn directly or via the receive slip buffer unaltered; RTFRMn has no relationship to Time Slot 0. Data is passed through from TTDATn directly or via the transmit slip buffer unaltered; TTFRMn has no influence. Slip buffer slips affect a group of 256 bits uniformly (skipped or repeated).

Basic frame alignment detection has two algorithms: Standard and Frame Hold-Off. The selection is determined by control bit BFAA (bit 5) in the Framer Configuration Register X+01H for each framer. When control bit BFAA is written with a 0, the Standard algorithm is selected. When written with a 1, the Frame Hold-Off algorithm is selected. The Standard framing algorithm operates continuously according to the following steps:

1- A valid frame alignment signal X0011011 is detected in Time Slot 0 of frame f (FAS frame).
2- The absence of a frame alignment signal is verified by checking that bit 2 is a 1 in Time Slot 0 of frame f+1 (NFAS frame).
3- A valid frame alignment signal X0011011 is detected in Time Slot 0 of frame f+2 (FAS frame).

If these criteria are met by three consecutive frames, then the framer is declared to be aligned. If step 2 fails, a new search for frame alignment is started in the next bit position of the current frame. The Frame Hold-Off algorithm uses the same steps as found in the Standard frame alignment search, except that the new search is initiated in the next bit position in the next frame. When the E1Fx8 is out of frame alignment, status bit OOF (bit 5) in register X+10H is set to a 1. An associated mask bit MOOF a latched event bit LOOF, a performance value POOF and a fault value FOOF are all bit 5 of registers X+14H, X+11H, X+12H and X+13H respectively. If control bit AUTRAI (bit 0) in register X+08H is set to a 1, RAI (bit 3 or “A” bit) in NFAS frames will also be set to a 1.

The E1Fx8 also supports frame alignment detection by validating a CRC-4 multiframe check sequence in addition to either of the basic frame alignment detection sequences. Each framer in the E1Fx8 can be configured for two types of CRC-4 multiframe check: manual or an automatic mode. The manual mode is selected by writing a 0 to control bit CRCA (bit 3) in register X+01H. In the manual mode, after frame alignment has been achieved (see above), multiframe alignment occurs if two valid CRC multiframe signals are detected within 8 milliseconds. After CRC multiframe is established the E1Fx8 begins checking the CRC bits. If multiframe cannot be achieved within the 8 millisecond period, a new search for frame alignment is initiated in parallel as well as a new search for multiframe alignment, and an Out Of CRC-4 Multiframe status indication OOFM (bit 2) in register X+10H continues. An associated mask bit MOOFM, a latched event bit LOOFM, a performance value POOFM and a fault value FOOFM are all bit 2 of registers X+14H, X+11H, X+12H and X+13H respectively. When control bits CRCMD1 and CRCMD0 (bits 3 and 2) in register X+07H are set to X0, an indication of CRC-4 multiframe alignment loss is sent to the distant end by setting the two E-bits in Time Slot 0 (bit 1 in frames 13 and 15) to zero.

The automatic mode is selected by writing a 1 to control bit CRCA (bit 3) in register X+01H. Within the automatic mode several options exist for searching for multiframe alignment; ITU-T G.706, ETS 300 011 and TBR 04 with ITAAB note 75 support. The table below describes the various options and how they affect the local and transmitted alarms. Alarm transmission assumes that control AUTRAI (bit 0) in register X+08H is set to a 1.

For ITU-T G.706 control bits CRCMD0, BFAA, CRCA, AAGS and AIW = 0X100. Initially OOF and OOFM status is active, RAI is set to a 1 and the E-bits are set to 0; the first basic frame alignment declaration clears RAI to 0 and OOF status where they remain until basic frame alignment is lost. When multiframe alignment is found, OOFM status is cleared, the E-bits are set to 1 and are only set to 0 when a sub-multiframe is found to have bad CRC-4; each sub-multiframe with bad CRC-4 is counted in a 10 bit error counter CRC0 - CRC9 with overflow bit CRCO in registers X+F2H and X+F3H with one-second shadow counter LCRC0 - LCRC9 and LCRCO in registers X+F0H and X+F1H. If multiframe is not found by the process described above within a 400 millisecond search period, the framer assumes that the distant end is not configured for CRC multiframe pattern, and sets a status bit, NCRC4 (bit 7) in register X+18H to a 1. Once the 400 millisecond timer times out, the E1Fx8 then inhibits further CRC-4 processing. When control bits CRCMD1 and CRCMD0 (bits 2 and 1) in register X+07H are set to X0, an indication of CRC-4 multiframe alignment loss is sent to the distant end by keeping the two E-bits in Time Slot 0 to zero.

For ISDN applications (ITU-T I.431 or ETS 300 011; non interworking) control bits CRCMD0, BFAA, CRCA, AAGS and AIW = 00110. Initially OOF and OOFM status is active, RAI is set to a 1 and the E-bits are set to 1; the first basic frame alignment declaration (using the Standard Algorithm) clears RAI to 0 and OOF status. When multiframe alignment is found, OOFM status is cleared, the E-bits remain set to 1 and are only set to 0 when a sub-multiframe is found to have bad CRC-4; each sub-multiframe with bad CRC-4 is counted in a 10 bit error counter CRC0 - CRC9 with overflow bit CRCO with one-second shadow counter LCRC0 - LCRC9 and LCRCO. If multiframe cannot be achieved within the 8 millisecond period, a new search for frame alignment is initiated in parallel as well as a new search for multiframe alignment, and an Out Of CRC-4 Multiframe status indication OOFM (bit 2) in register X+10H remains. In addition the RAI indication is sent until the parallel basic frame alignment is declared which clears RAI to 0. If multiframe is not found within a 400 millisecond search period, the framer assumes that the distant end is not configured for CRC multiframe pattern, and sets RAI continuously to a 1 even with basic frame alignment found with status remaining in OOFM. However, searching for multiframe alignment never ceases.

For ETSI ISDN interworking applications (TBR 04 with ITAAB note 75) control bits CRCMD0, BFAA, CRCA, AAGS and AIW = 00101. Initially OOF and OOFM status is active, RAI is set to a 1 and the E-bits are set to 0; the first basic frame alignment declaration (using the Standard Algorithm) clears RAI to 0 and OOF status where they remain until basic frame alignment is lost. When multiframe alignment is found, OOFM status is cleared, the E-bits are set to 1 and are only set to 0 when a sub-multiframe is found to have bad CRC-4; each sub-multiframe with bad CRC-4 is counted in a 10 bit error counter CRC0 - CRC9 with overflow bit CRCO with one-second shadow counter LCRC0 - LCRC9 and LCRCO. If multiframe cannot be achieved within the 8 millisecond period, a new search for frame alignment is initiated in parallel as well as a new search for multiframe alignment, and an Out Of CRC-4 Multiframe status indication OOFM (bit 2) continues. If multiframe is not found within a 400 millisecond search period, the framer assumes that the distant end is not configured for CRC multiframe pattern, and sets a status bit, NCRC4 (bit 7) in register X+18H to a 1, but continues further CRC-4 processing.

For both manual and automatic multiframe alignment the CRC-4 pattern is checked, and an Excessive CRC Error indication ECRCE (bit 6) in register X+164H is set to 1 when 915 or more of the last 1000 CRCs were received in error. An associated mask bit MECRCE, a latched event bit LECRCE, a performance value PECRCE and a fault value FECRCE are all bit 6 of registers X+166H, X+165H, X+167H and X+168H respectively. ECRCE forces an out of frame and is cleared when basic frame alignment is regained. The following table summarizes the control bits associated with selection of the frame alignment algorithm for one of the eight framers (where X=don't care):.

CRCMD1 X+07H:3	CRCMD0 X+07H:2	BFAA X+01H:5	CRCA X+01H:3	AAGS X+01H:0	AIW X+0AH:0	Framing Actions
0	1	0	X	X	X	Frame alignment detector is enabled using the Standard algorithm. The CRC-4 multiframe detector and generator are disabled.
0	1	1	X	X	X	Frame alignment detector is enabled using the Frame Hold-Off algorithm. The CRC-4 multiframe detector and generator are disabled.
X	0	0	0	0	X	Frame alignment detector is enabled using the Standard algorithm. The CRC-4 multiframe detector and generator are enabled for manual operation. In addition, the receive 10-bit CRC counter is enabled. The transmit E-bits are sent as zeros when the CRC-4 multiframe is lost. The 10-bit E-bit performance counter is also enabled, to count E-bit errors.
X	0	1	0	0	X	Frame alignment detector is enabled using the Frame Hold-Off algorithm. The CRC-4 multiframe detector and generator are enabled for manual operation. In addition, the receive 10-bit CRC counter is enabled. The transmit E-bits are sent as zeros when the CRC-4 multiframe is lost. The 10-bit E-bit performance counter is also enabled, to count E-bit errors.
X	0	0	1	0	0	ITU-T G.706 interworking: Frame alignment detector is enabled using the Standard algorithm. The CRC-4 multiframe detector and generator are enabled for automatic operation. In addition, the receive 10-bit CRC counter is enabled. Transmit E-bits are sent as zero when CRC-4 multiframe is lost. The 10-bit E-bit performance counter is also enabled for counting E-bit errors. 400 ms time-out for search; no RAI after basic frame alignment.
X	0	1	1	0	0	ITU-T G.706 interworking: Frame alignment detector is enabled using the Frame Hold-Off algorithm. The CRC-4 multiframe detector and generator are enabled for automatic operation. In addition, the receive 10-bit CRC counter is enabled. The transmit E-bits are sent as zero when CRC-4 multiframe is lost. The 10-bit E-bit performance counter is also enabled for counting E-bit errors. 400 ms time-out for search; no RAI after basic frame alignment.
X	0	0	1	1	0	ETSI ISDN non-interworking: Frame alignment detector is enabled using the Standard algorithm. The CRC-4 multiframe detector and generator are enabled for automatic operation. In addition, the receive 10-bit CRC counter is enabled. The transmit E-bits are sent as one when CRC-4 multiframe is lost. The 10-bit E-bit performance counter is also enabled for counting E-bit errors. 400 ms time-out for setting/clearing RAI after basic frame alignment but no multiframe alignment. No time-out for search.

CRCMD1 X+07H:3	CRCMD0 X+07H:2	BFAA X+01H:5	CRCA X+01H:3	AAGS X+01H:0	AIW X+0AH:0	Framing Actions
X	0	0	1	0	1	ETSI ISDN interworking: Frame alignment detector is enabled using the Standard algorithm. The CRC-4 multiframe detector and generator are enabled for automatic operation. In addition, the receive 10-bit CRC counter is enabled. The transmit E-bits are sent as zero when CRC-4 multiframe is lost. The 10-bit E-bit performance counter is also enabled for counting E-bit errors. No time-out for search; no RAI after basic frame alignment.
X	0	X	1	1	1	Not recommended.
1	1	0	0	X	X	Frame alignment detector is enabled using the Standard algorithm. The CRC-4 multiframe detector and generator are enabled for manual operation. In addition, the receive 10-bit CRC counter is enabled. The E-bits are always transmitted as 1s, if AAGS = 1; otherwise E-bits = 0 under OOF.
1	1	1	0	X	X	Frame alignment detector is enabled using the Frame Hold-Off algorithm. The CRC-4 multiframe detector is enabled for manual operation. In addition, the receive 10-bit CRC counter is enabled. The E-bits are always transmitted as 1s, if AAGS = 1; otherwise E-bits = 0 under OOF.
1	1	0	1	0	0	Frame alignment detector is enabled using the Standard algorithm. The CRC-4 multiframe detector and generator are enabled for automatic operation. The E-bits are always transmitted as 1s, if AAGS = 1; otherwise E-bits = 0 under OOF. The CRC-4 counter is enabled.
1	1	1	1	0	0	Frame alignment detector is enabled using the Frame Hold-Off algorithm. The CRC-4 multiframe detector and generator are enabled for automatic operation. The E-bits are always transmitted as 1s, if AAGS = 1; otherwise E-bits = 0 under OOF. The CRC-4 counter is enabled.
1	1	X	1	1	X	Not recommended
1	1	X	1	X	1	Not recommended

Received E-bits are counted once the E1Fx8 is in CRC-4 multiframe alignment. Each occurrence of a zero E-bit is counted in a 10 bit counter EBE0 - EBE9 with overflow bit EBEO in registers X+100H and X+101H. One-second shadow registers LEBE9 - LEBE0 and LEBEO are located at X+FEH and X+FFH.

Out Of Frame Alignment

An Out Of Frame (OOF) alarm is declared when a selected number of consecutive incorrect frame alignment patterns in Time Slot 0 is detected, or when 915 or more out of 1000 CRC-4 are received in error (ECRCE, bit 6 in register X164H). The OOF alarm is indicated at bit 5 in register X+10H. An associated mask bit MOOF, a latched event bit LOOF, a performance value POOF and a fault value FOOF are all bit 6 of registers X+14H, X+11H, X+12H and X+13H respectively. An incorrect frame alignment pattern is defined as an incorrect bit in at least one of the seven framing bits in an FAS Time Slot 0, or an error (i.e., a 0) in bit 2 in Time Slot 0 in the next (NFAS) frame. The number of incorrect frame alignment patterns in error is programmable using the OOF1 and OOF0

control bits (bits 2 and 1) in register X+01H. The Out Of Frame alignment condition starts the resynchronization process for basic frame alignment. In addition, the software can also initiate a resynchronization of the frame alignment detector by writing a one to control bit RSYNC (bit 6) in register X+0AH.

The following table lists the selection options for declaring an Out Of Frame (OOF) alarm.

OOF1 X01H:2	OOF0 X01H:1	Action
0	0	Three consecutive incorrect frame alignment patterns in the seven-bit framing sequence in an FAS Time Slot 0.
0	1	Four consecutive incorrect frame alignment patterns in the seven-bit framing sequence in an FAS Time Slot 0.
1	0	Three consecutive incorrect frame alignment patterns in the seven-bit framing sequence in an FAS Time Slot 0, or three consecutive incorrect bit 2 values of 0 in a NFAS Time Slot 0. This setting is recommended for ETSI applications.
1	1	Four consecutive incorrect frame alignment patterns in the seven-bit framing sequence in an FAS Time Slot 0, or four consecutive incorrect bit 2 values of 0 in a NFAS Time Slot 0.

Frame word errors (an incorrect bit in at least one of the seven framing bits in an FAS Time Slot 0, or an error (i.e., a 0) in bit 2 in Time Slot 0 in a NFAS frame) are counted in an eight bit counter FBE0-FBE7 with overflow bit FBEO in registers X+FCH and X+FDH. One-second shadow registers LFBE9-LFBE0 and LFBEO are located at X+FAH and X+FBH.

Either a change of basic frame alignment or a change of multiframe alignment may cause a new value to be loaded into the frame synchronization circuit after basic frame alignment (CRC-4 disabled) multiframe alignment (CRC-4 enabled) have been achieved. This condition is indicated in status bit CFA (bit 3) in register X+10H. An associated mask bit MCFA, a latched event bit LCFA, a performance value PCFA and a fault value FCFA are all bit 3 of registers X+14H, X+11H, X+12H and X+13H respectively.

Loss Of CRC-4 Multiframe Alignment

When the CRC-4 feature is enabled, a CRC-4 loss of multiframe indication OOFM (bit 2) in register X+10H is generated if control bit EOOCRC (bit 2) in register X+03H is set to a 1 and when basic frame alignment is lost either by consecutive incorrect basic frame alignment patterns or by 915 or more out of 1000 CRC-4 received in error, as indicated by the OOF alarm, bit 5 in register X+10H. The OOFM bit is cleared only when multiframe alignment is regained. An associated mask bit MOOFM, a latched event bit LOOFM, a performance value POOFM and a fault value FOOFM are all bit 2 of registers X+14H, X+11H, X+12H and X+13H respectively. The OOFM bit is also set if a loss of Time Slot 16 multiframe occurs with control bit EOO16M (bit 1) in register X+03H set to a 1 and control bit TS16EIC (bit 0) in register X+00H is set to a 1.

TRANSMIT FRAMER

Each of the eight transmit framers performs the following functions, unless the framer is configured for the transparent (unframed) mode of operation using the 2 Mbit/s Transmission Mode or Data Mode interfaces only:

- Generates the framing pattern (X0011011) in alternating (FAS) frames for Time Slot 0.
- Sets bit 2 to 1 in Time Slot 0 in (NFAS) frames not carrying the framing pattern.
- Inserts either the International bits for the basic format, or the CRC-4/E-bits with multiframe pattern for the CRC-4 multiframe format into Time Slot 0.
- Inserts the National bits, and Remote Alarm Indication bit, into NFAS Time Slot 0.
- Inserts Time Slots 1-15 and 17-31 into the transmitted frame.
- Inserts Time Slot 16 as either a clear channel, or Channel Associated Signaling (CAS) information from the transmit signaling buffers.
- Locks Time Slot 0 and Time Slot 16 CAS multiframes together for transmission.

Time Slot 0

The basic framed mode of operation is selected by writing control bits CRCMD1 (bit 3) and CRCMD0 (bit 2) in register X+07H to 01 and control bits RTFM and TTFM (bits 7 and 6) in register X+01H are set to 0 to enable framing for either the receive or the transmit path respectively. The mode selection is common to both the transmit and receive sides of a framer channel but transparency is individually selectable. The International bits from the transmit signaling highway (available in Transmission Mode only) are inserted into bit 1 of Time Slot 0, unless the CRC-4 feature is selected. The microprocessor can disable this path by writing a 0 to control bit TSIS (bit 7) in register X+E3H, which freezes the values of the two International bits, located at bit 7 in registers X90H (associated with FAS) and XB0H (associated with NFAS), and allows them to be written by the microprocessor.

The CRC-4 framing mode is selected by writing control bits CRCMD1 (bit 3) and CRCMD0 (bit 2) in register X+07H to X0 or 11. The insertion of the international bits from the signaling highway is disabled, and the transmit framer inserts the multiframe alignment pattern, the calculated CRC-4 value and the E-bits as shown in the chart in the Frame Structure section above. The E-bit generation is internal to the framer within the E1Fx8, and is not directly accessible by the microprocessor in the transmit direction. However, the E-bit may be set to a 0 or 1 initially and, depending on the framing mode options selectable by control bits CRCMD1, CRCMD0, AAGS, CRCA and AIW and the received framing pattern as described in the Frame Alignment section above, the E-bits may be fixed at a 0 or 1 or they may go from 1 to 0 to indicate each bad CRC-4 received.

The CRC multiframe alignment pattern is generated by the framer. The Time Slot 16 (TS16) multiframe alignment pattern is generated only when CAS signaling types are selected by control bits TYP1, TYP0 (bits 7 and 6) in register X+134H (=10 or 01). TS16 multiframe alignment is meaningless in TS16 clear channel mode (TYP1, TYP0 = 00). TS16 multiframe alignment is independent of the device framing mode but is locked to CRC-4 multiframe alignment for transmission to the E1 line when CRC-4 multiframe alignment mode is selected.

The Remote Alarm Indication (RAI) A-bit is assigned to bit 3 in alternating frames in both the framed and CRC-4 mode of operation. When control bit AUTRAI (bit 1) in register X+08H is set to 1, a loss of frame alignment on the receive side sets the transmitted RAI bit to 1 for the duration of the alarm. The microprocessor can also write the state of the RAI bit, independent of automatic RAI insertion. When the microprocessor writes a 1 to control bit TXRAI (bit 6) in register X+06H, the RAI bit is transmitted as a 1. In addition, when control bit EXTRAI (bit 4) in register X+06H is written with a 1, a 1 in bit “R” (bit 3) in Time Slot 0 NFAS frames (odd frames) from the signaling highway in the Transmission Mode only will also result in an RAI alarm being transmitted. See above for RAI set after 400 millisecond time out in ETSI mode.

The seven-bit framing pattern (X0011011) in alternating (FAS) frames for Time Slot 0, and the 1 value for bit 2 in Time Slot 0 in (NFAS) frames not carrying the framing pattern (X1XXXXXX), are generated by the framer.

Each framer also has the capability of generating framing pattern errors in FAS frames, Bit 2 errors in alternating (NFAS) frames, and CRC-4 errors. When control bit FRME (bit 6) in register X+106H is set to 1, the transmitter sends the frame alignment pattern and the International bit (used as CRC in CRC-4 multiframe mode) in error for one FAS frame. All the bits in the frame alignment sequence are inverted (Si0011011 becomes $\overline{Si}$1100100). This bit must be written with a 0 and then a 1 to send another FAS error. When control bit NFASE (bit 4) in X+106H is set to 1, the transmit framer sends bit 2 in Time Slot 0 as a 0 for a single NFAS frame. This bit must be written with a 0 and then a 1 to send another NFAS error. When control bit CRCE (bit 7) in register X+106H is set to 1, the CRC-4 bits in Time Slot 0 are transmitted in the inverted state once if control bits CRCMD1,0 (bits 3 and 2) in register X=07H are set to X0. To send another CRC-4 error, this bit must be first written with a 0, and then a 1.

National Bit Support

Full National bit support is provided for ISDN (ETSI 300 233), ITU-T G.704 synchronization status messages (SSM) and CEPT IRSM signaling ("En" bits). Received National bits are stored in byte wide registers aligned to the CRC-4 multiframe and byte wide registers which are provided for transmitting the National bits. The National bits can be sourced from the signaling highway, TTSIGn, in Transmission mode. The National bits may also be assigned to the HDLC controller.

The transmitted path for the individual National bits (Sa4 to Sa8) in Time Slot 0 in either framing mode can be assigned from the HDLC link (all system interface modes) or from the signaling highway (Transmission Mode only). In the CRC-4 multiframe mode, when control bits TSA4S through TSA8S (bits 4-0) in register X+E3H are set to a 0, control bit BNAL (bit 5) in register X+122H is set to a 0 and control bits SA4 through SA8 (bits 4-0) in register X+0CH are set to 0, the National bits can be sourced from registers XSA4(7-0), XSA5(7-0), XSA6(7-0), XSA7(7-0) and XSA8(7-0) in locations X+169H through X+16DH with bit 7 of each register transmitted in frame 2 of the multiframe, bit 6 in frame 4, etc.

In either framing mode National bits received are stored in the receive slip buffer at location X+60H, designated RNFAS, in bits 4-0 if control bits RSA4S through RSA8S (bits 4-0) in register X+3BH are set to 1. When in RSA4S through RSA8S are set to 0, RNFAS bit(s) 4-0 are frozen and can be written by the microprocessor. In Transmission Mode, the National bits are always read from RNFAS and placed on the receive signaling highway RTSIGn in bits 4 - 8 of Time Slot 0 in NFAS (odd numbered) frames. In the CRC-4 multiframe mode, if control bit ENRXNBR (bit 3) in register X+03H is set to a 1, National bits received are placed in registers RSA4(7-0), RSA5(7-0), RSA6(7-0), RSA7(7-0) and RSA8(7-0) in locations X+16FH through X+173H with bit 7 of each register storing the value received in frame 2, bit 6 storing the value received in frame 4, etc. Received Sa6 is further processed for identifying specific codes and for counting specific codes if control bit ENRXNBR is set to a 1. Read to clear status bits S68, S6A, S6C, S6E and S6F (bits 0, 1, 2, 3 and 4) in register X+175H when set to a 1, indicates that either code 1000, 1010, 1100, 1110 or 1111 was received for three sub-multiframes in a row. Read to clear status bit S6X (bit 5) in register X+175H when set to a 1, indicates another code was received for three sub-multiframes in a row. Each time code 00X1 is received in a sub-multiframe, 10 bit Sa6 counter no. 1, SA61(9-0), with overflow indicator SA16O in locations X+179H and X+17AH is pegged; this code corresponds to a far end error from ISDN Terminal Equipment. Shadow register bits LSA61(9-0) and LSA61O are located at X+177H and X+178H providing a one-second latched view if control bit SRGEN (bit 3) in register 00BH is set to a 1. Each time code 001X is received in a sub-multiframe, 10 bit Sa6 counter no. 2, SA62(9-0), with overflow indicator SA26O in locations X+17DH and X+17EH is pegged; this code corresponds to a far end error from ISDN T Reference point. Shadow register bits LSA62(9-0) and LSA62O are located at X+17BH and X+17CH providing a one-second latched view if control bit SRGEN (bit 3) in register 00BH is set to a 1.

When control bit BNAL is a 1, all the National bits are transmitted from the signaling highway via a buffer. The microprocessor enables transmission of the National bits from the Code Registers XSA47-XSA40 through XSA87-XSA80 (in registers X+169H through X+16DH) by setting bits TSA4S-TSA8S (bits 4-0 in register X+E3H) to 0. Note that writing bits TSA4S-TSA8S with zeros does not freeze bits 4-0 in register X+B0H, which is the transmit slip buffer location for NFAS, therefor microprocessor writes of the Sa bits at register X+B0H are not possible, since these bits are continuously updated from the system side. This is the recommended method of fixing the Sa bits to a specific value per ITU-T G.704 when using the basic framed mode. When control bit BNAL is written with a 0, the transmitted path will be either via the data link or via the signaling highway through the buffer. The bandwidth of the HDLC channel is controlled by control bits SA4-SA8 (bits 4-0) in register X+0CH. A 1 written to one or more bits selects those bits as the HDLC channel. For example, if control bits SA4-SA7 are set with a 1, then bits Sa4 to Sa7 in Time Slot 0 will transmit the HDLC channel providing a 16 kbit/s data link. The Sa8 bit Time Slot 0 path will be from the signaling highway via the buffer. When a 1 is written to control bits SA4-SA8 and control bit BNAL is set to a 0, HDLC flag characters are continuously sent in the National bits selected regardless of the setting of control bit EHT (bit 7) in register X+126H. The operation of the HDLC controller is described in the HDLC Channel section below. The table below summarizes the National bit options (where X=don't care):

CRCMD1,0 X+07H:3,2	BNAL X+122H:5	TSA4/8S X+E3H:4/0	RSA4/8S X+3BH:4/0	SA4/8 X+0CH:4/0	National bit Actions
01	0	X	0	0	Selected National bits to E1 line from TNFAS (X+B0H) and received National bits not written to RNFAS (X+60H). Values in RNFAS sent to RTSIGn (Transmission Mode).
01	0	X	0	1	Selected National bits to E1 line from HDLC controller and received National bits not written to RNFAS (X+60H) but sent to HDLC controller. Values in RNFAS sent to RTSIGn (Transmission Mode).
01	0	X	1	0	Selected National bits to E1 line from TNFAS (X+B0H) and received National bits written to RNFAS (X+60H). Values from E1 line sent to RTSIGn (Transmission Mode).
01	0	X	1	1	Selected National bits to E1 line from HDLC controller and received National bits written to RNFAS (X+60H) and sent to HDLC controller. Values from E1 line sent to RTSIGn (Transmission Mode).
01	1	0	0	0	Selected National bits to E1 line from TNFAS (X+B0H) and received National bits not written to RNFAS (X+60H). Values in RNFAS sent to RTSIGn (Transmission Mode).
01	1	0	0	1	Selected National bits to E1 line from TNFAS (X+B0H) and received National bits not written to RNFAS (X+60H) but sent to the HDLC controller. Values in RNFAS sent to RTSIGn (Transmission Mode).
01	1	1	0	0	Selected National bits to E1 line from TTSIGn (Transmission Mode) and received National bits not written to RNFAS (X+60H). Values in RNFAS sent to RTSIGn (Transmission Mode).
01	1	1	0	1	Selected National bits to E1 line from TTSIGn (Transmission Mode) and received National bits not written to RNFAS (X+60H) but sent to HDLC controller. Values in RNFAS sent to RTSIGn (Transmission Mode).
01	1	0	1	0	Selected National bits to E1 line from Code Registers XSA47-XSA40 through XSA87-XSA80 (in registers X+169H through X+16DH) and received National bits written to RNFAS (X+60H). Values from E1 line sent to RTSIGn (Transmission Mode).
01	1	0	1	1	Selected National bits to E1 line from Code Registers XSA47-XSA40 through XSA87-XSA80 (in registers X+169H through X+16DH) and received National bits written to RNFAS (X+60H) and HDLC controller. Values from E1 line sent to RTSIGn (Transmission Mode).
01	1	1	1	0	Selected National bits to E1 line from TTSIGn (Transmission Mode) and received National bits written to RNFAS (X+60H). Values from E1 line sent to RTSIGn (Transmission Mode).

CRCMD1,0 X+07H:3,2	BNAL X+122H:5	TSA4/8S X+E3H:4/0	RSA4/8S X+3BH:4/0	SA4/8 X+0CH:4/0	National bit Actions
01	1	1	1	1	Selected National bits to E1 line from TTSIGn (Transmission Mode) and received National bits written to RNFAS (X+60H) and to HDLC controller. Values from E1 line sent to RTSIGn (Transmission Mode).
11 or X0	0	0	0	0	Selected National bits to E1 line from XSA4 - XSA8. Received National bits stored in RSA4 - RSA8 and Sa6 code detectors and counters enabled if ENRXNBR = 1. Received National bits not written to RNFAS (X+60H). Values in RNFAS sent to RTSIGn (Transmission Mode).
11 or X0	0	0	0	1	Selected National bits to E1 line from HDLC controller and received National bits not written to RNFAS (X+60H) but sent to HDLC controller. Values in RNFAS sent to RTSIGn (Transmission Mode). Received National bits stored in RSA4 - RSA8 and Sa6 code detectors and counters enabled if ENRXNBR = 1.
11 or X0	0	0	1	0	Selected National bits to E1 line from XSA4 - XSA8. Received National bits stored in RSA4 - RSA8 and Sa6 code detectors and counters enabled if ENRXNBR = 1. Received National bits written to RNFAS (X+60H). Values from E1 line sent to RTSIGn (Transmission Mode).
11 or X0	0	0	1	1	Selected National bits to E1 line from HDLC controller and received National bits written to RNFAS (X+60H) and sent to HDLC controller. Values from E1 line sent to RTSIGn (Transmission Mode). Received National bits stored in RSA4 - RSA8 and Sa6 code detectors and counters enabled if ENRXNBR = 1.
11 or X0	0	1	0	0	Selected National bits to E1 line from TNFAS (X+B0H). Received National bits stored in RSA4 - RSA8 and Sa6 code detectors and counters enabled if ENRXNBR = 1. Received National bits not written to RNFAS (X+60H). Values in RNFAS sent to RTSIGn (Transmission Mode).
11 or X0	0	1	0	1	Selected National bits to E1 line from HDLC controller and received National bits not written to RNFAS (X+60H) but sent to HDLC controller. Values in RNFAS sent to RTSIGn (Transmission Mode). Received National bits stored in RSA4 - RSA8 and Sa6 code detectors and counters enabled if ENRXNBR = 1.
11 or X0	0	1	1	0	Selected National bits to E1 line from TNFAS (X+B0H). Received National bits stored in RSA4 - RSA8 and Sa6 code detectors and counters enabled if ENRXNBR = 1. Received National bits written to RNFAS (X+60H). Values from E1 line sent to RTSIGn (Transmission Mode).

CRCMD1,0 X+07H:3,2	BNAL X+122H:5	TSA4/8S X+E3H:4/0	RSA4/8S X+3BH:4/0	SA4/8 X+0CH:4/0	National bit Actions
11 or X0	0	1	1	1	Selected National bits to E1 line from HDLC controller and received National bits written to RNFAS (X+60H) and sent to HDLC controller. Values from E1 line sent to RTSIGn (Transmission Mode). Received National bits stored in RSA4 - RSA8 and Sa6 code detectors and counters enabled if ENRXNBR = 1.
11 or X0	1	0	0	0	Selected National bits to E1 line from XSA4 - XSA8. Received National bits stored in RSA4 - RSA8 and Sa6 code detectors and counters enabled if ENRXNBR = 1. Received National bits not written to RNFAS (X+60H). Values in RNFAS sent to RTSIGn (Transmission Mode).
11 or X0	1	0	0	1	Selected National bits to E1 line from Code Registers XSA47-XSA40 through XSA87-XSA80 (in registers X+169H through X+16DH). Received National bits not written to RNFAS (X+60H) but sent to HDLC controller. Values in RNFAS sent to RTSIGn (Transmission Mode). Received National bits stored in RSA4 - RSA8 and Sa6 code detectors and counters enabled if ENRXNBR = 1.
11 or X0	1	0	1	0	Selected National bits to E1 line from XSA4 - XSA8. Received National bits stored in RSA4 - RSA8 and Sa6 code detectors and counters enabled if ENRXNBR = 1. Received National bits written to RNFAS (X+60H). Values from E1 line sent to RTSIGn (Transmission Mode).
11 or X0	1	0	1	1	Selected National bits to E1 line from HDLC controller. Received National bits written to RNFAS (X+60H) and sent to HDLC controller. Values from E1 line sent to RTSIGn (Transmission Mode). Received National bits stored in RSA4 - RSA8 and Sa6 code detectors and counters enabled if ENRXNBR = 1.
11 or X0	1	1	0	0	Selected National bits to E1 line from TNFAS (X+B0H). Received National bits stored in RSA4 - RSA8 and Sa6 code detectors and counters enabled if ENRXNBR = 1. Received National bits not written to RNFAS (X+60H). Values in RNFAS sent to RTSIGn (Transmission Mode).
11 or X0	1	1	0	1	Selected National bits to E1 line from TFNAS (X+B0H). Received National bits not written to RNFAS (X+60H) but sent to HDLC controller. Values in RNFAS sent to RTSIGn (Transmission Mode). Received National bits stored in RSA4 - RSA8 and Sa6 code detectors and counters enabled if ENRXNBR = 1.

CRCMD1,0 X+07H:3,2	BNAL X+122H:5	TSA4/8S X+E3H:4/0	RSA4/8S X+3BH:4/0	SA4/8 X+0CH:4/0	National bit Actions
11 or X0	1	1	1	0	Selected National bits to E1 line from TNFAS (X+B0H). Received National bits stored in RSA4 - RSA8 and Sa6 code detectors and counters enabled if ENRXNBR = 1. Received National bits written to RNFAS (X+60H). Values from E1 line sent to RTSIGn (Transmission Mode).
11 or X0	1	1	1	1	Selected National bits to E1 line TFNAS (X+B0H). Received National bits written to RNFAS (X+60H) and sent to HDLC controller. Values from E1 line sent to RTSIGn (Transmission Mode). Received National bits stored in RSA4 - RSA8 and Sa6 code detectors and counters enabled if ENRXNBR = 1.

Fast Sync Mode

The E1Fx8 provides a fast sync mode which may be used for testing purposes. The fast sync mode for the receiver side is selected when control bit RXFS (bit 1) in register X+1FFH is written with a 1 in the NRZ mode and the RNEGn/RSCANn is not being used for LOS input or counting Code Violations (see Line Interface Selection above). A positive pulse on lead RSCANn that is one clock cycle wide in bit position 256 of the last frame in the CRC-4 multiframe forces the framer into synchronization. It can occur repetitively at 2 ms intervals, or it can be pulsed once provided the received framing sequence is valid afterwards.

The fast sync mode for the transmitter side is selected when control bit TDFME (bit 7) in register X+07H is written with a 1 in the NRZ mode and TNEGn/TDRVn is not being used as a drive bit (see Line Interface Selection above). The TDRVn output in this mode is a one clock cycle wide pulse in bit position 256 of the last frame in the CRC-4 multiframe that occurs every 2 ms if control bit TLMF (bit 5) in register X+07H is set to a 1; if TLMF is set to a 0, a pulse occurs in bit position 256 of every frame providing a 125 µs signal. This allows an external device to be synchronized to the E1Fx8.

SLIP BUFFERS

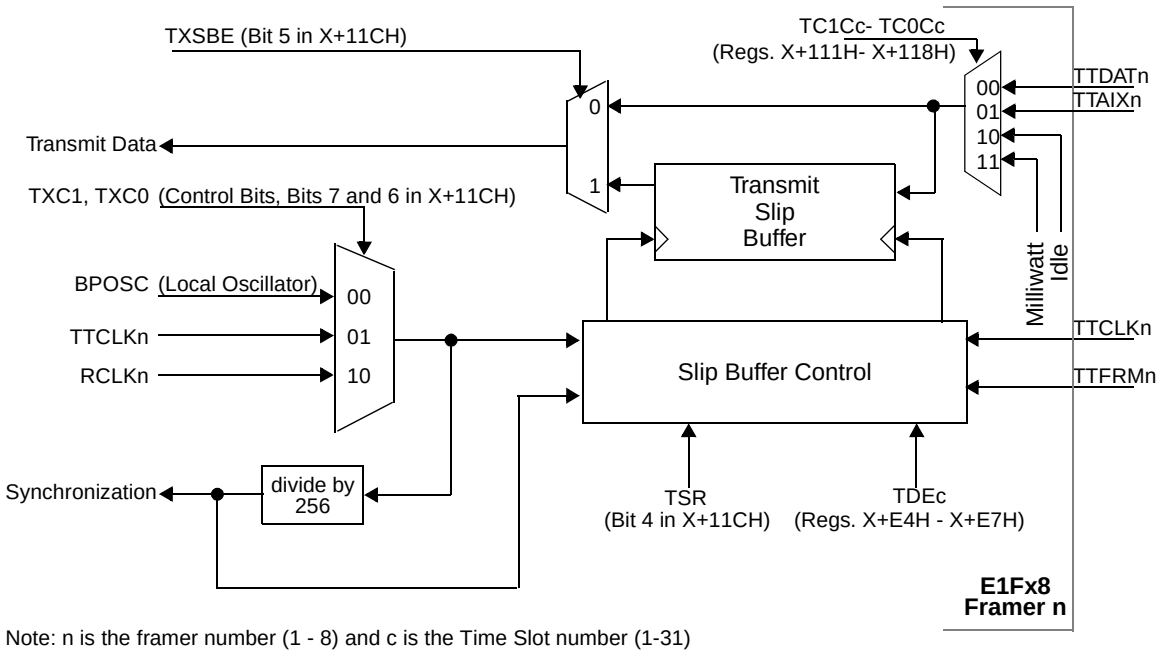
The Time Slots 1-15 and 17-31 are inserted into the transmitted frame from the transmit slip buffer when it is enabled, or directly from the data highway, leads TTDATn and TTAIXn when it is bypassed (2 Mbit/s Transmission Mode and Data Mode only). Likewise, Time Slots 1-15 and 17-31 received from the E1 line are written to the receive slip buffer when it is enabled or directly to the data highway, lead RTDATn when it is bypassed. Time Slot 16 is treated like the other Time Slots in reception from the E1 line, being slip buffered, if selected, and placed on RTDATn. The transmitted Time Slot 16 is treated like the other Time Slots and taken from the transmit slip buffer or directly from TTDATn or TTAIXn if CCS signaling is selected (control bits TYP1 and TYP0 in register X+134H are both set to 0). Time Slot 16 is generated by the framer if CAS signaling is selected (control bits TYP1 and TYP0 in register X+134H are not both set to 0). The transmit slip buffer locations are registers X+91H - X+AFH (frame 1) and X+B1H - X+CFH (frame 2). Locations X+90H and X+B0H contain TFAS and TNFAS as described above. The receive slip buffer locations are registers X+41H - X+5FH (frame 1) and X+61H - X+7FH (frame 2). Locations X+40H and X+60H contain RFAS and RNFAS as described above. An individual transmit time slot in the buffer can be frozen by writing a 0 to one or more control bits TDE1 - TDE31 in registers X+E4H - X+E7H; data from the data highways will no longer be written to the selected time slot(s) but the contents of the transmit slip buffer will still be output to the E1 line. An individual receive time slot in the buffer can be frozen by writing a 0 to one or more control bits RDE1 - RDE31 in registers X+3CH - X+3FH; data from the E1 line will no longer be written to the selected time slot(s) but the contents of the receive slip buffer will still be output to the data highway. The individual time slots in both frames can be accessed by the microprocessor, as well as written by the microprocessor in place of data. This permits the microprocessor to write idle or service codes for one or more framer time slots. Please note that both buffer locations (i.e., frame 1 and frame 2) must be written.

Each framer contains a two-frame slip buffer in both the transmit and receive data directions. Either of the slip buffers can be bypassed, if required, in the Transmission and Data Modes only. The slip buffers must be enabled in the MVIP and H-MVIP/H.100 Modes. Both the transmit and receive data time slots (1-15 & 17-31 plus 16 for CCS) and the framing time slots (Time Slot 0) are passed through the slip buffers. The signaling states are buffered in a separate memory location and are not subjected to slips. Each buffer is organized as a circular queue two frames in length. If data is arriving faster than it is being removed, the buffer will begin to fill. Before the buffer becomes totally full, a controlled slip will occur and one frame of data will be discarded. This is accomplished by moving the write pointer back one frame and overwriting the previous frame that was written. If the data is being removed faster than it is arriving, the buffer will begin to empty. Before the buffer becomes completely empty, a controlled slip occurs in the opposite direction, and a frame of data is added to the buffer. This is accomplished by moving the read pointer back one frame and repeating the last frame read. The Transmit or Receive slip buffer may be manually toggled by setting the TSR or RSR control bits (bits 4) in control registers X+11CH and X+11BH to a 1, respectively. Manual toggling may be used to control delay.

The transmit slip buffer is used to absorb low speed jitter in the transmit direction. The transmit slip buffer is enabled by writing a 1 to control bit TXSBE (bit 5) in control register X+11CH. When enabled, time slots are written into the transmit slip buffer by the system clock (TTCLKn), and read out by the recovered receive clock (RCLKn), the system clock (TTCLKn), or the local oscillator (BPOSC). Control bits TXC1 and TXC0 (bits 7 and 6) in register X+11CH select the clock source. The time slots (c = 1-31) from the transmit data bus (TTDATn and /or TTAIXn) are written into the slip buffer when their respective enable bits (TDEc) in registers X+E4H, X+E5H, X+E6H and X+E7H are written with a 1.

If a phase shift between the two clocks is detected, a deletion or repetition of one frame of data occurs by the buffer reaching an almost full or almost empty threshold. A transmit slip is indicated by status bit SLIP (bit 1) in register X+10H. An associated mask bit MSLIP, a latched event bit LSLIP, a performance value PSLIP and a fault value FSLIP are all bit 1 in registers X+14H, X+11H, X+12H and X+13H, respectively. The transmit slip buffer detailed status is indicated by reading status bits TXS1 and TXS0 (bits 7 and 6) in register X+16H, which indicate if a slip has occurred and if it is a repetition, deletion or error. Since the SLIP status bit is shared with the receive slip buffer, when both slip buffers are enabled the status bits RXS1 and RXS0 (bits 7 and 6) in register X+15H should also be read. A simplified schematic of the transmit slip buffer is shown in Figure 50.

Shutting off the BPOSC and TTCLKn or RTCLKn clock signals should be avoided when the slip buffers are enabled in the MVIP and H-MVIP/H.100 modes since otherwise a constant slip error may result even after the clocks are restored. If this cannot be avoided, then a software reset for that channel should be generated to ensure clearance of the slip error, when the same condition is detected, and the value of the transmit/receive delay register is close to zero (less than 5).



Note: n is the framer number (1 - 8) and c is the Time Slot number (1-31)

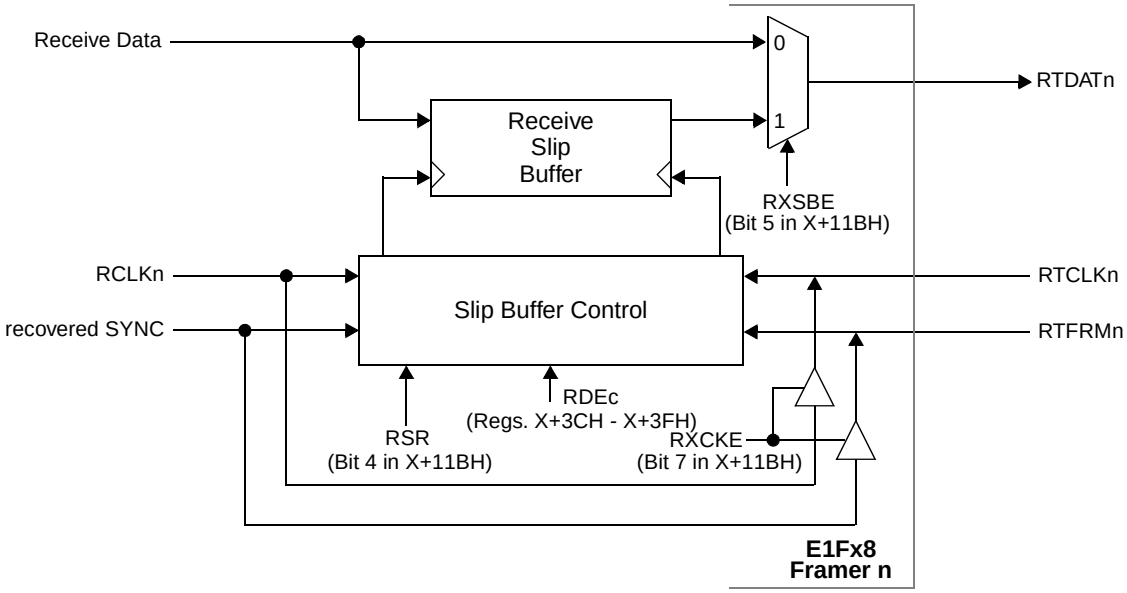
Figure 50. Transmit Slip Buffer

The receive slip buffer is typically used when the receive system clock (RTCLKn) is provided from an external source which is accomplished by setting control bit RXCKE (bit 7) in register X+11BH to a 0 and control bit RXSBE (bit 5) in the same register to a 1. The receive slip buffer controls the time slot access and retiming, providing a two-frame buffer that is optionally bypassable in the Transmission and Data Modes only. The slip buffer must be enabled in MVIP and H-MVIP/H.100 Modes. Time slots from the line interface are written into the slip buffer by the recovered receive clock (RCLKn), and read out by the system clock (RTCLKn). If a phase shift between the two clocks is detected, a deletion or repetition of one frame of data occurs by the buffer reaching an almost full or almost empty threshold, respectively. The time slots (c = 1 - 31) from the receive line signal are written into the slip buffer when their respective enable bits (RDEc) in registers X+3CH, X+3DH, X+3EH and X+3FH are written with a 1. RSIS and RSA4S-RSA8S in register X+3BH for Time Slot 0 are written with a 1 control the National and International bits as described above.

Individual time slots can be accessed by the microprocessor, and they can be written by the microprocessor in place of data. When a time slot enable control bit RDEc in register locations X+3CH-X+3FH is written with a 0, the content of the two-frame slip buffer location is frozen for that time slot. The microprocessor can write an idle, code word or service code in the location that will be transmitted to the receive data highway. The receive slip buffer data locations RTS1-RTS31 are X+41H (Time Slot 1) to X+5FH (Time Slot 31) for frame 1, and X+61H (Time Slot 1) to X+7FH (Time Slot 31) for frame 2. The receive Time Slot 0 for FAS frames and NFAS frame are located at X+40H and X+60H respectively. Please note that both buffer locations (i.e., frame 1 and frame 2) must be written. A simplified schematic of the receive slip buffer is shown in Figure 51.

A receive slip is indicated by status bit SLIP (bit 1) in register X+10H which is shared with the transmit slip as described above. The receive slip buffer status is indicated by reading status bits RXS1 and RXS0 (bits 7 and 6) in register X+15H which indicate if a slip has occurred and if it is a repetition, deletion or error. Since the

SLIP status bit is shared with the transmit slip buffer, when both slip buffers are enabled the status bits TXS1 and TXS0 (bits 7 and 6) in register X+16H should also be read.



Note: n is the framer number (1 - 8) and c is the Time Slot number (1 - 31)

Figure 51. Receive Slip Buffer

The receive slip buffer has its read and write pointers available in register X+20H through X+23H and the transmit slip buffer has its read and write pointers available in registers X+26H through X+29H. In addition, delay values are available. The value present in status registers RXSBD8 (bit 6) at location X+23H and RXSBD7 - RXSBD0 at location X+24H represents the difference between the receive slip buffer write pointer and read pointer yielding a delay value in increments of 1 bit. This delay value can be read periodically to determine the frequency offset between RCLKn and RTCLKn. The value present in status register TXSBD7-TXSBD0 at location X+25H and TXSBD8 (bit 6) in register X+29H represents the difference between the transmit slip buffer write pointer and read pointer, yielding a delay value in increments of 1 bits.

Slip Buffering Unframed Signals (Transmission or Data Mode only)

When control bit TTFM (bit 6) in register X+01H is set to a 1 and TXSBE (bit 5) in register X+11CH is set to a 1, the transmit slip buffer is operating on all 256 bits of data present on TTDATn every 125 microseconds, and they are passed unaltered (except for the coder function) to the transmit line side, without frame bits or signaling bits being inserted. TTFRMn, TTSIGn and TTAIXn inputs are ignored. Slips caused by clock differences between TTCLKn and the transmit line clock source (RCLKn or BPOSC) will be implemented by a repeat or skip of 256 bits, not the payload (Time Slots 1-15 and 17-31 plus 16 for CCS) as is done when TTFM is set to a 0.

When control bit RTFM (bit 7) in register X+01H is set to a 1 and RXSBE (bit 5) in register X+11BH is set to a 1, the receive slip buffer is operating on all 256 bits received from the line and no attempt is made to find frame alignment. The data on RTDATn is unaltered data from the received line except for the decoder function if enabled. Data on RTSIGn and RTFRMn is to be ignored. Slips caused by clock differences between RCLKn and RTCLKn will be implemented by a repeat or skip of all 256 bits, not the payload (Time Slots 1 - 15 and 17 - 31 plus 16 for CCS) as is done when RTFM is set to a 0. Control bit TS0FZ (bit 5) in register X+134H must be set to a 1 to permit Time Slot 0 to be treated as a telephone channel and slip buffered as Time Slots 1 - 31.

DELAY

Delay through the E1Fx8 is a function mainly of the slip buffers, though other factors also influence the amount of delay. The table below gives the typical delay through the framer from line to system and from system to line. The delay numbers are with the slip buffers disabled. The total delay with the slip buffers enabled can be estimated by adding the slip buffer delay (8 to 378, see Notes 1 and 2). All numbers are in bit times for a clock rate of 2048 kHz.

Direction of Signal Flow	RXCP/ TXCP	Overall Delay	
		NRZ	AMI/HDB3
RPOSn/RNRZn to RTDATn	RXCP=0	8	12.5
	RXCP=1	7	11
TTDATn/TTAIXn to TPOSn/TNRZn	TXCP=0	5	9
	TXCP=1	4.5	8.5

Note 1: When the framer is reset, the nominal delay is 128 bits through the slip buffer. Recenter (control bit RSR or TSR toggled) will cause a slip.

Note 2: The actual delay value in bits may be determined by reading the value from registers X+24H and bit 6 of X+23H (receive slip buffer) or registers X+25H and bit 6 of X+29H (transmit slip buffer).

SIGNALING

There are two types of signaling schemes used for the E1 telephone channels: Common Channel Signaling (CCS), and Channel Associated Signaling (CAS). Common Channel Signaling, such as CCS No. 7 or ISDN D channel, can be assigned to be carried in one or more of the time slots, including Time Slot 16. The E1Fx8 does not process any part of the Common Channel Signaling format. Instead, it is passed transparently through the system to the data bus. The clear channel capability for Time Slot 16 is selected when control bits TYP1 and TYP0 (bits 7 and 6) in register X+134H are written with 00. Time Slot 16 for CCS applications may also be switched via the Auxiliary Port where it can be processed by a device such as the TranSwitch MCHDLC VLSI device.

Time Slot 16 may be used to carry Channel Associated Signaling. The Channel Associated Signaling feature is selected when control bits TYP1 and TYP0 (bits 7 and 6) in register X+134H are written with a value other than 00. The signaling information is carried as ABCD signaling bits that are associated with Time Slots 1 through 15, and 17 through 31. A sixteen-frame format, referred to as a signaling multiframe, is used to carry the signaling information. Please note that the signaling multiframe may be received arbitrarily with respect to the multiframe structure carried in Time Slot 0. However, Time Slot 0 multiframe and Time Slot 16 multiframe are synchronized for transmission. The following table shows the signaling multiframe structure for Time Slot 16.

Frame	Bit 1	2	3	4	5	6	7	8
0	0	0	0	0	X0	Y	X1	X2
1	A1	B1	C1	D1	A16	B16	C16	D16
2	A2	B2	C2	D2	A17	B17	C17	D17
3	A3	B3	C3	D3	A18	B18	C18	D18
4	A4	B4	C4	D4	A19	B19	C19	D19
5	A5	B5	C5	D5	A20	B20	C20	D20

Frame	Bit 1	2	3	4	5	6	7	8
6	A6	B6	C6	D6	A21	B21	C21	D21
7	A7	B7	C7	D7	A22	B22	C22	D22
8	A8	B8	C8	D8	A23	B23	C23	D23
9	A9	B9	C9	D9	A24	B24	C24	D24
10	A10	B10	C10	D10	A25	B25	C25	D25
11	A11	B11	C11	D11	A26	B26	C26	D26
12	A12	B12	C12	D12	A27	B27	C27	D27
13	A13	B13	C13	D13	A28	B28	C28	D28
14	A14	B14	C14	D14	A29	B29	C29	D29
15	A15	B15	C15	D15	A30	B30	C30	D30

Where: Ac Bc Cc Dc represents the signaling information associated with the telephone channel number (c = 1-30). Channel 1 corresponds to Time Slot 1, while channel 16 corresponds to Time Slot 17, since Time Slot 16 is assigned to carry the signaling information.

The Y-bit is used for a multiframe alarm indication. A 1 indicates an alarm.

The X0, X1 and X2 spare bits are not used, and are normally set to 1.

Channel Associated Signaling Multiframe Alignment

Time Slot 16 may be assigned for Channel Associated Signaling or as a clear channel. Different modes of Channel Associated Signaling are selected when control bits TYP1 and TYP0 (bits 7 and 6) in register X+134H are equal to 01, 10, or 11. When control bits TYP1 and TYP0 are equal to 00, Time Slot 16 is designated as a clear channel, and the transmitted path is from the data highway as described above. The selection is common for the receive side of the same framer.

The E1Fx8 supports two CAS multiframe alignment operating modes for each framer: Standard, or Enhanced. The Standard algorithm is selected by writing a 0 to control bit CASA (bit 4) in register X+01H. The Enhanced algorithm is selected when a 1 is written to the control bit CASA. The Standard multiframe alignment algorithm is compatible with ITU-T Recommendation G.732. Standard Channel Associated Signaling multiframe alignment is declared when the E1Fx8 detects a 0000 pattern in bits 1 to 4 in Time Slot 16 and this was preceded by a Time Slot 16 with a non-zero pattern in bits 1-4. For the Enhanced algorithm, multiframe alignment is declared only when the 0000 pattern is found after the previous 15 frames contained a Time Slot 16 that did not carry the 0000 pattern in bits 1-4.

The status bit TS16ME (bit 4) in register X+18H is assigned for a multiframe error indication for each framer. A 1 indicates that an error was detected in the 0000 multiframe alignment pattern (bits 1-4 of Time Slot 16 frame 0). When a 1 is written to control bit EOO16M (bit 1) in register X+03H, a loss of Time Slot 16 multiframe indication is set when any of the following conditions occurs:

- The 4-bit all zero pattern (bits 1-4) In Time Slot 16 is lost for two consecutive multiframes.
- Time Slot 16 is all zeros for 16 consecutive frames.
- Basic frame alignment is lost (OOF alarm)

The Time Slot 16 loss of multiframe alarm status bit OO16M (bit 2) is in register X+164H. An associated mask bit MOO16M, a latched event bit LOO16M, a performance value POO16M and a fault value FOO16M are all bit

2 in registers X+166H, X+165H, X+167H and X+168H, respectively. When control bit TS16EIC (bit 0) in register X+00H is set to a 1, status bit OOFM will also indicate the alarm. When control bit AUTY (bit 0) in register X+08H is set to a 1, a loss of Time Slot 16 multiframe causes the transmitted Time Slot 16 Y-bit (bit 6 of Time Slot 16 frame 0) to be set to a 1.

Time Slot 16 AIS is detected by receiving three or less zeros in each of two consecutive Time Slot 16 multiframe periods. If control bit E16AIS (bit 0) in register X+05H is set to a 1, status bit AIS16 (bit 6) in register X+164H will indicate Time Slot 16 AIS. An associated mask bit MAIS16, a latched event bit LAIS16, a performance value PAIS16 and a fault value FAIS16 are all bit 6 in registers X+166H, X+165H, X+167H and X+168H, respectively. When control bit TS16EIC (bit 0) in register X+00H is set to a 1, status bit AIS will also indicate the alarm.

Time Slot 16 RAI is detected if three consecutive received Y-bits (bit 6 of Time Slot 16 frame 0) are set to a 1. If control bit ENRAIY (bit 0) in register X+04H is set to a 1, status bit RAI16 (bit 4) in register X+164H will indicate Time Slot 16 RAI. An associated mask bit MRAI16, a latched event bit LRAI16, a performance value PRAI16 and a fault value FRAI16 are all bit 4 in registers X+166H, X+165H, X+167H and X+168H, respectively. When control bit TS16EIC (bit 0) in register X+00H is set to a 1, status bit RAI will also indicate the alarm.

Channel Associated Signaling is inserted into Time Slot 16 of the transmitted frame from the signaling highway via buffer locations. The buffer location for reading the multiframe pattern, spare bits, and multiframe alarm is register X+D0H. The buffer locations for the ABCD bits of the signaling channels are registers X+D1H through X+DEH. All signaling states (i.e., all 30 ABCD signaling bits) can be frozen by writing a 1 to control bit TXSFZ (bit 0) in register X+134H. The contents of an individual signaling nibble in buffer locations X+D1H through X+DEH can also be frozen by writing a 0 to one or more of control bits TSE1-TSE30 in registers X+ECH-X+EFH. When a signaling a nibble is frozen, the transmitted signaling state is the value sitting in the buffer at the time bit TSEc was set to 0. The microprocessor can write a new signaling state, or a service code, for the frozen nibble to effect trunk conditioning or originate signaling control, for example.

Frame 0 in the 16-frame multiframe carries the 4-bit multiframe pattern, 3 spare bits, and the remote multiframe alarm (RAI) in the Y-bit. The E1Fx8 regenerates the 4-bit multiframe alignment pattern. The spare and Y-bits from the signaling highway can be read by the microprocessor in register X+D0H (bits 3-0). The Y-bit can be set if the receiver detects a Time Slot 16 out of multiframe alignment as described above. The microprocessor can also generate a remote multiframe alarm by writing a 1 to control bit TS16YE (bit 5) in register X06H. The 3 spare bits, X0, X1 and X2, may be taken from the signaling highway in Transmission Mode if control bits TX0S, TX1S and TX2S (bits 0, 1 and 2) in register X+E2H are set to a 1. When TX0S, TX1S and TX2S are set to 0, the values stored in location X+D0H (bits 3, 1 and 0).

Time Slot 16 AIS may be inserted as all ones in Time Slot 16 (including the multiframe pattern in frame 0) by setting control bit TAIS16 (bit 1) in register X+07H to a 1.

The following table, which is common to both the receive and transmit sections, lists the states for signaling.

TYP1	TYP0	Signaling Type
0	0	Time Slot 16 is assigned as a clear channel (CCS).
0	1	Time Slot 16 assigned for CAS. ABCD signaling bits from transmit signaling buffer and to receive signaling buffer. If ABCD = 0000 from the transmit signaling highway or stored in the transmit signaling buffer (evaluated after the TSINV function), the value is replaced by ABCD = 1111 to prevent mimics of the Time Slot 16 multiframe alignment pattern.
1	0	Time Slot 16 assigned for CAS. ABCD signaling bits from transmit signaling buffer and to receive signaling buffer.
1	1	Not used.

Receive Signaling Buffers

The receive signaling buffers that are used to interface the E1Fx8 to the system are 360 bits in length. The transmit signaling buffers that are used to interface the E1Fx8 to the system are 120 bits in length. In the receive direction, the signaling bits are extracted from the data stream and placed in the receive signaling buffer after Time Slot 16 multiframe alignment is detected as described above. Three storage locations are provided for each signaling bit received to permit signaling debouncing to be accomplished under control of control bit SIGDB (bit 4) in register X+134H. A simplified schematic of the receive signaling buffer is shown in Figure 52. In the Transmission Mode, eight signaling bits are sent each frame, and all signaling states are sent over the 16 frames. Receive signaling bits are clocked out by the system clock (RTCLKn), which is sourced by either the system interface or the E1Fx8. These bits can be extracted using the receive synchronization signal RTFRMn. In the Data, MVIP and H-MVIP/H.100 Modes, all the signaling bits are sent for every time slot every frame (125 microseconds) from the receive signaling buffer by using the system clock (RTCLKn) and sync pulse (RTFRMn).

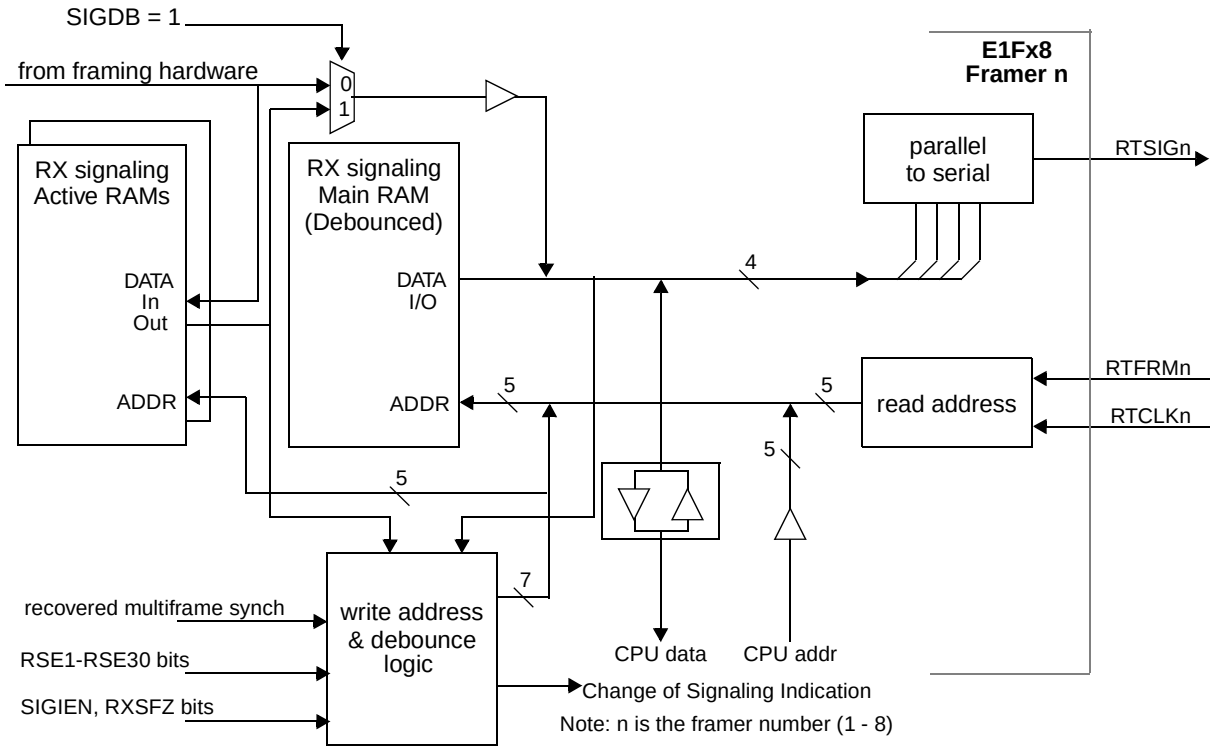


Figure 52. Receive Signaling Buffer

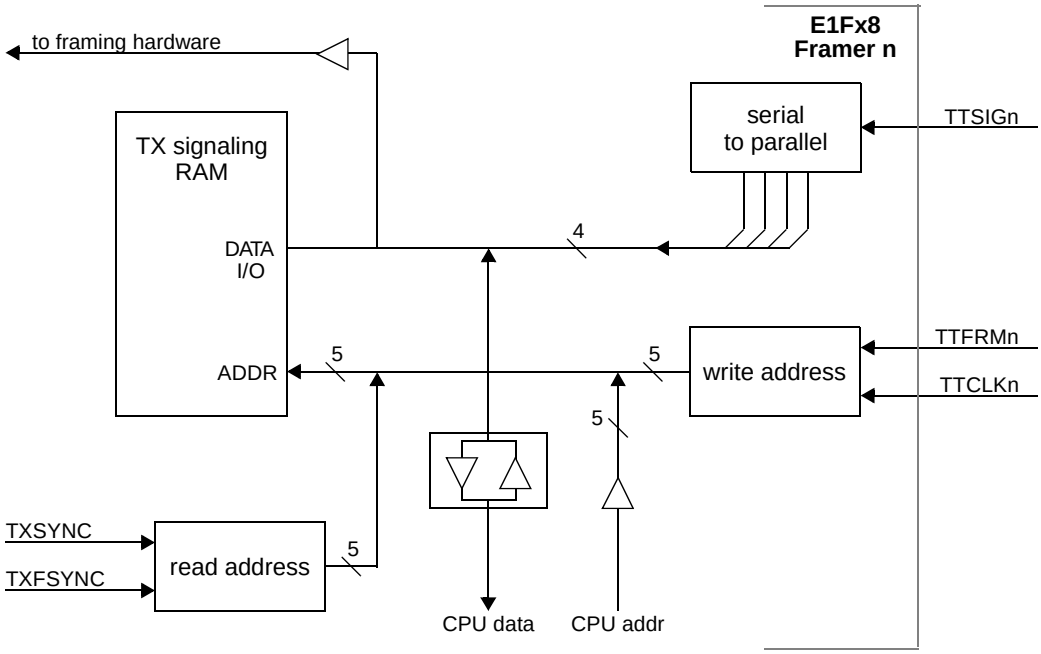
The received signaling bits are stored sequentially in the receive signaling buffer in the order they are received. Two temporary RAMs are provided at locations X+138H through X+146H for RAM 1 and X+148H through X+156H for RAM 2. Signaling RAM 1 contains the current value and signaling RAM 2 keeps a count of the number of frames the current value and the just received value match. The signaling bits in the receive main or debounced signaling buffer (register locations X+81H through X+8FH) may be read at any time by the microprocessor in order to monitor the signaling states, or written to modify the outgoing values. When signaling debounce is used, the signaling bits are enabled to be stored by control bits RSE1-RSE30 in registers X+E8H through X+EBH and are written to the Active RAM 1 first. If the just received signaling nibble matches the value in RAM 1, RAM 2 for that location is incremented. If the just received signaling nibble does not match the value stored in RAM 1 for a specific location, the associated RAM 2 location is cleared to 0H. When the value stored in a specific location of RAM 2 is equal to or exceeds that value written into DEBVAL(3-0) (bits 3-0) of register 0FEH, the signaling nibble for that specific location is transferred from RAM 1 to the main signaling

buffer; this value is used to output on the signaling highway or to be read by the microprocessor. For test purposes both Active RAMs are also available to the microprocessor, which is not shown in Figure 52.

Since the buffer is accessed by multiple asynchronous processes, the read and write cycles for the signaling buffer are synchronized to the internal clocks. Simultaneous accesses are serviced sequentially. The priority of service depends on the amount of latency acceptable between when the request was received and when the data is required to be available. When the signaling debounce is enabled (SIGDB = 1), updates by the microprocessor should be preceded by a signaling freeze by setting control bit RXSFZ (bit 1) in register X+134H to a 1, which will prevent a debounced value from overwriting the microprocessor value. When a 0 is written into control bit RSEc, the signaling buffer for time slot c signaling is frozen. The frozen states will be sent on the signaling highway until the RSEc bit is written with a 1 or the microprocessor writes a new signaling value to the Main RAM. The signaling bits in the receive direction are automatically frozen in their present states when loss of signal or loss of synchronization occurs (LOS, AIS, OOF or OOF16M). A signaling freeze may also be initiated manually by writing a 1 to control bit RXSFZ. A receive signaling freeze indication is given by unlatched status bit RXSF (bit 1) in register X+17H.

Transmit Signaling Buffers

A simplified schematic of the transmit signaling buffer is shown in Figure 53. Transmit signaling bits on the signaling lead TTSIGn are clocked into the transmit signaling buffer using the transmit system clock TTCLKn and sync pulse TTFRMn. In the Transmission Mode, four signaling bits are provided each frame. In the Data, MVIP and H-MVIP/H.100 Modes, all signaling bits are written to the TX signaling RAM for every channel every other frame (250 microseconds). However, signaling on the signaling highway must be provided every frame.



Note: n is the framer number (1 - 8)

Figure 53. Transmit Signaling Buffer

The transmit signaling bits from the signaling highway are stored sequentially in the transmit signaling buffer in the order they are received. The signaling bits in the transmit signaling buffer (register locations X+D1H through X+DFH) may be read at any time by the microprocessor in order to monitor the signaling states, or written to modify the outgoing values. Since the buffer is accessed by multiple asynchronous processes, the read and write cycles for the signaling buffer are synchronized to the internal clocks. Simultaneous accesses are serviced sequentially. The priority of service depends on the amount of latency acceptable between when the request was received and when the data is required to be available. When the corresponding signaling

enable bits TSE1- TSE30 in register locations X+ECH (telephone channels 1-8), X+EDH (telephone channels 9 - 16), X+EEH (telephone channels 17 - 24) and X+EFH (telephone channels 25-30) are written with a 1, the signaling bits are written into the transmit signaling buffer. For example, a 1 written to control bit TSEc enables the signaling bits from the signaling highway for time slot c to be written into the signaling buffer. When a 0 is written into control bit TSEc, the signaling buffer for time slot c signaling is frozen. The frozen states will be transmitted until the TSEc bit is written with a 1 or the microprocessor writes a new signaling value.

A transmit signaling freeze indication occurs when control bit TXSFZ (bit 0) in register X+134H is written with a 1 (manual freeze). A transmit signaling freeze indication is given by status bit TXSF (bit 0) in register X+17H.

Signaling Change of State Interrupt

A change of signaling state indication and associated interrupt is provided if control bit SIGIEN (bit 3) in register X+134H is set to a 1. This feature operates on the receive signaling data as is referenced in Figure 52. This feature should only be used with signaling debounce in situations where rotary dial addressing is not expected. When SIGIEN is set to a 1 any change in any signaling bit is detected and status bit SCHG (bit 0) in register X+10H will be set to a 1 momentarily. An associated mask bit MSCHG, a latched event bit LSCHG, a performance value PSCHG and a fault value FSCHG are all bit 0 in registers X+14H, X+11H, X+12H and X+13H, respectively.

Signaling Nibble Substitution for AIS and RAI

When line side or system side alarms are present, specific signaling codes may be substituted for the signaling ABCD nibbles normally used. When control bit RX0AISE (bit 7) in register X+03H is set to a 1 and E1 AIS, LOS or OOF is detected and enabled by control bits ENAIS, ENLOOF and ENLOS (bits 7-5) in register X+02H, all the signaling nibbles on signaling highway, RTSIGn, are replaced with a code written to CODEAIS (bits 3-0) in register 02CH. CODEAIS may be forced to the signaling highway signaling nibbles by setting RT0AIS (bit 6) in register X+03H to a 1. This feature may be used to meet ITU-T G.732 requirement on the detection of excessive bit error rate as calculated by framing word error counts (see LFBE0 - LFBE9) by setting CODEAIS to FH and setting RT0AIS to a 1 on excessive BER.

Likewise, if RAI from the E1 line is detected and control bit RX0RAI (bit 5) in register X+03H is set to a 1, all the signaling nibbles on the signaling highway, RTSIGn, are replaced with a code written to CODERAI (bits 7-4) in register 02CH. CODERAI may be forced to the signaling highway signaling nibbles by setting RT0RAI (bit 4) in register X+03H to a 1.

If AIS is detected on the signaling highway (in Transmission Mode only) by having the “A” bits set to 1, if control bit TX0AISE (bit 1) in register X+06H is set to a 1 and control bit EXTAIS (bit 5) in register X+06H is set to a 0, only Time Slot 16 signaling nibbles transmitted to the E1 line are affected by being replaced with CODEAIS (bits 3-0) in register 02CH. CODEAIS may be forced on Time Slot 16 signaling nibbles transmitted to the E1 line by setting control bit ST0AIS (bit 0) in register X+06H to a 1.

CLOCKING AND SYNCHRONIZATION

The clocking and synchronization portion of the E1Fx8 includes the receive clock configuration, transmit clock synchronization, and the slip buffers for each of the framers. The following table provides a summary of the RTCLKn clock operation in the receive direction.

Interface Mode	Clock Rate	Sync Edge In	Data/Sig Edge Out	Comments
Transmission	2.048 MHz	Pos.	Neg.	Clock and sync pulse may be outputs* in which RTCLKn clock is derived from the recovered received clock (RCLKn).
MVIP	2.048 MHz	Pos.	Pos.	System clock and sync pulse must be inputs.
Data	2.048 MHz	Pos.	Neg.	Clock and sync pulse may be outputs* in which RTCLKn clock is derived from the recovered received clock (RCLKn).
H-MVIP/H.100	16.384 MHz	Pos.	Neg.	System clock and sync pulse must be inputs.

* Note: Control bit RXCKE (bit 7) in register X+11BH configures RTCLKn as an input or output for each of the framers. In the MVIP and H-MVIP/H.100 Modes, the system clock must be an input.

In the transmit direction, the system clock TTCLKn and sync pulse TTFRMn are always inputs to the E1Fx8. The transmit data input on TTDATn or TTAIXn is clocked out of the slip buffer by either the transmit system clock (TTCLKn), the local oscillator input (BPOSC), or the recovered receive clock (RCLKn). The clock selection for each framer is controlled by TXC1 (bit 7), and TXC0 (bit 6) in Framer Clock Control Register X+11CH. The local oscillator input (lead BPOSC) has a nominal frequency of 2.048 MHz and should be accurate to ± 50 ppm. BPOSC is the source for the RCLKn output when RXCKE = 1 and LOS is detected.

The following table provides a summary of the TTCLKn clock operation in the transmit direction.

Interface Mode	Clock Rate	Sync Edge In	Data/Sig Edge In	Comments
Transmission	2.048 MHz	Pos.	Pos.	System clock and sync pulse must be inputs.
MVIP	2.048 MHz	Pos.	Neg.	System clock and sync pulse must be inputs.
Data	2.048 MHz	Pos.	Pos.	System clock and sync pulse must be inputs.
H-MVIP/H.100	16.384 MHz	Pos.	Pos.	System clock and sync pulse must be inputs.

Clock Reference

For system applications that require the recovered receive clock, the E1Fx8 can provide two reference clocks derived from any of the eight clock inputs (RCLKn), when enabled. The recovered receive clock input RCLKn that is used to derive the reference clock SCOUT1 is determined by the value written to control bits S1YNC2 - S1YNC0 (bits 2, 1 and 0) in register 024H. The recovered receive clock that is used to derive the reference clock SCOUT2 is determined by the value written to control bits S2YNC2 - S2YNC0 (bits 2, 1 and 0) in register 025H. The following table lists the various conditions for enabling/disabling the clock reference signal on the SCOUT1 and SCOUT2 leads. The loss of signal condition can be internally detected in Dual Unipolar mode when control bit RAIL (bit 7) in register X+00H is set to a 1 or it can be enabled in the NRZ mode through the RSCANn input lead as described in the Line Interface Selection Section above. The S1CTRI, S2CTRI, S18KHZ and S28KHZ control bits are located in registers 024H and 025H.

S1CTRI S2CTRI	LOS(n) (Alarm)	S1YNCEN S2YNCEN	S18KHZ S28KHZ	Action
1	X	X	X	SCOUT1/SCOUT2 lead tristated.
0	0	0	1	8 kHz Reference provided on SCOUT1/SCOUT2. The 8 kHz signal is derived from the recovered clock that is selected (RCLKn) by control bits S1YNC2 - S1YNC0/S2YNC2 - S2YNC0.
0	0	0	0	2048 kHz Reference provided on SCOUT1/SCOUT2. The 2048 kHz signal is derived from the recovered clock that is selected (RCLKn) by control bits S1YNC2 - S1YNC0/S2YNC2 - S2YNC0.
0	1	0	X	SCOUT1/SCOUT2 lead continues to put out clock when LOS is detected on the selected reference input.
0	1	1	X	SCOUT1/SCOUT2 lead is forced low when LOS is detected on the selected reference input.

Note: X=don't care

When the 8 kHz reference option is chosen, setting control bit SYNLF (bit 6) in register 00CH to a 1 causes SCOUT1 and SCOUT2 pulses to occur in synchronism with the selected line's frame pulse as shown in Figure 33. For an AMI or HDB3 setting of the Line Decoder by control bit RAIL (bit 7) in register X+00H set to 1, the 8 kHz pulse on SCOUT1 and SCOUT2 is coincident with the fourth bit of a frame if control bit SYNLF (bit 6) in register 00CH is set to a 1 and control bit RXCP (bit 3) in register X+00H is set to a 0; for RXCP set to a 1, the 8 kHz pulse is coincident with the third bit of the frame. For NRZ mode (RAIL set to 0) the pulse is coincident with the first bit of a frame if control bit SYNLF (bit 6) in register 00CH is set to a 1 and control bit RXCP (bit 3) in register X+00H is set to a 0; for RXCP set to a 1, the 8 kHz pulse is coincident with the last bit of the frame. This feature works in framed modes only. Control bit BYPASS (bit 0) in register X+161H when set to a 1 sources the clock after it has been filtered by the dejitter buffer.

One-Second Clock Selection

The source of the clock used for internal one-second timing functions can be derived from several sources. It should be noted that for proper ITU-T G.703 compliance this source should be accurate to ± 50 ppm. Lead SREGT, lead BPOSC, or one of the eight RCLKn can be used for the one-second clock source when the shadow register feature or the DS0 remote loopback feature is enabled. When one of the eight RCLKn is selected and this lead experiences a loss of signal, the BPOSC signal is substituted if control bit S1CIEN (bit 7) in register 00CH is set to a 1. Control bits S1YNC2-S1YNC0 (bits 2, 1 and 0) in register 024H select which of the eight RCLKn are to be used for the one-second clock. The table below indicates the various clock selections which are under control of global control bits S1SEXTB (selects the external source SREGT when set to 0) and S1SINT (selects one of the internal sources):

LOS (alarm)	S1SEXTB Bit 4 reg. 024H	S1SINT Bit 3 reg. 024H	Action
X	0	X	Lead SREGT is selected as the clock source for one-second timing.
X	1	0	The 2048 kHz clock from lead BPOSC is divided down to a one-second source.
False	1	1	The 2048 kHz clock from lead RCLKn as selected by control bits S1YNC2-S1YNC0 is divided down to a one-second source.
True	1	1	The 2048 kHz clock from lead BPOSC is divided down to a one-second source if S1CIEN is set to 1.

Note: X=don't care

AIS GENERATION AND DETECTION

Two type of frame AIS and Time Slot 16 AIS are detected in the received E1 line signal. When control bit ENAISI (bit 5) in register 00CH is set to 0, line AIS is detected when the received line signal has two or less zeros in each of two consecutive double-frame periods (512 bits each). Recovery occurs when each of two consecutive double-frame periods contains three or more zeros after basic frame alignment has been detected. This corresponds to ITU-T G.775 recommendations. When control bit ENAISI (bit 5) in register 00CH is set to 1, line AIS is detected when the received line signal has two or less zeros in each of two consecutive frame periods (256 bits each). Recovery occurs when each of two consecutive frame periods contains three or more zeros after basic frame alignment has been detected. This corresponds to ISDN applications as recommended by ITU-T I.431. The status of line AIS is given by the status bit AIS (bit 6) in register X+10H if control bit ENLAIS (bit 1) in register X+05H is set to a 1. An associated mask bit MAIS, a latched event bit LAIS, a performance value PAIS and a fault value FAIS are all bit 6 in registers X+14H, X+11H, X+12H and X+13H, respectively. In Transmission Mode AIS can cause the “A” bits on the signaling highway to be set to 1 if control bits ENAIS (bit 7) and ENABIT (bit 4) in register X+02H are set to 1. Similarly in any mode AIS can cause all ones on the data highway if control bits ENAIS (bit 7) and ENDBIT (bit 3) in register X+02H are set to 1.

An AIS in Time Slot 16 is detected as described above. The status of Time Slot 16 AIS is given by the AIS16 status bit (bit 6) in register X+164H if enabled. Time Slot 16 AIS may be included in AIS if control bit TS16EC (bit 0) in register X+00H is set to a 1.

The E1Fx8 can generate E1 line AIS (all ones) if control bit TXAIS (bit 7) in register X+06H is set to a 1. Line AIS may also be generated in Transmission Mode by setting control bit EXTAIS (bit 5) in register X+06H to a 1 and having the A-bits received from the signaling highway, TTSIGn, set to 1. During a local loopback, AIS may be substituted for the transmitted test signal if control bit TXLAIS (bit 6) is set to a 1 while control bit LLP (bit 7) is set to a one both in register X+107H.

AUXILIARY PATTERN GENERATION AND DETECTION

The Auxiliary pattern is an unframed continuous alternating binary “10” pattern on the E1 line used in ISDN applications. The Auxiliary Pattern is detected when 254 or more alternating binary “10” patterns are detected in a 250 microsecond period. If control bit ENRXAUXP (bit 0) in register X+03H is set to a 1, status bit AUXP (bit 0) in register X+164H is set to a 1 if the Auxiliary Pattern is detected. An associated mask bit MAUXP, a latched event bit LAUXP, a performance value PAUXP and a fault value FAUXP are all bit 0 in registers X+166H, X+165H, X+167H and X+168H, respectively.

To send the Auxiliary Pattern, set control bit ENTXAUXP (bit 3) in register X+06H to a 1 and an unframed, alternating binary “10” pattern will be transmitted to the E1 line.

HDLC CHANNEL

This channel is used to send messages at 4 to 20 kbit/s between network elements using any one or a combination of the National bits. This channel uses an HDLC protocol. A HDLC message frame is composed of four parts: an opening flag, the message (which consists of multiple bytes), a two-byte CRC-16 frame check sequence, and a closing flag, as shown in Figure 54 below.

Bit	8	7	6	5	4	3	2	1
Opening Flag	0	1	1	1	1	1	1	0
Message	Address and Control Information							
CRC-16								
Closing Flag	0	1	1	1	1	1	1	0

Figure 54. HDLC Format

The opening and closing flags are represented by a single, unique 8 bit character defined as 01111110, which contains six contiguous ones. To avoid the occurrence of a false flag within the data stream, a zero is inserted (stuffed) after each string of five contiguous ones in the message or CRC-16. Reception of more than six contiguous ones is interpreted as a frame abort sequence. When an abort sequence is received, the remainder of the current frame is ignored and the received portion is discarded as an invalid frame. A two-byte CRC-16 frame check sequence is computed across the contents of the message (after the opening flag), and appended to the end of the message. The time between consecutive frames is filled with one or more flags. When two or more flags occur in sequence, they may share the boundary zero between them (011111101111110).

Operation at either 4, 8, 12, 16 or 20 kbit/s is supported. The bandwidth of the facility data link is normally 4 kHz, when Sa4 is assigned to carry HDLC messages. Control bits SA4 through SA8 (bits 4-0) in register X+0CH when set to a 1 assign the specific National bits to the HDLC controller.

The facility data link bandwidth selection is described in the following table. These control bits are also common with the transmit side.

A 128-byte FIFO is provided in each direction for each framer, which permits many messages to be transmitted and received without having the microprocessor service the FIFOs. For longer messages interrupts and status information are provided to facilitate FIFO servicing by the microprocessor. For both message types, the HDLC link controller performs the following functions:

- Zero bit stuffing/destuffing (11111 to 111110 /111110 to 11111)
- ITU-T CRC-16 generation/checking (16-bit sequence)
- Flag generation/detection (01111110)
- Abort generation/detection (01111111...)
- Start of frame detection
- End of frame detection
- FIFO overflow and underflow

The HDLC receiver is enabled when a 1 is written to control bit EHR (bit 7) in register X+123H. When enabled, the HDLC receiver will remove the stuffed zero bits, search for the opening flag and place the message contents in a 128-byte FIFO. The HDLC link controller will compute a CRC and compare it against the CRC that is received. The received CRC is not stored in the FIFO and is discarded after being received and checked.

The receive FIFO is monitored for fill level, with maskable interrupts and latched indications provided. Bits RXFS1 and RXFS0 (bits 4 and 3) in status register X+0EH indicate when the receive FIFO is less than half full, equal to or greater than half full, full and overflowed. An interrupt may also be sent at the end of the message, or when the FIFO is half full, using the RHIE control bit (bit 6) in register X+123H to control the conditions for which status bits RHIS2-RHIS0 (bits 7 - 5) in register X+0EH change. Thus, when the messages are always expected to be shorter than the maximum FIFO depth of 128 bytes, the HDLC link controller will generate an interrupt only on the completion of the message by setting RHIE = 0. If mask bits MRHIS2-MRHIS0 (bits 7-5) in register X+0FH are set to 001, an interrupt will occur when RHIS2-RHIS0 = 010; event bits LRHIS2-LRHIS0 (bits 7-5) in register X+0DH hold the latched value. When the messages are expected to exceed the maximum FIFO depth of 128 bytes, the controller will generate an interrupt when the FIFO is half filled by setting RHIE = 1; mask bits MRHIS2-MRHIS0 should be set to 001, but now the interrupt based on RHIS2-RHIS0 = 010 will occur both at the end of message and when the FIFO reaches half full. This same function may be accomplished by leaving RHIE = 0 and by monitoring the FIFO fill level using status bits RXFS1 and RXFS0 to indicate FIFO fullness. To generate an interrupt from the RXFS1 and RXFS0 status bits, mask bits MRXFS1 and MRXFS0 (bits 4 and 3) in register X+0FH should be set to 00; when the receive FIFO reaches half full, event bits LRXFS1 and LRXFS0 (bits 4 and 3) in register X+0DH will be set to 01 and an interrupt will be generated. Interrupts from RHIS2-RHIS0 can be used to indicate message completions only.

Bits DPT7 - DPT0 in register X+125H provide the number of bytes presently stored in the receive FIFO. Bits RHIS2-RHIS0 (bits 7-5) in register X+0EH provide message status and error indications. The HDLC link controller will generate a maskable interrupt for start of message detected, valid message received, CRC in error,

and message aborted. The message bytes are read by the microprocessor at bits RHD7-RHD0 in register X+124H for each framer. Bit 0 corresponds to the first bit received in a byte. To facilitate message reception, both a mask register and a latched event register are provided at locations X+0FH and X+0DH, respectively, in like bit positions for status bits RHIS2- RHIS0 and RXFS1, RXFS0.

To accommodate back-to-back messages, a message length register MSL6-MSL0 (bits 6 through 0) in register X+128H is provided which is loaded at the end of every message (valid received, abort or received with bad CRC). When an interrupt occurs indicating a message has been received, MSL6-MSL0 should be read. The message length along with message status may be queued for processing later. The value in DPT7-DPT0 is not reset at the end of a message. This allows the microprocessor to read out the receive FIFO per received message while another message is being received or wait until several messages exist in the FIFO before reading them out and processing them. When initializing the HDLC controller, RHD7-RHD0 must be read repeatedly until the depth value in DPT7-DPT0 is zero. It should be noted that messages with bad CRC or messages that were aborted must be cleared from the FIFO also.

The HDLC transmitter is enabled when a 1 is written to control bit EHT (bit 7) in register X+126H. When enabled, the HDLC link controller will transmit flags until data is placed in the transmit FIFO. Up to 128 bytes can be placed in the FIFO. The message bytes are written into bits THD7-THD0 in register X+127H. Bit 0 corresponds to the first bit transmitted. The transmit bytes are read from the transmit FIFO, zero insertion is performed as needed and a 16-bit CRC is computed until the end of message is detected. When the last byte of the message is written into the FIFO, the microprocessor must set the end of message status bit EOM (bit 5) in register X+126H. The computed 16-bit CRC will be appended to the end of the message followed by at least one flag before another message is transmitted. When the transmit FIFO is emptied without setting the EOM bit, the FIFO will set an underflow indication in status bits TXFS1 and TXFS0 (bits 2 and 1) in register X+0EH coded to 11, and an abort character will be transmitted, thereby terminating the message.

The transmit HDLC link controller provides latched event bits and maskable interrupt bits related to the transmit FIFO status. Information such as underflow and fill status is provided by reading status bits TXFS1-TXFS0 (bits 2 and 1) in register X+0EH and the corresponding latched event bits LTXFS1 - LTXFS0 (bits 2 and 1) in register X+0DH.

Transmit HDLC FIFO service interrupts may be programmed to occur when the transmit FIFO is half empty, or when the last byte is sent, by setting control bit THIE (bit 3) in register X+126H. For short messages, the entire message may be written into the FIFO, and the controller will generate an interrupt, indicated by status bit THIS (bit 0) in register X+0EH, when the message has been sent. For longer messages, the controller will generate an interrupt when the FIFO is ready to accept more data. To facilitate message transmission both a mask register and a latched event register are provided at locations X+0FH and X+0DH, respectively in like bit positions for status bits THIS and TXFS1, TXFS0.

There are four general types of message transfers, which are described below: transmitting long and short messages, and receiving long and short messages. The difference between the long and short messages is primarily in how the 128-byte FIFOs are serviced. With many messages, the entire message will fit into the FIFOs and interrupts will be generated when the end of the message occurs. With longer messages, the message will not fit into the FIFO, and the message will have to be transmitted or received in several segments. Since long and short received messages are similar, their processing is described under the same heading.

Transmit Short Message

To transmit a short message (up to 128 bytes, excluding flags and CRC-16), first configure the transmitter to generate an interrupt at the end of message by writing a 0 to control bit THIE (bit 3) in register X+126H. Then write a 1 to control bit EHT (bit 7) in register X+126H to enable the transmitter. The HDLC link controller will continue to transmit flags until data is written into the transmit HDLC FIFO. Flags are sent in the selected National bits as a continuous idle pattern even when the HDLC controller is not enabled.

Write the message into the transmit FIFO by writing each byte in turn to THD7-THD0 in register X+127H. Bit 0 represents the first bit in the byte to be transmitted. The bytes written into THD7-THD0 are transferred auto-

matically into the FIFO. After the last byte is written into the FIFO, the EOM (bit 5) in register X+126H is written with a 1. The transmitter will then begin to send the message bytes until the FIFO is empty. Since the EOM bit was set, the completion of the message will generate an interrupt, if not masked, indicated by the latched status bit LTHIS (bit 0) in register X+0DH. This latched status indication indicates that the message is complete or the FIFO is empty. After the CRC-16 is sent, the HDLC link controller will start to send flags again.

Transmit Long Message

To transmit a long message (greater than 128 bytes, excluding flags and CRC-16), first configure the transmitter to generate an interrupt at the half full level of the FIFO by writing a 1 to control bit THIE (bit 3) in register X+126H. Then write a 1 to control bit EHT (bit 7) in register X+126H to enable the transmitter. The HDLC link controller will continue to transmit flags until data is written into the transmit HDLC FIFO. Flags are sent in the selected National bits as a continuous idle pattern even when the HDLC controller is not enabled.

Write the first 128-byte message segment into the transmit FIFO by writing each byte in turn to THD7-THD0 in register X+127H. Bit 0 represents the first bit in the byte to be transmitted. The bytes written into THD7-THD0 are transferred automatically into the FIFO. The HDLC link controller will then start to send the message bytes. When the FIFO empties to the half full level, the LTHIS bit (bit 0) in register X+0DH will be latched, and an interrupt generated, if the corresponding mask bit MTHIS (bit 0) in register X+0FH is set to 0. This is an indication for the microprocessor to write another 64 bytes into the transmit HDLC FIFO. This process of sending and refilling is repeated, 64 bytes at a time, until the last byte in the message is written into the FIFO. This is followed by writing the EOM (bit 5) in register X+126H with a 1. The transmitter continues to send the final message bytes until the FIFO is empty. When the last byte is transmitted and the FIFO is empty, the LTHIS bit will latch while EOM=1, indicating completion of the message. After the CRC-16 is sent, the HDLC link controller will start to send flags again. The latched event register X+0DH should be cleared before sending the next message to enable the reception of the status of the next transmitted message. Status bits TXFS1-TXFS0 (bits 2-1) in register X+0EH indicate the fill level of the transmit FIFO. If a message is to be aborted, setting control bit TAB (bit 6) in register X+126H to a 1 will force the abort code 7FH to be transmitted followed by flags and the clearing of the transmit FIFO.

Receive Message

To receive a message, first configure the receiver to generate an interrupt at the end of message and at the half full level of the FIFO by writing a 0 to control bit RHIE (bit 6) in register X+123H and writing mask bits MRHIS2-MRHIS0 (bits 7 - 5) in register X+0FH to 001 and MRXFS1,0 (bits 4 and 3) in register X+0FH to 00. Initialize the receive FIFO by reading RHD7-0 in register X+124H repeatedly until the FIFO is emptied, which is indicated by DPT7-DPT0 = 00H in register X+125H. Then enable the receiver by writing a 1 to control bit EHR (bit 7) in register X+123H.

The receiver will generate an interrupt when the FIFO is half full, as indicated by the latched status bits LRXFS1,0 (bits 4 and 3) in register X+0DH being set to 01 or when an end of message is detected by latched status bits LRHIS2-LRHIS0 (bits 7 - 5) in register X+0DH being set to 010 for a valid message received (= 011 for a completed message with CRC error or = 1XX for an aborted message received). If a half full interrupt is received, the FIFO should be emptied. The receive message is read from the FIFO by reading the bytes RHD7-RHD0 in register X+124H. Bit 0 represents the first bit in the byte to be received. The bytes in RHD7-RHD0 are transferred automatically from the receive FIFO. If some time has elapsed since the interrupt, the depth register DPT7-DPT0 may be read to determine the size of the message received so far. If the end of message indication is set, the microprocessor should read the message bytes from RHD7-RHD0 using the message length register MSL6-MSL0 (bits 6-0) in register X+128H to detect the remaining number of bytes stored in the receive FIFO. Please note that the message length is updated when the end of message event indication is latched and interrupt generated, and will not be modified until it is read and cleared by the microprocessor or if another completed message is received. The receive FIFO must be read for any type of message termination (good CRC, bad CRC or abort).

Several short messages may be left in the receive FIFO and read out at a later time. This is accomplished by storing the message length value read from MSL6-MSL0 and the latched status read from LRHIS2-LRHIS0 and LRXFS1,0 in a queue. The message boundaries and validity of the messages read from the FIFO may be determined from latched status and message length values.

GLOBAL MICROPROCESSOR CONTROLS AND ALARMS

The following line level and Time Slot 0 alarms for each of the eight framers are detected in the E1Fx8: Loss Of Signal (LOS), Alarm Indication Signal (AIS), Out Of Frame (OOF), Remote Alarm Indication (RAI), Change Of Frame Alignment (CFA), Out Of Multiframe (OOFM), transmit or receive slip (SLIP) and Change of Signaling State (SCHG). These alarms are provided by the Status, Event and Mask Registers (registers X+10H, X+11H and X+12H). A second bank of registers covering Time Slot 16 and miscellaneous alarms is provided for each of the eight framers: Time Slot 16 AIS (AIS16), Excessive CRC-4 Error Indication (ECRCE), Time Slot 16 RAI (RAI16), Out Of Time Slot 16 Multiframe (OO16M) and the Auxiliary Pattern (AUXP). These alarms are provided by the Status, Event and Mask Registers (registers X+164H, X+165H and X+166H). Control bit TS16EIC (bit 0) in register X+00H when set to a 1 permits AIS16, RAI16 and OO16M to be “ored” with AIS, RAI and OOFM. In addition, the following HDLC link level alarms are supported by the E1Fx8: Receive HDLC event and status, Transmit HDLC event and status, Receive FIFO event and status and Transmit FIFO event and status (registers X+0DH and X+0EH with masks in X+0FH). Control of the DS0 remote loopback activate and deactivate sequences, and the PRBS analyzer generate status and latched event indications for the receipt of a DS0 Remote Loopback Activation request (intermediate and complete), a DS0 Remote Loopback Deactivation Request (intermediate and complete), Transmit DS0 Activation or Deactivation sequence complete, and PRBS Analyzer out of lock (registers X+129H and X+12AH with masks in X+12B) are also provided. To aid in locating signaling change of state sources, SIGACT7-SIGACT0 in register X+19H indicates which group(s) of four time slots triggered the interrupt for status bit SCHG.

The latched status event indication (which can also be referred to as a software interrupt indication) for an alarm or condition is latched on either positive transitions, negative transitions, or both transitions. Control bits RISE (bit 7), and FALL (bit 6) in the Global Configuration register 00BH determine the transitions that cause an event bit to latch for all eight framers, as shown in the following table:

RISE (bit 7)	FALL (bit 6)	Action
0	0	Latched status bit indications in all registers disabled. Hardware and software interrupt indications disabled.
1	0	Latched status indication sets on positive alarm transition, along with generating a hardware interrupt provided the corresponding mask bit and the global interrupt status indication bit GIM (bit 5) in register 00BH are both 0.
0	1	Latched status indication sets on negative alarm transition, and generates a hardware interrupt provided the corresponding mask bit and the global interrupt mask bit GIM (bit 5) in register 00BH are both 0.
1	1	Latched status indication sets on both positive and negative alarm transitions, and generates a hardware interrupt provided the corresponding mask bit and the global interrupt mask bit GIM (bit 5) in register 00BH are both 0.

The latched event is cleared by writing a 0 to the associated bit position in the latched status indication register. The E1Fx8 also provides a Global Interrupt Mask (GIM) bit for the microprocessor interrupt lead (INT/$\overline{IRQ}$). When a 1 is written to control bit GIM (bit 5) in the Global Configuration Register 00BH, this hardware interrupt indication lead is tristated when a latched indication (event) bit is set. When a 0 is written into the GIM bit, the hardware interrupt lead is enabled. When enabled, the polarity of the interrupt lead can be inverted by writing a 1 to control bit IPOL (bit 4) in the Global Configuration Register 00BH.

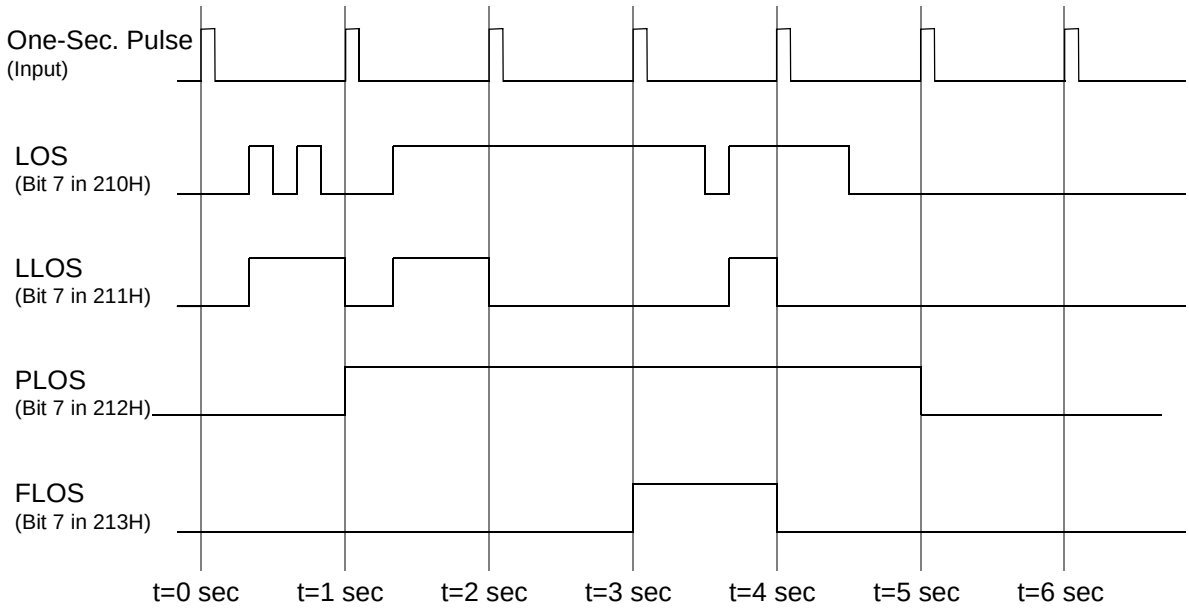
Besides providing individual unlatched and latched alarm status indications, and interrupt mask bits, on a per framer basis, the E1Fx8 provides global interrupt status indication bits, as well as global interrupt mask bits and framer alarm event pointer bits in the Global Register segment (registers 011H-01CH). A global interrupt status indication bit is set to 1 in registers 011H and 01AH if the same type of alarm occurs in any of the eight framers, provided that the corresponding global mask bit in registers 012H or 01BH is not set to 1 and the E1Fx8 is configured to latch on one of or both transitions of the alarm. Registers 014H (CHL8-1), 016H (CHD8-1), 019H (CHR8-1) and 01CH (CHS8-1) provide pointers to the specific framer or framers which caused the line or Time Slot 0 event, HDLC link event, DS0 remote loopback request/PRBS out of lock event or Time Slot 16/ miscellaneous event, respectively, that triggered the interrupt.

For example, assuming a loss of signal alarm occurred in framer 1 only, the LOS alarm will set the LOS bit (bit 7) in the unlatched register 210H (i.e., X+10H, with X=200 for framer 1). This alarm indication bit will be set to 1 for the duration of the alarm. Assuming that control bits RISE and FALL (bits 7 and 6) in the Global Configuration Register 00BH are set to 10 (latched event set on a positive transition), the transition from 0 to 1 of the LOS alarm will cause the LLOS bit (bit 7) in register 211H to latch. A hardware interrupt will be generated on lead INT/$\overline{IRQ}$ if the interrupt mask bit MLOS (bit 7) in register 214H is a 0, and the global interrupt mask bit GIM (bit 5) in register 00BH is a 0. If either of these bits is set to 1, the hardware interrupt will not occur. In addition, the latched LOS indication will also cause a Global LOS indication, GLOS (bit 7) in register 011H. The framer in which the loss of signal alarm was detected can be found by reading bits 7-0 in register 014H. Reading the register confirms that the loss of signal alarm occurred in framer 1. The interrupt will be reset by first reading the LLOS latched alarm bit position (bit 7) in register 211H and then writing a 0 into the bit position. This will also clear the GLOS indication bit. If the LOS alarm persists, it will not cause the latched bit position to relatch. The alarm status can be determined by now reading periodically the unlatched status bit (bit 7) in register 210H, until it becomes 0, indicating that recovery has taken place. This clearing sequence may be selected to occur automatically as described below for Shadow Registers.

Shadow Registers

The E1Fx8 also provides shadow registers for the alarms of each of the eight framers. The shadow register feature in the E1Fx8 is enabled by writing a 1 to the Shadow Register Enable control bit (SRGEN), bit 3 in the Global Configuration register 00BH. By applying a pulse at one-second intervals to lead SREGT (or selecting a one-second clock from lead BPOSC or one of the receive line clocks, RCLKn, as described above in the Clock Selections section), an indication bit will be set in register X+12H if the corresponding line alarm occurred at any time in the last one-second interval. In addition, an indication bit will be set in register X+13H if the alarm is active, but the transition to the active state did not occur in the last one-second interval (i.e., the alarm has persisted for longer than one-second). The rising edge of the one-second pulse will also reset a latched event bit position in register X+11H independent of the microprocessor.

Figure 55 illustrates the operation of the shadow registers for a loss of signal (LOS) alarm for framer 1. The behavior shown in the diagram also applies to the other signal alarms in the same register X+10H (AIS, OOF, RAI, CFA, OOFM, SLIP, and SCHG) or in register X+164H (AIS16, ECRCE, RAI16, OO16M and AUXP). This figure assumes that control bits RISE and FALL (bits 7 and 6) in the Global Configuration Register 00BH are set to 10 (latched event set on a positive transition only). Please note that the LOS alarm causes a latched status indication LLOS (bit 7) in register 211H, and that the latched bit is reset by the rising edge of the selected one-second pulse (either on lead SREGT or via leads BPOSC/RCLKn and controls described in the Clock Selections section). The PLOS status bit (bit 7) in register 212H is a 1 whenever there is a transition to LOS during the last one-second interval or LOS is present at the end of the last one-second interval. The FLOS status bit (bit 7) in register 213H is a 1 if the LOS alarm is active but did not become active during the previous one-second interval.



Note 1: For this example, latched events are set only on positive event transitions.

Note 2: PLOS = LOS + LLOS evaluated at one-second boundaries (where '+' is a logical or).

Note 3: FLOS = LOS & $\overline{\text{LLOS}}$ evaluated at one-second boundaries (where '&' is a logical and, and $\overline{X}$ is a logical inversion).

Figure 55. Shadow Register Operation

In addition, shadow registers have been provided for monitoring the number of line errors that have occurred in one-second intervals. When the Shadow Register Enable control bit (SRGEN), bit 3 in the Global Configuration register 00BH, is a 1, the following shadow registers are updated with the count from the previous one-second interval on the rising edges of the one-second pulse provided (either on lead SREGT or via leads BPOSC/ RCLKn and controls described in the Clock Selections section): a 10-bit register for a CRC-4 error count, a 10-bit register an E-bit = 0 count, a 10-bit register for Sa6 = 00X1, a 10-bit register for Sa6 = 001X, a 16-bit register for a coding violations count, a 15-bit Test Analyzer out of lock counter, and an 8-bit register for a framing word error count. The rising edge of the one-second pulse also clears the counters that were holding the count for the transfer to the shadow registers.

For example, the shadow register for monitoring frame word errors in framer 1 works in the following way. The 8-bit framing word error counter FBE7-FBE0 in register 2FCH counts the number of frame word errors over a one-second interval, which is determined by the selected one-second pulse. At the rising edge of the one-second pulse, the count in register 2FCH is transferred to the shadow register LFBE7-LFBE0 in location 2FAH. The frame bit error counter in register 2FCH is cleared at the same instant and it starts the error count for the next one-second interval. At the end of the next one-second interval, the shadow register is updated with the new count. A counter overflow bit FBEO is also provided (bit 7 in register 2FDH), with a corresponding shadow overflow bit LFBEO (bit 7) in register 2FBH. The microprocessor can also clear the counter in register 2FCH by writing 00H to it. The shadow register holds its count during a microprocessor read cycle.

MAINTENANCE

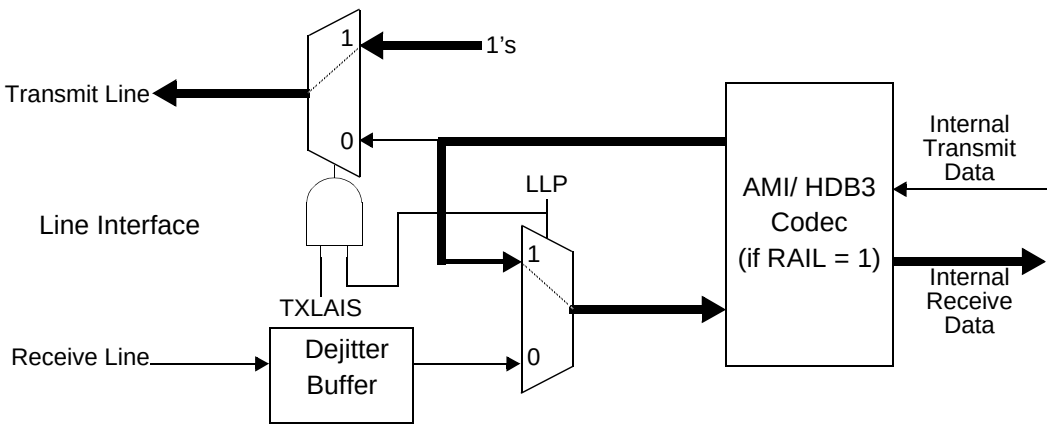
To assist in testing, a built-in Pseudo Random Binary Sequence (PRBS) Generator and Analyzer blocks are provided on a per E1 basis, framed or unframed. The PRBS Generator and Analyzer supports the 2^{15}-1 bit pseudo-random binary sequence which is specified in the ITU-T Recommendation O.151. In addition the O.151 2^{20}-1 (QRSS), 2^{11}-1 (O.152), and a 2^{23}-1 pseudo-random binary sequences are also provided. An optional 32 bit code word may be substituted for the PRBS in framed mode only. Each E1 framer may select where the PRBS Generator and Analyzer are connected so that both line testing (Generator on the transmit side and Analyzer on the receive side) and system testing (Generator on the receive side and Analyzer on the transmit side) can be supported. The output of the Analyzer is provided in a per channel register as well as counted in a 16 bit out of lock counter. The PRBS may operate in a framed or unframed mode for the entire E1 channel or it may operate over a single or group of time slots to support fractional E1 and per time slot maintenance.

The E1Fx8 also provides a local line loopback (transmit framer looped to receive framer), remote line loopback (receive line signal looped to transmit line), and payload loopback (time slots 1 through 31 from receive line looped back but with a locally generated Time Slot 0) options for each E1 channel. In addition any one or more received time slot (except Time Slot 0) may be selected and looped back and transmitted in place of the time slot input from the data highway or any one of the transmit time slots may be substituted for a received time slot.

The E1Fx8 provides time slot loopback activate and deactivate code detection and generation in support of the ANSI T1.231 / T1.403-CORE standard permitting single person “trans-atlantic” loopback testing of fractional T1s/E1s using the E1Fx8.

Local Line Loopback

Local line loopback for a framer is enabled when a 1 is written to control bit LLP (bit 7) in register X+107H. Local line loopback connects the transmit path with the receive path in the direction toward the line, as illustrated in Figure 56 below. The loopback is independent of the line interface selected, NRZ or dual unipolar (rail). When control bit TXLAIS (bit 6) in register X+107H is written to 1, an AIS (all ones signal) is transmitted to the line instead of test data. Please note that transmit line AIS can be enabled independent of the local loopback feature.

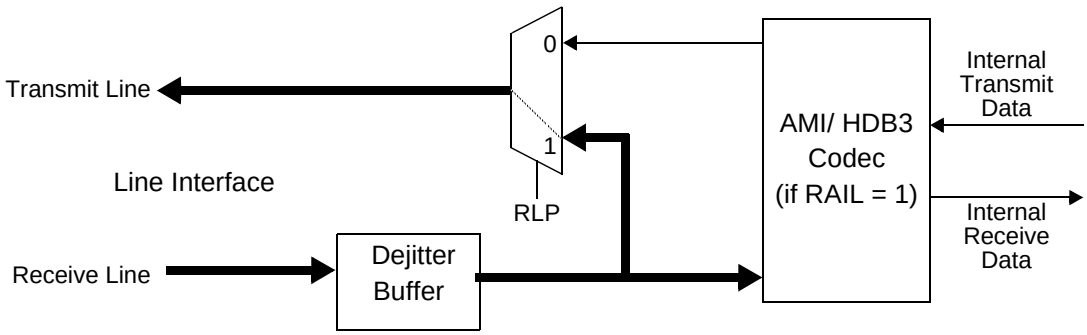


Note: Bold/dashed lines show paths used for TXLAIS=1 and LLP=1.

Figure 56. Local Loopback

Remote Line Loopback

Remote line loopback for a framer is enabled when a 1 is written to control bit RLP (bit 5) in register X+107H. Remote line loopback connects the receive line data back to the transmitter, as illustrated in Figure 57 below. The loopback is performed before the AMI/HDB3 codec. The loopback is independent of the line interface selected, NRZ or dual unipolar (RAIL = 1). A dual unipolar loopback will loop back coding violations if they exist.

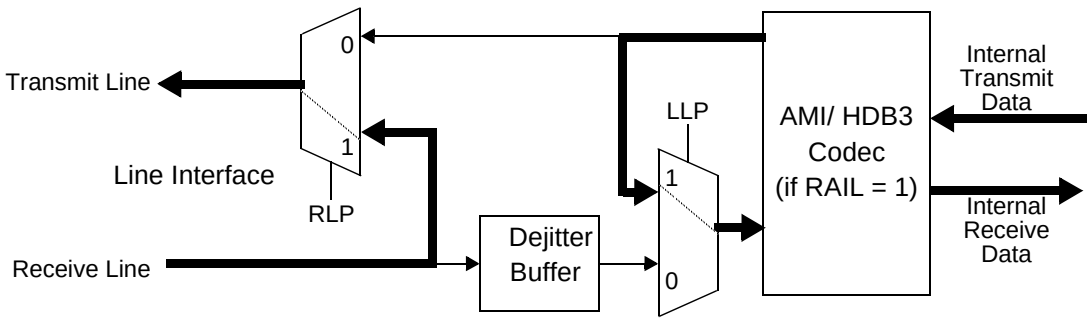


Note: Bold/dashed lines show paths used for RLP=1.

Figure 57. Remote Line Loopback

Bi-Directional Loopback

A Bi-directional loopback for a framer is enabled when a 1 is written to both control bits LLP (bit 7) and RLP (bit 5) in register X+107H. The Bi-directional loopback connects the receive line data back to the transmitter, as illustrated in Figure 58 below. The remote half of the loopback is performed before the AMI/HDB3 codec. The Dejitter Buffer is in neither path during this loopback. The loopback is independent of the line interface selected, NRZ or dual unipolar (RAIL = 1). A dual unipolar loopback will loop back coding violations if they exist.



Note: Bold/dashed lines show paths used for LLP=1 and RLP=1.

Figure 58. Bi-Directional Loopback

Time Slot Remote Loopback

The Time Slot remote loopback feature is enabled when a 0 is written to control bit TSRLOP (bit 7) in register X+109H. One or more Time Slots can be looped back by writing a 1 to the corresponding control bit TSRL32-TSRL1 in registers X+10AH, X+10BH, X+10CH and X+10DH as shown in Figure 59. Existing transmit data traffic is not affected if the corresponding Time Slot is not looped.

The loopback takes place after the slip buffer and is provided whether the receive slip buffer is enabled or disabled. Control bits TSRLOP and TSRL32- TSRL1 are set to 0 upon a hardware reset. This function requires the presence of TTCLKn to operate correctly. Since the transmit framer is reading from the receive slip buffer, contentions may occur due to clock asynchronism between the receive and transmit paths; these are addressed by the E1Fx8 and may cause a 'slip' to occur on the looped time slot(s) only. Unlatched status RTSLPP (bit 5) in register X+15H indicates the phase used for remote time slot loopbacks. A change in value of RTSLPP indicates that the time slots being looped back were either repeated or skipped for a single frame.

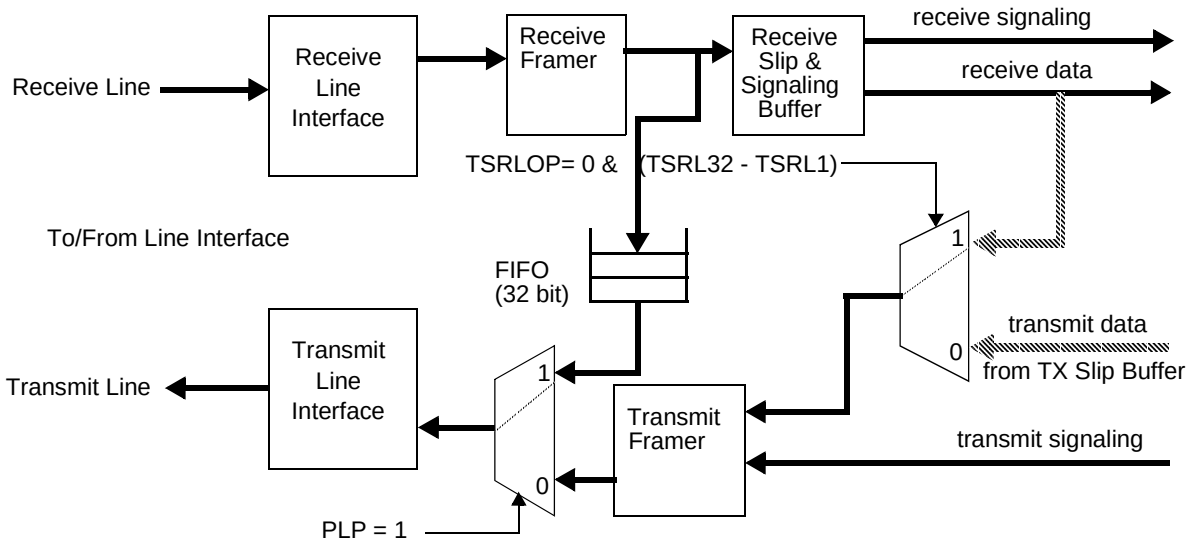


Figure 59. Time Slot Remote and Payload Loopbacks

Payload Remote Loopback

The E1Fx8 device provides two payload remote loopback mechanisms; one that essentially skips the received and transmitted framing byte positions but inserts received non-frame time slot bits into transmit non-frame time slot bit opportunities as soon as possible; The other one maintains time slot integrity by utilizing the Time Slot Loopback feature for all 30 or 31 time slots. For the bit-by-bit style mechanism setting control bit PLP (bit 4) in register X+107H provides this feature in a way that only the sequence integrity of the payload is kept. A small FIFO is provided between the receive and transmit sides of the framer as shown in Figure 59 above to account for skipping the receive Time Slot 0 and inserting the transmit Time Slot 0. Therefore, the framing position of the outgoing bit stream is changed relative to the payload signals of the incoming bit stream from the line.

In order to keep the framing bit and payload relation intact, the E1Fx8 also provides a payload remote loopback by enabling all 30 or 31 time slot loopbacks. This function requires the presence of TTCLKn to operate correctly. In this way, the transmit data highway selects the data from the receive data payload through the slip buffers via control bits TSRL32 - TSRL1 in registers X+10AH, X+10BH, X+10CH and X+10DH all being set to a 1 and control bit TSRLOP (bit 7) in register X+109H set to a 0 which permits received time slot data to be mapped to transmit time slot position for n = 1 through 32 as shown in Figure 59 above.

Time Slot Local Loopback

The Time Slot local loopback feature is enabled when a 1 is written to control bit TSLLP (bit 1) in register X+109H. One or more Time Slots can be looped back by writing a 1 to the corresponding control bit TSLL32-TSLL1 in registers X+12DH, X+12EH, X+12FH and X+130H as shown in Figure 60. Existing receive data traffic is not affected if the corresponding Time Slot is not looped.

The loopback takes place after the transmit slip buffer and is provided whether the transmit slip buffer is enabled or disabled. Control bits TSLLP and TSLL32-TSLL1 are set to 0 upon a hardware reset. This function requires the presence of RTCLKn to operate correctly. Since the receive framer is reading from the transmit slip buffer, contentions may occur due to clock asynchronism between the receive and transmit paths; these are addressed by the E1Fx8 and may cause a 'slip' to occur on the looped time slot(s) only. Unlatched status LTSLPP (bit 5) in register X+16H indicates the phase used for remote time slot loopbacks. A change in value of LTSLPP indicates that the time slots being looped back were either repeated or skipped for a single frame.

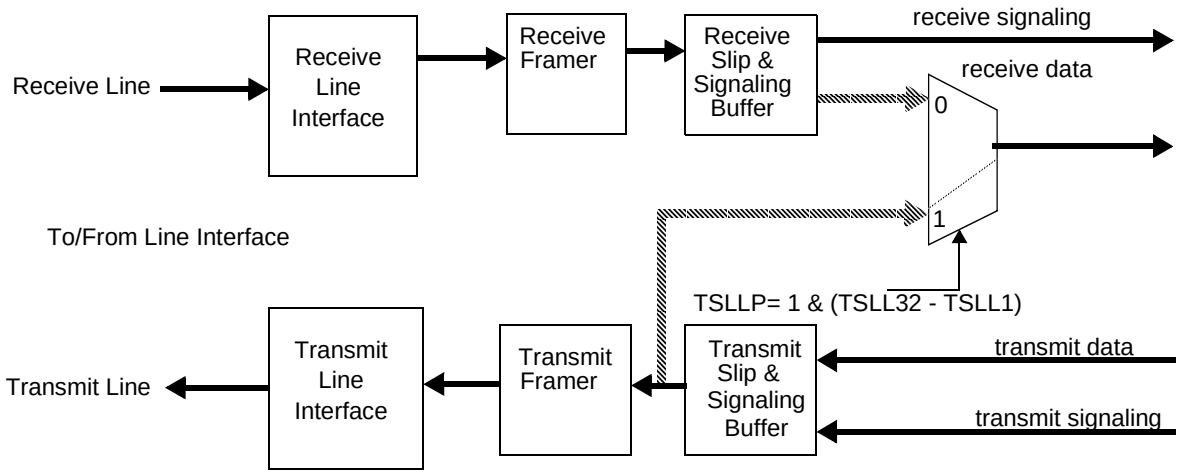


Figure 60. Time Slot Local Loopback

DS0 Remote Loopback

The DS0 Fractional Channel Loopback requirement is specified in ANSI document T1.403-1998, Annex B. By definition, remote loopback is the transmission of remote loopback sequence by the local framer to the distant framer. The DS0 Fractional Channel Loopback can involve one or more time slots which may or may not be contiguous but the time slots must all be 64 kbit/s. The intent is to provide single person loopback capability for Nx 64 kbit/s channels that pass through a Gateway Exchange whether they are framed by a T1 framer such as the T1Fx8 or an E1 framer such as the E1Fx8. Figure 61 is a simplified diagram of the code sequence generator. The sequence starting point and ending point in the sequence is arbitrary.

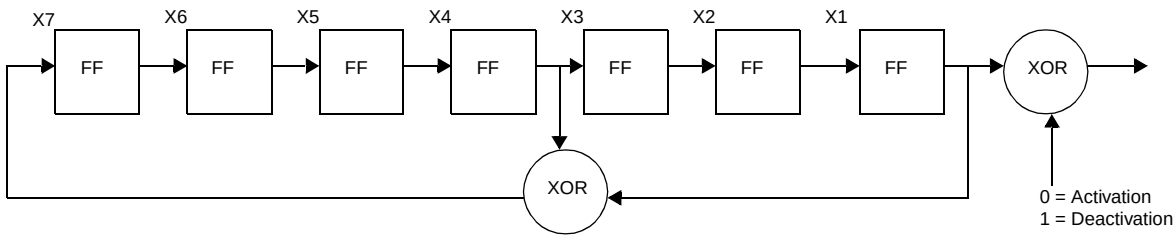


Figure 61. DS0 remote Loopback Code Sequence Generator

To activate the DS0 remote loopback feature at the distant end, the loopback activation code for one or more time slots is transmitted for a period of not less than 2 seconds. This will followed by the transmission of an all ones pattern for not less than 2 seconds. The responding end (i.e. distant end) should activate a loopback within the two-second interval immediately following the end of the loopback activation code sequence.

To deactivate DS0 at the distant end, the loopback deactivation code is transmitted for a period of not less than 2 seconds, followed by transmission of an all ones pattern for not less than 2 seconds. The responding end should deactivate a loopback within the two-second interval immediately following the end of the loopback deactivation code sequence.

For the purpose of either sending the DS0 loopback sequences or receiving them, the DS0 channel functionality and capacity must be taken into consideration. All the DS0s in a fractional group must be 64 kbit/s clear channels to permit functional transparency with the E1 environment. It is also expected that Alternate Digit Inversion, Zero Code Suppression and echo cancellation are not present on the path under test. For T1 facilities that do not support clear channel capability, it is assumed that the method of alternating DS0s of a fraction with all ones DS0s as recommended in ANSI T1.403 Annex B is utilized.

DS0 Loopback Activate and Deactivate Generation

In the transmit direction, the remote loopback feature for a fractional channel is configured by writing a 1 to one or more control bits TSRL32-TSRL1 in registers X+10AH through X+10DH when control bit TSRLOP (bit 7) in register X+109H is a 1. Control bit TSRLOP enables the TSRL32-TSRL1 bits to be used for the remote loopback generation feature. Writing a 0 to control bit TSRLOP enables the TSRL32-TSRL1 control bits to be used for time slot remote loopback as described above. The TSRL32-TSRL1 control bits select the time slots that define the fractional channel. This approach enables the transmit side to be either configured for sending the remote loopback sequence or enabling a remote time slot loopback locally, but not both configurations at the same time.

The remote loopback feature requires the one-second feature to be available (SREGT lead, BPOSC lead or selected RCLKn) in order for this feature to function. The transmission of the sequence is locked to nearest starting location of the one-second pulse.

The following table reflects the operation of the control bits associated with this feature. Control bit DS0DA (bit 6) in register X+109H when set to a 0 selects the activation sequence and when set to 1 selects the deactivation sequence. Control bit TRDSLP (bit 5) in register X+109H when set to a 1 initiates the four-second sequence selected by DS0DA to be transmitted on only those DS0s selected by TSRL32-TSRL1.

DS0 Remote Loopback Control

DS0DA	TRDSLP	Action
0	0	DS0 remote loopback feature is disabled, DS0 remote loopback feature is configured for activation pattern but no action taken.
1	0	DS0 remote loopback feature is disabled, DS0 remote loopback feature is configured for deactivation pattern but no action taken.
0	1	DS0 remote loopback feature activation pattern is sent for the time slots selected (TSRL32-TSRL1). The starting point of the DS0 remote loopback activation sequence can be arbitrary.
1	1	To send the deactivation pattern, the microprocessor must first write a 0 to the TRDSLP bit followed by a 1. The DS0 remote loopback feature deactivation pattern is sent for the DS0 channels selected (TSRL32- TSRL1).

Note: TSRLOP = 1

The completion of the four-second transmit DS0 sequence is indicated by unlatched status bit DS0TXC (bit 4) in register X+129H, and latched status indication LDS0TXC (bit 4) in register X+12AH. Please note that the unlatched bit position is a momentary indication. The latched bit is set on positive transitions only. Assuming the corresponding mask bit MDS0TXC (bit 4) in register X+12BH is set to 0, a global indication GDS0TC (bit 3) in global register 017H occurs along with an interrupt indication if global control bit GMDS0TC (bit 3) in register 018H is set to 0.

The microprocessor upon reading the global indication status bit GDS0TC should next read the framer pointer register CHR8-CHR1 at location 019H to determine the framer which has completed the transmission of the sequence. After reading the latched indication (LDS0TXC - DS0 Transmit Complete) to indicate that the transmission of the sequence is indeed complete, the microprocessor needs to write a 0 to the latched status to clear it. The microprocessor can now write a new time slot in which the send the activate code, or leave the time slot the same for sending the deactivate code. A new sequence cannot be transmitted until control bit TRDSLP is first written by a 0 followed by a 1.

Please note, it is the responsibility of the user not to write a new time slot location before the sequence is completed, because the sequence will be transmitted over the new time slot selection and not the old location.

Monitoring for ANSI DS0 Remote Loopback Codes from the Network

The receive side framer can monitor the time slots that have been designated by the microprocessor as a fractional channel. The standard (ANSI T1.403-1998) does not specify activation/deactivation detection parameters other than that there be a two-second transition period which corresponds to 2 seconds of all ones.

The E1Fx8 provides the capability of monitoring a single fractional channel at one time. The microprocessor writes the time slots that are to be monitored in control bits TSLL32-TSLL1 in registers X+12DH through X+130H for the activate/deactivate sequence. Control bit TSRLOP (bit 7) in register X+109H must be written with a 0 to enable the TSRL32-TSRL1 control bits in registers X+10AH through X+10DH to be used for local loopback upon detection of an activate/deactivate sequence. Please note that when control bit TSRLOP is written with a 1, the framer is configured for sending remote loopback, not receiving it, nor being in local loopback. The DS0 remote loopback monitor feature is enabled when control bit RLPEN (bit 0) in register X+109H is a 1.

The PRBS repeated sequence (which is repeated every 128 bits) is monitored for n frames after lock is acquired. The value of n is programmable from 1 to 256 frames (32 ms), by writing the binary value to control bits SRTT7-SRTT0 in register X+12CH. The value 0 is not valid.

An indication of a remote loopback request and release is given by both intermediate unlatched status, mask control, and latched status bits INTACT, MINTACT, LINTACT (bit 3) in registers X+129H, X+12BH and X+12AH respectively and INTDCT, MINTDCT, LINTDCT (bit 2) in registers X+129H, X+12BH and X+12AH respectively which are activated as soon as the activate or deactivate PRBS pattern is received for the number of frames indicated by control bits SRTT7-SRTT0 in register X+12CH. Latched status bits LDS0ACT and LDS0DCT (bits 7 and 6) in register X+12AH are set after the complete PRBS sequence is received followed by the all ones pattern. LDS0ACT and LDS0DCT do not change state until after two frames of continuous ones are received in the monitored fraction in the two-second all ones interval after the two-second activate/deactivate sequence is received. The intermediate indications LINACT and LINDCT are to be used when more than one fraction per E1 is to be monitored simultaneously; the microprocessor can update the control bits TSLL32-TSLL1 (registers X+12DH through X+130H) in a round robin fashion monitoring LINTACT and LINTDCT until a request in progress is detected, at which point the control bits TSLL32-TSLL1 are to be left unchanged until LDS0ACT or LDS0DCT indicates a complete sequence. There are also unlatched bits DS0ACT and DS0DCT (bits 7 and 6) in register X+129H associated with the latched bits. Thus, a valid indication is detected internally, and the activate/deactivate indication is only given at the start of the two-second action time. This is an indication to the microprocessor that a sequence has been detected. The interrupt mask bits are defined as MDACT and MDDCT (bits 7 and 6) in register X+12BH.

A global indication is given by status bit GDS0RS (bit 7) in register 017H for the activate sequence, and status bit GDS0DC (bit 6) in register 017H for the deactivate sequence. A global indication of the intermediate results

is given by GINTACT (bit 3) in register 017H for the activate PRBS pattern and by GINTDCT (bit 2) in register 017H for the deactivate PRBS pattern. These status bits are the logical or of a valid DS0 remote loopback activate PRBS pattern, deactivate PRBS pattern, activation request or deactivation request from the 8 framers. The microprocessor upon reading the global indications should also read the channel pointer, CHR8-CHR1 in register 019H, to determine which of the 8 framers was requesting a DS0 remote loopback activation or a deactivation request.

The microprocessor upon reading the framer n status bits LDS0ACT and LDS0DCT, may either set or reset the DS0 local loopback control bits TSRL32-TSRL1 in registers X+10AH through X+10DH accordingly, as determined by the channel selected by control bits TSLL32-TSLL1. Please note that it is the responsibility of the user to read the latched indications and take the appropriate action. If the microprocessor does not read the status bits, a new activate or deactivate sequence cannot be detected. The microprocessor should not perform a new channel selection until the activate or deactivate indication is cleared.

PRBS GENERATOR AND ANALYZER

The E1Fx8 provides the ability to separately generate a pseudo-random bit pattern or to detect a pseudo-random bit pattern on a per E1 basis or on a NxTime Slot basis. A common generator/ analyzer pair is used for both E1 and NxTime Slot functions.

E1 Test Generation and Analysis

Both a remote and local PRBS test can be performed. To perform the remote PRBS test writing a 1 to control bit INPRBS (bit 0) in register X+106H enables the framer to transmit a framed or unframed E1 PRBS pattern to the E1 line; control bit SINPRBS (bit 0) in register X+107H must be set to a 0. Writing a 1 to control bit PRBRE (bit 1) in register X+106H enables the analyzer to monitor the entire E1 received bit stream for a lock status (PRBS errors); control bit SPRBRE (bit 1) in register X+107H must be set to a 0. Control bit TTFM, transmit transparent mode, (bit 6) in register X+01H determines if the PRBS pattern is to be transmitted framed or unframed. Control bit RTFM, receive transparent mode, (bit 7) in register X+01H determines if the PRBS pattern is to be received framed or unframed. Enabling framing permits the PRBS pattern to be overwritten with the frame bits at the transmit framer an allows the frame bit positions to be ignored (interpreted as “don’t care”) at the receive framer. To run a PRBS pattern over just the payload, which holds the pattern while the framing bit is inserted and removes the frame bits for analysis, the DS0 feature described below is to be used. To perform the local PRBS test writing, a 1 to control bit SINPRBS (bit 0) in register X+107H enables the E1Fx8 to transmit an unframed E1 PRBS pattern to the receive data highway, RTDATn; control bit INPRBS (bit 0) in register X+106H must be set to a 0. Writing a 1 to control bit SPRBRE (bit 1) in register X+107H enables the analyzer to monitor the E1 stream received at the input to the Transmit Slip Buffer for a lock status (PRBS errors); control bit PRBRE (bit 1) in register X+106H must be set to a 0.

The E1Fx8 provides the ability to select one of four PRBS patterns; either a 2^{11}-1 pattern as defined in ITU-T O.152, a 2^{23}-1 pattern as defined in ITU-T O.151, a 2^{15}-1 pattern as defined in ITU-T O.151, and ANSI T1M1.3-005R1 (April 1993) or the 2^{20}-1 QRSS pattern as defined in T1M1.3-005R1 (April 1993), ITU-T O.151 and ANSI T1.403-1995/1997 can be selected. Control bits TTPRN2, TPRN1 and TPRN0 (bits 4, 3 and 2) in register X+109H select the particular test pattern to be sent and/or received; TPRN1 and TPRN0 = 11 is not valid for a full E1 test pattern generation.

The PRBS and test word analyzer provides an out of lock indication via status bit TPLOL (bit 5) in register X+129H which is latched in LTPLOL (bit 5) in register X+12AH. The indication is valid when the mode of the received signal and analyzer match (for framed or unframed). A global status bit GDSOTP (bit 5) in register 017H indicates if any of the eight framers has a latched out of lock event. An activity bit per framer is provided by status bits CHR1-CHR8 in register 019H. The global status and activity bits are cleared by writing a 0 to all of the set LTPOL bits. A mask bit MTPLOL (bit 5) in register X+12AH prevents an interrupt from being generated if set to a 1. The interrupt caused by an out of lock condition can also be masked by setting control bit

GMDS0TP (bit 5) in register 018H to a 1. A 16 bit error counter is provided which counts out of lock events which is designated TESTP14-TESTP0 in registers X+159H and X+15AH with TESTPO (bit 7) in register X+15AH being the most significant bit or overflow indicator. A latched value LTESTP14-LTESTP0 with LTESTPO in registers X+157H and X+158H being the most significant bit or overflow indicator is also provided which is updated on a one-second basis along with the other performance counters. This feature provides a simple error rate detector for an E1line or payload.

For applications of code word testing, such as placing a pattern in every time slot or group of time slots, the Time Slot Test Generator Analyzer described below may be used.

Time Slot Test Generation

The E1Fx8 supports the ability to generate a time slot PRBS pattern or a test pattern for each of the framers. With the wide variety of time slot loopbacks available, most any board level, system level or network level test can be supported. This feature is provided in addition to the E1 level Test pattern generator and analyzer, and functions the same at the individual time slot or Nx time slot level. The receive side is capable of monitoring the data stream for the PRBS pattern or test pattern for an out of lock status, and can count the number of out of lock times.

The Time Slot Test Generator uses the same control bits, TSRL32-TSRL1 in registers X+10AH through X+10DH that are used for selecting the time slots which are also used for sending the activate/deactivate DS0 Remote Loopback sequence. The Time Slot Test Generator also uses TSLL32-TSLL1 in register X+12DH through X+130H which are used to monitor DS0 loopbacks for sending system side patterns. The ability to transmit a time slot is valid when control bit TSRLOP (bit 7) in register X+109H is a 1. The ability to generate a time slot test sequence is disabled when control bit TSRLOP is a 0. The type of time slot test sequence that is generated depends on the values of control bits TPRN2, TPRN1 and TPRN0 (bits 4, 3 and 2) in register X+109H, as shown in the following table (where X=don't care).

E1/ Time Slot Test Pattern Selection

TPRN2	TPRN1	TRRN0	Action
X	0	0	Not used
0	0	1	QRSS pattern (2^{20}-1) pattern defined in T1M1.3-005R1 (April 1993), ITU-T O.151 and ANSI T1.403-1998, 1997
0	1	0	PRBS 2^{15}-1 pattern defined in ITU-T O.151, and T1M1.3-005R1 (April 1993)
X	1	1	Register Test Word (for time slot applications only)
1	0	1	PRBS 2^{11}-1 pattern defined in ITU-T O.152
1	1	0	PRBS 2^{23}-1 pattern defined in ITU-T O.151

The time slot test pattern selected by the control bits specified above is transmitted to the E1 line when control bit SPRN (bit 3) in register X+131H is written with a 1 for the time slots selected by control bits TSRL32-TSRL1 in registers X+10AH through X+10DH. The time slot test pattern selected by the control bits specified above is transmitted to the system side on RTDATn when control bit SSPRN (bit 1) in register X+131H is written with a 1 for the time slots selected by control bits TSLL32- TSLL1 in registers X+12DH through X+130H. The various insertion possibilities are shown in Figure 62 below.

Please note that the ability to send the DS0 remote loopback has a higher priority than sending the time slot test pattern. Thus, if control bit TRDSLP is written with a 1, the ability to send a test pattern is disabled until the four-second sequence is completed.

Time Slot Test Analyzer

The Time Slot Test Analyzer is enabled to monitor the output of the line decoder when control bit RTPAE (bit 2) in register X+131H is a 1. The Time Slot Test Analyzer is provided as a bridging function in addition to the circuit that is used to monitor the DS0 remote loopback sequence. The microprocessor writes the time slots that are to be monitored for the test pattern in control bits TSLL32-TSLL1 in registers X+12DH through X+130H. Please note that these bits are also used to select the time slots for the DS0 Remote Loopback activate and deactivate codes. The ability to monitor for a test pattern is independent of control bit TSRLOP.

The Time Slot Test Analyzer is enabled to monitor the input of the transmit slip buffer when control bit SRTPAE (bit 0) in register X+131H is a 1. The Time Slot Test Analyzer is provided as a bridging function. The microprocessor writes the time slots that are to be monitored for the test pattern in control bits TSRL32-TSRL1 in registers X+10AH through X+10DH.

When enabled, the test pattern that is to be monitored depends on the setting of the test pattern selection bits TPRN2, TPRN1, TPRN0, (bits 4, 3 and 2) in register X+109H. Please note that the transmitter must comply with the receiver for both the test pattern selected for proper operation when two different E1 ports are used. By the appropriate placement of the Time Slot Analyzer and Generator a variety of testing possibilities exist. The various insertion possibilities are shown in Figure 62 below.

When TPRN1 and TPRN0 are set to 11, the Test Word as defined in registers X+15BH through X+15EH is selected. This allows a mechanism by which the microprocessor slip buffer write option can be used as a test pattern generator; for example using the receive slip buffer to write a test word, the entire path through an application can be used to carry the test pattern which can then arrive at the transmit data highway of a E1Fx8; by placing the E1Fx8 in local loopback, the Time Slot Test Analyzer can verify the integrity of the path. The Time Slot Test Analyzer can also be used to monitor for network generated codes (e.g., idle).

The PRBS and test word analyzer provides an out of lock indication via status bit TPLOL (bit 5) in register X+129H which is latched in LTPLOL (bit 5) in register X+12AH. The indication is valid when the mode of the received signal and analyzer match (for framed or unframed). A global status bit GDSOTP (bit 5) in register 017H indicates if any of the eight framers has a latched out of lock event. An activity bit per framer is provided by status bits CHR1-CHR8 in register 019H. The global status and activity bits are cleared by writing a 0 to all of the set LTPOL bits. A mask bit MTPLOL (bit 5) in register X+12AH prevents an interrupt from being generated if set to a 1. The interrupt caused by an out of lock condition can also be masked by setting control bit GMDS0TP (bit 5) in register 018H to a 1. A 16 bit error counter is provided which counts out of lock events which is designated by TESTP14-TESTP0 in registers X+159H and X+15AH with TESTPO (bit 7) in register X+15AH being the most significant bit or overflow indicator. A latched value LTESTP14-LTESTP0 with LTESTPO in registers X+157H and X+158H being the most significant bit or overflow indicator is also provided which is updated on a one-second basis along with the other performance counters.

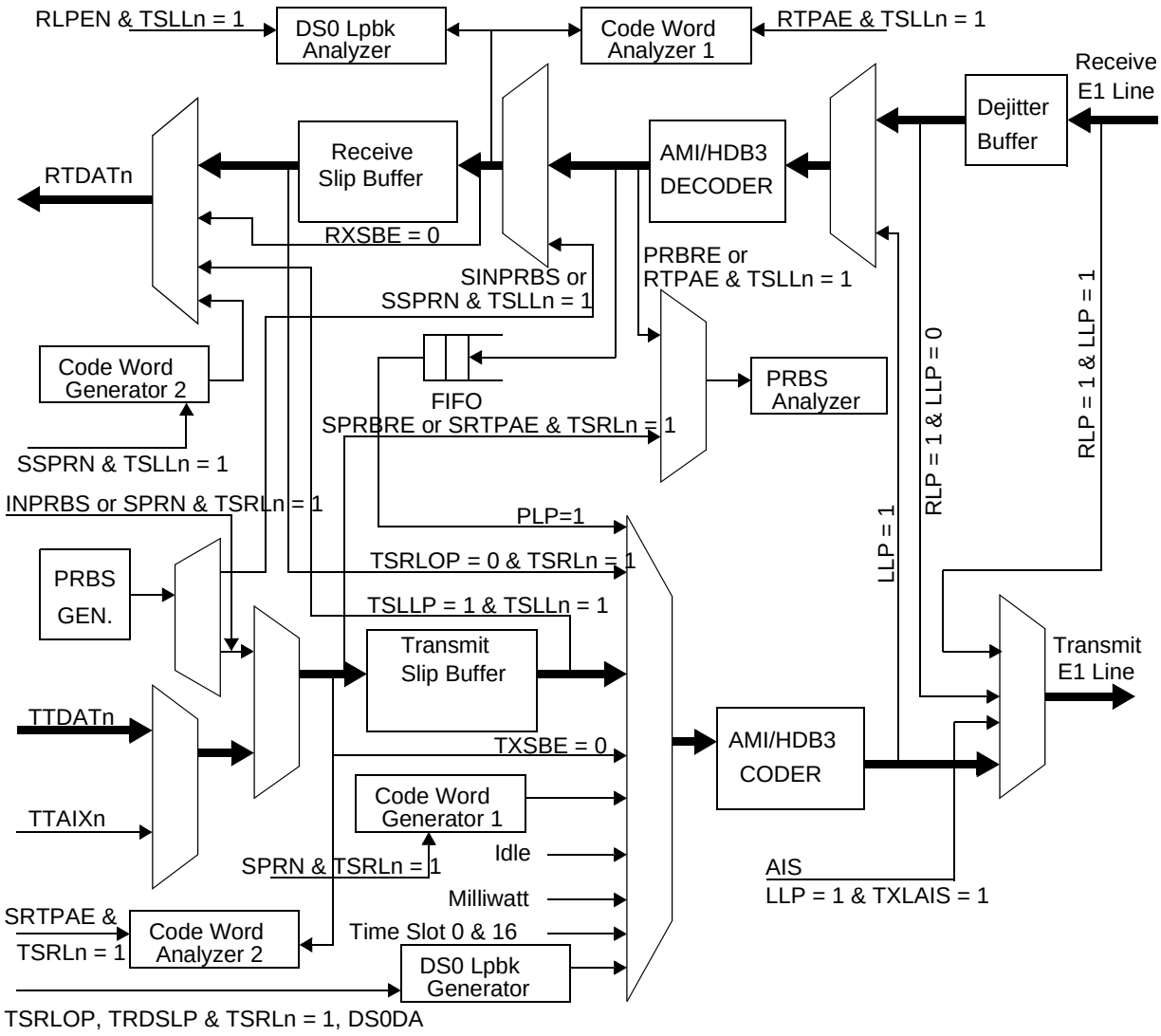


Figure 62. PRBS/ Code Word Generator/ Analyzer Options with Loopbacks

The following table lists the test features supported. Please refer to Figure 62 for the paths under test.

Loopback Modes with PRBS/ Code Word for the E1Fx8

Loopback Type	Description	External	Internal	Generator	Analyzer
Framed PRBS Remote E1	PRBS Generator through TX slip buffer, coder, line TX to RX or local loop and decoder to PRBS Analyzer.	Loop external line at local LIU or at far end.	LLP = 1	INPRBS = 1 TTFM = 0	PRBRE = 1 RTFM = 0

Loopback Modes with PRBS/ Code Word for the E1Fx8

Loopback Type	Description	External	Internal	Generator	Analyzer
Unframed PRBS Remote E1	PRBS Generator through TX slip buffer, coder, line TX to RX or local loop and decoder to PRBS Analyzer.	Loop external line at local LIU or at far end.	LLP = 1	INPRBS = 1 TTFM = 1	PRBRE = 1 RTFM = 1
Time Slot Remote PRBS	PRBS Generator through TX slip buffer, coder, line TX to RX or local loop and decoder to PRBS Analyzer.	Loop external line at local LIU or at far end.	LLP = 1	SPRN = 1 TSRLn = 1 for all time slots selected TTFM = 0 TPRN2-0 selects PRBS	RTPAE = 1 TSLLn = 1 for all time slots selected RTFM = 0 TPRN2-0 selects PRBS
Time Slot Remote Code Word	Code Word Generator (1) through coder, line TX to RX or local loop and decoder to Code Word Analyzer (1).	Loop external line at local LIU or at far end.	LLP = 1	SPRN = 1 TSRLn = 1 for all time slots selected TTFM = 0 TPRN2-0=x11	RTPAE = 1 TSLLn = 1 for all time slots selected RTFM = 0 TPRN2-0=x11
Local E1 PRBS all 32 Time Slots	PRBS Generator through RX slip buffer, RTDATn to TTDATn to PRBS Analyzer	Loop RTDATn to TTDATn		SINPRBS = 1 TPRN2-0 selects PRBS	SPRBRE = 1 TPRN2-0 selects PRBS
Time Slot Local PRBS	PRBS Generator through RX slip buffer, RTDATn to TTDATn to PRBS Analyzer	Loop RTDATn to TTDATn		SSPRN = 1 TSLLn = 1 for all time slots selected TPRN2-0 selects PRBS	SRTPAE = 1 TSRLn = 1 for all time slots selected TPRN2-0 selects PRBS
Time Slot Local Code Word	Code Word Generator (2) to RTDATn to TTDATn to Code Word Analyzer (2)	Loop RTDATn to TTDATn		SSPRN = 1 TSLLn = 1 for all time slots selected TPRN2-0=x11	SRTPAE = 1 TSRLn = 1 for all time slots selected TPRN2-0=x11
Board Test E1 PRBS Framed	PRBS Generator through RX slip buffer, RTDATn looped to TTDATn to TX slip buffer, to coder, line TX to RX or local loopback, to decoder, to PRBS Analyzer	Loop RTDATn to TTDATn Loop TX line to RX line at local LIU or at far end.	LLP = 1	SINPRBS = 1 TTFM = 0 TPRN2-0 selects PRBS	PRBRE = 1 RTFM = 0 TPRN2-0 selects PRBS

Loopback Modes with PRBS/ Code Word for the E1Fx8

Loopback Type	Description	External	Internal	Generator	Analyzer
Board Test E1 PRBS Unframed	PRBS Generator through RX slip buffer, RTDATn looped to TTDATn to TX slip buffer, to coder, line TX to RX or local loopback, to decoder, to PRBS Analyzer	Loop RTDATn to TTDATn Loop TX line to RX line at local LIU or at far end.	LLP = 1	SINPRBS = 1 TTFM = 1 TPRN2-0 selects PRBS	PRBRE = 1 RTFM = 1 TPRN2-0 selects PRBS
Board Test PRBS Time Slot	PRBS Generator through RX slip buffer, RTDATn looped to TTDATn to TX slip buffer, to coder, line TX to RX or local loopback, to decoder, to PRBS Analyzer	Loop RTDATn to TTDATn Loop TX line to RX line at local LIU or at far end.	LLP = 1	SSPRN = 1 TTFM = 0 TSLLn = 1 for all time slots selected TPRN2-0 selects PRBS	RTPAE = 1 RTFM = 0 TSLLn = 1 for all time slots selected TPRN2-0 selects PRBS
Board Test Code Word Time Slot	Code Word Generator to RTDATn looped to TTDATn to TX slip buffer, to coder, line TX to RX or local loopback, to decoder, to Code Word Analyzer	Loop RTDATn to TTDATn Loop TX line to RX line at local LIU or at far end.	LLP = 1	SSPRN = 1 TTFM = 0 TSLLn = 1 for all time slots selected TPRN2-0=x11	RTPAE = 1 RTFM = 0 TSLLn = 1 for all time slots selected TPRN2-0=x11
Self Test PRBS	PRBS Generator through RX slip buffer, remote time slot loopback to coder local loopback to decoder, to PRBS Analyzer		LLP = 1 TSRLOP = 0 TSRLn = 1 for all time slots selected	SSPRN = 1 TSLLn = 1 for all time slots selected TPRN2-0 selects PRBS	RTPAE = 1 TSLLn = 1 for all time slots selected TPRN2-0 selects PRBS

The following are highest to lowest priority for Loopbacks etc.: E1 PRBS (highest), Time Slot Remote Loopback, DS0 activate/deactivate, PRBS or Code Word insertion, Digital Milliwatt/ Idle Word and Normal Data.

High Impedance Test Mode

The E1Fx8 provides a lead to tristate all output drivers (except lead TBDO) to facilitate board testing. A low placed on lead $\overline{\text{HIGHZ}}$ provides this function.

E1 TANDEM FRAMING MONITORING FUNCTION

When control bit BPCRC4 (bit 7) in register X+08H is set to a 1, the signal present on RPOSn/RNRZn and RNEGn is looped to the Transmit Framer for output on TPOSn/TNRZn and TNEGn unaltered except for dejittering if the Dejitter Buffer is enabled, with any of the Sa4-Sa8 bits updated from local sources and with the CRC-4 updated only to account for the new Sa4-Sa8 bits. Control bits SA4UP through SA8UP (bits 6-2) in register X+08H when set to 1 select a local source for the National bits Sa4 - Sa8. The local source can be the HDLC controller (as selected by control bits SA4-SA8; bits 4-0 in register X+0CH), the Transmit Signaling Highway / Transmit Slip Buffer (as selected by control bit BNAL; bit 5 in register X+122H set to a 1 and control bits TSA4S-TSA8S; bits 4-0 in register X+E3H) or the Transmit Sa4-Sa8 Code Registers XSA47-XSA40 through XSA87-XSA80 in registers X+169H through X+16DH. The CRC-4 update is only done for the specific bits selected by SA4UP through SA8UP and follows the ITU-T G.706 (1995) Annex C recommendations. Figure 63 provides a functional overview of the E1 Tandem Monitoring function. For example, an E1 line can be monitored for alarms and the entire E1 signal received can be retransmitted except for Sa4 and Sa5 with Sa4 sourced from the code register XSA47-XSA40 for a G.704 synchronization code and Sa5 sourced from the HDLC controller. Only Sa4 and Sa5 bits are replaced (SA4UP = 1 and SA5UP = 1) and the CRC-4 for each sub-multiframe is updated to account for the changes introduced by Sa4 and Sa5. If bit errors have been introduced along the way, end-to-end CRC-4 checking will catch them and report block errors via the E-bits. For bidirectional performance monitoring and Sa4-Sa8 insertion, two E1 channels are required.

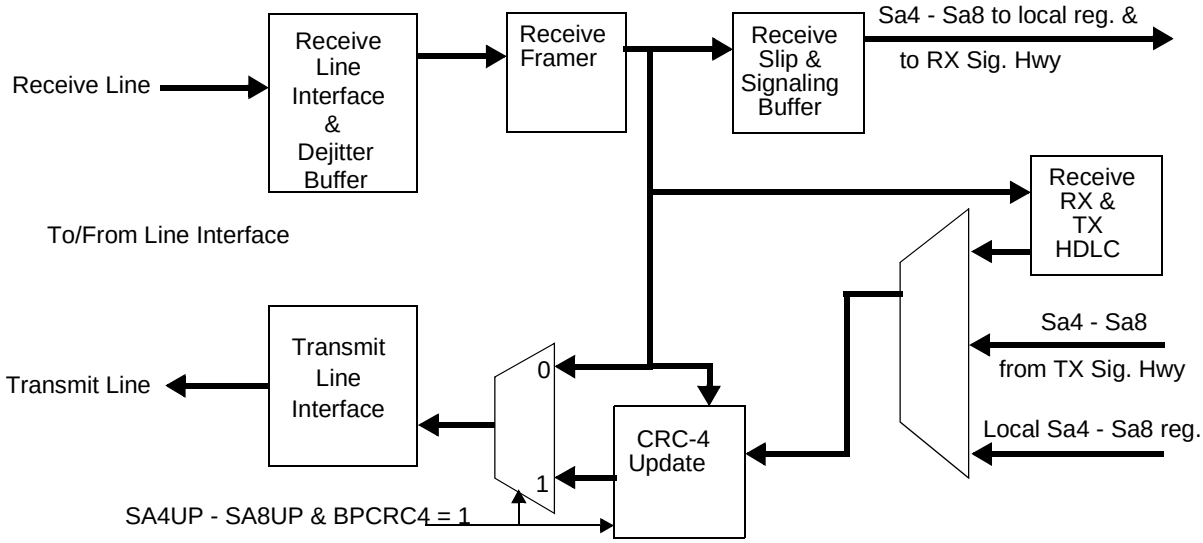


Figure 63. Tandem Frame Monitoring with National Bit Insertion

AUXILIARY PORT

For system applications that need to support ISDN PRI, ISDN BRI (multiplexed) or ITU G.964 V5.1 functionality, an auxiliary port is provided with 32 transmit and 32 receive 64 kbit/s time slots, each individually programmable to any receive or any transmit time slot (1 to 31) to or from any of the eight E1 framer channels on either the line or system side. Limited concatenation functionality is supplied if all time slots are contiguous. Setting control bit CONCATEN (bit 4) in register 037H to a 1 enables the concatenation capability for frame N (2 to 31) contiguous time slots to be sourced from a single E1 channel (same direction) and sent out the RADAT lead as contiguous time slots or sourced from the TADAT lead and sent to a single E1 channel (same direction) as contiguous time slots. Such connections will maintain correct byte sequence frame to frame and any slips to account for clock differences between the Auxiliary Port and the E1 channel will affect all time slots equally.

Each connection is passed through a FIFO function with independent depth control to account for line side or system side clock differences to the Auxiliary Port clock. Buffering is provided by this block to match this block's clock with the 16 transmit E1 and the 16 receive E1 line clock domains. For data output from this port on RADAT lead clock and frame reference, RACLK and RASYNC, may be an input or an output which is either derived from BPOSC lead or from either of the reference clock selection outputs. Control bits RACKSEL and RADIRSEL (bits 1 and 0) in register 037H determine the direction of the RACLK and RASYNC signals and whether BPOSC or a selected receive line is used as a clock source when these signals are outputs. Input data, clock and frame are provided by input leads TADAT, TACLK, and TASYNC. Control bits TACKSEL and TADIRSEL (bits 3 and 2) in register 037H determine the direction of the TACLK and TASYNC signals and whether BPOSC or a selected receive line is used as a clock source when these signals are outputs.

Figure 64 below shows the basic block diagram of the Auxiliary Port and how it is connected to each of the 8 channel blocks. The TX Data Selection Logic block operates off of the per framer channel timing and controls the insertion of time slots into the receive path or the transmit path. Control bits RDIR31 through RDIR0 in registers 038H through 03BH select which side of the framer each time slot for the Receive Auxiliary path is sourced; a 0 selects the decoder output and a 1 selects output of the Transmit Slip Buffer. Control bits RAFRSEL0(2-0)-RAFRSEL31(2-0) (bits 7-5) in registers 040H through 05FH selects the framer from which each time slot is sourced and control bits RATSSEL0(4-0)-RATSSEL31(4-0) (bits 4-0) in the same registers selects the time slot within the framer that sources the Receive Auxiliary Port time slot. Control bits TDIR31 through TDIR0 in registers 03CH through 03FH select which side of the framer each time slot from the Transmit Auxiliary Port is substituted; a 0 selects the Receive Slip Buffer input and a 1 selects the Coder input. Control bits TAFRSEL0(2-0)-TAFRSEL31(2-0) (bits 7-5) in registers 060H through 07FH selects the framer to which each time slot is supplied and control bits TATSSEL0(4-0)-TATSSEL31(4-0) (bits 4-0) in the same registers selects the time slot within the framer that is replaced by the Transmit Auxiliary Port time slot.

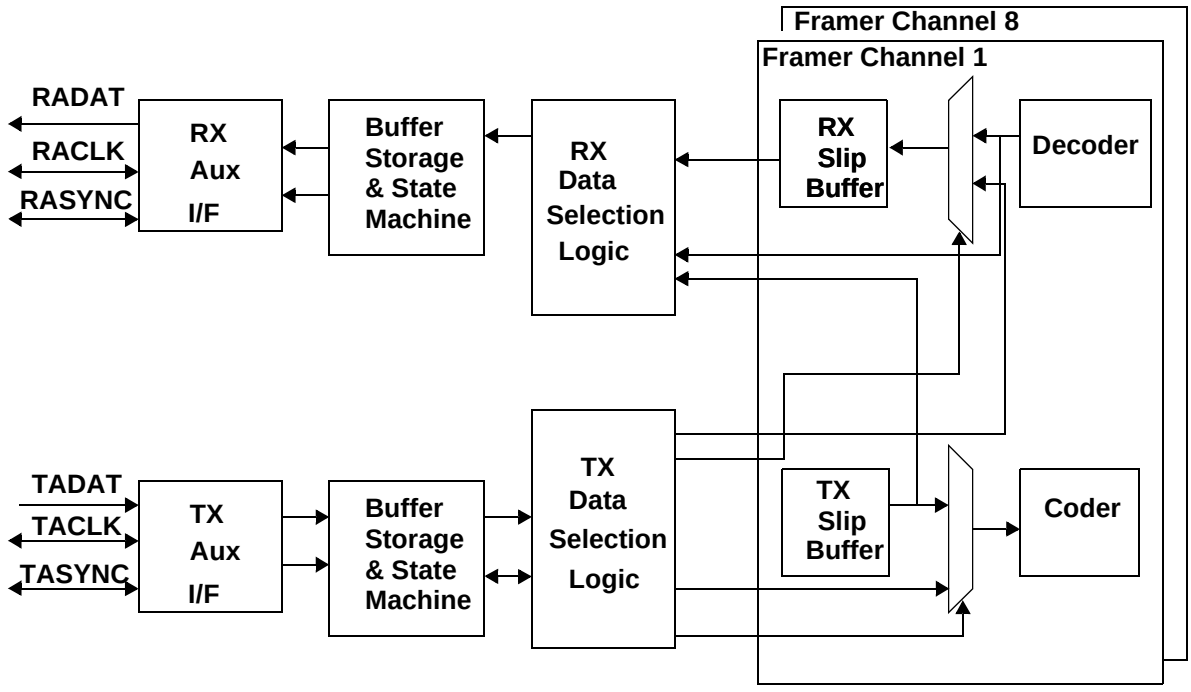


Figure 64. Auxiliary Port Connections

BOUNDARY SCAN

Introduction

The IEEE 1149.1 Standard defines the requirements of a boundary scan architecture that has been specified by the IEEE Joint Test Action Group (JTAG). Boundary scan is a specialized scan architecture that provides observability and controllability for the interface leads of the device. The Test Access Port block, which implements the boundary scan functions, consists of a Test Access Port (TAP) controller, instruction and data registers, and a boundary scan register path bordering the input and output leads, as illustrated in Figure 65. The boundary scan test bus interface consists of four input signals (i.e., the Test Clock (TBCK), Test Mode Select (TBMS), Test Data Input (TBDI) and Test Reset ($\overline{\text{TRS}}$) signals) and a Test Data Output (TBDO) output signal.

The TAP controller receives external control information via a Test Clock (TBCK) signal, a Test Mode Select (TBMS) signal, and a Test Reset ($\overline{\text{TRS}}$) signal, and it sends control signals to the internal scan paths. The scan path architecture consists of a two-bit serial instruction register and two or more serial data registers. The instruction and data registers are connected in parallel between the serial Test Data Input (TBDI) and Test Data Output (TBDO) signals. The Test Data Input (TBDI) signal is routed to both the instruction and data registers and is used to transfer serial data into a register during a scan operation. The Test Data Output (TBDO) is selected to send data from either register during a scan operation.

When boundary scan testing is not being performed, the boundary scan register is transparent, allowing the input and output signals at the device leads to pass to and from the E1Fx8 device's internal logic, as illustrated in Figure 65. During boundary scan testing, the boundary scan register disables the normal flow of input and output signals to allow the device to be controlled and observed via scan operations. A timing diagram for the boundary scan feature is provided in Figure 28.

Boundary Scan Support

The maximum frequency the E1Fx8 device will support for boundary scan is 10 MHz. The E1Fx8 device performs the following boundary scan test instructions:

- EXTEST
- SAMPLE/PRELOAD
- IDCODE
- BYPASS

EXTEST Test Instruction:

One of the required boundary scan tests is the external boundary test (EXTEST) instruction. When this instruction is shifted in, the E1Fx8 device is forced into an off-line test mode. While in this test mode, the test bus can shift data through the boundary scan registers to control the external E1Fx8 input and output leads.

SAMPLE/PRELOAD Test Instruction:

When the SAMPLE/PRELOAD instruction is shifted in, the E1Fx8 device remains fully operational. While in this test mode, E1Fx8 input data, and data destined for device outputs, can be captured and shifted out for inspection. The data is captured in response to control signals sent to the TAP controller.

BYPASS Test Instruction:

When the BYPASS instruction is shifted in, the E1Fx8 device remains fully operational. While in this test mode, a scan operation will transfer serial data from the TBDI input, through an internal scan cell, to the TBDO lead. The purpose of this instruction is to abbreviate the scan path through the circuits that are not being tested to only a single clock delay.

IDCODE Test Instruction:

The format of the IDCODE test instruction is "10".

Boundary Scan Reset

Specific control of the $\overline{TRS}$ lead is required in order to ensure that the boundary scan logic does not interfere with normal device operation. This lead must either be held low, asserted low, or asserted low then high (pulsed low), to asynchronously reset the Test Access Port (TAP) controller during power-up of the E1Fx8. If boundary scan testing is to be performed and the lead is held low, then a pulldown resistor value should be chosen which will allow the tester to drive this lead high, but still meet the V_{IL} requirements listed in the 'Input, Output and Input/Output Parameters' section of this Data Sheet for worst case leakage currents of all devices sharing this pull-down resistor.

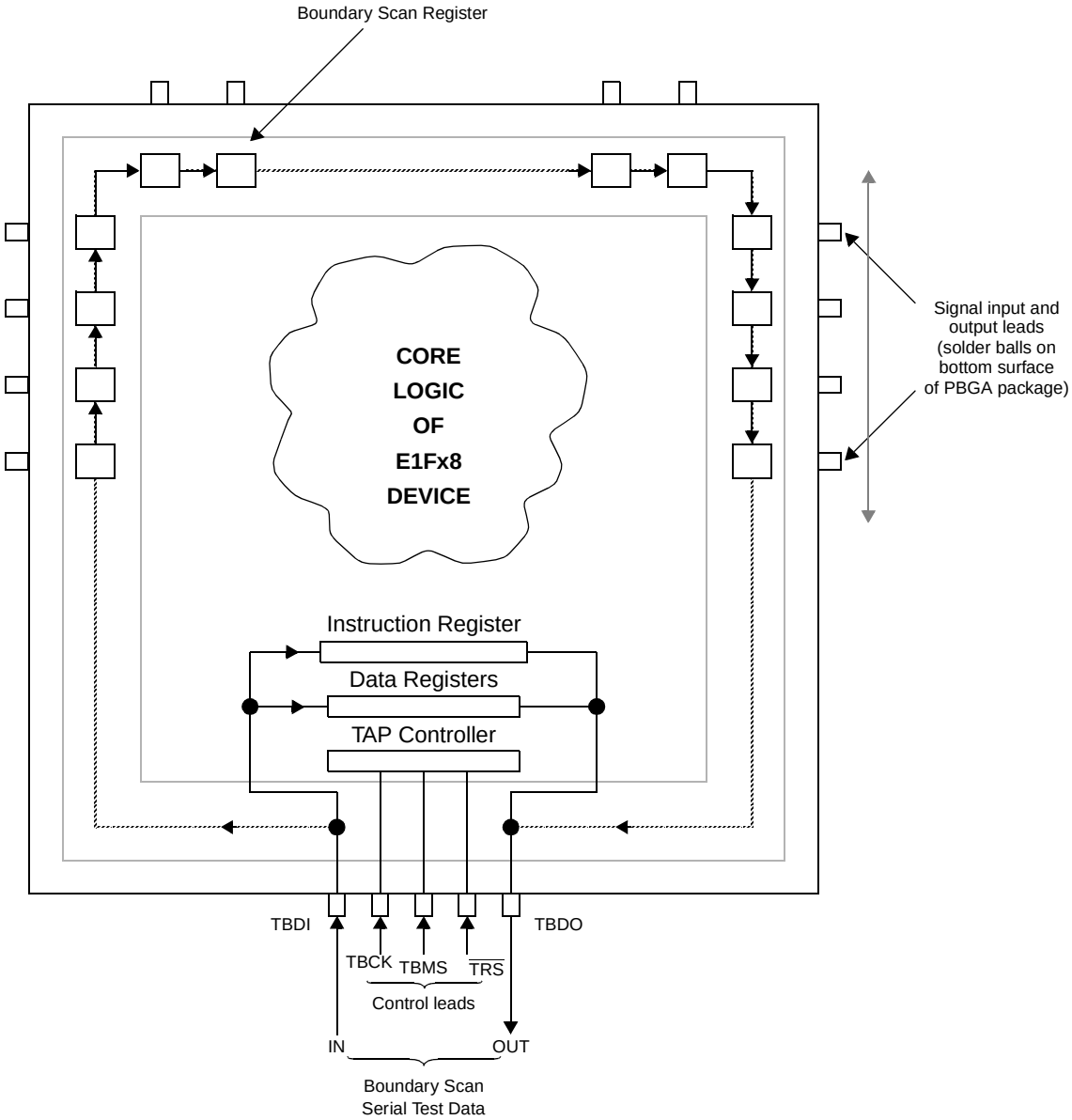


Figure 65. Boundary Scan Schematic

Boundary Scan Chain

There are 297 scan cells in the E1Fx8 boundary scan chain. The chain is the same in the 256-lead and 208-lead versions except that access to selected leads in the 208-lead version is not available. Bidirectional device leads require two scan cells. Additional scan cells are used for direction control as needed. The following table shows the listed order of the scan cells and their functions. Cells that are not associated with a lead are marked "NA"; I/O marked “internal” are scan cells for internal leads not brought to balls. BSDL files are made available via the Product Software page of the TranSwitch Internet World Wide Web site at www.transwitch.com as they are released.

Scan Cell No.	I/O	Lead No. 208 Pkg.	Lead No. 256 Pkg.	Lead Symbol	Comments
296	INTERNAL	NA	NA		
295	INPUT	B4	C5	RCLK1	
294	INPUT	A4	A4	RPOS1	
293	INPUT	C4	B5	RNEG1	
292	INTERNAL	NA	NA		
291	OUTPUT3	B5	C6	TNEG1	
290	OUTPUT3	A5	D7	TPOS1	
289	OUTPUT3	C5	A5	TCLK1	
288	OUTPUT3	D5	B6	$\overline{\text{LCS1}}$	
287	INTERNAL	NA	NA		
286	OUTPUT3	B6	C7	RTCLK1	
285	INPUT	B6	C7	RTCLK1	
284	OUTPUT3	A6	A6	RTFRM1	
283	INPUT	A6	A6	RTFRM1	
282	OUTPUT3	D6	B7	RTSIG1	
281	OUTPUT3	D6	A7	RTAUX1	
280	INPUT	B7	C8	E208	
279	INPUT	A7	B8	CONF0	
278	CONTROL	NA	NA	TFT1CG_ENB1	A 0 makes lead TTSIG1 an output
277	INPUT	C7	A8	CONF1	
276	OUTPUT3	D7	D9	RTDAT1	
275	INPUT	B8	C9	TTAIX1	
274	INPUT	A8	B9	TTDAT1	
273	OUTPUT3	C8	A9	TTAUX1	
272	CONTROL	NA	NA	RXC1	A 0 makes leads RTFRM1 and RTCLK1 outputs
271	OUTPUT3	C8	D10	TTSIG1	
270	INPUT	C8	D10	TTSIG1	
269	INPUT	D9	C10	TTFRM1	

Scan Cell No.	I/O	Lead No. 208 Pkg.	Lead No. 256 Pkg.	Lead Symbol	Comments
268	INPUT	C9	B10	TTCLK1	
267	CONTROL	NA	NA	TFT1CG_ENB2	A 0 makes lead TTSIG2 an output
266	INPUT	B9	A10	MOTO	
265	OUTPUT3	A9	A11	RTCLK2	
264	INPUT	A9	A11	RTCLK2	
263	OUTPUT3	D10	C11	RTFRM2	
262	INPUT	D10	C11	RTFRM2	
261	OUTPUT3	C10	B11	RTSIG2	
260	OUTPUT3	C10	A12	RTAUX2	
259	OUTPUT3	A10	B12	RTDAT2	
258	INPUT	B10	C12	TTAIX2	
257	CONTROL	NA	NA	RXC2	A 0 makes leads RTFRM2 and RTCLK2 outputs
256	INPUT	D11	D12	TTDAT2	
255	OUTPUT3	C11	A13	TTAUX2	
254	OUTPUT3	C11	B13	TTSIG2	
253	INPUT	C11	B13	TTSIG2	
252	INPUT	A11	C13	TTFRM2	
251	INPUT	B11	A14	TTCLK2	
250	CONTROL	NA	NA	TFTICG_ENB3	A 0 makes lead TTSIG3 an output
249	OUTPUT3	D12	B14	RTCLK3	
248	INPUT	D12	B14	RTCLK3	
247	OUTPUT3	C12	C14	RTFRM3	
246	INPUT	C12	C14	RTFRM3	
245	OUTPUT3	A12	A15	RTSIG3	
244	OUTPUT3	A12	B15	RTAUX3	
243	OUTPUT3	D13	D14	RTDAT3	
242	INPUT	A13	C15	TTAIX3	
241	INPUT	C13	A16	TTDAT3	
240	CONTROL	NA	NA	RXC3	A 0 makes leads RTFRM3 and RTCLK3 outputs
239	OUTPUT3	B13	B16	TTAUX3	
238	OUTPUT3	B13	C16	TTSIG3	
237	INPUT	B13	C16	TTSIG3	
236	INPUT	A14	A17	TTFRM3	
235	INPUT	B14	A18	TTCLK3	

Scan Cell No.	I/O	Lead No. 208 Pkg.	Lead No. 256 Pkg.	Lead Symbol	Comments
234	OUTPUT3	A15	D16	RTCLK4	
233	INPUT	A15	D16	RTCLK4	
232	CONTROL	NA	NA	TXAUX_EN	A 0 makes leads TACLK and TASYNC outputs
231	OUTPUT3	NA	C17	TACLK	
230	INPUT	NA	C17	TACLK	Input with pull-up
229	OUTPUT3	C14	B17	RTFRM4	
228	INPUT	C14	B17	RTFRM4	
227	CONTROL	NA	NA	RXAUX_EN	A 0 makes leads RACLK and RASYNC outputs
226	OUTPUT3	NA	A19	RACLK	
225	INPUT	NA	A19	RACLK	Input with pull-up
224	OUTPUT3	NA	A20	RASYNC	
223	INPUT	NA	A20	RASYNC	Input with pull-up
222	OUTPUT3	NA	C18	TASYNC	
221	INPUT	NA	C18	TASYNC	Input with pull-up
220	CONTROL	NA	NA	DPLLREF_EN	A 0 makes lead DPLLREF an output
219	OUTPUT3	A16	B20	DPLLREF	
218	INPUT	A16	B20	DPLLREF	
217	OUTPUT3	B16	C19	RTSIG4	
216	INPUT	NA	D18	TADAT	Input with pull-up
215	OUTPUT3	B16	E17	RTAUX4	
214	OUTPUT3	C16	C20	RTDAT4	
213	INPUT	D16	D19	TTAIX4	
212	CONTROL	NA	NA	RXC4	A 0 makes leads RTFRM4 and RTCLK4 outputs
211	INPUT	D15	E18	TTDAT4	
210	OUTPUT3	D14	D20	TTAUX4	
209	CONTROL	NA	NA	TFTICG_ENB4	A 0 makes lead TTSIG4 an output
208	OUTPUT3	D14	E19	TTSIG4	
207	INPUT	D14	E19	TTSIG4	
206	INPUT	E15	F18	TTFRM4	
205	INPUT	E16	G17	TTCLK4	
204	OUTPUT3	E13	E20	MONFRM	
203	OUTPUT3	E13	F19	LSDI	
202	INPUT	E13	F19	LSDI	

Scan Cell No.	I/O	Lead No. 208 Pkg.	Lead No. 256 Pkg.	Lead Symbol	Comments
201	CONTROL	NA	NA	MONFRM_EN	A 0 enables lead LSDI to be an output
200	OUTPUT3	F15	G18	SCOUT2	
199	CONTROL	NA	NA	EN_REF_CLK2	A 0 enables lead SCOUT2 to be an output
198	INPUT	F16	F20	$\overline{\text{HIGHZ}}$	
197	INTERNAL	NA	NA		
196	INPUT	F14	G19	BPOSC	
195	OUTPUT3	NA	G20	RADAT	
194	OUTPUT3	F13	H18	MONCLK	
193	OUTPUT3	F13	H19	LSCLK	
192	OUTPUT3	G15	H20	MONDAT	
191	CONTROL	NA	NA	MON_EN	A 0 enables leads MONDAT, MONFRM and MONCLK to be outputs
190	OUTPUT3	G15	J17	LSDO	
189	CONTROL	NA	NA	SPMON_EN	A 0 enables leads LSDO and LSCLK to be outputs
188	OUTPUT3	G16	J18	D7	
187	INPUT	G16	J18	D7	
186	OUTPUT3	G13	J19	D6	
185	INPUT	G13	J19	D6	
184	OUTPUT3	H15	J20	D5	
183	INPUT	H15	J20	D5	
182	OUTPUT3	H16	K17	D4	
181	INPUT	H16	K17	D4	
180	CONTROL	NA	NA	DT_EN	A 0 makes leads D0 through D7 outputs
179	OUTPUT3	H13	K18	D3	
178	INPUT	H13	K18	D3	
177	OUTPUT3	J13	K19	D2	
176	INPUT	J13	K19	D2	
175	INPUT	J14	L20	$\overline{\text{WR}}$	
174	OUTPUT3	J15	L18	D1	
173	INPUT	J15	L18	D1	
172	OUTPUT3	K13	L19	D0	
171	INPUT	K13	L19	D0	
170	INPUT	K14	M20	$\overline{\text{RD}}$	

Scan Cell No.	I/O	Lead No. 208 Pkg.	Lead No. 256 Pkg.	Lead Symbol	Comments
169	INPUT	K16	M19	$\overline{SEL}$	
168	OUTPUT3	K15	M18	RDY/$\overline{DTACK}$	
167	INTERNAL	NA	NA		
166	CONTROL	NA	NA	RDY_EN	A 0 enables lead RDY/$\overline{DTACK}$ to be an output
165	INTERNAL	NA	NA		Internal input with pull-down
164	OUTPUT3	L13	M17	INT/$\overline{IRQ}$	
163	INPUT	L14	N20	$\overline{RESET}$	
162	INTERNAL	NA	NA		
161	INPUT	L16	N19	A0	
160	INPUT	L15	N18	A1	
159	INPUT	M13	P19	A2	
158	INPUT	M14	P18	A3	
157	INPUT	M16	R20	A4	
156	INPUT	M15	R19	A5	
155	INPUT	N16	P17	A6	
154	INPUT	N14	R18	A7	
153	INPUT	N15	T19	A8	
152	INPUT	P16	T18	A9	
151	INPUT	P15	U20	A10	
150	INPUT	R16	V20	A11	
149	INTERNAL	NA	NA		Internal input with pull-down
148	INTERNAL	NA	NA		Internal input with pull-down
147	INTERNAL	NA	NA		Internal input with pull-down
146	INPUT	P14	U19	A12	
145	INTERNAL	NA	NA		Internal input with pull-down
144	INTERNAL	NA	NA		Internal input with pull-down
143	INTERNAL	NA	NA		Internal input with pull-down
142	OUTPUT3	R15	V18	SCOUT1	
141	CONTROL	NA	NA	EN_REF_CLK1	A 0 enables lead SCOUT1 to be an output
140	CONTROL	NA	NA	S1EXT_B	A 0 enables lead SREGT to be an output
139	OUTPUT3	T16	W18	SREGT	
138	INPUT	T16	W18	SREGT	
137	OUTPUT3	T15	V17	RTCLK5	

Scan Cell No.	I/O	Lead No. 208 Pkg.	Lead No. 256 Pkg.	Lead Symbol	Comments
136	INPUT	T15	V17	RTCLK5	
135	OUTPUT3	R14	U16	RTFRM5	
134	INPUT	R14	U16	RTFRM5	
133	OUTPUT3	T14	Y18	RTSIG5	
132	CONTROL	NA	NA	RXC5	A 0 makes leads RTFRM5 and RTCLK5 outputs
131	OUTPUT3	T14	W17	RTAUX5	
130	OUTPUT3	T13	V16	RTDAT5	
129	INPUT	R13	Y17	TTAIX5	
128	INPUT	R12	W16	TTDAT5	
127	OUTPUT3	T12	V15	TTAUX5	
126	OUTPUT3	T12	U14	TTSIG5	
125	INPUT	T12	U14	TTSIG5	
124	CONTROL	NA	NA	TFT1CG_ENB5	A 0 makes lead TTSIG5 an output
123	INPUT	P12	Y16	TTFRM5	
122	INPUT	N12	W15	TTCLK5	
121	OUTPUT3	R11	V14	RTCLK6	
120	INPUT	R11	V14	RTCLK6	
119	OUTPUT3	T11	Y15	RTFRM6	
118	INPUT	T11	Y15	RTFRM6	
117	CONTROL	NA	NA	RXC6	A 0 makes leads RTFRM6 and RTCLK6 outputs
116	OUTPUT3	P11	W14	RTSIG6	
115	OUTPUT3	P11	Y14	RTAUX6	
114	OUTPUT3	N11	V13	RTDAT6	
113	INPUT	R10	W13	TTAIX6	
112	INPUT	T10	Y13	TTDAT6	
111	OUTPUT3	R9	U12	TTAUX6	
110	INPUT	P10	V12	$\overline{\text{TEST}}$	
109	OUTPUT3	R9	W12	TTSIG6	
108	INPUT	R9	W12	TTSIG6	
107	INPUT	T9	Y12	TTFRM6	
106	CONTROL	NA	NA	TFT1CG_ENB6	A 0 makes lead TTSIG6 an output
105	INPUT	P9	U11	TTCLK6	
104	OUTPUT3	N8	V11	RTCLK7	
103	INPUT	N8	V11	RTCLK7	

Scan Cell No.	I/O	Lead No. 208 Pkg.	Lead No. 256 Pkg.	Lead Symbol	Comments
102	OUTPUT3	P8	W11	RTFRM7	
101	INPUT	P8	W11	RTFRM7	
100	CONTROL	NA	NA	RXC7	A 0 makes leads RTFRM7 and RTCLK7 outputs
99	OUTPUT3	T8	Y11	RTSIG7	
98	OUTPUT3	T8	Y10	RTAUX7	
97	OUTPUT3	R8	V10	RTDAT7	
96	INPUT	N7	W10	TTAIX7	
95	CONTROL	NA	NA	TFT1CG_ENB7	A 0 makes lead TTSIG7 an output
94	INPUT	P7	Y9	TTDAT7	
93	OUTPUT3	T7	W9	TTAUX7	
92	OUTPUT3	T7	V9	TTSIG7	
91	INPUT	T7	V9	TTSIG7	
90	INPUT	R7	U9	TTFRM7	
89	INPUT	N6	Y8	TTCLK7	
88	OUTPUT3	P6	W8	RTCLK8	
87	INPUT	P6	W8	RTCLK8	
86	OUTPUT3	T6	V8	RTFRM8	
85	INPUT	T6	V8	RTFRM8	
84	CONTROL	NA	NA	RXC8	A 0 makes leads RTFRM8 and RTCLK8 outputs
83	OUTPUT3	R6	Y7	RTSIG8	
82	OUTPUT3	R6	W7	RTAUX8	
81	OUTPUT3	N5	V7	RTDAT8	
80	INPUT	P5	Y6	TTAIX8	
79	INPUT	R5	W6	TTDAT8	
78	OUTPUT3	N4	U7	TTAUX8	
77	CONTROL	NA	NA	TFT1CG_ENB8	A 0 makes lead TTSIG8 an output
76	OUTPUT3	N4	V6	TTSIG8	
75	INPUT	N4	V6	TTSIG8	
74	INPUT	T4	Y5	TTFRM8	
73	INPUT	P4	W5	TTCLK8	
72	INPUT	R4	V5	RCLK8	
71	INPUT	T3	Y4	RPOS8	
70	INPUT	R3	Y3	RNEG8	
69	INPUT	T2	U5	SYSCI	

Scan Cell No.	I/O	Lead No. 208 Pkg.	Lead No. 256 Pkg.	Lead Symbol	Comments
68	INTERNAL	NA	NA		
67	OUTPUT3	P3	W4	TNEG8	
66	INTERNAL	NA	NA		
65	INTERNAL	NA	NA		
64	OUTPUT3	R2	V2	TPOS8	
62	OUTPUT3	T1	T4	TCLK8	
61	OUTPUT3	R1	V1	$\overline{\text{LCS8}}$	
60	INTERNAL	NA	NA		
59	INPUT	P2	T3	RCLK7	
58	INPUT	P1	U1	RPOS7	
57	INPUT	N1	T2	RNEG7	
56	OUTPUT3	N3	R3	TNEG7	
55	OUTPUT3	M2	P4	TPOS7	
54	OUTPUT3	M1	T1	TCLK7	
53	OUTPUT3	M3	R2	$\overline{\text{LCS7}}$	
52	INTERNAL	NA	NA		
51	INPUT	M4	R1	RCLK6	
50	INPUT	L2	P2	RPOS6	
49	INPUT	L1	P1	RNEG6	
48	INTERNAL	NA	NA		
47	OUTPUT3	L3	N3	TNEG6	
46	OUTPUT3	L4	N2	TPOS6	
45	OUTPUT3	K2	N1	TCLK6	
44	INTERNAL	NA	NA		
43	OUTPUT3	K1	M4	$\overline{\text{LCS6}}$	
42	INTERNAL	NA	NA		
41	INPUT	K3	M3	RCLK5	
40	INPUT	K4	M2	RPOS5	
39	INPUT	J2	M1	RNEG5	
38	INTERNAL	NA	NA		
37	OUTPUT3	J1	L4	TNEG5	
36	OUTPUT3	J3	L3	TPOS5	
35	OUTPUT3	J4	L2	TCLK5	
34	INTERNAL	NA	NA		
33	OUTPUT3	H4	K1	$\overline{\text{LCS5}}$	

Scan Cell No.	I/O	Lead No. 208 Pkg.	Lead No. 256 Pkg.	Lead Symbol	Comments
32	INTERNAL	NA	NA		
31	INPUT	H3	K3	RCLK4	
30	INPUT	H1	K2	RPOS4	
29	INPUT	H2	J1	RNEG4	
28	INTERNAL	NA	NA		
27	OUTPUT3	G4	J2	TNEG4	
26	OUTPUT3	G3	J3	TPOS4	
25	OUTPUT3	G1	J4	TCLK4	
24	INTERNAL	NA	NA		
23	OUTPUT3	G2	H1	$\overline{\text{LCS4}}$	
22	INTERNAL	NA	NA		
21	INPUT	F4	H2	RCLK3	
20	INPUT	F3	H3	RPOS3	
19	INPUT	F1	G1	$\overline{\text{PWDN}}$	
18	INPUT	F2	G2	RNEG3	
17	OUTPUT3	E4	G3	TNEG3	
16	OUTPUT3	E3	F1	TPOS3	
15	OUTPUT3	E1	F2	TCLK3	
14	INTERNAL	NA	NA		
13	INTERNAL	NA	NA		
12	OUTPUT3	D4	G4	$\overline{\text{LCS3}}$	
11	INTERNAL	NA	NA		
10	INPUT	D1	F3	RCLK2	
9	INPUT	D3	E1	RPOS2	
8	INPUT	D2	E2	RNEG2	
7	OUTPUT3	C2	E3	TNEG2	
6	OUTPUT3	C1	D1	TPOS2	
5	INTERNAL	NA	NA		
4	OUTPUT3	B1	C1	TCLK2	
3	INTERNAL	NA	NA		
2	OUTPUT3	C3	D2	$\overline{\text{LCS2}}$	
1	INTERNAL	NA	NA		
0	CONTROL	NA	NA	IOTRI_B	A 1 enables the outputs of I/O type OUTPUT3

RESET PROCEDURE

After power-up the E1Fx8 requires a hardware reset. This reset will reset all the per channel control registers in the memory map. It will also reset all of the global registers at addresses 004H through 0FFH. A low placed on the $\overline{\text{RESET}}$ lead for at least 10 cycles of SYSCI after all clocks become stable will accomplish the hardware reset. After applying a hardware reset, the entire set of control registers must be programmed to the desired configuration.

A global software reset is also available and should be applied at least 40 ms after power-up. This resets the internal state machines; it does not change the state of any of the control registers, performance counters or shadow registers. Writing a 1 to control bit RESET (bit 7) in register 00AH places the E1Fx8 in a reset state. Writing a 0 to control bit RESET will take the E1Fx8 out of the reset state. The RESET bit can be read to determine the reset state of the E1Fx8. A value of 80H in register 00AH indicates the E1Fx8 is in a reset state; a value of 00H indicates the E1Fx8 is not in reset. A per channel version of this function is available by writing a 1 to control bit SRST (bit 7) in register X+0AH followed by writing a 0 to control bit SRST. Note that all the memory locations at addresses X+40H through X+1FFH are located in a per channel internal RAM and are not reset by either a hardware reset or a software reset.

Changing the mode of operation of a framer, which includes initializing the framer for the first time after power-up, should be followed by a per channel software reset (SRST). The mode bits can be found in framer per channel registers X+00H through X+0AH. Not resetting the framer after changing most mode control bits will have minimal effect. However, if control bits BFAA, CRCA, OOF1, OOF0, AAGS (bits 5 and 3-0 in register X+01H), CRCMD1, CRCMD0 (bits 3 and 2 in register X+07H) and AIW (bit 0 in register X+0AH) are changed, a per channel reset procedure is required.

If not all 8 channels of the E1Fx8 are implemented in an application, the channels that are not used should be powered down (control bit PWRD, bit 7 in register X+05H is set to a 1) and all interrupts masked (registers X+14H and X+166H are set to FFH).

MEMORY MAP

The E1Fx8 memory map contains registers and counters which may be accessed by the microprocessor. Addresses which are shown as spare, or which are not listed in the memory map, must not be accessed by the microprocessor. The status designation R indicates a read-only unlatched register location, R(L) a read-only latched register location, W a write-only register location and R/W a read/write register location. R and R(L) register bit positions designated as Reserved (R) will read out an indeterminate value unless a 0 or 1 read value is indicated. Some RW Reserved (R) bit positions do not exist (i.e., they have no memory associated with them), so that any values written to these bits cannot be read. Those that do have associated memory should be written to 0, as indicated in the following tables. RW Reserved (R) bit positions should not be used for storage of any application information.

COMMON REGISTERS

Device ID Registers (See Descriptions on page 179)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
000	R	1	1	0	1	0	1	1	1
001	R	0	1	0	1	0	0	0	0
002	R	1	1	0	0	0	0	1	0
003	R	0	0	0	1	0	0	0	0

Customer Notebook Registers (See Descriptions on page 179)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
004 to 009	RW	User Defined Register (e.g., scratch pad)							

Global Software Reset Register (See Descriptions on page 179)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00A	R/W	RESET	Reserved, set to 0						

Global Configuration Registers (See Descriptions on page 180)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00B	R/W	RISE	FALL	GIM	IPOL	SRGEN	HWMEN	DINTF	R = 0

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00C	R/W	S1CIEN	SYNLF	ENAISI	Reserved, set to 0				
00D	R/W	Spare							
00E	R/W	Spare							
00F	R/W	Spare							
010	R/W	Spare							

Global Status, Mask and Pointer Registers (See Descriptions on page 181)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
011	R	GLOS	GAIS	GOOF	GRAI	GCFA	GOOMF	GSLIP	GSCHG
012	R/W	GMLOS	GMAIS	GMOOF	GMRAI	GMCFA	GMOOMF	GMSLIP	GMSCHG
013	R/W	Spare							
014	R	CHL8	CHL7	CHL6	CHL5	CHL4	CHL3	CHL2	CHL1
015	R/W	Spare							
016	R	CHD8	CHD7	CHD6	CHD5	CHD4	CHD3	CHD2	CHD1
017	R	GDS0RS	GDS0DC	GDS0TP	GDS0TC	GINTACT	GINTDCT	GOVERF	GUNDERF
018	R/W	GMDS0RS	GMDS0DC	GMDS0TP	GMDS0TC	GMINTACT	GMINTDCT	GMOVERF	GMUNDERF
019	R	CHR8	CHR7	CHR6	CHR5	CHR4	CHR3	CHR2	CHR1
01A	R	R	GAIS16	GCRCE	GRAI16	R	GOOM16	R = 0	GAUXP
01B	R/W	R=0	GMAIS16	GMCRCE	GMRAI16	R=0	GMOOM16	R = 0	GMAUXP
01C	R	CHS8	CHS7	CHS6	CHS5	CHS4	CHS3	CHS2	CHS1

Line Interface Control Registers (See Descriptions on page 186)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01D	R/W	BDCST	ESP	ESPBMON	Reserved, set to 0		E1CHS2	E1CHS1	E1CHS0
01E	R/W	LCB7 - LCB0 (Command Byte)							
01F	R/W	LDO7 - LDO0 (Data Output to LIU)							
020	R	LDI7 - LDI0 (Data Input to LIU)							
021	R/W	Spare							

Monitor Control Register (See Descriptions on page 187)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
022	R/W	MONRX	MONRF	MONTR	Reserved, set to 0		MFR2	MFR1	MFR0
023	R/W	Spare							

Synchronization Control Registers (See Descriptions on page 188)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
024	R/W	S18KHZ	S1CTRI	S1YNCEN	S1SEXTB	S1SINT	S1YNC2	S1YNC1	S1YNC0
025	R/W	S28KHZ	S2CTRI	S2YNCEN	Reserved, set to 0		S2YNC2	S2YNC1	S2YNC0
026-029	R/W	Spare							

Loss of Signal Detection Interval, Ones Density and Code for RAI, and AIS (Trunk Condition) Registers (See Descriptions on page 190)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
02A	R/W	LOSI7 -LOSI0							
02B	R/W	ENLOSI	R = 0	OND5 -OND0					
02C	R/W	CODERAI(3-0)				CODEAIS(3-0)			
02D	R/W	Spare							

Receive and Transmit Framing Pulse (Sync) Delay Control Registers (See Descriptions on page 191)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
02E	R/W	RFRM7-RFRM0 (Frame Pulse Delay, RFRM7 = bit 7)							
02F	R/W	TFRM7-TFRM0 (Frame Pulse Delay, TFRM7 = bit 7)							
030	R	Spare							

Auxiliary Port Clock Selection and Time Slot Direction Registers (See Descriptions on page 191)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
037	R/W	Reserved, set to 0			CONCATEN	TACKSEL	TADIRSEL	RACKSEL	RADIRSEL

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
038	R/W	RDIR7	RDIR6	RDIR5	RDIR4	RDIR3	RDIR2	RDIR1	RDIR0
039	R/W	RDIR15	RDIR14	RDIR13	RDIR12	RDIR11	RDIR10	RDIR9	RDIR8
03A	R/W	RDIR23	RDIR22	RDIR21	RDIR20	RDIR19	RDIR18	RDIR17	RDIR16
03B	R/W	RDIR31	RDIR30	RDIR29	RDIR28	RDIR27	RDIR26	RDIR25	RDIR24
03C	R/W	TDIR7	TDIR6	TDIR5	TDIR4	TDIR3	TDIR2	TDIR1	TDIR0
03D	R/W	TDIR15	TDIR14	TDIR13	TDIR12	TDIR11	TDIR10	TDIR9	TDIR8
03E	R/W	TDIR23	TDIR22	TDIR21	TDIR20	TDIR19	TDIR18	TDIR17	TDIR16
03F	R/W	TDIR31	TDIR30	TDIR29	TDIR28	TDIR27	TDIR26	TDIR25	TDIR24

Auxiliary Port Receive and Transmit Data Selection Registers (See Descriptions on page 192)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
040	R/W	RAFRSEL0(2-0)			RATSSEL0(4-0)				
041	R/W	RAFRSEL1(2-0)			RATSSEL1(4-0)				
042	R/W	RAFRSEL2(2-0)			RATSSEL2(4-0)				
043	R/W	RAFRSEL3(2-0)			RATSSEL3(4-0)				
044	R/W	RAFRSEL4(2-0)			RATSSEL4(4-0)				
045	R/W	RAFRSEL5(2-0)			RATSSEL5(4-0)				
046	R/W	RAFRSEL6(2-0)			RATSSEL6(4-0)				
047	R/W	RAFRSEL7(2-0)			RATSSEL7(4-0)				
048	R/W	RAFRSEL8(2-0)			RATSSEL8(4-0)				
049	R/W	RAFRSEL9(2-0)			RATSSEL9(4-0)				
04A	R/W	RAFRSEL10(2-0)			RATSSEL10(4-0)				
04B	R/W	RAFRSEL11(2-0)			RATSSEL11(4-0)				
04C	R/W	RAFRSEL12(2-0)			RATSSEL12(4-0)				
04D	R/W	RAFRSEL13(2-0)			RATSSEL13(4-0)				
04E	R/W	RAFRSEL14(2-0)			RATSSEL14(4-0)				
04F	R/W	RAFRSEL15(2-0)			RATSSEL15(4-0)				
050	R/W	RAFRSEL16(2-0)			RATSSEL16(4-0)				
051	R/W	RAFRSEL17(2-0)			RATSSEL17(4-0)				
052	R/W	RAFRSEL18(2-0)			RATSSEL18(4-0)				

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
053	R/W	RAFRSEL19(2-0)			RATSSEL19(4-0)				
054	R/W	RAFRSEL20(2-0)			RATSSEL20(4-0)				
055	R/W	RAFRSEL21(2-0)			RATSSEL21(4-0)				
056	R/W	RAFRSEL22(2-0)			RATSSEL22(4-0)				
057	R/W	RAFRSEL23(2-0)			RATSSEL23(4-0)				
058	R/W	RAFRSEL24(2-0)			RATSSEL24(4-0)				
059	R/W	RAFRSEL25(2-0)			RATSSEL25(4-0)				
05A	R/W	RAFRSEL26(2-0)			RATSSEL26(4-0)				
05B	R/W	RAFRSEL27(2-0)			RATSSEL27(4-0)				
05C	R/W	RAFRSEL28(2-0)			RATSSEL28(4-0)				
05D	R/W	RAFRSEL29(2-0)			RATSSEL29(4-0)				
05E	R/W	RAFRSEL30(2-0)			RATSSEL30(4-0)				
05F	R/W	RAFRSEL31(2-0)			RATSSEL31(4-0)				
060	R/W	TAFRSEL0(2-0)			TATSSEL0(4-0)				
061	R/W	TAFRSEL1(2-0)			TATSSEL1(4-0)				
062	R/W	TAFRSEL2(2-0)			TATSSEL2(4-0)				
063	R/W	TAFRSEL3(2-0)			TATSSEL3(4-0)				
064	R/W	TAFRSEL4(2-0)			TATSSEL4(4-0)				
065	R/W	TAFRSEL5(2-0)			TATSSEL5(4-0)				
066	R/W	TAFRSEL6(2-0)			TATSSEL6(4-0)				
067	R/W	TAFRSEL7(2-0)			TATSSEL7(4-0)				
068	R/W	TAFRSEL8(2-0)			TATSSEL8(4-0)				
069	R/W	TAFRSEL9(2-0)			TATSSEL9(4-0)				
06A	R/W	TAFRSEL10(2-0)			TATSSEL10(4-0)				
06B	R/W	TAFRSEL11(2-0)			TATSSEL11(4-0)				
06C	R/W	TAFRSEL12(2-0)			TATSSEL12(4-0)				
06D	R/W	TAFRSEL13(2-0)			TATSSEL13(4-0)				
06E	R/W	TAFRSEL14(2-0)			TATSSEL14(4-0)				
06F	R/W	TAFRSEL15(2-0)			TATSSEL15(4-0)				
070	R/W	TAFRSEL16(2-0)			TATSSEL16(4-0)				
071	R/W	TAFRSEL17(2-0)			TATSSEL17(4-0)				

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
072	R/W	TAFRSEL18(2-0)			TATSSEL18(4-0)				
073	R/W	TAFRSEL19(2-0)			TATSSEL19(4-0)				
074	R/W	TAFRSEL20(2-0)			TATSSEL20(4-0)				
075	R/W	TAFRSEL21(2-0)			TATSSEL21(4-0)				
076	R/W	TAFRSEL22(2-0)			TATSSEL22(4-0)				
077	R/W	TAFRSEL23(2-0)			TATSSEL23(4-0)				
078	R/W	TAFRSEL24(2-0)			TATSSEL24(4-0)				
079	R/W	TAFRSEL25(2-0)			TATSSEL25(4-0)				
07A	R/W	TAFRSEL26(2-0)			TATSSEL26(4-0)				
07B	R/W	TAFRSEL27(2-0)			TATSSEL27(4-0)				
07C	R/W	TAFRSEL28(2-0)			TATSSEL28(4-0)				
07D	R/W	TAFRSEL29(2-0)			TATSSEL29(4-0)				
07E	R/W	TAFRSEL30(2-0)			TATSSEL30(4-0)				
07F	R/W	TAFRSEL31(2-0)			TATSSEL31(4-0)				

Spare Register Locations

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
031 - 036 080 - 0FD	R/W	Reserved, set to 0							

Other Control Registers (See Descriptions on page 193)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0FE	R/W	Reserved, set to 0		RESECKSYN	DISECKSYN	DEBVAL(3-0)			
0FF	R/W	WG	Reserved, set to 0				OBT1SI	Reserved, set to 0	

PER CHANNEL CONTROL AND STATUS INDICATION REGISTERS

The following registers configure, control or provide status information on a per channel (framer) basis. The memory map uses a 13-bit address, with the 9 least significant bits addressing 512 per framer or common (global) registers and the 4 most significant bits used to address a framer (from 1 to 8) or the common registers. The first 512 addresses are used for the common registers described above. Each framer's register range (X+00H to X+FFH) is 512 addresses, as shown below:

Framer Channel	Address Range (Hex)	X = (Hex)
Common	0000 - 01FF	0000
Framer No. 1	0200 - 03FF	0200
Framer No. 2	0400 - 05FF	0400
Framer No. 3	0600 - 07FF	0600
Framer No. 4	0800 - 09FF	0800
Framer No. 5	0A00 - 0BFF	0A00
Framer No. 6	0C00 - 0DFF	0C00
Framer No. 7	0E00 - 0FFF	0E00
Framer No. 8	1000 - 11FF	1000

Framer configuration and Control Registers (See Descriptions on page 195)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+00	R/W	RAIL	BE	RXCP	RXNRZ	EXLOS	ELOSN	ENZC	TS16EIC
X+01	R/W	RTFM	TTFM	BFAA	CASA	CRCA	OOF1	OOF0	AAGS
X+02	R/W	ENAIS	ENOOF	ENLOS	ENABIT	ENDBIT	RTAIS	ENRAI	RTRAI
X+03	R/W	RX0AISE	RT0AIS	RX0RAI	RT0RAI	ENRXNBR	EOOCRC	EOO16M	ENRXAUXP
X+04	R/W	RDINV	RSINV	TDINV	TSINV	RDADI	TDADI	ENRAIA	ENRAIY
X+05	R/W	PWRD	FDAT	FPOL	SYFZ	TXCP	TXNRZ	ENLAIS	E16AIS
X+06	R/W	TXAIS	TXRAI	EXTAIS	EXTRAI	ENTXAUXP	ULAW	TX0AISE	ST0AIS
X+07	R/W	TDFME	TXDRV	TLMF	FE1M	CRCMD1	CRCMD0	TAIS16E	TS16YE
X+08	R/W	BPCRC4	SA4UP	SA5UP	SA6UP	SA7UP	SA8UP	AUTRAI	AUTY
X+09	R/W	Reserved, set to 0							
X+0A	R/W	SRST	RSYNC	Reserved, set to 0					AIW

Receiver Fractional E1 Channel Control Registers (See Descriptions on page 205)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+1A	R/W	RCHMK	Reserved, set to 0						

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+1B	R/W	RFCH7-RFCH0 (Receive Fractional E1 Channels 7-0)							
X+1C	R/W	RFCH15-RFCH8 (Receive Fractional E1 Channels 15-8)							
X+1D	R/W	RFCH23-RFCH16 (Receive Fractional E1 Channels 23-16)							
X+1E	R/W	RFCH31-RFCG24 (Receive Fractional E1 Channels 31-24)							
X+1F	R/W	Spare							

Transmit Fractional E1 Channel, Digital Milliwatt and Idle Code Control Registers (See Descriptions on page 205)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+110	R/W	TCHMK	Reserved, set to 0						
X+111	R/W	TC1C3	TC0C3	TC1C2	TC0C2	TC1C1	TC0C1	TC1C0	TC0C0
X+112	R/W	TC1C7	TC0C7	TC1C6	TC0C6	TC1C5	TC0C5	TC1C4	TC0C4
X+113	R/W	TC1C11	TC0C11	TC1C10	TC0C10	TC1C9	TC0C9	TC1C8	TC0C8
X+114	R/W	TC1C15	TC0C15	TC1C14	TC0C14	TC1C13	TC0C13	TC1C12	TC0C12
X+115	R/W	TC1C19	TC0C19	TC1C18	TC0C8	TC1C17	TC0C17	TC1C16	TC0C16
X+116	R/W	TC1C23	TC0C23	TC1C22	TC0C22	TC1C21	TC0C21	TC1C20	TC0C20
X+117	R/W	TC1C27	TC0C27	TC1C26	TC0C26	TC1C25	TC0C25	TC1C24	TC0C24
X+118	R/W	TC1C31	TC0C31	TC1C30	TC0C30	TC1C29	TC0C29	TC1C28	TC0C28
X+119	R/W	IDL7-IDL0 (Idle code written by Microprocessor), where IDL7 is bit 1 transmitted							
X+161	R/W	Reserved set to 0					ATTNLIM	RECENTER	BYPASS

Receive and Transmit Facility Data Link Control Registers (See Descriptions on page 207)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+122	R/W	Reserved, set to 0		BNAL	Reserved, set to 0				
X+123	R/W	EHR	RHIE	Reserved, set to 0					
X+124	R	RHD7 - RHD0 (HDLC Receive Data, RHD0 is the first bit received on the line)							
X+125	R	DPT7 - DPT0 (HDLC Receive FIFO Depth)							
X+126	R/W	EHT	TAB	EOM	R=0	THIE	Reserved, set to 0		
X+127	W	THD7 - THD0 (HDLC Transmit Data, THD0 is the first bit transmitted on the line)							

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+128	R	R	MSL6	MSL5	MSL4	MSL3	MSL2	MSL1	MSL0
X+0C	R/W	Reserved set to 0			SA4	SA5	SA6	SA7	SA8

Receive and Transmit Facility Data Link Status Registers (See Descriptions on page 209)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+0D	R/W	LRHIS2	LRHIS1	LRHIS0	LRXFS1	LRXFS0	LTXFS1	LTXFS0	LTHIS
X+0E	R	RHIS2	RHIS1	RHIS0	RXFS1	RFXS0	TXFS1	TXFS0	THIS
X+0F	R/W	MRHIS2	MRHIS1	MRHIS0	MRXFS1	MRXFS0	MTXFS1	MTXFS0	MTHIS
X+160	R/W	Reserved, set to 0							

Receive and Transmit Slip Buffer Control Registers (See Descriptions on page 211)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+11B	R/W	RXCKE	R = 0	RXSBE	RSR	Reserved; set to 0			
X+11C	R/W	TXC1	TXC0	TXSBE	TSR	Reserved; set to 0			

Receive and Transmit Slip Buffer Status Registers (See Descriptions on page 212)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+15	R	RXS1	RXS0	RTSLPP	Reserved				
X+16	R	TXS1	TXS0	LTSLPP	Reserved				

Receive and Transmit Slip Buffer Pointer Status Registers (See Descriptions on page 213)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+20	R/W	RWP7-TRP0 (Receive Slip Buffer Write Pointer)							
X+21	R/W	RRP7-RRP0 (Receive Slip Buffer Read Pointer)							
X+22	R/W	RWSBS	Reserved			RWPF3-RWPF0 (Receive Write Pointer Frame)			
X+23	R/W	RRSBS	RXSBD8	Reserved		RRPF3-RRPF0 (Receive Read Pointer Frame)			

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+24	R	RXSBD7-RXSBD0 (Receive slip buffer delay in increments of 1 bits)							
X+25	R	TXSBD7-TXSBD0 (Transmit slip buffer delay in increments of 1 bits)							
X+26	R/W	TWP7-TWP0 (Transmit Slip Buffer Write Pointer)							
X+27	R/W	TRP7-TRP0 (Transmit Slip Buffer Read Pointer							
X+28	R/W	TWSBS	Reserved			TWPF3-TWPF0 (Transmit Write Pointer Frame)			
X+29	R/W	TRSBS	TXSBD8	Reserved		TRPF3-TRPF0 (Transmit Read Pointer Frame)			

Receive Slip Buffer Control Registers (See Descriptions on page 215)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+3A	R/W	Reserved, set to 0					RX2S	RX1S	RX0S
X+3B	R/W	RSIS	Reserved, set to 0		RSA4S	RSA5S	RSA6S	RSA7S	RSA8S
X+3C	R/W	RDE7-RDE1 (Receive Time Slots 7-1 Selection)							R=0
X+3D	R/W	RDE15-RDE8 (Receive Time Slots 15-8 Selection)							
X+3E	R/W	RDE23-RDE16 (Receive Time Slots 23-16 Selection)							
X+3F	R/W	RDE31-RDE24 (Receive Time Slots 31-24 Selection)							

Receive Slip Buffer Frame Storage Registers (See Descriptions on page 217)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+40	R/W	RFAS - Receive Frame Alignment Pattern FAS channel 1 (Time Slot 0 - Frame 1)							
X+41 to X+5F	R/W	Frame 1 RTS1-RTS31 (Receive Time Slots TS1 - TS31) X41 - Time Slot 1 X5F - Time Slot 31							
X+60	R/W	RNFAS - Receive No Frame Alignment Pattern NFAS channel 1 (Time Slot 0 - Frame 1)							
X+61 to X+7F	R/W	Frame 2 RTS1-RTS31 (Receive Time Slots TS1 - TS31) X61 - Time Slot 1 X7F - Time Slot 31							
X+132	R/W	Reserved, set to 0							

Transmit Slip Buffer Control Registers (See Descriptions on page 218)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+E2	R/W	Reserved, set to 0					TX2S	TX1S	TX0S
X+E3	R/W	TSIS	Reserved, set to 0		TSA4S	TSA5S	TSA6S	TSA7S	TSA8S
X+E4	R/W	TDE7-TDE1 (Transmit Time Slots 7-1 Selection)							R=0
X+E5	R/W	TDE15-TDE8 (Transmit Time Slots 15-8 Selection)							
X+E6	R/W	TDE23-TDE16 (Transmit Time Slots 23-16 Selection)							
X+E7	R/W	TDE31-TDE24 (Transmit Time Slots 31-24 Selection)							

Transmit Slip Buffer Frame Storage Registers (See Descriptions on page 220)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+90	R/W	TFAS - Transmit Frame Alignment Pattern FAS channel 1 (Time Slot 0 - Frame 1)							
X+91 to X+AF	R/W	Frame 1 TTS1-TTS31 (Transmit Time Slots TS1 - TS31) X91 - Time Slot 1 XAF - Time Slot 31							
X+B0		TNFAS - Transmit No Frame Alignment Pattern NFAS channel 1 (Time Slot 0 - Frame 1)							
X+B1 to X+CF	R/W	Frame 2 TTS1-TTS31 (Transmit Time Slots TS1 - TS31) XB1 - Time Slot 1 XCF - Time Slot 31							
X+133	R/W	Reserved; set to 0							

Receive and Transmit Signaling State Control Registers (See Descriptions on page 221)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+134	R/W	TYP1	TYP0	TS0FZ	SIGDB	SIGIEN	R = 0	RXSFZ	TXSFZ

Receive Signaling Control Registers (See Descriptions on page 222)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+E8	R/W	RSE8-RSE1 (Receive Signaling Enable for Channels 8-1 Selection)							
X+E9	R/W	RSE16-RSE9 (Receive Signaling Enable for Channels 16-9 Selection)							

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+EA	R/W	RSE24-RSE17 (Receive Signaling Enable for Channels 24-17 Selection)							
X+EB	R/W	Reserved, set to 0		RSE30-RSE25 (Receive Signaling Enable for Channels 30-25 Selection)					

Receive Signaling State Registers (Debounce Buffer) (See Descriptions on page 223)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+80	R/W	Receive Multiframe Pattern RSIGMAS (0000)				RX0	RY	RX1	RX2
X+81 to X+8F	R/W	Receive Signaling Bits RA1-RD1 (A1 B1 C1 D1) to RA15-RD15 (A15 B15 C15 D15)				Receive Signaling Bits RA16-RD16 (A16 B16 C16 D16) to RA30-RD30 (A30 B30 C30 D30)			

Receive Signaling State Registers (Active Buffer 1) (See Descriptions on page 227)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+137	R/W	Receive Multiframe Pattern RRSIGMAS (0000)				RRX0	RRY	RRX1	RRX2
X+138 to X+146	R/W	Receive Signaling Bits RRA1-RRD1 (A1 B1 C1 D1) to RRA15-RRD15 (A15 B15 C15 D15)				Receive Signaling Bits RRA16-RRD16 (A16 B16 C16 D16) to RRA30-RRD30 (A30 B30 C30 D30)			

Receive Signaling State Match Count Registers (See Descriptions on page 232)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+147	R/W	Reserved							
X+148	R/W	RSNM1(3-0)				RSNM16(3-0)			
X+149	R/W	RSNM2(3-0)				RSNM17(3-0)			
X+14A	R/W	RSNM3(3-0)				RSNM18(3-0)			
X+14B	R/W	RSNM4(3-0)				RSNM19(3-0)			
X+14C	R/W	RSNM5(3-0)				RSNM20(3-0)			
X+14D	R/W	RSNM6(3-0)				RSNM21(3-0)			
X+14E	R/W	RSNM7(3-0)				RSNM22(3-0)			

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+14F	R/W	RSNM8(3-0)				RSNM23(3-0)			
X+150	R/W	RSNM9(3-0)				RSNM24(3-0)			
X+151	R/W	RSNM10(3-0)				RSNM25(3-0)			
X+152	R/W	RSNM11(3-0)				RSNM26(3-0)			
X+153	R/W	RSNM12(3-0)				RSNM27(3-0)			
X+154	R/W	RSNM13(3-0)				RSNM28(3-0)			
X+155	R/W	RSNM14(3-0)				RSNM29(3-0)			
X+156	R/W	RSNM15(3-0)				RSNM30(3-0)			

Transmit Signaling Control Registers (See Descriptions on page 239)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+EC	R/W	TSE8-TSE1 (Transmit Signaling Enable for Channels 8-1 Selection)							
X+ED	R/W	TSE16-TSE9 (Transmit Signaling Enable for Channels 16-9 Selection)							
X+EE	R/W	TSE24-TSE17 (Transmit Signaling Enable for Channels 24-17 Selection)							
X+EF	R/W	Reserved, set to 0		TSE30-TSE25 (Transmit Signaling Enable for Channels 30-25 Selection)					

Transmit Signaling State Registers (See Descriptions on page 241)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+D0	R/W	Transmit Multiframe Pattern TSIGMAS (0000)				TX0	TY	TX1	TX2
X+D1 to X+DF	R/W	Transmit Signaling Bits TA1-TD1 (A1 B1 C1 D1) to TA15-TD15 (A15 B15 C15 D15)				Transmit Signaling Bits TA16-TD16 (A16 B16 C16 D16) to TA30-TD30 (A30 B30 C30 D30)			

E1 Line Status Registers (See Descriptions on page 245)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+10	R	LOS	AIS	OOF	RAI	CFA	OOFM	SLIP	SCHG
X+11	R/W	LLOS	LAIS	LOOF	LRAI	LCFA	LOOFM	LSLIP	LSCHG

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+12	R/W	PLOS	PAIS	POOF	PRAI	PCFA	POOFM	PSLIP	PSCHG
X+13	R/W	FLOS	FAIS	FOOF	FRAI	FCFA	FOOFM	FSLIP	FSCHG
X+14	R/W	MLOS	MAIS	MOOF	MRAI	MCFA	MOOFM	MSLIP	MSCHG
X+164	R	R=0	AIS16	ECRCE	RAI16	R=0	OO16M	R=0	AUXP
X+165	R/W	R=0	LAIS16	LECRCE	LRAI16	R=0	LOO16M	R=0	LAUXP
X+166	R/W	R=0	MAIS16	MECRCE	MRAI16	R=0	MOO16M	R=0	MAUXP
X+167	R/W	R=0	PAIS16	PECECE	PRAI16	R=0	POO16M	R=0	PAUXP
X+168	R/W	R=0	FAIS16	FECRCE	FRAI16	R=0	FOO16M	R=0	FAUXP

Non-Interrupt Status Registers (See Descriptions on page 254)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+17	R	Reserved, set to 0		TABIT	TYBIT	Reserved, set to 0		RXSF	TXSF
X+18	R	NCRC4	Reserved		TS16ME	Reserved			
X+19	R to clear	SIGACT7-SIGACT0							
X+175	R	Reserved		S6X	S6F	S6E	S6C	S6A	S68

Transmit Sa4 - Sa8 Code Registers (See Descriptions on page 255)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+169	R/W	XSA47-XSA40							
X+16A	R/W	XSA57-XSA50							
X+16B	R/W	XSA67-XSA60							
X+16C	R/W	XSA77-XSA70							
X+16D	R/W	XSA87-XSA80							
X+16E	R/W	Spare							

Receive Sa4 - Sa8 Code Registers (See Descriptions on page 256)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+16F	R	RSA47-RSA40							
X+170	R	RSA57-RSA50							
X+171	R	RSA67-RSA60							
X+172	R	RSA77-RSA70							
X+173	R	RSA87-RSA80							
X+174	R	Spare							

Performance Counters and Counters Shadow Registers (See Descriptions on page 257)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+F0	R/W	LCRC7-LCRC0 (Latched CRC-4 Error Counter Shadow Register 10 bits)							
X+F1	R/W	LCRCO	Reserved, set to 0					LCRC9	LCRC8
X+F2	R/W	CRC7-CRC0 (CRC-4 Error Counter 10 bits)							
X+F3	R/W	CRCO	Reserved, set to 0					CRC9	CRC8
X+F4	R/W	LCV7-LCV0 (Latched Coding Violations Error Counter Shadow Register 16 bits)							
X+F5	R/W	LCV15-LCV8 (Latched Coding Violations Error Counter Shadow Register 16 bits)							
X+F6	R/W	LCVO	Reserved, set to 0						
X+F7	R/W	CV7-CV0 (Coding Violations Error Counter 16 bits)							
X+F8	R/W	CV15-CV8 (Coding Violations Error Counter 16 bits)							
X+F9	R/W	CVO	Reserved, set to 0						
X+FA	R/W	LFBE7-LFBE0 (Latched Framing Word Error Counter Shadow Register 8 bits)							
X+FB	R/W	LFBEO	Reserved, set to 0						
X+FC	R/W	FBE7-FBE0 (Framing Word Error Counter 8 bits)							
X+FD	R/W	FBEO	Reserved, set to 0						
X+FE	R/W	LEBE7-LEBE0 (Latched E-bit Error Counter Shadow Registers, 10 bits)							
X+FF	R/W	LEBEO	Reserved, set to 0					LEBE9	LEBE8
X+100	R/W	EBE7-LEBE0 (E-bit Error Counter, 10 bits)							
X+101	R/W	EBEO	Reserved, set to 0					EBE9	EBE8

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+102 to X+105	R/W	Reserved, set to 0							
X+157	R/W	LTESTP7-LTESTP0(Latched Lower byte test analyzer OOL counter)							
X+158	R/W	LTESTPO	LTESTP14-LTESTP8(Latched upper byte test analyzer OOL counter)						
X+159	R/W	TESTP7-TESTP0(Lower byte test analyzer OOL counter)							
X+15A	R/W	TESTPO	TESTP14-TESTP8(Upper byte test analyzer OOL counter)						
X+177	R/W	LSA617-LSA610(Latched lower byte)							
X+178	R/W	LSA61O	Reserved, set to 0					LSA619	LSA618
X+179	R/W	SA617-SA610(Lower byte)							
X+17A	R/W	SA61O	Reserved, set to 0					SA619	SA618
X+17B	R/W	LSA627-LSA620(Latched lower byte)							
X+17C	R/W	LSA62O	Reserved, set to 0					LSA629	LSA628
X+17D	R/W	SA627-SA620(Lower byte)							
X+17E	R/W	SA62O	Reserved, set to 0					SA629	SA628

Test Generation Registers (See Descriptions on page 263)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+106	R/W	CRCE	FRME	BPVE	NFASE	Reserved; set to 0		PRBRE	INPRBS
X+107	R/W	LLP	TXLAIS	RLP	PLP	Reserved; set to 0		SPRBRE	SINPRBS
X+108	R/W	Reserved; set to 0							

Time Slot/DS0 Loopback, Test Pattern Status and DPLL Status Registers (See Descriptions on page 265)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+129	R	DS0ACT	DS0DCT	TPLOL	DS0TXC	INTACT	INTDCT	OVERF	UNDERF
X+12A	R/W	LDS0ACT	LDS0DCT	LTPLOL	LDS0TXC	LINTACT	LINTDCT	LOVERF	LUNDERF
X+12B	R/W	MDACT	MDDCT	MTPLOL	MDS0TXC	MINTACT	MINTDCT	MOVERF	MUNDERF

Time Slot/DS0 Test Pattern Control Registers (See Descriptions on page 268)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+109	R/W	TSRLOP	DS0DA	TRDSLP	TRPN2	TPRN1	TPRN0	TSLLP	RLPEN
X+10A	R/W	TSRL8	TSRL7	TSRL6	TSRL5	TSRL4	TSRL3	TSRL2	TSRL1
X+10B	R/W	TSRL16	TSRL15	TSRL14	TSRL13	TSRL12	TSRL11	TSRL10	TSRL9
X+10C	R/W	TSRL24	TSRL23	TSRL22	TSRL21	TSRL20	TSRL19	TSRL18	TSRL17
X+10D	R/W	TSRL32	TSRL31	TSRL30	TSRL29	TSRL28	TSRL27	TSRL26	TSRL25
X+12C	R/W	SRTT7-SRTT0							
X+12D	R/W	TSLL8	TSLL7	TSLL6	TSLL5	TSLL4	TSLL3	TSLL2	TSLL1
X+12E	R/W	TSLL16	TSLL15	TSLL14	TSLL13	TSLL12	TSLL11	TSLL10	TSLL9
X+12F	R/W	TSLL24	TSLL23	TSLL22	TSLL21	TSLL20	TSLL19	TSLL18	TSLL17
X+130	R/W	TSLL32	TSLL31	TSLL30	TSLL29	TSLL28	TSLL27	TSLL26	TSLL25
X+131	R/W	Reserved, set to 0				SPRN	RTPAE	SSPRN	SRTPAE
X+15B	R/W	Test Word first byte							
X+15C	R/W	Test Word second byte							
X+15D	R/W	Test Word third byte							
X+15E	R/W	Test Word fourth byte							

Test Registers (See Descriptions on page 271)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+17F to X+1FE	R/W	Reserved							
X+1FF	R/W	Reserved, set to 0					OBLOL	RXFS	R = 0

SPARE AND RESERVED REGISTERS

Spare Registers

Registers that are not assigned to functions, or reserved, are designated as spare. Spare registers must not be accessed for read or write operations by the microprocessor. The following registers are spares: 00D through 010, 013, 015, 021, 023, 026 through 029, 02D, 030, 031 through 036, 080 through 0FD, X+0B, X+1F, X+2A, X+2B, X+2C, X+2D, X+2E, X+2F, X+11A, X+135, X+136, X+162, X+16E, X+174.

Reserved and Test Registers

The following bit locations in read/write registers are designated as reserved, and some require zeros to be written into them as indicated in the tables below. Some of these bits are designated as internal test bits, etc. Per framer test registers may be read but must not be written during normal operation.

Global Registers

Register	Bits	Comments
00A	6-0	Set to zero
00B	0	Set to zero
00C	4-0	Set to zero
01A	1	Set to zero
01A	7, 3	
01B	7, 3, 1	Set to zero
01D	4, 3	Set to zero
022	4, 3	Set to zero
025	4, 3	Set to zero
02B	6	Set to zero
037	7-5	Set to zero
0FF	1, 0	Set to zero

Per Framer Registers

Register	Bits	Comments
X+09	7-0	Set to zero
X+0A	5-1	Set to zero
X+0C	7-5	Set to zero
X+15	4-0	
X+16	4-0	
X+1A	6-0	Set to zero
X+22	6-4	
X+23	5, 4	
X+28	6-4	

Register	Bits	Comments
X+29	5, 4	
X+36	7-0	
X+37	7-0	
X+3A	7-3	Set to zero
X+3B	6, 5	Set to zero
X+3C	0	Set to zero
X+58-X+5F	7-0	
X+78-X+7F	7-0	
X+E2	7-3	Set to zero
X+E3	6, 5	Set to zero
X+E4	0	Set to zero
X+EB	7-6	
X+EF	7-6	
X+F1	6-2	Set to zero
X+F3	6-2	Set to zero
X+F6	6-0	Set to zero
X+F9	6-0	Set to zero
X+FB	6-0	Set to zero
X+FD	6-0	Set to zero
X+FF	6-2	Set to zero
X+101	6-2	Set to zero
X+102-X+105	7-0	Set to zero
X+106	3, 2	Set to zero
X+107	3, 2	Set to zero
X+108	7-0	Set to zero
X+110	6-0	Set to zero
X+11B	6, 3-0	Set to zero
X+11C	3-0	Set to zero
X+122	4-0	Set to zero
X+123	5-0	Set to zero
X+126	4	Set to zero
X+131	7-4	Set to zero
X+132	7-0	Set to zero
X+133	7-0	Set to zero

Register	Bits	Comments
X+134	2	Set to zero
X+147	7-0	
X+160	7-0	Set to zero
X+163	7-0	Set to zero
X+165-X+168	7, 3, 1	Set to zero
X+178	6-2	Set to zero
X+17A	6-2	Set to zero
X+17C	6-2	Set to zero
X+17E	6-2	Set to zero
X+17F-X+1FE	7-0	
X+1FF	7-3, 0	Set to zero

MEMORY MAP DESCRIPTIONS

COMMON REGISTERS

Device ID Registers

The manufacturer ID, part number code and version of the E1Fx8 are implemented in registers 000H - 003H with read-only capability, as shown in the Memory Map section. The manufacturer ID is 107 (decimal), and has been assigned for TranSwitch by the Joint Electron Device Engineering Council (JEDEC) of the Solid State Products Engineering Council. This field is 11 bits in length, and is assigned to bits 3 through 0 in register 001H, and bits 7 through 1 in register 000H. Bit 0 in register 000H (LSB) is assigned to the value 1. The 11 bit manufacturer ID plus the LSB contains value 0D7H. The part number is 16 bits long. The part number code used here for the E1Fx8 is 03109 (decimal). The binary equivalent of 03109 (decimal) is assigned to bits 3-0 in register 003H, bits 7-0 in register 002H, and bits 7-4 (LSB) in register 001H (0C25H). The Revision Level field at bits 7-4 in register 003H represents the version number of the device and is set to 1H, but this value may be changed as the device evolves.

MSB LSB

Version	Part Number	Manufacturer Identify	1
4 bits	16 bits	11 bits	1 bit

Customer Notebook Register

Address (Hex)	Bit	Symbol	Description
004 to 009	7-0	Notebook	**User Defined Register:** The bits in this read/write register are provided for use by the application software. The contents of this read/write register will have no direct effect on the operation of the E1Fx8.

Global Software Reset Register

The control bit in this read/write register location is used for resetting the E1Fx8.

Address (Hex)	Bit	Symbol	Description
00A	7	RESET	**Software Reset:** This register location is provided in addition to the hardware reset for resetting internal state machines. Performance counters and shadow registers must be written to 0 if it is desired to clear them; if control bit SRGEN (register 00BH, bit 3) is set to a 1, a one-second clock from the SREGT lead or a selected derived clock will clear these counters and registers. The reset will be released when a 0 is written into this bit position.
	6-0		**Reserved:** Write these bits to 0.

Global Configuration Registers

The bits in these read/write registers control E1Fx8 operations on a global basis for all eight framers.

<table>
<tr><th>Address (Hex)</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td rowspan="9">00B</td><td>7</td><td>RISE</td><td>Rising Edge Latched Status Event Selection: This control bit works in conjunction with the FALL control bit for controlling the edge for latching an alarm.
<u>RISE</u> <u>FALL</u> <u>Action</u>
0 0 The latched bit indications for all 8 framers will be disabled. The hardware interrupt is disabled.
0 1 Latched status indication bits for all framers set on negative transitions (off state) of an alarm.
1 0 Latched status indication bits for all framers set on positive transitions (on state) of an alarm.
1 1 Latched status indication bits for all framers set on positive or negative transitions of an alarm.</td></tr>
<tr><td>6</td><td>FALL</td><td>Falling Edge Latched Status Event Selection: This control bit works in conjunction with the RISE control bit (described above) for controlling the edge for latching an alarm, as defined in the table given above.</td></tr>
<tr><td>5</td><td>GIM</td><td>Global Interrupt Mask Disable: A 1 disables (masks) the hardware interrupt lead. When set to 0, the hardware interrupt lead is enabled.</td></tr>
<tr><td>4</td><td>IPOL</td><td>Interrupt Polarity Sense Control: A 1 will invert the polarity of the hardware interrupt from active high to active low for the Intel compatible microprocessor bus, and from active low to active high for the Motorola compatible microprocessor bus.</td></tr>
<tr><td>3</td><td>SRGEN</td><td>Shadow Register Feature Enabled: A 1 will enable the shadow register feature; must be set for PM/FM and counter latching.</td></tr>
<tr><td>2</td><td>HWMEN</td><td>Hardware Mask Hierarchy Enable: When this bit is set to 1, the masking hierarchy for the alarms is enabled according to the table below:
Alarm Suppression Table (Shaded Columns indicate suppressed alarms)
<table>
<tr><th>Direction</th><th>LOS</th><th>Line AIS</th><th>OOF</th><th>TS16 AIS</th><th>RAI</th><th>CRC OOMF</th><th>TS16 OOMF</th><th>TS16 RAI</th><th>TS16 ME</th></tr>
<tr><td rowspan="4">Line Port to System</td><td>X</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td></td><td>X</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td></td><td></td><td>X</td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td></td><td></td><td></td><td>X</td><td></td><td></td><td></td><td></td><td></td></tr>
</table></td></tr>
<tr><td>1</td><td>DINTF</td><td>Data Interface Enable: A 1 will configure the system side interface for data operation for the transmission interface. In H-MVIP mode a 1 will select a two clock cycle sync. pulse (H.100 timing); a 0 defaults H-MVIP to a four clock cycle sync. pulse.</td></tr>
<tr><td>0</td><td></td><td>Reserved: Write this bit to 0.</td></tr>
</table>

Address (Hex)	Bit	Symbol	Description
00C	7	S1CIEN	**Substitution Clock on LOS Enable:** A 1 enables an the external clock to be substituted for the receive line clock when an loss of signal alarm is detected.
	6	SYNLF	**Synchronous Framing Pulse to Line Frame:** A 1 causes the 8 kHz framing pulse (when enabled) on the SCOUT1 and SCOUT2 leads to be synchronous with the start of Time Slot 0 in the receive line signal. The exact phase is a function of the codec option (NRZ, AMI / HDB3) and clock edge option (RXCP = 1,0) selected. See descriptions for leads SCOUT1 and SCOUT2 in the lead description section, and associated timing diagrams.
	5	ENAISI	**Enable AIS Detection per ISDN:** When set to a 1 AIS is detected as defined in ITU-T I.431; AIS is declared if two or less zeros are detected in two consecutive frames (one double frame); AIS is cleared when three or more zeros are detected in a double frame after basic frame alignment. When set to a 0, AIS is detected per ITU-T G.775; AIS is declared if two or less zeros are detected in two consecutive double frames (4 frames total); AIS is cleared when three or more zeros are detected in a two consecutive doubles frame after basic frame alignment.
	4-0		**Reserved:** Write these bits to 0.

Global Status, Mask and Pointer Registers

These registers are read-only, except for the mask registers 012H, 018H and 01BH, which are read/write. The bits in the Global Status Indication Registers 011H and 01AH indicate an alarm caused by a line Time Slot 0 or Time Slot 16 event on a global basis (i.e., in any framer). Each Global Status Indication bit is formed by or-gating the corresponding latched event bits in each of the eight framer channels (registers X+11H or X+164H) to provide the individual status indication in global registers 011H and 01AH. A 1 written into a bit position in the Global Mask Register 012H or 01BH will mask the interrupt indication for the corresponding bit position in register 011H or 01AH. The bits in register locations 014H and 01BH provide a pointer to the framer or framers which caused the line latched event. A similar procedure is supported for HDLC events and DS0 loop back activate and deactivate codes. For HDLC events a separate pointer is provided by register 016H which indicates which framer or framers caused the latched event; there are no global mask bits for HDLC events since they are provided on a per framer basis. For DS0 loop back activity and the PRBS/Code Word Analyzer, the bits in the Global Status Indication Register 017H indicate an alarm caused by an Analyzer out of lock, an activate/deactivate pattern or a complete activate/deactivate code received on a global basis (i.e., in any framer). Each Global Status Indication bit is formed by or-gating the corresponding latched event bits in each of the eight framer channels (registers X+129H) to provide the individual status indication in global register 017H. A 1 written into a bit position in the Global Mask Register 018H will mask the interrupt indication for the corresponding bit position in register 017H. The bits in register locations 019H provide a pointer to the framer or framers which caused the latched event.

Address (Hex)	Bit	Symbol	Description
011	7	GLOS	**Global Indication for Loss of Signal:** This bit position indicates when any of the 8 framers has detected a loss of signal. This bit position is cleared when the corresponding framer alarm is cleared.

Address (Hex)	Bit	Symbol	Description
011 (cont.)	6	GAIS	**Global Indication for AIS:** This bit position indicates when any of the 8 framers has detected an AIS. This bit position is cleared when the corresponding framer alarm is cleared.
	5	GOOF	**Global Indication for Out Of Frame:** This bit position indicates when any of the 8 framers has detected an out of frame. This bit position is cleared when the corresponding framer alarm is cleared.
	4	GRAI	**Global Indication for RAI (A-bit = 1) Indication:** This bit position indicates when any of the 8 framers has detected an RAI indication. This bit position is cleared when the corresponding framer alarm is cleared.
	3	GCFA	**Global Indication for Change in Frame Alignment:** This bit position indicates when any of the 8 framers has detected an Change in Frame Alignment indication. This bit position is cleared when the corresponding framer alarm is cleared.
	2	GOOMF	**Global Indication for Out Of MultiFrame Alignment Error:** This bit will be set if there is an out of multiframe error in any of the 8 framers. This bit will be cleared when all OOMF errors have been cleared in the individual channel event registers.
	1	GSLIP	**Global Indication for Transmit or Receive Slip Alarm:** This bit position indicates when any of the 8 framers has detected a transmit or receive slip. This bit position is cleared when the corresponding framer alarm is cleared.
	0	GSCHG	**Global Indication for Change of Signaling:** This bit position indicates when any of the 8 framers has detected a debounced signaling bit change. This bit position is cleared when the corresponding framer alarm is cleared.
012	7	GMLOS	**Global Loss of Signal Mask Bit:** When set to 1, this bit disables the hardware interrupt for a loss of signal indication from any of the 8 framers.
	6	GMAIS	**Global AIS Mask Bit:** When set to 1, this bit disables the hardware interrupt for an AIS indication from any of the 8 framers.
	5	GMOOF	**Global Out Of Frame Mask Bit:** When set to 1, this bit disables the hardware interrupt for an OOF indication from any of the 8 framers.
	4	GMRAI	**Global RAI (A-bit = 1) Indication Mask Bit:** When set to 1, this bit disables the hardware interrupt for an RAI indication from any of the 8 framers.
	3	GMCFA	**Global Change in Frame Alignment Mask Bit:** When set to 1, this bit disables the hardware interrupt for a CFA from any of the 8 framers.
	2	GMOOMF	**Global Out Of MultiFrame Mask Bit:** When set to 1, this bit disables the hardware interrupt for a OOMF from any of the 8 framers.
	1	GMSLIP	**Global Transmit or Receive Slip Mask Bit:** When set to 1, this bit disables the hardware interrupt for a transmit or receive slip indication from any of the 8 framers.
	0	GMSCHG	**Global Transmit Slip Mask Bit:** When set to 1, this bit disables the hardware interrupt for a debounced signaling bit change indication from any of the 8 framers.

Address (Hex)	Bit	Symbol	Description
014	7-0	CHL8-CHL1	**Channel Activity Line Event for Channels 1 through 8:** When a bit is set to 1, it indicates the framer (1 through 8) that caused the global line indication (LOS, AIS, OOF, RAI, CFA, Slip, or SCHG alarms).
016	7-0	CHD8-CHD1	**Channel Activity HDLC Event for Channels 1 through 8:** When a bit is set to 1, it indicates the framer (1 through 8) that caused the global HDLC indication (receive or transmit).
017	7	GDS0RS	**Global Indication for DS0 Receive Remote Loopback Activate Request Indication:** This bit position indicates when any of the 8 framers has detected a DS0 remote loopback activate request. This bit position is cleared when the corresponding framer indication is cleared.
	6	GDS0DC	**Global Indication for DS0 Receive Remote Loopback Deactivate Request Indication:** This bit position indicates when any of the 8 framers has detected a DS0 remote loopback deactivate request. This bit position is cleared when the corresponding framer indication is cleared.
	5	GDS0TP	**Global Indication for Time Slot Receive Out Of Lock Indication:** This bit position indicates when any of the 8 framers has detected a time slot out of lock indication for a time slot test pattern. This bit position is cleared when the corresponding framer indication is cleared.
	4	GDS0TC	**Global Indication for DS0 Transmit Remote Loopback Sequence Complete:** This bit position indicates when any of the 8 framers has completed transmitting a DS0 remote loopback activate/deactivate request. This bit position is cleared when the corresponding framer indication is cleared.
	3	GINTACT	**Global Intermediate Indication for DS0 Receive Remote Loopback Activate Request:** This bit position indicates when any of the 8 framers has detected a DS0 remote loopback intermediate activate request (only activate PRBS pattern received). This bit position is cleared when the corresponding framer indication is cleared
	2	GINTDCT	**Global Intermediate Indication for DS0 Receive Remote Loopback Deactivate Request:** This bit position indicates when any of the 8 framers has detected a DS0 remote loopback intermediate deactivate request (only deactivate PRBS pattern received). This bit position is cleared when the corresponding framer indication is cleared.
	1	GOVERF	**Global Overflow Indication:** This bit position indicates when any of the 8 framers has detected a DPLL FIFO overflow. This bit position is cleared when the corresponding framer indication is cleared
	0	GUNDERF	**Global Underflow Indication:** This bit position indicates when any of the 8 framers has detected a DPLL FIFO underflow. This bit position is cleared when the corresponding framer indication is cleared.

Address (Hex)	Bit	Symbol	Description
018	7	GMDS0RS	**Global Receive Indication for DS0 Receive Remote Loopback Activate Request Indication Mask:** When set to 1, this bit disables the hardware interrupt for a DS0 remote loopback activate request indication from any of the 8 framers.
	6	GMDS0DC	**Global Receive Indication for DS0 Receive Remote Loopback Deactivate Request Indication Mask:** When set to 1, this bit disables the hardware interrupt for a DS0 remote loopback deactivate request indication from any of the 8 framers.
	5	GMDS0TP	**Global Receive Indication for Time Slot Receive Out Of Lock Indication Mask:** When set to 1, this bit disables the hardware interrupt for a time slot out of lock indication for the time slot Test Pattern from any of the 8 framers.
	4	GMDS0TC	**Global Transmit Indication for DS0 Receive Remote Loopback Sequence Complete Mask:** When set to 1, this bit disables the hardware interrupt for completing a transmit DS0 remote loopback activate/deactivate request indication from any of the 8 framers.
	3	GMINTACT	**Global Receive Intermediate Indication for DS0 Receive Remote Loopback Activate Request Indication Mask:** When set to 1, this bit disables the hardware interrupt for a DS0 remote loopback intermediate activate request indication from any of the 8 framers.
	2	GMINTDCT	**Global Receive Intermediate Indication for DS0 Receive Remote Loopback Deactivate Request Indication Mask:** When set to 1, this bit disables the hardware interrupt for a DS0 remote loopback intermediate deactivate request indication from any of the 8 framers.
	1	GMOVERF	**Global Overflow Indication Mask:** When set to 1, this bit disables the hardware interrupt for a DPLL FIFO overflow indication from any of the 8 framers.
	0	GMUNDERF	**Global Underflow Indication Mask:** When set to 1, this bit disables the hardware interrupt for a DPLL FIFO underflow from any of the 8 framers.
019	7-0	CHR8-CHR1	**Channel Activity DS0 Remote Loopback Request or Time Slot Out Of Lock Indication for Channels 1 through 8:** When a bit is set to 1, it indicates the framer (1 through 8) that caused the global DS0 Remote Loopback Request (receive activate/deactivate, receive activate/deactivate PRBS pattern or transmit sequence complete) or out of lock indication (from the PRBS/ Code Word Analyzer).

Address (Hex)	Bit	Symbol	Description
01A	7		**Reserved:** Indeterminate value.
	6	GAIS16	**Global Indication for Time Slot 16 AIS:** This bit position indicates when any of the 8 framers has detected a Time Slot 16 AIS. This bit position is cleared when the corresponding framer alarm is cleared.
	5	GCRCE	**Global Indication for Excessive CRC-4 Error:** This bit position indicates when any of the 8 framers has detected an Excessive CRC-4 error. This bit position is cleared when the corresponding framer alarm is cleared
	4	GRAI16	**Global Indication for Time Slot 16 RAI:** This bit position indicates when any of the 8 framers has detected a Time Slot 16 RAI. This bit position is cleared when the corresponding framer alarm is cleared
	3		**Reserved:** Indeterminate value.
	2	GOOM16	**Global Indication for Out Of Time Slot 16 MultiFrame Alignment:** This bit position indicates when any of the 8 framers has detected a Time Slot 16 Multiframe Alignment Error. This bit position is cleared when the corresponding framer alarm is cleared.
	1		**Reserved:** Indeterminate value.
	0	GAUXP	**Global Indication for the Auxiliary Pattern Alarm:** This bit position indicates when any of the 8 framers has detected an Auxiliary Pattern Alarm. This bit position is cleared when the corresponding framer alarm is cleared.
01B	7		**Reserved:** Write this bit to 0.
	6	GMAIS16	**Global Mask for Time Slot 16 AIS Indication:** This bit disables the hardware interrupt for a Time Slot 16 AIS from any of the 8 framers.
	5	GMCRCE	**Global Mask for Excessive CRC Error Indication:** This bit disables the hardware interrupt for an Excessive CRC error from any of the 8 framers.
	4	GMRAI16	**Global Mask for Time Slot 16 RAI Indication:** This bit disables the hardware interrupt for a Time Slot 16 RAI from any of the 8 framers.
	3		**Reserved:** Write this bit to 0.
	2	GMOOM16	**Global Mask for Out Of Time Slot 16 MultiFrame Alignment Indication:** This bit disables the hardware interrupt for a Time Slot 16 Multiframe Alignment Error from any of the 8 framers.
	1		**Reserved:** Write this bit to 0.
	0	GMAUXP	**Global Mask for Auxiliary Pattern Indication:** This bit disables the hardware interrupt for an Auxiliary Pattern Alarm from any of the 8 framers.
01C	7-0	CHS8-CHS1	**Channel Activity Line Event for Channels 1 through 8:** When a bit is set to 1, it indicates the framer (1 through 8) that caused the global line indication (AIS16, Excessive CRC, RAI16, OOMF for Time Slot 16, or Aux. Pattern alarms).

Line Interface Control Registers

These registers are read/write, except for register 020H, which is read-only unlatched. The control bits in these registers determine the Line Interface Control information flow between the E1Fx8 and the external line interface transceivers that support "Host Mode" control. It also enables the monitor mode for the E1Fx8 in the 208-lead package.

Address (Hex)	Bit	Symbol	Description
01D	7	BDCST	**Broadcast Command:** When set to 1, the two bytes in the command byte and the data output byte are broadcasted to all external line interface transceivers. This is accomplished by forcing all line interface chip select leads ($\overline{\text{LCSn}}$) to an active low state.
	6	ESP	**Enable Line Interface:** When set to 1, a data transfer takes place between the E1Fx8 and the selected line interface transceiver (E1CHS2-E1CHS0). This bit must be first written to a 0 before another data transfer can take place
	5	ESPBMON	**Enable Serial Port / Monitoring Port Select:** When set to 1 and the 208-lead version is used, MONCLK, MONFRM, and MONDAT use leads LSCLK, LSDI, and LSDO respectively. When this bit is set to 0, leads LSCLK, LSDI and LSDO are used for line interface transceiver control
	4-3		**Reserved:** Write these bits to 0.
	2-0	E1CHS2-E1CHS0	**External Line Interface Selection:** Selects the external line interface transceiver, according to the table given below: **E1CHS2 E1CHS1 E1CHS0 External Transceiver** 0 0 0 Framer 1 0 0 1 Framer 2 0 1 0 Framer 3 0 1 1 Framer 4 1 0 0 Framer 5 1 0 1 Framer 6 1 1 0 Framer 7 1 1 1 Framer 8
01E	7-0	LCB7-LCB0	**Line Interface Control Command Byte:** The bits in this register location form the command byte for the external transceivers. This byte is shifted out of this register starting with bit LCB0 first.
01F	7-0	LDO7-LDO0	**Line Interface Data Output Byte:** The bits in this register location form the data output byte for the external transceivers. This byte is shifted out of this register starting with bit LDO0 first.
020	7-0	LDI7-LDI0	**Line Interface Data Input Byte:** The bits in this register location form the data input byte from the external transceivers. This byte is shifted into this register starting with bit LDI0 first.

Monitor Control Registers

These registers select the source of the E1 signal to be monitored, if any, on leads MONCLK, MONDAT and MONFRM or leads LSCLK, LSDO and LSDI in the 208-lead version when control bit ESPBMON (bit 5) in register 01DH is set to a 1. They also determine where in the selected framer (transmit, receive line or receive framer) the E1 signal is monitored.

Address (Hex)	Bit	Symbol	Description
022	7	MONRX	**Monitor Receive (or Transmit) Framer:** Works in conjunction with the MONRF and MONTR control bits according to the following table. **MONRX** **MONRF** **MONTR** **Action** X X 1 Monitor data, clock, and framing pulse leads tristated. 0 X 0 Monitor transmit framer output 1 0 0 Monitor input to receive framer 1 1 0 Monitor output from receive framer
	6	MONRF	**Monitor Receive Framer Output:** Works in conjunction with the MONRX and MONTR control bits according to the table given above.
	5	MONTR	**Monitor Leads Tristate enable:** Works in conjunction with the MONRX and MONTF control bits according to the table given above.
	4-3		**Reserved:** Write these bits to 0.
	2-0	MFR2-MFR0	**Monitor Framer Selection:** Selects the framer to be monitored according to the table given below. **MFR2** **MFR1** **MFR0** **Framer to be Monitored** 0 0 0 Framer 1 0 0 1 Framer 2 0 1 0 Framer 3 0 1 1 Framer 4 1 0 0 Framer 5 1 0 1 Framer 6 1 1 0 Framer 7 1 1 1 Framer 8

Synchronization Control Registers

These read/write registers control the signals placed on clock reference output leads SCOUT1 and SCOUT2 and the source of the one-second clock used for performance monitoring functions.

Address (Hex)	Bit	Symbol	Description
024	7	S18KHZ	**Synchronization 8 kHz Reference Enable No.1:** A 1 selects the synchronization output clock reference for the framer selected to be an 8 kHz rate. A 0 selects the clock reference to be a 2048 kHz rate.
	6	S1CTRI	**Synchronization Output Clock Lead Tristate Enable No. 1:** A 1 causes the synchronization output clock lead (SCOUT1) to tristate.
	5	S1YNCEN	**Synchronization Output Clock Lead Low on LOS Enable No. 1:** A 1 enables the synchronization output clock lead (SCOUT1) to go low when a receive line loss of signal is detected. When set to 0, the selected clock continues to be output.
	4	S1SEXTB	**Source One-second Clock External:** When set to 0, the one-second clock source is from lead SRGET. A 1 selects either a received line clock or the backplane oscillator (from lead BPOSC) as a clock source and causes lead SRGET to become an output. See the table below for S1SINT.
	3	S1SINT	**Source One-second Clock Internal Selection:** This bit is used in conjunction with control bits S1SEXTB and S1YNC2-S1YNC0 to select the one-second clock for supporting automatic FDL, shadow counter and performance register latching, loop up and down code timing, and DS0 loopback activate and deactivate timing. The selection is according to the table below (where X=don't care): **S1SEXTB** / **S1SINT** / **Source of One-second Clock** 0 / X / External lead SREGT 1 / 0 / Internal from lead BPOSC; One-second Clock out on SRGET 1 / 1 / Internal from one of the 8 framer line receive clocks as selected by S1YNC2 - S1YNC0; One-second Clock out on SRGET
	2-0	S1YNC2-S1YNC0	**Synchronization Clock Selection No.1:** Selects the framer from which the clock (2048 kHz or 8 kHz) is to be monitored according to the table given below. **S1YNC2** / **S1YNC1** / **S1YNC0** / **Framer to be Monitored** 0 / 0 / 0 / Framer 1 0 / 0 / 1 / Framer 2 0 / 1 / 0 / Framer 3 0 / 1 / 1 / Framer 4 1 / 0 / 0 / Framer 5 1 / 0 / 1 / Framer 6 1 / 1 / 0 / Framer 7 1 / 1 / 1 / Framer 8

Address (Hex)	Bit	Symbol	Description
025	7	S28KHZ	**Synchronization 8 kHz Reference Enable No.2:** A 1 selects the synchronization output clock reference for the framer selected to be an 8 kHz rate. A 0 selects the clock reference to be a 2048 kHz.
	6	S2CTRI	**Synchronization Output Clock Lead Tristate Enable No. 2:** A 1 causes the synchronization output clock lead (SCOUT2) to tristate.
	5	S2YNCEN	**Synchronization Output Clock Lead Low on LOS Enable No. 2:** A 1 enables the synchronization output clock lead (SCOUT2) to go low when a receive line loss of signal is detected. When set to 0, the selected clock continues to be output.
	4-3		**Reserved:** Write these bits to 0.
	2-0	S2YNC2-S2YNC0	**Synchronization Clock Selection No.2:** Selects the framer from which the clock (2048 kHz or 8 kHz) is to be monitored according to the table given below. **S2YNC2 / S2YNC1 / S2YNC0 / Framer to be Monitored** 0 0 0 Framer 1 0 0 1 Framer 2 0 1 0 Framer 3 0 1 1 Framer 4 1 0 0 Framer 5 1 0 1 Framer 6 1 1 0 Framer 7 1 1 1 Framer 8

Loss of Signal Detection Interval, Ones Density and Code for RAI, and AIS (Trunk Conditioning) Registers

Address (Hex)	Bit	Symbol	Description
02A	7-0	LOSI7-LOSI0	**Loss of Signal Detection and Recovery Interval Select:** The binary value written to this register selects the number of consecutive missing pulses used to declare loss of signal. The normal range is between 10 and 255. Bit 0 is the LSB. This value can be extended via control bit ENLOSI (bit 7) in register 02BH. This value is also used to set the duration of the recovery interval (see register 02BH).
02B	7	ENLOSI	**Enable LOS detection for ISDN:** When set to 1, the value for LOSI7-LOSI0 in register 02AH is multiplied by 16 for the detection period only (this permits up to 2 millisecond period to detect LOS); the recovery interval remains unchanged. When set to a 0, LOSI7-LOSI0 is multiplied by 1. To comply with ITU-T G.775 set this bit to 0 and use LOSI7-LOSI0 to set the detection window. To comply with ITU-T I.431 set this bit to a 1 and LOSI7-LOSI0 to 7FH.
	6		**Reserved:** Write this bit to 0.
	5-0	OND5-OND0	**Ones Density Loss of Signal Recovery Threshold Select:** The binary value written to this register selects the minimum number of ones that must occur in the recovery interval set up by register 02AH to recover loss of signal. This value must be less than the value written in register 02AH. For a loss of signal recovery interval value of 255, the recovery threshold value is normally set to 32. Bit 0 is the LSB.
02C	7-4	CODERAI (3-0)	**Code for RAI for Signaling:** When the E1Fx8 detects a RAI, the value in this register may be substituted for the signaling nibbles forwarded to the signaling highway under control of control bit RX0RAI (bit 5) in register X+03H. Do not set this code to 0000 as it may mimic the signaling multiframe pattern. Control bit RSINV (bit 6) in register X+04H when set to a 1 will invert the value placed on the signaling highway.
	3-0	CODEAIS (3-0)	**Code for AIS for Signaling:** When the E1Fx8 detects AIS, the signaling nibbles on the signaling highway may have this code substituted in place of the frozen values in the Receive Signaling RAM. Control bit RX0AISE (bit 7) in register X+03H controls this function. If the A-bits are set to a 1 on the transmit signaling highway and control bit TX0AISE (bit 1) in register X+06H is set to a 1, this code may be substituted for all the signaling nibbles in Time Slot 16 in place of the Transmit Signaling RAM values. Do not set this code to 0000 as it may mimic the signaling multiframe pattern. Control bit RSINV (bit 6) in register X+04H when set to a 1 will invert the value placed on the signaling highway for RT0AIS (bit 6) in register X+03H or for control bit RX0AISE (bit 7) in register X+03H set to a 1 and E1 AIS, LOS or OOF is detected.

Receive and Transmit Framing Pulse (Sync) Delay Control Registers

The values written in these two read/write registers control the number of clock cycles by which the transmit framing pulse (TTFRMn) and receive framing pulse (RTFRMn) will be delayed relative to the transmit system data (TTDATn) and receive system data (RTDATn), respectively.

Address (Hex)	Bit	Symbol	Description
02E	7-0	RFRM7-RFRM0	**Receive Framing Pulse Position Selection:** The control bits in this register determine the location of the framing pulse (RTFRMn) relative to the receive data lead (RTDATn). The clock (RTCLKn) and frame pulse (RTFRMn) must be inputs (slip buffer enabled also). When set to 00H, the frame pulse is synchronous with bit 8 of the last time slot in transmission mode or the start of frame in Data mode, MVIP or H-MVIP mode. Each bit advances the frame pulse one 2.048 MHz clock cycle or eight 16.384 MHz clock cycles. The default value is 00H.
02F	7-0	TFRM7-TFRM0	**Transmit Framing Pulse Position Selection:** The control bits in this register determine the location of the framing pulse (TTFRMn) relative to the transmit data lead (TTDATn). The slip buffer must be enabled. The delay is the same as RFRM7-RFRM0 above. Each bit advances the frame pulse one 2.048 MHz clock cycle or eight 16.384 MHz clock cycles. The default value is 00H.

Auxiliary Port Clock Selection and Time Slot Direction Registers

Address (Hex)	Bit	Symbol	Description
037	7-5		**Reserved:** Write these bits to 0.
	4	CONCATEN	**Concatenation Control:** When set to a 1, a check is made for all Auxiliary Port transfers such that a contiguous group of time slots will be switched to another contiguous group of time slots with all source time slots from frame N being placed in destination time slots for frame M. When set to a 0, source time slots from frame N will be placed in the defined destination time slots at the next available opportunity without regard for the decisions made for other time slots.
	3	TACKSEL	**Transmit Auxiliary Port Clock Selection:** This control bit works in conjunction with control bit TADIRSEL to select the source of TACLK and TASYNC when they are outputs; see below.
	2	TADIRSEL	**Transmit Auxiliary Port Clock Direction:** When set to a 0 TACLK and TASYNC are inputs. When set to a 1 TACLK and TASYNC are outputs per the following selection by control bit TACKSEL above (where X=don't care). **TACKSEL** **TADIRSEL** **Clock Selection Criteria** X 0 TACLK and TASYNC are inputs 0 1 Receive Line Clock is source for TACLK and TASYNC which are outputs; S1YNC2-S1YNC0 (bits 2-0) in register 024H select the received line. 1 1 Lead BPOSC is source for TACLK and TASYNC which are outputs.

Address (Hex)	Bit	Symbol	Description
037 (cont.)	1	RACKSEL	**Receive Auxiliary Port Clock Selection:** This control bit works in conjunction with control bit RADIRSEL to select the source of RACLK and RASYNC when they are outputs; see below.
	0	RADIRSEL	**Receive Auxiliary Port Clock Direction:** When set to a 0 RACLK and RASYNC are inputs. When set to a 1 RACLK and RASYNC are outputs per the following selection by control bit RACKSEL above (where X=don't care). **RACKSEL / RADIRSEL / Clock Selection Criteria** X / 0 / RACLK and RASYNC are inputs 0 / 1 / Receive Line Clock is source for RACLK and RASYNC which are outputs; S1YNC2-S1YNC0 (bits 2-0) in register 024H select the received line. 1 / 1 / Lead BPOSC is source for RACLK and RASYNC which are outputs.
038	7-0	RDIR7-RDIR0	**Receive Auxiliary Port Directionality Register for Time Slots 31 through 0:** A 0 on RDIRn will connect time slot n on the Receive Auxiliary Port to the output of the receive decoder for the framer and time slot selected control bits RAFRSELn(2-0) and RATSSELn(4-0). A 1 on RDIRn will connect time slot n on the Receive Auxiliary Port to the output of the Transmit Slip Buffer for the framer and time slot selected control bits RAFRSELn(2-0) and RATSSELn(4-0).
039	7-0	RDIR15-RDIR8	
03A	7-0	RDIR23-RDIR9	
03B	7-0	RDIR31-RDIR24	
03C	7-0	TDIR7-TDIR0	**Transmit Auxiliary Port Directionality Register for Time Slots 31 through 0:** A 1 on TDIRn will connect time slot n on the Transmit Auxiliary Port in place of the input to the Receive Slip Buffer for the framer and time slot selected control bits TAFRSELn(2-0) and TATSSELn(4-0). A 0 on TDIRn will connect time slot n on the Transmit Auxiliary Port in place of the output of the Transmit Slip Buffer for the framer and time slot selected control bits TAFRSELn(2-0) and TATSSELn(4-0).
03D	7-0	TDIR15-TDIR8	
03E	7-0	TDIR23-TDIR9	
03F	7-0	TDIR31-TDIR24	

Auxiliary Port Receive and Transmit Data Selection Registers

Address (Hex)	Bit	Symbol	Description
040 through 05F	7-5	RAFRSEL31(2-0)-RAFRSEL0(2-0)	**Receive Auxiliary Port Time Slot Control Register for Time Slots 31-0:** For each time slot, n, on the Receive Auxiliary Port, RAFRSELn(2-0) selects the framer (000 for framer #1 to 111 for framer #8) and RATSSELn(4-0) selects the time slot on the selected framer's port (00000 for Time Slot 0 to 11111 for Time Slot 31).
	4-0	RATSSEL31(4-0)-RATSSEL0(4-0)	

Address (Hex)	Bit	Symbol	Description
060 through 07F	7-5	TAFRSEL31(2-0)-TAFRSEL0(2-0)	**Transmit Auxiliary Port Time Slot Control Register for Time Slots 31-0:** For each time slot, n, on the Transmit Auxiliary Port, TAFRSELn(2-0) selects the framer (000 for framer #1 to 111 for framer #8) and TATSSELn(4-0) selects the time slot on the selected framer's port (00000 for Time Slot 0 to 11111 for Time Slot 31).
	4-0	TATSSEL31(4-0)-TATSSEL0(4-0)	

Other Control Registers (common to all channels)

The reserve bits in both registers must be set to 0 for normal device operation.

Address (Hex)	Bit	Symbol	Description
0FE	7-6		**Reserved:** Write these bits to 0.
	5	RESECKSYN	**Reset Clock Synthesis in E1 Mode:** This bit when set to a 1 causes the internal clock synthesis block to be reset if control bit DISECKSYN is set to a 0. If this bit is set to a 0, the internal clock synthesis block if selected by DISECKSYN also set to a 0. See the table below in the description of DISECKSYN.
	4	DISECKSYN	**Disable Clock Synthesis:** This bit when set to a 1 causes the internal clock synthesis block to be disabled and an external clock reference needs to be applied to lead DPLLREF for Receive Dejitter Buffer operation. When this control bit is a 0 the internal clock synthesis block is enabled, generating a reference clock 31.5 times the clock input at lead BPOSC and output on lead DPLLREF. This control bit works in conjunction with control bits RESECKSYN (in this register), RECENTER and BYPASS (bits 1 and 0) in register X+161H to control the Receive Dejitter Buffer function (where X=don't care).
	3-0	DEBVAL(3-0)	**Signaling Debounce Value:** The value set in this register determines the number of multiframes that any particular signaling nibble must remain the same to be placed in the Receive Debounce Signaling Buffer and placed on the signaling highway when signaling debounce is enabled by control bit SIGDB (bit 4) in register X+134H being set to a 1. DEBVAL(3-0) may not be set to 0H if SIGDB is set to 1.

DISECKSYN	RESECKSYN	BYPASS	Function
X	X	0	E1 DPLL bypassed
1	1	0	E1 DPLL bypassed and DJB powered down
0	0	1	E1 internal DPLL
0	1	1	E1 internal DPLL held reset
1	1	1	E1 external reference

<table>
<tr><th>Address (Hex)</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td rowspan="4">0FF</td><td>7</td><td>WG</td><td>Test Equipment BPV Selection: A 1 enables the decoder to detect coding violations as found in certain test equipment (e.g., Wandel and Golterman™). A 0 enables the decoder to detect coding violations as found in other types of test equipment (e.g., Tberd™). The following table summarizes the two decoding procedures of coding violations:
<table>
<tr><th>BPV HDB3</th><th>1 (Wandel and Golterman)</th><th>0 (Tberd)</th></tr>
<tr><td>+ + or - -</td><td>000 (preceding bit changed)</td><td>11</td></tr>
<tr><td>0BV or 000V</td><td>0000</td><td>1010 or 0001</td></tr>
<tr><td>BB00V after odd</td><td>1000</td><td>1101</td></tr>
<tr><td>BB00V after even</td><td>1000</td><td>1001</td></tr>
</table></td></tr>
<tr><td>6-3</td><td></td><td>Reserved: Write these bits to 0.</td></tr>
<tr><td>2</td><td>OBT1SI</td><td>Observe One-second: When set to 1, the internally selected one-second clock is output on the MONFRM lead. Otherwise set this bit to 0.</td></tr>
<tr><td>1-0</td><td></td><td>Reserved: Write these bits to 0.</td></tr>
</table>

PER CHANNEL REGISTERS

Framer Configuration and Control Registers

The following register descriptions pertain to each of the eight channels (framers). The control bits in the following read/write registers are used to configure the E1Fx8 for the various modes of operation on a per channel basis.

Address (Hex)	Bit	Symbol	Description
X+00	7	RAIL	**Dual Unipolar/NRZ Mode Selection:** A 1 will enable the receive and transmit framer interface for dual unipolar operation, while a 0 enables the receive and transmit framer interface for an NRZ interface.
	6	BE	**HDB3 Enable:** When set to 1 in Dual Unipolar mode (RAIL above set to a 1), the HDB3 transcoder will be enabled. When set to 0 in Dual Unipolar mode (RAIL above set to a 1), the AMI mode will be selected for the codec.
	5	RXCP	**Receive Clock Polarity Selection:** A 1 enables the receive line signals to be clocked in on rising edges of the line clock (or substitution clock when enabled), while a 0 enables the line input to be clocked in on falling edges of the line clock (RCLKn).
	4	RXNRZ	**Receive NRZ Data Polarity Inversion Enable:** The RAIL bit above must be set to 0 for this control bit to be enabled. A 1 inverts the polarity of the receive NRZ data lead (RNRZn).
	3	EXLOS	**Receive External Loss of Signal Enable:** Enabled when control bit RAIL is 0 (NRZ interface). A 0 enables an external bipolar count to be clocked into the framer on signal lead RSCANn and counted by the 16 bit BPV counter. A 1 enables an external loss of signal indication to be clocked into the framer. This loss of signal function is treated in the same way as an internally detected LOS function for alarm propagation and consequent actions.
	2	ELOSN	**Receive External Loss of Signal Sense:** Enabled when control bit RAIL is a 0, and control bit EXLOS is a 1. A 0 written to this bit indicates the external input LOS signal true sense is positive. A 1 indicates the sense is negative.
	1	ENZC	**Enable Excess Zeros Count:** The RAIL bit must be set to 1 for this control bit to take effect. A 1 sets the BPV counter to count an excessive zeros condition. For a HDB3 line code, every 4 consecutive zeros will be counted as a single error. For the AMI line code, every 16 consecutive zeros will be counted as a single error.
	0	TS16EIC	**Time Slot 16 Event Indication Configuration:** The Time Slot 16 event indications (Time Slot 16 AIS, Time Slot 16 RAI, etc. alarms) are combined with normal channel event indications when set to 1. Such combination is disabled when set to 0 and the Time Slot 16 specific events indications will show up at 01AH and 01CH globally and from X+164H through X+168H on a per channel basis, so they can be distinguished from other channel events.

Address (Hex)	Bit	Symbol	Description
X+01	7	RTFM	**Receive Framer Transparent Control Bit:** This bit works in conjunction with the TTFM control bit according to the following table (where X=don't care). **RTFM** / **TTFM** / **Format Selected** 1 / X / Receive framer transparent. X / 1 / Transmit framer transparent.
	6	TTFM	**Transmit Framer Transparent Control Bit:** This bit works in conjunction with the RTFM control bit according to the above table.
	5	BFAA	**Basic Frame Alignment Algorithm:** When set to 0, the Standard algorithm is selected. When set to 1, the Frame Hold-Off algorithm is selected. Note: When in a particular mode, a change in state of this bit will trigger a realignment procedure. The Operations section describes the differences between the two modes (algorithms).
	4	CASA	**Channel Associated Signaling Alignment:** When set to zero selects the G.732 compatible algorithm. When set to one selects the Enhanced algorithm. Any transition on this signal will trigger a realignment procedure using the selected algorithm.
	3	CRCA	**Automatic CRC-4 / Non CRC-4 Interworking:** When set to 0 the manual operation is selected. A search for multiframe alignment is started in consecutive 8 millisecond periods; 2 multiframe alignment patterns separated by a multiple of 2 milliseconds is required to establish multiframe alignment. If alignment is not established, the process is to be repeated; in addition an off line research for basic frame alignment is to be performed. If control bit AAGS is set to a 1, the RAI alarm is set for a single NFAS frame and returned to zero. Control bit AIW when set to a 0 causes the 400 millisecond timer to monitor the process; if multiframe alignment fails to be found in 400 milliseconds RAI is set continuously until multiframe alignment is found. When set to 1 and control bit AIW is set to a 0, the automatic operation for ITU-T G.706 is selected. The RAI A-bit is set to 0 from a 1 (OOF) indicating basic frame alignment and the E-bit is set to a 0 (FEBE). A search for multiframe alignment is started in consecutive 8 millisecond periods; 2 multiframe alignment patterns separated by a multiple of 2 milliseconds is required to establish multiframe alignment. If alignment is not established, the process is to be repeated; in addition an off line re-search for basic frame alignment is to be performed. After 400 milliseconds interworking is to be assumed not to exist if multiframe alignment cannot be found and the E1Fx8 will remain in basic frame alignment. If multiframe alignment is found before the 400 millisecond timer expires, interworking is established with the E-bit being set to 1 (set to a 0 only to indicate a CRC-4 error in a sub multiframe). For ETSI interworking for CTR-4, no 400 millisecond time out is used, hence set control bit AIW to a 1 (there is no time out if CRCA = 0). Note: When control bit AIW is set to a 1, the 400 millisecond time out does not apply to either algorithm, but the rest of either algorithm is used. Any transition on this signal will trigger a realignment procedure using the selected option. Once in multiframe alignment only excessive CRC-4 errors or loss of basic frame alignment will cause a restart of these algorithms.

Address (Hex)	Bit	Symbol	Description
X+01 (cont.)	2-1	OOF1-OOF0	**Out Of Frame Detection Criteria:** The OOF bits determine the Out Of Frame detection criteria according to the following table: **OOF1** **OOF0** **Out Of Frame Detection Criteria** 0 0 Three consecutive FAS patterns in error. 0 1 Four consecutive FAS patterns in error. 1 0 Three consecutive FAS patterns in error or three consecutive NFAS patterns in error. 1 1 Four consecutive FAS patterns in error or four consecutive NFAS patterns in error. The FAS pattern is defined as X0011011, and the NFAS pattern is defined as X1XXXXXX. These two patterns occur in alternating frames.
	0	AAGS	**Alternate Alarm Generation Selection:** When set to 1, A- and E-bit alarm generation with respect to out of frame and out for multiframe will behave as specified in ETS 300 011 (also see ITU-T G.704, G.706, 1988). A-bit (RAI) will be set each time a re-search for multiframe alignment is performed and the E-bits will be set to 1 unless CRC-4 errors are detected after multiframe alignment is achieved. When set to 0, A- and E-bit alarm generation with respect to out of frame and out of multiframe will behave as specified in ITU-T G.704, G.706, 1991. In this case the E-bits are set to 0 and the A-bit is set to 1 initially. When basic frame alignment is reached the A-bit is set to 0. The A-bit is only set to 1 again if basic frame alignment is lost due to loss of the Time Slot 0 FAS and NFAS codes for excessive CRC-4 errors after multiframe alignment is reached (not if an alternate frame position is chosen of if multiframe alignment can not be reached). The E-bits are set to 1 once multiframe alignment is reached, one E-bit toggling to 0 for each sub-multiframe error detected in a multiframe using the CRC-4 check.
X+02	7	ENAIS	**Enable Receive AIS on AIS Alarm:** A 1 enables the generation of AIS downstream by forcing the A-bits in the signaling highway to 1 (transmission Interface only) when control bit ENABIT is a 1, or all ones on the data highway when control bit ENDBIT is a 1 upon the detection of AIS.
	6	ENOOF	**Enable Receive AIS on an OOF Alarm:** A 1 enables the generation of AIS downstream by forcing the A-bit in the signaling highway to 1 (transmission highway only) when control bit ENABIT is a 1, or all ones on the data highway when control bit ENDBIT is a 1 upon the detection of an OOF alarm.
	5	ENLOS	**Enable Receive AIS on an LOS Alarm:** A 1 enables the generation of AIS downstream by forcing the A-bit in the signaling highway to 1 (transmission interface only) when control bit ENABIT is a 1, or all ones on the data highway when control bit ENDBIT is a 1 upon the detection of an LOS (also external LOS if enabled) alarm.

Address (Hex)	Bit	Symbol	Description
X+02 (cont.)	4	ENABIT	**Enable Receive Signaling Highway A-bit Alarm Indication:** When set to 1 in the Transmission Mode, a OOF, AIS, or LOS alarm when enabled by the corresponding enable bit (ENOOF, ENAIS, or ENLOS) causes the one state for the RTSIGn receive signaling highway A-bits for the duration of the alarm.
	3	ENDBIT	**Enable AIS on Receive Data Highway:** When set to 1, a E1 OOF, AIS, or LOS alarm when enabled by the corresponding enable bit (ENOOF, ENAIS, or ENLOS) causes unframed AIS to be generated on lead RTDATn for the duration of the alarm.
	2	RTAIS	**Send Receive System Side AIS:** A 1 will set the A-bit in the signaling highway (in the Transmission Mode only) to a 1, when control bit ENABIT is a 1. A 1 will also cause an unframed AIS on the data highway when control bit ENDBIT is a 1.
	1	ENRAI	**Enable RAI on Receive Signaling Highway:** When set to 1, a receive RAI alarm causes the R-bit (bit 3) in Time Slot 0 of odd frames in the RTSIGn signaling highway for the Transmission Mode to be 1 for the duration of the received RAI alarm.
	0	RTRAI	**Send Receive System Side RAI Indication:** A 1 causes the R-bit (bit 3) in Time Slot 0 of odd frames on the signaling highway for the Transmission Mode to be 1.
X+03	7	RX0AISE	**Receive Time Slot AIS Enable:** A 1 enables Time Slot AIS to be sent when a E1 OOF, AIS, or LOS alarm is detected. Time Slot AIS is defined as a special signaling code ABCD=CODEAIS (bits 3-0) in register 02CH. This signaling code is inserted into the signaling bits to the signaling highway for all channels. Setting CODEAIS =1111 may be used to comply with ITU-T G.732 automatically.
	6	RT0AIS	**Sent Receive Time Slot AIS:** A 1 causes the Time Slot AIS signaling code (ABCD=CODEAIS (bits 3-0) in register 02CH) to be inserted into all system side Time Slot signaling bits. Setting CODEAIS = 1111 may be used to meet ITU-T G.732 manually on excessive BER as detected by framing word error counts.
	5	RX0RAI	**Receive Time Slot RAI Enable:** A 1 enables Time Slot RAI to be sent in all system side time slots signaling bits on the signaling highway when a E1 RAI alarm is detected. Time Slot RAI is defined as a special signaling code ABCD= CODERAI (bits 7 - 4) in register 02CH. This signaling code is inserted into the signaling bits for all channels.
	4	RT0RAI	**Sent Receive Time Slot RAI:** A 1 causes the Time Slot RAI signaling code (ABCD= CODERAI (bits 7 - 4) in register 02CH) to be inserted into all system side time slot signaling bits.

Address (Hex)	Bit	Symbol	Description
X+03 (cont.)	3	ENRXNBR	**Enable Receive National Bit Registers:** A 1 enables the E1Fx8 channel to receive National bits as bytes in registers RSA4(7-0) through RSA8(7-0) and to process alarms for ISDN from the national bit Sa6. See the Sa6 status register at X+175H, the Sa6 counters at X+177H through X+17EH and RSA4(7-0) through RSA8(7-0) in registers X+16FH through X+173H. Control bits CRCMD1,0 (bits 3 and 2) in register X+07H should be set to a CRC-4 mode for RSA4 through RSA8 byte alignment to the multiframe.
	2	EOOCRC	**Enable Out Of Multiframe Alarm on Loss of CRC Multiframe:** A 1 enables a Time Slot 0 loss of CRC multiframe to cause an Out Of Multiframe alarm. When TS16EIC is set, an Out Of Multiframe Alarm may also be caused by a Time Slot 16 loss of multiframe alignment. The following table summarizes the enable bits associated with the Out Of Multiframe alarm. **EOOCRC** / **EOO16M** / **Action** 0 / 0 / Out Of Multiframe alarm disabled. 0 / 1 / A Time Slot 16 Loss of Multiframe causes an Out Of Multiframe alarm. 1 / 0 / A Time Slot 0 Loss of CRC multiframe causes an Out Of Multiframe alarm. 1 / 1 / A Time Slot 16 Loss of Multiframe or a Time Slot 0 Loss of CRC multiframe causes an Out Of Multiframe alarm.
	1	EOO16M	**Enable Out Of Multiframe Alarm on Time Slot 16 Loss of Multiframe:** A 1 enables a Time Slot 16 loss of multiframe to cause an Out Of TS16 Multiframe alarm. When enabled and TS16EIC is set, an Out Of Multiframe Alarm may also be caused by Time Slot 16 loss of multiframe alignment. The table given above summarizes the operation of this bit.
	0	ENRXAUXP	**Enable Reception of the Auxiliary Pattern:** When set to a 1, an unframed alternating binary “10” pattern received 254 or more times on lead RPOSn/RNEGn or RNRZn for 250 microseconds will be detected as AUXP (bit 0) in register X+164H.
X+04	7	RDINV	**Receive Data Channels Inverted:** A 1 inverts the time slot bits in all time slots to the data highway (lead RTDATn); see RDADI below.
	6	RSINV	**Receive Signaling Bits Inverted:** A 1 inverts the ABCD signaling bits for all time slots to the signaling highway (lead RTSIGn); Time Slot 0 and alarm bits are not inverted. Also Time Slot 16 frame 0 (TS16 multiframe, X0, Y, X1 and X2) and A-bits are not inverted.
	5	TDINV	**Transmit Data Channels Inverted:** A 1 inverts the time slot bits in all time slots from the data or auxiliary highways (lead TTDATn/TTAIXn); see TDADI below.
	4	TSINV	**Transmit Signaling Bit Inverted:** A 1 inverts the ABCD signaling bits for all time slots from the signaling highway (lead TTSIGn); Time Slot 0 and alarm bits are not inverted. Also Time Slot 16 frame 0 (TS16 multiframe, X0, Y, X1 and X2) and A-bits are not inverted.

<table>
<tr><th>Address (Hex)</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td rowspan="5">X+04 (cont.)</td><td>3</td><td>RDADI</td><td>Receive Alternate Digit Inversion: When set to a 1, the time slots transmitted on RTDATn will have bits 2, 4, 6 and 8 inverted. When set to 0, the time slots are not to be inverted. Used to supply true A-law from ITU-T G.711 A-law. This control bit works in conjunction with control bit RDINV to produce the following options.

<table>
<tr><th>RDINV</th><th>RDADI</th><th>Function on Data to RTDATn</th></tr>
<tr><td>0</td><td>0</td><td>Data to the system side is not inverted</td></tr>
<tr><td>0</td><td>1</td><td>Bits 2, 4, 6 and 8 from every time slot to the system side will be inverted. Convert from G.711 A-law.</td></tr>
<tr><td>1</td><td>0</td><td>All bits from every time slot to the system side will be inverted.</td></tr>
<tr><td>1</td><td>1</td><td>Bits 1, 3, 5 and 7 to every time slot from the system side will be inverted.</td></tr>
</table></td></tr>
<tr><td>2</td><td>TDADI</td><td>Transmit Alternate Digit Inversion: When set to a 1, the time slots taken from TTDATn will have bits 2, 4, 6 and 8 inverted. When set to 0, the time slots are not to be inverted. Used to convert true A-law to ITU-T G.711 A-law. This control bit works in conjunction with control bit TDINV to produce the following options.

<table>
<tr><th>TDINV</th><th>TDADI</th><th>Function on Data from TTDATn</th></tr>
<tr><td>0</td><td>0</td><td>Data from the system side is not inverted</td></tr>
<tr><td>0</td><td>1</td><td>Bits 2, 4, 6 and 8 from every time slot from the system side will be inverted. Convert to G.711 A-law.</td></tr>
<tr><td>1</td><td>0</td><td>All bits from every time slot from the system side will be inverted.</td></tr>
<tr><td>1</td><td>1</td><td>Bits 1, 3, 5 and 7 from every time slot from the system side will be inverted.</td></tr>
</table></td></tr>
<tr><td>1</td><td>ENRAIA</td><td>Enable RAI Status From A-Bit: A 1 enables the detection of the A-bit in TS0 of odd-numbered frames to produce RAI status (bit 4 in register X+164H and/or X+10H).</td></tr>
<tr><td>0</td><td>ENRAIY</td><td>Enable RAI Status From Y-Bit: A 1 enables the detection of the Y-bit in TS16 to produce RAI status (bit 4 in register X+164H and/or X+10H) if control bit TS16EIC is set to a 0.</td></tr>
</table>

Address (Hex)	Bit	Symbol	Description
X+05	7	PWRD	**Power-Down Selection:** When set to 1, a power-down state is entered by the framer. The forcing function permits a deterministic output to be sent to the line interface unit. This function occurs prior to the selected line encoding function. This control bit works in conjunction with the FDAT and FPOL control bits below, according to the following table (where X=don't care): **PWRD FDAT FPOL Action** 0 0 X Normal Operation 0 1 0 Power-up with transmit output forced to 0. 0 1 1 Power-up with transmit output forced to 1. 1 0 X Do not use. 1 1 0 Power-down, transmit output set to 0. 1 1 1 Power-down, transmit output set to 1. Note: The line clocks are enabled in the power-down mode.
	6	FDAT	**Force Transmit Data Power-Down Mode:** Works in conjunction with the PWRD and FPOL bits as described in the table above.
	5	FPOL	**Force Transmit State Upon Power-Down:** Works in conjunction with the PWRD and FDAT control bits as described in the table above.
	4	SYFZ	**System Freeze:** A 1 forces the output line clock TCLKn (and RTCLKn if output) to 0, and gates off RCLKn/ RTCLKn/TTCLKn clocks, until this bit is written to a 0.
	3	TXCP	**Transmit Clock Polarity Selection:** A 1 enables the transmit line signals to be clocked out on rising edges of the line clock (TCLKn), while a 0 enables the line signals to be clocked out on falling edges of the line clock.
	2	TXNRZ	**Transmit NRZ Data Polarity Inversion Enable:** The RAIL bit must be set to 0 for this control bit to be enabled. A 1 inverts the polarity of the transmit NRZ data lead (TNRZn).
	1	ENLAIS	**Enable AIS Indication on Line AIS Detected:** A 1 enables detection of a line AIS to cause an AIS alarm, as shown in the table below.
	0	E16AIS	**Enable AIS Indication on AIS Detected in Time Slot 16:** A 1 enables an AIS detected in Time Slot 16 to cause an AIS alarm. When enabled, detection of a line AIS may be enabled to cause an AIS alarm by setting bit ENLAIS and TS16EIC to 1. The following table summarizes the enable bits associated with the AIS alarm. **E16AIS ENLAIS Action** 0 0 AIS Alarm detection disabled. 0 1 Line AIS detected causes an AIS alarm (bit 6) in register X+10H set to a 1. 1 0 Time Slot 16 AIS detected causes an AIS alarm. 1 1 Time Slot 16 AIS detected or line AIS detected causes an AIS alarm.

Address (Hex)	Bit	Symbol	Description
X+06	7	TXAIS	**Transmit AIS:** A 1 causes an unframed AIS (all ones unframed) to be transmitted continuously to the line until this bit is written with a 0.
	6	TXRAI	**Transmit RAI (Yellow) Alarm Indication:** A 1 causes an RAI (Yellow), the remote alarm indication to be transmitted to the line by setting bit 3 in all time slots 0 not carrying the frame alignment pattern (NFAS) to a 1. The RAI alarm indication will be sent continuously until this bit is written with a 0. Please note that the generation of an AIS will override the generation of an RAI (Yellow) alarm indication.
	5	EXTAIS	**External AIS Enable:** A 1 enables the generation of an unframed AIS to the line when the A-bits in the transmit signaling highway (lead TTSIGn) in the transmission interface are a 1.
	4	EXTRAI	**External RAI (Yellow) Alarm Enable:** A 1 enables the generation of an RAI (A-bit in Time Slot 0 NFAS frames set to 1) alarm in the transmit direction to the line when the R-bit (bit 3) in Time Slot 0 in NFAS (odd) frames on the transmit signaling highway is a 1 for the Transmission Mode only.
	3	ENTXAUXP	**Enable Transmission of the Auxiliary Pattern:** When set to a 1, the Auxiliary pattern, an unframed alternating binary “10” pattern, is transmitted on the E1 line continuously until this bit is written to a 0.
	2	ULAW	**mu-law Digital Milliwatt Select:** When set to a 1 the mu-law digital milliwatt specified in ITU-T G.711 Table 6/G.711 is provided for a time slot when TC1Cn, TC0Cn is set to 11. When set to 0 the A-law digital milliwatt specified in G.711 Table 5/G.711 will be provided for a time slot when TC1Cn, TC0Cn is set to 11.
	1	TX0AISE	**Transmit Time Slot AIS Enable:** A 1 enable Times Slot AIS to be inserted into all line side channel signaling bits when the A-bits in the transmission format are detected as a 1. Time Slot AIS is defined as a special signaling code ABCD= CODEAIS (bits 3 - 0) in register 02CH. This signaling code replaces the ABCD codes normally sent in Time Slot 16.
	0	ST0AIS	**Sent Transmit Time Slot AIS:** A 1 forces the Time Slot AIS signaling code (ABCD= CODEAIS (bits 3-0) in register 02CH) to replace the ABCD codes normally sent in Time Slot 16.
X+07	7	TDFME	**Transmit Drive Framing Pulse Enable:** Enabled when control bit RAIL is a 0 (NRZ interface). When this bit is written with a 0, the state written to TXDRV determines the state of the TDRVn signal. When this bit is a 1, a framing pulse is provided on the TDRVn lead.
	6	TXDRV	**Transmit Drive:** Enabled when control bit RAIL is a 0 (NRZ interface), and control bit TDFME is a 0. A 1 causes the TDRVn signal to a high, while a 0 causes the TDRVn signal to a low.
	5	TLMF	**Transmit Line Multiframe Framing Indication:** Enabled when control bit RAIL is a 0 (NRZ interface), and control bit TDFME is a 1. A 1 causes a 2 ms framing pulse to be transmitted on the TDRV lead. A 0 causes a 125 µs framing pulse to be transmitted on the TDRVn lead.

Address (Hex)	Bit	Symbol	Description
X+07 (cont.)	4	FE1M	**Fractional E1 Mode:** When set to 1 and the 208-lead version is used, RTAUXn, and TTAUXn uses leads RTSIGn, and TTSIGn respectively. The signaling highways are replaced with gapped clock or channel marker functions. When this bit is set to 0, leads RTSIGn and TTSIGn remain the signaling highways.
	3-2	CRCMD1, CRCMD0	**CRC Framing Mode:** The CRCMD1 and CRCMD0 control bits determines the CRC framing mode, according to the table given below: **CRCMD1** / **CRCMD0** / **CRC Framing Mode** 0 / 0 / Framed mode. CRC-4 enabled. When in sync the E-bits carry the results to the distant end. When out of sync, the E-bits are 0. 0 / 1 / Framed mode. CRC-4 disabled. Si bit used. 1 / 0 / Framed mode. CRC-4 enabled. When in sync the E-bits carry the results to the distant end. When out of sync, the E-bits are 0. 1 / 1 / Framed mode. CRC-4 enabled. The E-bits are always set to 1, if AAGS = 1 (otherwise, E-bits are set to 0 on a OOF condition).
	1	TAIS16E	**Transmit Time Slot 16 AIS Enable:** When set to 1, AIS (all ones) is transmitted in Time Slot 16, including the multiframe alignment pattern in frame 0 of a Time Slot 16 multiframe. AIS is defined as all ones. AIS is transmitted in Time Slot 16 until this bit is written with a 0.
	0	TS16YE	**Generate Remote Multiframe Alarm:** When set to 1, a Remote Multiframe Alarm is generated in TS16 (Y-bit; bit 6 in Time Slot 16 in frame 0 of a Time Slot 16 multiframe) until set to 0.
X+08	7	BPCRC4	**Bypass CRC-4 Mode:** When set to a 1 the receive framer output after the decoder and dejitter buffer is looped to the transmit framer input where one or more of the National bits (Sa4 through Sa8) may be replaced by being sourced from the Transmit Facility Data Link (any control bit in register X+0CH SA4 - SA8 set to a 1), from the signaling highway (control bit BNAL in register X+122H set to a 1) or from the Transmit Sa4-Sa8 Code Registers (TSA4S-TSA8S in register X+E3H set to 0). Otherwise, time slots 0 through 31 are passed through intact. CRC-4 is updated per ITU-T G.706 -1995 Annex C, not recalculated. Note that the transition of the BPCRC4 bit will cause bit errors. The receive framer may monitor alarms, but control bits AUTRAI and AUTY behave as if set to 0. Note that control bits PLP, RLP and LLP in register X+107H must be set to 0.
	6	SA4UP	**Sa4 Bit Update:** When set to a 1 and control bit BPCRC4 is set to a 1, the Sa4 bit is provided locally by the transmit framer and the CRC-4 is updated based on this bit's new value. When set to a 0 and BPCRC4 is set to a 1, Sa4 comes from the received line unchanged.
	5	SA5UP	**Sa5 Bit Update:** When set to a 1 and control bit BPCRC4 is set to a 1, the Sa5 bit is provided locally by the transmit framer and the CRC-4 is updated based on this bit's new value. When set to a 0 and BPCRC4 is set to a 1, Sa5 comes from the received line unchanged.

Address (Hex)	Bit	Symbol	Description
X+08 (cont.)	4	SA6UP	**Sa6 Bit Update:** When set to a 1 and control bit BPCRC4 is set to a 1, the Sa6 bit is provided locally by the transmit framer and the CRC-4 is updated based on this bit's new value. When set to a 0 and BPCRC4 is set to a 1, Sa6 comes from the received line unchanged.
	3	SA7UP	**Sa7 Bit Update:** When set to a 1 and control bit BPCRC4 is set to a 1, the Sa7 bit is provided locally by the transmit framer and the CRC-4 is updated based on this bit's new value. When set to a 0 and BPCRC4 is set to a 1, Sa7 comes from the received line unchanged.
	2	SA8UP	**Sa8 Bit Update:** When set to a 1 and control bit BPCRC4 is set to a 1, the Sa8 bit is provided locally by the transmit framer and the CRC-4 is updated based on this bit's new value. When set to a 0 and BPCRC4 is set to a 1, Sa8 comes from the received line unchanged.
	1	AUTRAI	**Automatic Time Slot 0 RAI Generation:** The RAI bit is defined as a Remote Alarm Indication, and it is carried in bit 3 in Time Slot 0 in the (NFAS) frames which are not carrying the frame alignment pattern. A 1 enables a loss of basic frame alignment on the receive side (as well as re-attempts to find CRC-4 multiframe alignment when control bit AAGS (bit 0) in register X+01H is set to a 1) to be transmitted as an RAI on the transmit side. Please note that the microprocessor can generate a Remote Alarm Indication independent of this feature by writing a 1 to control bit TXRAI (bit 6) in register X+06H. Set this bit to 0 when control bit RTFM (bit 7) in register X+01H = 1.
	0	AUTY	**Automatic Time Slot 16 RAI Generation:** The Y-bit is defined as a Remote Multiframe Alarm Indication in Time Slot 16. A 1 enables a loss of multiframe alignment caused by a loss of basic frame alignment in Time Slot 0 or a loss of Time Slot 16 multiframe alignment, as selected by the EOO16M (if control bit TS16EIC (bit 0) in register X+00H is set to a 1) control bits (bit 2) in register X+03H, on the receive side to set the Y-bit (bit 6) in Time Slot 16 in frame 0 of the multiframe to be transmitted as a 1. A 0 disables this automatic feature. Please note that the microprocessor can generate a Remote Multiframe Alarm Indication independent of this feature by writing a 1 to control bit TS16YE (bit 0) in register X+07H. Set the AUTY bit to 0 when control bit RTFM (bit 7) in register X+01H = 1.
X+0A	7	SRST	**Software Reset Channel:** When set to 1, the channel is initialized and held in the reset state until a 0 is written into this bit position.
	6	RSYNC	**Receive Framer Resynchronization:** A 1 forces the framer to reset the frame alignment circuit and start a new frame alignment search, treating the present position as a last choice. To start another search, this bit must be first written with a 0, followed by a 1.
	5-1		**Reserved:** Write these bits to 0.

Address (Hex)	Bit	Symbol	Description
X+0A (cont.)	0	AIW	**Alternate Alarm Integration Window Control:** When set to a 1, the 400 millisecond timer used to time the end of CRC-4/Non CRC-4 interworking search period or the 400 millisecond timer associated with sending a continuous RAI when control bit AAGS (bit 0) in register X+01H is set to a 1 are to be suspended. When this bit is a 0, the 400 millisecond timers are allowed to time out.

Receive Fractional E1 Channel Control Registers

Address (Hex)	Bit	Symbol	Description
X+1A	7	RCHMK	**Receive Channel Marker:** A 1 written into this bit selects a 64 kHz channel marker to be output on lead RTAUXn for the receive fractional E1 channels, selected by control bits RFCH0-RFCH31 in registers X+1BH, X+1C, X+1D and X+1E. A 0 selects a 64 kbit/s gapped clock for the fractional channels selected by control bits RFCH0-RFCH31.
	6-0		**Reserved:** Write these bits to 0.
X+1B	7-0	RFCH7-RFCH0	**Receive Fractional E1 Time Slot 7-0 Enable:** Enabled for Transmission and Data Modes only. A 1 written to one or more control bits in this register, causes a 64 kHz gapped clock or channel marker to be generated on the RTAUXn lead.
X+1C	7-0	RFCH15-RFCH8	**Receive Fractional E1 Time Slot 15-8 Enable:** Enabled for Transmission and Data Modes only. A 1 written to one or more control bits in this register, causes a 64 kHz gapped clock or channel marker to be generated on the RTAUXn lead.
X+1D	7-0	RFCH23-RFCH16	**Receive Fractional E1 Channels 23-16 Enable:** Enabled for Transmission and Data Modes only. A 1 written to one or more control bits in this register, causes a 64 kHz gapped clock or channel marker to be generated on the RTAUXn lead.
X+1E	7-0	RFCH31-RFCH24	**Receive Fractional E1 Channels 32-25 Enable:** Enabled for Transmission and Data Modes only. A 1 written to one or more control bits in this register, causes a 64 kHz gapped clock or channel marker to be generated on the RTAUXn lead.

Transmit Fractional E1 Channel, Digital Milliwatt, and Idle Code Control Registers

Address (Hex)	Bit	Symbol	Description
X+110	7	TCHMK	**Transmit Channel Marker:** When this bit is a 1, a channel marker instead of a gapped clock is generated for the transmit fractional E1 channels selected by TC1Cc, TC0Cc.
	6-0		**Reserved:** Write these bits to 0.

Address (Hex)	Bit	Symbol	Description
X+111	7 6 5 4 3 2 1 0	TC1C3 TC0C3 TC1C2 TC0C2 TC1C1 TC0C1 TC1C0 TC0C0	**Transmit Control for Time Slots 31-0:** Provides the various modes of operation according to the following table. Where c is time slots 31-0. **TC1Cc** **TC0Cc** **Action** 0 0 Normal Operation 0 1 Fractional E1 Channel; gapped clock or marker on TTAUXn; data from TTAIXn 1 0 Idle Code Insertion 1 1 A-law or mu-law Digital Milliwatt Note: Time Slot 0 contents are generated internally; TC1C0, TC0C0 only can generate a gapped clock on TTAUXn
X+112	7-0	TC1C7-TC0C4	
X+113	7-0	TC1C11-TC0C8	
X+114	7-0	TC1C15-TC0C12	
X+115	7-0	TC1C19-TC0C16	
X+116	7-0	TC1C23-TC0C20	
X+117	7-0	TC1C27-TC0C24	
X+118	7-0	TC1C31-TC0C28	
X+119	7-0	IDL7-IDL0	**Idle Code Insertion:** The value written to this register by the microprocessor is transmitted when the idle code feature is selected by the control bits TC1Cc-TC0Cc in registers X+111H through X+118H. Bit 7 represents the first bit to be transmitted.
X+161	7-3		**Reserved:** Write these bits to 0.
	2	ATTNLM	**Attenuation Limit:** When set to a 0, the dejitter buffer will not recenter due to an overflow or underflow, but will pass the signal through with the jitter received at its input; no data will be lost or repeated. When set to a 1, the dejitter buffer will recenter on an overflow or underflow; data may be lost or repeated.
	1	RECENTER	**Recenter the Dejitter Buffer:** When set to a 1, the dejitter buffer will be recentered. This bit is to be written to a 0 before another recenter command can be given.
	0	BYPASS	**Bypass the Dejitter Buffer:** When set to a 0, the dejitter buffer for this framer will be bypassed.

Receive and Transmit Facility Data Link Control Registers

These registers control the operation of the 4 to 20 kbit/s HDLC channel that uses the National bits. Registers X+124H, X+125H and X+128H are read-only, while register X+127H is write-only. For registers X+124H, X+125H, X+127H and X+128H, a write operation may not be followed by a read operation unless at least 7 cycles of SYSCI occur following the end of the last write cycle.

Address (Hex)	Bit	Symbol	Description
X+122	7-6		**Reserved:** Write these bits to 0.
	5	BNAL	**Bypass National Bits:** Enabled in the Transmission Mode. When set to 1, the national bits from the signaling highway (TSIGLn) in Transmission Mode only or microprocessor-written bits are used in place of the HDLC data link in the transmit direction.
	4-0		**Reserved:** Write these bits to 0.
X+123	7	EHR	**Enable HDLC Receive Controller:** A 1 enables the HDLC receive controller. After flag detection and zero bit destuffing the receive bytes are written into a receive FIFO for microprocessor access. A 0 disables the HDLC controller, and disables the HDLC receive interrupts.
	6	RHIE	**Receive Half Full Interrupt Enable:** A 1 enables the receive HDLC controller to generate an interrupt when the receive HDLC FIFO is half full or has detected an end of message. When set to 0, the HDLC controller generates an interrupt only at the end of the message, or when a FIFO overflow has occurred.
	5-0		**Reserved:** Write these bits to 0.
X+124	7-0	RHD7-RHD0	**HDLC Receive Data:** A read cycle to this location transfers one byte from the receive HDLC FIFO into this location. Bit 0 corresponds to the first bit received in the HDLC message. The receive FIFO must be cleared by reading this location the number of times indicated by the HDLC FIFO Depth Register (register X+125H) or until the HDLC FIFO Depth Register becomes 0.
X+125	7-0	DPT7-DPT0	**HDLC FIFO Depth:** This register indicates the number of data bytes present in the receive HDLC FIFO. The value is in binary. For example, the value 0000 0000 indicates that the FIFO is empty, while a value 0111 1111 indicates that 127 bytes are present. This value is not reset when a new frame is received. The previous frame length is stored in MSL6-MSL0 (bits 6-0 in register X+128H) which is updated every time a new complete frame (good or errored) is received. This register value is decreased by microprocessor reads of RHD7-RHD0 (register X+124H) only. At initialization this location should read 00H; If it does not, repeated reads of RHD7-RHD0 should be performed until it reads 00H.

Address (Hex)	Bit	Symbol	Description
X+126	7	EHT	**Enable HDLC Transmit Controller:** A 1 enables the HDLC transmit controller. The transmitter will send Flags when the transmit HDLC FIFO is empty. The bytes are formatted into a message when the FIFO has bytes present, which is done by loading THD7- THD0 (register X+127H) repeatedly with the byte content of the message to be sent. At the end of the message, a CRC is calculated and transmitted. A 0 disables the HDLC controller, clears the transmit FIFO, and disables the HDLC transmit interrupts.
	6	TAB	**Transmit Abort:** A 1 causes the HDLC transmit controller to generate and transmit an abort sequence, after the next data byte. This will be followed by clearing the FIFO and transmitting continuous flags.
	5	EOM	**Transmit End Of Message:** A 1 instructs the HDLC controller that the transmit HDLC FIFO contains the last byte in the message. When the FIFO has emptied, the CRC is calculated and transmitted. When this bit is set to a 0, if the Transmit FIFO has emptied, an abort character will be transmitted.
	4		**Reserved:** Write this bit to 0.
	3	THIE	**Transmit Half Full Interrupt Enable:** This bit controls the THIS status bit logic to allow interrupts to occur at the FIFO half empty or message complete only. A 1 enables the transmit HDLC controller to generate an interrupt when the transmit HDLC FIFO is half full or has detected an end of message. When set to 0, the HDLC controller generates an interrupt only at the end of the message, or when a FIFO underflowed has occurred.
	2-0		**Reserved:** Write these bits to 0.
X+127	7-0	THD7-THD0	**HDLC Transmit Data:** The byte written into this location will be written into the transmit FIFO. Bit 0 corresponds to the first bit transmitted in an HDLC message byte.
X+128	7		**Reserved:** Indeterminate value.
	6-0	MSL6-MSL0	**Message Length:** This register is loaded with the number of bytes in the last received frame if an end of message, abort, or message received with bad CRC event occurs. The microprocessor must read this value before the end of another complete frame is received.
X+0C	7-5		**Reserved:** Write these bits to 0.
	4-0	SA4-SA8	**Enable Sa Bits:** Any or all of these bits can be set high to map the HDLC channel into the combined bandwidth of the National reserved bit positions (Sa4-Sa8) of Time Slot 0.

Receive and Transmit Facility Data Link Status Registers

These registers are all read/write, except X+0EH, which is read-only. The status bits in the X+0DH registers represent the latched status and interrupt request indications generated by the receive and transmit HDLC link controllers and the FIFOs. The latched event bits are a result of a receive or transmit status indication or interrupt request in the HDLC Link Status register X+0EH. The bits latch on either the positive transitions, the negative transitions, or both positive and negative transitions of the current status or interrupt request event bits as defined by the RISE/FALL control bits (bits 7 and 6) in the Global Configuration Register 00BH. A latched bit causes a hardware interrupt indication when the corresponding mask bit in the HDLC Link Mask Register X+0FH is written with a 0 if the global mask bit GIM is also set to 0. The status bits in register X+0EH represent the current (unlatched) status and interrupt request indications generated by the receive and transmit HDLC link controllers and FIFOs.

Address (Hex)	Bit	Symbol	Description
X+0D	7-5	LRHIS2-LRHIS0	**Receive HDLC Interrupt Latched Status:** The latched bits in this location set on a receive HDLC interrupt status indication. The RISE/FALL control bits determine the transition on which these bits latch. An interrupt indication occurs when a bit latches, and the corresponding mask bits are disabled. A latched bit is cleared by writing a 0 to it. These latched status bits will change to indicate a corresponding change in RHIS2-RHIS0 (bits 7-5, in register X+0EH) except when RHIS2-RHIS0 changes to all zeros, where these latched status bits will retain the previously latched value.
	4-3	LRXFS1-LRXFS0	**Receive HDLC FIFO Interrupt Latched Status:** The latched bits in this location set on a receive HDLC FIFO status indication. The RISE/FALL control bits determine the transition on which these bits latch. An interrupt indication will occur when a bit latches, and the corresponding mask bits are disabled. A latched bit is cleared by writing a 0 to it. These latched status bits will change to indicate a corresponding change in RXFS1-RXFS0 (bits 4-3, in register X+0EH) except in the case when RXFS1-RXFS0 changes to all zeros, where these latched status bits will retain the previously latched value.
	2-1	LTXFS1-LTXFS0	**Transmit HDLC FIFO Interrupt Latched Status:** The latched bits in this location set on a transmit HDLC FIFO status indication. The RISE/FALL control bits determine the transition on which these bits latch. An interrupt indication will occur when a bit latches, and the corresponding mask bits are disabled. A latched bit is cleared by writing a 0 to it. These latched status bits will change to indicate a corresponding change in TXFS1-TXFS0 (bits 2-1, in register X+0EH) except in the case when TXFS1-TXFS0 changes to all zeros, where these latched status bits will retain the previously latched value.
	0	LTHIS	**Transmit HDLC Interrupt Latched Status:** The latched bit in this location set on an transmit HDLC Interrupt status indication. The RISE/FALL control bits determine the transition on which these bits latch. An interrupt indication will occur when a bit latches, and the corresponding mask bit is a disabled. A latched bit is cleared by writing a 0 to it.

<table>
<tr><th>Address (Hex)</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td>X+0E</td><td>7-5</td><td>RHIS2-RHIS0</td><td>Receive HDLC Interrupt Status: The following table lists the various interrupt status indications associated with the HDLC message. These bits are controlled by control bit RHIE (bit 6) in register X+123H.
<table>
<tr><th>RHIS2</th><th>RHIS1</th><th>RHIS0</th><th>RHIE</th><th>Condition Present</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>X</td><td>Idle condition</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>X</td><td>Start of message indication</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>Valid message received; (CRC checked OK, message is ≤128 bytes), or the receive FIFO needs servicing (full or overflow).</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>Valid message received; (CRC checked OK, message is ≤128 bytes), or the receive FIFO needs servicing (half full or more).</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>X</td><td>Message received with CRC error</td></tr>
<tr><td>1</td><td>X</td><td>X</td><td>X</td><td>Abort message received</td></tr>
</table>
Note: X=don’t care.</td></tr>
<tr><td></td><td>4-3</td><td>RXFS1-RXFS0</td><td>Receive HDLC FIFO Interrupt Status: The following table lists the various FIFO status indications associated with the received HDLC FIFO.
<table>
<tr><th>RXFS1</th><th>RXFS0</th><th>Condition Present</th></tr>
<tr><td>0</td><td>0</td><td>Normal. HDLC FIFO less than half full.</td></tr>
<tr><td>0</td><td>1</td><td>FIFO equal to or more than half full</td></tr>
<tr><td>1</td><td>0</td><td>FIFO full</td></tr>
<tr><td>1</td><td>1</td><td>FIFO Overflow</td></tr>
</table></td></tr>
<tr><td></td><td>2-1</td><td>TXFS1-TXFS0</td><td>Transmit HDLC FIFO Interrupt Status: The following table lists the various FIFO status indications associated with the transmit HDLC FIFO.
<table>
<tr><th>TXFS1</th><th>TXFS0</th><th>Condition Present</th></tr>
<tr><td>0</td><td>0</td><td>Normal. HDLC FIFO equal to or more than half full</td></tr>
<tr><td>0</td><td>1</td><td>FIFO less than half full</td></tr>
<tr><td>1</td><td>0</td><td>FIFO overflow (attempt to write to a full FIFO)</td></tr>
<tr><td>1</td><td>1</td><td>FIFO Underflow</td></tr>
</table></td></tr>
<tr><td></td><td>0</td><td>THIS</td><td>Transmit HDLC Interrupt Status: A 1 indicates that the transmit HDLC FIFO needs servicing, either because the message is completed, or because the FIFO is half full. Control bit THIE (bit 3) in register X+126H determines if an interrupt is generated at the half full point.</td></tr>
</table>

Address (Hex)	Bit	Symbol	Description
X+0F	7-5	MRHIS2-MRHIS0	**Receive HDLC Interrupt Mask:** When one or more bits are set to a 1, the corresponding bits in the receive HDLC interrupt latched status bits LRHIS2-LRHI0 are masked (disabled) from causing an interrupt to occur.
	4-3	MRXFS1-MRXFS0	**Receive HDLC FIFO Interrupt Mask:** When one or more bits are set to a 1, the corresponding bits in the receive HDLC FIFO interrupt latched status bits LRXFS1-LRXFS0 are masked (disabled) from causing an interrupt to occur.
	2-1	MTXFS1-MTXFS0	**Transmit HDLC FIFO Interrupt Mask:** When one or more bits are set to a 1, the corresponding bits in the transmit HDLC FIFO interrupt latched status bits LTXFS1-LTXFS0 are masked (disabled) from causing an interrupt to occur.
	0	MTHIS	**Transmit Interrupt Mask:** When this bit is set to a 1, the corresponding bit in the transmit interrupt latched status bit LTHIS is masked (disabled) from causing an interrupt to occur.
X+160	7-0		**Reserved:** Write these bits to 0.

Receive and Transmit Slip Buffer Control Registers

These are read/write registers.

<table>
<tr><th>Address (Hex)</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td>X+11B</td><td>7</td><td>RXCKE</td><td>Receive Slip Buffer Clock Select: Works in conjunction with the RXSBE control bit in this register according to the following table. Please note that the slip buffer must be enabled for the MVIP and H-MVIP interfaces.
<table>
<tr><th>RXCKE</th><th>RXSBE</th><th>Action</th></tr>
<tr><td>0</td><td>0</td><td>Invalid combination.</td></tr>
<tr><td>0</td><td>1</td><td>Slip Buffer enabled. RTCLKn and RTFRMn leads are inputs.</td></tr>
<tr><td>1</td><td>0</td><td>Slip Buffer disabled. RTCLKn and RTFRMn leads are outputs.</td></tr>
<tr><td>1</td><td>1</td><td>Slip Buffer enabled. RTCLKn and RTFRMn leads are outputs.</td></tr>
</table></td></tr>
<tr><td></td><td>6</td><td></td><td>Reserved: Write this bit to 0.</td></tr>
<tr><td></td><td>5</td><td>RXSBE</td><td>Receive Slip Buffer Enable: Works in conjunction with the RXCKE control bit as described in the table above.</td></tr>
<tr><td></td><td>4</td><td>RSR</td><td>Receive Slip Buffer Recenter: Toggling RSR from a 0 to a 1 causes the receive slip buffer to recenter. This may cause either an increase or a decrease in delay. The delay value may be read in register bits RXSBD8-RXSBD0 in registers X+23H and X+24H. When set to 0, the receive slip buffer will recenter automatically as needed to prevent overrun or underrun.</td></tr>
<tr><td></td><td>3-0</td><td></td><td>Reserved: Write these bits to 0.</td></tr>
</table>

Address (Hex)	Bit	Symbol	Description
X+11C	7-6	TXC1-TXC0	**Transmit Clock Source:** The transmit clock source is selected according to the following table. TXC1 / TXC0 / Action 0 / 0 / Back plane Oscillator (BPOSC) 0 / 1 / System clock (TTCLKn) 1 / 0 / Receive Line Clock (RCLKn) 1 / 1 / Not valid
	5	TXSBE	**Transmit Slip Buffer Enable:** A 1 written to this bit position enables the transmit slip buffer, while a 0 causes the slip buffer to be bypassed.
	4	TSR	**Transmit Slip Buffer Recenter:** Toggling TSR from a 0 to a 1 causes the receive slip buffer to recenter. This may cause either an increase or a decrease in delay. The delay value may be read in register bits TXSBD8-TXSBD0 in registers X+25H and X+29H. When set to 0, the transmit slip buffer will recenter automatically as needed to prevent overrun or underrun.
	3-0		**Reserved:** Write these bits to 0.

Receive and Transmit Slip Buffer Status Registers

The following unlatched read-only registers provide status information on the slip buffers. When a common slip error indication is present on status bits SLIP and LSLIP (bit 1) in registers X+10H and X+11H, respectively, these registers provide more detail.

Address (Hex)	Bit	Symbol	Description
X+15	7-6	RXS1-RXS0	**Receive Slip Buffer Status:** The following table indicates the direction of a receive slip. RXS1 / RXS0 / Action 0 / 0 / No slips have occurred 0 / 1 / Slip buffer overflow. One frame dropped 1 / 0 / Slip buffer underflow. One frame repeated 1 / 1 / Slip buffer error. Two slips in a row
	5	RTSLPP	**Remote Time Slot Loopback Phase:** This is the phase indication that is used for Remote Time Slot Loopbacks. A change indicates a slip of only the time slot(s) being remotely looped back has occurred, to prevent a clash between the Receive Slip Buffer write and the Transmit Slip Buffer read.
	4-0		**Reserved:** Indeterminate value.

<table>
<tr><th>Address (Hex)</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td rowspan="3">X+16</td><td>7-6</td><td>TXS1-TXS0</td><td>Transmit Slip Buffer Status: The following table indicates the direction of a transmit slip.

<table>
<tr><th>TXS1</th><th>TXS0</th><th>Action</th></tr>
<tr><td>0</td><td>0</td><td>No slips have occurred</td></tr>
<tr><td>0</td><td>1</td><td>Slip buffer overflow. One frame dropped</td></tr>
<tr><td>1</td><td>0</td><td>Slip buffer underflow. One frame repeated</td></tr>
<tr><td>1</td><td>1</td><td>Slip buffer error. Two slips in a row</td></tr>
</table></td></tr>
<tr><td>5</td><td>LTSLPP</td><td>Local Time Slot Loopback Phase: This is the phase indication that is used for Local Time Slot Loopbacks. A change indicates a slip of only the time slot(s) being locally looped back has occurred, to prevent a clash between the Transmit Slip Buffer write and the Receive Slip Buffer read.</td></tr>
<tr><td>4-0</td><td></td><td>Reserved: Indeterminate value.</td></tr>
</table>

Receive and Transmit Slip Buffer Pointer Status Registers

The following register locations provide receive read and write pointer information, and transmit read and write pointer information, from the receive and transmit slip buffers, respectively. Registers X+24H and X+25H are read-only, the rest are read/write but are generally written only by the E1Fx8 channel. These pointers are updated at the line rate and are provided for diagnostic purposes; in developing applications, they can be used in conjunction with the System Freeze control bit SYFZ (bit 4) in register X+05H, which will stop the slip buffers and allow for analysis to be performed. Please note that the 32 register pairs X+20H/X+21H, X+22H/X+23H, X+26H/X+27H and X+28H/X+29H are constructed for 16-bit word read operations. Each pair must always be read in two consecutive read operations, with the even-numbered register being read first, e.g., 220H followed by 221H. Doing so will ensure that the read and write side results correspond to the same time instant. If the odd-numbered register is accessed first, data for the read and write sides may correspond to two different time instants. Write operations have no such restriction.

The slip buffer delay registers (X+23H (bit 6), X+24H, X+25H and X+29H (bit 6)), however, are updated once per frame and tend to change very slowly. They are meant to provide wander information between the write and read clocks and can be used in a microprocessor-based DPLL algorithm.

Address (Hex)	Bit	Symbol	Description
X+20	7-0	RWP7-RWP0	**Receive Slip Buffer Write Pointer:** The value in this register is the current value of the receive slip buffer write pointer. The value will be between 0 and 255.
X+21	7-0	RRP7-RRP0	**Receive Slip Buffer Read Pointer:** The value in this register is the current value of the receive slip buffer read pointer. The value will be between 0 and 255.

Address (Hex)	Bit	Symbol	Description
X+22	7	RWSBS	**Receive Slip Buffer Write Side:** A 1 indicates that the upper side of the receive slip buffer is currently being written. A 0 indicates the lower side is being written.
	6-4		**Reserved:** Indeterminate value.
	3-0	RWPF3-RWPF0	**Receive Slip Buffer Write Pointer Frame:** The bits in this location indicate for which frame of the multiframe the receive slip buffer write pointer is being written. Bit 0 is the LSB. The value will be between 0 and 15.
X+23	7	RRSBS	**Receive Slip Buffer Read Side:** A 1 indicates that the upper side of the receive slip buffer is currently being read. A 0 indicates the lower side is being read.
	6	RXSBD8	**Receive Slip Buffer Delay (Bit 8):** The value in this bit indicates the MSB of current delay through the receive slip buffer. RXSBD7-RXSBD0 are the lower bits (7-0) of the current delay.
	5-4		**Reserved:** Write these bits to 0.
	3-0	RRPF3-RRPF0	**Receive Slip Buffer Read Pointer Frame:** The bits in this location indicate for which frame of the multiframe the receive slip buffer read pointer is being read. Bit 0 is the LSB. The value will be between 0 and 15.
X+24	7-0	RXSBD7-RXSBD0	**Receive Slip Buffer Delay (Bits 7-0):** The value in this register indicates the current bits of delay through the receive slip buffer in increments of 1 bits. RXSBD0 is the LSB.
X+25	7-0	TXSBD7-TXSBD0	**Transmit Slip Buffer Delay (Bits 7-0):** The value in this register indicates the current bits of delay through the transmit slip buffer in increments of 1 bits. TXSBD0 is the LSB.
X+26	7-0	TWP7-TWP0	**Transmit Slip Buffer Write Pointer:** The value in this register is the current value of the transmit slip buffer write pointer. The value will be between 0 and 255.
X+27	7-0	TRP7-TRP0	**Transmit Slip Buffer Read Pointer:** The value in this register is the current value of the transmit slip buffer read pointer. The value will be between 0 and 255.
X+28	7	TWSBS	**Transmit Slip Buffer Write Side:** A 1 indicates that the upper side of the transmit slip buffer is currently being written. A 0 indicates the lower side is being written.
	6-4		**Reserved:** Indeterminate value.
	3-0	TWPF3-TWPF0	**Transmit Slip Buffer Write Pointer Frame:** The bits in this location indicate for which frame of the multiframe the transmit slip buffer write pointer is being written. Bit 0 is the LSB. The value will be between 0 and 15.

Address (Hex)	Bit	Symbol	Description
X+29	7	TRSBS	**Transmit Slip Buffer Read Side:** A 1 indicates that the upper side of the transmit slip buffer is currently being read. A 0 indicates the lower side is being read.
	6	TXSBD8	**Transmit Slip Buffer Delay (Bit 8):** The value in this bit indicates the MSB of current delay through the transmit slip buffer. TXSBD7-TXSBD0 are the lower bits (7-0) of the current delay.
	5-4		**Reserved:** Write these bits to 0.
	3-0	TRPF3-TRPF0	**Transmit Slip Buffer Read Pointer Frame:** The bits in this location indicate for which frame of the multiframe the transmit slip buffer read pointer is being read. Bit 0 is the LSB. The value will be between 0 and 15.

Receive Slip Buffer Control Registers

The control bits in the following read/write registers are used to enable or disable (freeze) the receive slip buffer locations for the system highway, and to allow the microprocessor to write in service codes and idle codes. These registers control the receive slip buffer write actions from the receive line port. Control bits RDEc, when written to 0, can freeze the individual time slots in the slip buffer for analysis or for microprocessor writing to force specific time slot codes to be output on the system side data highway (where c = 1 - 31).

Address (Hex)	Bit	Symbol	Description
X+3A	7-3		**Reserved:** Write these bits to 0.
	2-0	RX2S-RX0S	**Receive Time Slot 16 Spare Bits Select:** Bits RX2S-RX0S correspond to the spare bits X2-X0 in bit positions 8, 7 and 5 in Time Slot 16 of frame 0 in the Time Slot 16 multiframe. When a bit is set to 1, the corresponding spare bit received in Time Slot 16 is sent to the receive signaling highway via a buffer (when operating in Transmission Mode). When set to 0, the receive spare bit in the multiframe is disabled from being written into the buffer, and the value sitting in the buffer is frozen. The value of the bit in the buffer may be rewritten by the microprocessor for sending to the receive signaling highway.
X+3B	7	RSIS	**Receive International Bits (Si) Select:** When set to 1, the two international bits received from the line (in bit 1 of Time Slot 0 in alternating FAS and NFAS frames) are sent to the receive signaling highway (when operating in Transmission Mode), and to the data highway, via a buffer. When set to 0, the received international bits are disabled from being written into the buffer, and the value sitting in the buffer is frozen. The value of these bits in the buffer may be rewritten by the microprocessor.
	6-5		**Reserved:** Write these bits to 0.
	4-0	RSA4S-RSA8S	**Receive National Bits Select:** When set to 1, The National bits received from the E1 line are sent to the receive signaling highway (when operating in a Transmission Mode), via a buffer. When set to 0, the National bits are sent to the signaling highway from the last value in the receive buffer; this value is writable by the microprocessor.

Address (Hex)	Bit	Symbol	Description
X+3C	7-1	RDE7-RDE1	**Receive Time Slot Enable for Time Slots 7-1:** When a bit in this register is set to 1, the corresponding received time slot is written into the receive slip buffer. The time slot is then read from the receive slip buffer for the receive data highway. When a bit in this register is written with a 0, the corresponding time slot will not be written into the receive slip buffer. Instead, the microprocessor may write the value of the time slot into the receive slip buffer and this value will be read from the receive slip buffer for the receive data highway. Bit 7 is assigned to receive Time Slot 7. The receive slip buffers are located in registers X+47H-X+41H (frame 1) and X+67H-X+61H (frame 2).
	0		**Reserved:** Write this bit to 0.
X+3D	7-0	RDE15-RDE8	**Receive Time Slot Enable for Time Slots 15-8:** When a bit in this register is set to 1, the corresponding received time slot is written into the receive slip buffer. The time slot is then read from the receive slip buffer for the receive data highway. When a bit in this register is written with a 0, the corresponding time slot will not be written into the receive slip buffer. Instead, the microprocessor may write the value of the time slot into the receive slip buffer and this value will be read from the receive slip buffer for the receive data highway. Bit 7 is assigned to receive Time Slot 15. The receive slip buffers are located in registers X+4FH-X+48H (frame 1) and X+6FH-X+68H (frame 2).
X+3E	7-0	RDE23-RDE16	**Receive Time Slot Enable for Time Slots 23-16:** When a bit in this register is set to 1, the corresponding received time slot is written into the receive slip buffer. The time slot is then read from the receive slip buffer for the receive data highway. When a bit in this register is written with a 0, the corresponding time slot will not be written into the receive slip buffer. Instead, the microprocessor may write the value of the time slot into the receive slip buffer and this value will be read from the receive slip buffer for the receive data highway. Bit 7 is assigned to receive Time Slot 23. The receive slip buffers are located in registers X+57H-X+50H (frame 1) and X+77H-X+70H (frame 2).
X+3F	7-0	RDE31-RDE24	**Receive Time Slot Enable for Time Slots 31-24:** When a bit in this register is set to 1, the corresponding received time slot is written into the receive slip buffer. The time slot is then read from the receive slip buffer for the receive data highway. When a bit in this register is written with a 0, the corresponding time slot will not be written into the receive slip buffer. Instead, the microprocessor may write the value of the time slot into the receive slip buffer and this value will be read from the receive slip buffer for the receive data highway. Bit 7 is assigned to receive Time Slot 31. The receive slip buffers are located in registers X+5FH-X+58H (frame 1) and X+7FH-X+78H (frame 2).

Receive Slip Buffer Frame Storage Registers

The bits in these read/write registers are the received time slots that are present in the receive slip buffer including Time Slot 0.

Address (Hex)	Bit	Symbol	Description
X+40	7-0	RFAS	**Receive Time Slot 0 FAS Buffer:** The time slot bits for Time Slot 0 in frames carrying the frame alignment pattern (FAS, frame 1) are written into this location from the line when control bit TS0FZ (bit 5) in register X+134H is set to a 0 and is not slip buffered. When TS0FZ is set to a 1, Time Slot 0 may or may not contain a FAS pattern and this location is slip buffered. If RTFM is set to a 0, it will contain either FAS or NFAS, if RTFM is set to a 1 this location may contain any data. When control bit RSIS (bit 7) in register X+3BH, is written with a 0, the state of the international bit from the line cannot be written into the buffer, and the buffer value is frozen. The microprocessor can now write the value of the international bit for receive Time Slot 0 to the system. The other bits represent the frame alignment sequence in Time Slot 0.
X+41-X+5F	7-0	RTS1-RTS31 for Frame 1	**Receive Slip Buffer Time Slots 1-31 Storage Locations - Frame 1:** Register locations X+41H-X+5FH represent frame 1 in the two-frame slip buffer for the data highway. The register locations for a time slot are enabled when the corresponding receive time slot enable bits (RDE1-RDE31) are written with a 1. When one or more control bits in RDE1-RDE31 are written with a 0, the corresponding receive time slot is disabled from being written into the buffer location, and the corresponding values in the two buffer locations are frozen. The microprocessor can now write an idle or service code to the corresponding buffer location. Please note that both frame locations in the slip buffer must be written for a time slot (see X+61H to X+7FH below).
X+60	7-0	RNFAS	**Receive Time Slot 0 NFAS Buffer:** The Time Slot 0 bits for frames not carrying the frame alignment pattern (NFAS, frame 2) are written into this location from the line when control bit TS0FZ (bit 5) in register X+134H is set to a 0 and is not slip buffered. When TS0FZ is set to a 1, Time Slot 0 may or may not contain a NFAS pattern and this location is slip buffered. If RTFM is set to a 0, it will contain either FAS or NFAS, if RTFM is set to a 1 this location may contain any data. When control bit RSIS (bit 7) and RSA4S-RSA8S (bits 4-0) in register X+3BH are set to 0, the states of the corresponding international bit and national bits from the line cannot be written into the buffer, and the corresponding buffer value is frozen. The microprocessor can now write the value of the corresponding international bit and national bits for receive Time Slot 0 to the system.
X+61-X+7F	7-0	RTS1-RTS31 for Frame 2	**Receive Slip Buffer Time Slots 1-31 Storage Locations - Frame 2:** Register locations X+61H-X+7FH represent frame 2 in the two-frame slip buffer for the data highway. The register locations for a time slot are enabled when the corresponding receive time slot enable bits (RDE1-RDE31) are written with a 1. When one or more control bits in RDE1-RDE31 are written with a 0, the corresponding receive time slot is disabled from being written into the buffer location, and the corresponding values in the two buffer locations are frozen. The microprocessor can now write an idle or service code to the corresponding buffer location. Please note that both frame locations in the slip buffer must be written for a time slot (see X+41H-X+5FH above).

Transmit Slip Buffer Control Registers

The control bits in the following read/write registers are used to enable or disable (freeze) the transmit slip buffer locations for the transmit line, and to allow the microprocessor to write in service codes and idle codes. These registers control the transmit slip buffer write actions from the system side transmit port. Control bits TDEc, when written to 0, can freeze the individual time slots in the slip buffer for analysis or for microprocessor writing to force specific time slot codes to be output on the transmit line (where c = 1 - 31).

Address (Hex)	Bit	Symbol	Description
X+E2	7-3		**Reserved:** Write these bits to 0.
	2-0	TX2S-TX0S	**Transmit Time Slot 16 Spare Bits Select:** Bits TX2S-TX0S correspond to the spare bits X2-X0 in bit positions 8, 7 and 5 in Time Slot 16 of frame 0 in the Time Slot 16 multiframe. When a bit is set to 1, the corresponding spare bit in Time Slot 16 from the transmit signaling highway is transmitted via a buffer. When set to 0, the transmit spare bit is disabled from being written into the buffer, and the value sitting in the buffer will frozen. The value of the bit in the buffer may be rewritten by the microprocessor for sending to the line.
X+E3	7	TSIS	**Transmit International Bits (Si) Select:** This bit is enabled when the CRC framing mode bits CRCMD1 and CRCMD0 (bits 3 and 2) in register X+07H are equal to 01. When set to 1, the two international bits for frames 1 and 2 in Time Slot 0 from the signaling highway are sent as the transmit bits via a buffer. When set to 0, the transmit international bits are disabled from being written into the buffer, and the value sitting in the buffer is frozen. The value of these bits in the buffer may be rewritten by the microprocessor for sending to the line. The buffer locations are registers X+90H (FAS, frame 1) and X+B0H (NFAS, frame 2).
	6-5		**Reserved:** Write these bits to 0.
	4-0	TSA4S-TSA8S	**Transmit National Bits (Sa4-Sa8) Select:** Bit 4 corresponds to the transmit Sa4 bit in Time Slot 0 of NFAS frames. When a bit is set to 1, the corresponding transmit national bit of frame 2 received in Time Slot 0 on the transmit signaling highway (when in Transmission Mode) is transmitted via a buffer when control bit BNAL (bit 5) in register X+122H is a 1. When a bit is set to 0, the corresponding transmit national bit from the signaling highway is written into the buffer, but is disabled from being written into the line and the value sitting in the buffer is frozen. The value of the national bit is taken from the Transmit Sa4 - Sa8 Code Registers for sending to the line.
X+E4	7-1	TDE7-TDE1	**Transmit Time Slot Enable for Time Slots 7-1:** When a bit in this register is set to 1, the corresponding transmit time slot from the transmit data highway is written into the transmit slip buffer. The time slot is then read from the transmit slip buffer for the transmit line. When a bit in this register is written with a 0, the corresponding time slot from the transmit data highway will not be written into the transmit slip buffer. Instead, the microprocessor writes the value of the time slot into the transmit slip buffer and this value will be read from the transmit slip buffer for the transmit line. Bit 7 is assigned to transmit Time Slot 7. The transmit slip buffers are located in registers X+97H - X+91H (Frame 1) and X+B7H -X+B1H (Frame 2).
	0		**Reserved:** Write this bit to 0.

Address (Hex)	Bit	Symbol	Description
X+E5	7-0	TDE15-TDE8	**Transmit Time Slot Enable for Time Slots 15-8:** When a bit in this register is set to 1, the corresponding transmit time slot from the transmit data highway is written into the transmit slip buffer. The time slot is then read from the transmit slip buffer for the transmit line. When a bit in this register is written with a 0, the corresponding time slot from the transmit data highway will not be written into the transmit slip buffer. Instead, the microprocessor writes the value of the time slot into the transmit slip buffer and this value will be read from the transmit slip buffer for the transmit line. Bit 7 is assigned to transmit Time Slot 15. The transmit slip buffers are located in registers X+9FH - X+98H (Frame 1) and X+BFH -X+B8H (Frame 2).
X+E6	7-0	TDE23-TDE16	**Transmit Time Slot Enable for Time Slots 23-16:** When a bit in this register is set to 1, the corresponding transmit time slot from the transmit data highway is written into the transmit slip buffer. The time slot is then read from the transmit slip buffer for the transmit line. When a bit in this register is written with a 0, the corresponding time slot from the transmit data highway will not be written into the transmit slip buffer. Instead, the microprocessor writes the value of the time slot into the transmit slip buffer and this value will be read from the transmit slip buffer for the transmit line. Bit 7 is assigned to transmit Time Slot 23. The transmit slip buffers are located in registers X+A7H - X+A0H (Frame 1) and X+C7H -X+C0H (Frame 2).
X+E7	7-0	TDE31-TDE24	**Transmit Time Slot Enable for Time Slots 31-24:** When a bit in this register is set to 1, the corresponding transmit time slot from the transmit data highway is written into the transmit slip buffer. The time slot is then read from the transmit slip buffer for the transmit line. When a bit in this register is written with a 0, the corresponding time slot from the transmit data highway will not be written into the transmit slip buffer. Instead, the microprocessor writes the value of the time slot into the transmit slip buffer and this value will be read from the transmit slip buffer for the transmit line. Bit 7 is assigned to transmit Time Slot 31. The transmit slip buffers are located in registers X+AFH - X+A8H (Frame 1) and X+CFH -X+C8H (Frame 2).

Transmit Slip Buffer Frame Storage Registers

The bits in these read/write registers are the time slots to be transmitted and come from the transmit slip buffer.

Address (Hex)	Bit	Symbol	Description
X+90	7-0	TFAS	**Transmit Time Slot 0 FAS Buffer:** The time slot bits for Time Slot 0 in frames carrying the frame alignment pattern (FAS, frame 1) are written into this location from the signaling highway when a Transmission Mode is selected, and from the data highway when the 2 Mbit/s MVIP Mode or 8 Mbit/s H-MVIP Mode is selected. When control bit TSIS (bit 7) in register X+E3H is written with a 0, the state of the international bit from the system interface (signaling highway or data highway) cannot be written into the buffer and the buffer value is frozen. The microprocessor can now write the value of the international bit for transmit Time Slot 0 that will be sent to the line.
X+91-X+AF	7-0	TTS1-TTS31 for Frame 1	**Transmit Slip Buffer Time Slots 1-31 Storage Locations - Frame 1:** Register locations X+91H-X+AFH represent frame 1 in the two-frame slip buffer from the data highway. The register locations for a time slot are enabled when the corresponding transmit time slot enable bits (TDE1-TDE31) are written with a 1. When one or more control bits in TDE1-TDE31 are written with a 0, the corresponding transmit time slot is disabled from being written into the buffer location, and the corresponding values in the two buffer locations are frozen. The microprocessor can now write an idle or service code to the corresponding buffer location. Please note that both frame locations in the slip buffer must be written for a time slot (see X+B1H-X+CFH below).
X+B0	7-0	TNFAS	**Transmit Time Slot 0 NFAS Buffer:** The time slot bits for Time Slot 0 in frames not carrying the frame alignment pattern (NFAS, frame 2) are written into this location from the signaling highway when a Transmission Mode is selected, and from the data highway when the 2 Mbit/s MVIP Mode or 8 Mbit/s H-MVIP Mode is selected. When control bit TSIS and TSA4S-TSA8S are set to 0, the states of the corresponding international bit and national bits from the system interface (signaling highway or data highway) cannot be written into the line from the buffer, although the buffer continues updating. The microprocessor can now write the values of the corresponding international bit for transmit Time Slot 0 into the code registers X+169H through X+16DH that will be sent to the line.
X+B1-X+CF	7-0	TTS1-TTS31 for Frame 2	**Transmit Slip Buffer Time Slots 1-31 Storage Locations - Frame 2:** Register locations X+B1H-X+CFH represent frame 2 in the two-frame slip buffer from the data highway. The register locations for a time slot are enabled when the corresponding transmit time slot enable bits (TDE1-TDE31) are written with a 1. When one or more control bits in TDE1-TDE31 are written with a 0, the corresponding transmit time slot is disabled from being written into the buffer location, and the corresponding values in the two buffer locations are frozen. The microprocessor can now write an idle or service code to the corresponding buffer location. Please note that both locations in the slip buffer must be written for a time slot (see X+91H-X+AFH above).

Receive and Transmit Signaling State Control Registers

The following read/write registers control how signaling is to be handled in the E1Fx8.

Address (Hex)	Bit	Symbol	Description
X+134	7-6	TYP1-TYP0	**Signaling Type Selection:** The following table lists the signaling selection formats in the transmit and receive directions that are controlled by bits TYP1 and TYP0. **TYP1** / **TYP0** / **Signaling Type** 0 / 0 / Time Slot 16 assigned as a clear channel. 0 / 1 / Time Slot 16 assigned for CAS. ABCD bits carried. ABCD = 0000 from the transmit signaling highway (evaluated after TSINV application) or from stored locations in the transmit signaling RAM sent on the E1 line in Time Slot 16 as 1111 to prevent mimics of the Time Slot 16 multiframe alignment pattern. 1 / 0 / Time Slot 16 assigned for CAS. ABCD bits carried. 1 / 1 / Not used The Time Slot 16 multiframe alignment pattern is generated for all options except TYP1, TYP0 is equal to 00. When TYP1, TYP0 is equal to 00, Time Slot 16 is slip buffered as a telephone channel. When TYP1, TYP0 is not equal to 00, Time Slot 16 uses the signaling buffers.
	5	TS0FZ	**Time Slot 0 Slip Buffer Freeze:** When set to a 0 the Receive Slip Buffer Frame Storage Registers at X+40H and X+60H are used to store FAS and NFAS as received from the line. When set to a 1 Time Slot 0 is treated as a telephone channel and slip buffered as time slots 1 through 31.
	4	SIGDB	**Signaling Debounce:** When set to a 1, the signaling bits are debounced. Each signaling nibble must be the same for the number of consecutive multiframes determined by control bits DEBVAL(3-0) (bits 3-0) in register 0FEH before being placed in the signaling buffer or placed on the signaling highway.
	3	SIGIEN	**Signaling Interrupt Enabled:** When set to a 1, the change of state after debouncing (control bit SIGDB set to a 1) of any of the received signaling bits for time slots which have signaling enabled (RSEn = 1) causes an interrupt if not masked. Note control bits TYP0, TYP1 can not equal 00.
	2		**Reserved:** Write this bit to 0.
	1	RXSFZ	**Receive Signaling Freeze:** A 1 causes a freeze of the signaling states in the receive signaling buffer, by disabling writing to the buffer from the line. The contents of the frozen state are sent on the signaling highway repeatedly for the duration of the signaling freeze. The microprocessor is permitted to write the signaling states.
	0	TXSFZ	**Transmit Signaling Freeze:** A 1 causes a freeze of the signaling states in the transmit signaling buffer, by disabling writing to the buffer from the system. The contents of the transmit signaling buffer are repeatedly transmitted for the duration of the signaling freeze. The microprocessor is permitted to write the signaling states for call control, trunk conditioning, etc.

Receive Signaling Control Registers

The bits in these read/write registers control the receive signaling for telephone channels 1 through 30.

Address (Hex)	Bit	Symbol	Description
X+E8	7-0	RSE8-RSE1	**Receive Signaling Enable for Channels 8-1:** When a bit in this register is set to 1, the receive signaling bits for the corresponding telephone channel are enabled. The ABCD signaling bits are written into the receive signaling buffers from the receive line, and are inserted into the receive signaling highway. When set to 0, the signaling states in the receive signaling buffers are frozen. The ability to internally write the signaling bits from the line into the receive signaling buffers is disabled. This enables the microprocessor to write the signaling states into the receive signaling registers. Bit 7 is the enable bit for telephone channel 8 or time slot 8. Signaling information for telephone channel c is carried in Time Slot c.
X+E9	7-0	RSE16-RSE9	**Receive Signaling Enable for Channels 16-9:** When a bit in this register is set to 1, the receive signaling bits for the corresponding telephone channel are enabled. The ABCD signaling bits are written into the receive signaling buffers from the receive line, and are inserted into the receive signaling highway. When set to 0, the signaling states in the receive signaling buffers are frozen. The ability to internally write the signaling bits from the line into the receive signaling buffers is disabled. This enables the microprocessor to write the signaling states into the receive signaling registers. Bit 7 is the enable bit for channel 16. Signaling information for telephone channel c is carried in Time Slot c, except for channel 16, which is carried in Time Slot 17.
X+EA	7-0	RSE24-RSE17	**Receive Signaling Enable for Channels 24-17:** When a bit in this register is set to 1, the receive signaling bits for the corresponding telephone channel are enabled. The ABCD signaling bits are written into the receive signaling buffers from the receive line, and are inserted into the receive signaling highway. When set to 0, the signaling states in the receive signaling buffers are frozen. The ability to internally write the signaling bits from the line into the receive signaling buffers is disabled. This enables the microprocessor to write the signaling states into the receive signaling registers. Bit 7 is the enable bit for channel 24. Signaling information for telephone channel c is carried in Time Slot c+1.
X+EB	7-6		**Reserved:** Write these bits to 0.
	5-0	RSE30-RSE25	**Receive Signaling Enable for Channels 30-25:** When a bit in this register is set to 1, the receive signaling bits for the corresponding telephone channel are enabled. The ABCD signaling bits are written into the receive signaling buffers from the receive line, and are inserted into the receive signaling highway. When set to 0, the signaling states in the receive signaling buffers are frozen. The ability to internally write the signaling bits from the line into the receive signaling buffers is disabled. This enables the microprocessor to write the signaling states into the receive signaling registers. Bit 5 is the enable bit for channel 30. Signaling information for telephone channel c is carried in Time Slot c+1.

Receive Signaling State Debounce Registers (Debounce Buffer)

The contents of these locations are raw received values always for RX0, RY, RX1 and RX2. If SIGDB is set to a 0, signaling bits An - Dn are raw received values. If SIGDB is set to a 1, debounced values for An - Dn are stored in these registers.

Address (Hex)	Bit	Symbol	Description
X+80	7-4	RSIGMAS	**Received Signaling Multiframe Alignment Signal:** The bits in this register contains the states of the received multiframe alignment pattern (Time Slot 16 bits 1-4 in frame 0) in the receive signaling buffer. This pattern is normally 0000. Bit 7 is received bit 1.
	3-0	RX0, RY, RX1, RX2	**Received Signaling Spare Bits and Remote Alarm Bit:** Bits 3, 1 and 0 in this register contains the states of the received X0, X1, X2 bits (spare bits) in Time Slot 16, which correspond to bits 5, 7, and 8 in frame 0 of the Time Slot 16 multiframe. The RY bit (bit 2) is defined as the loss of multiframe indication bit and is carried in bit 6 in frame 0 of the Time Slot 16 multiframe.
X+81	7-4 3-0	RA1-RD1 RA16-RD16	**Receive A1-D1 and A16-D16 Signaling Bits:** The signaling bits in this register are the states of the received A1 to D1 bits and the A16 to D16 bits in the receive signaling buffer. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 1 (Time Slot 1) and 16 (Time Slot 17). Bit 7 is the A1 signaling bit value. Please note that a receive signaling state is written into the receive signaling buffer when the corresponding channel enable bit RSEc is written with a 1 (where c is the channel number, from 1 to 30). When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position in this register represents the last value written into the buffer. The microprocessor can write the state of the outgoing signaling bits to the receive signaling highway for channels 1 and 16 in this register.
X+82	7-4 3-0	RA2-RD2 RA17-RD17	**Receive A2-D2 and A17-D17 Signaling Bits:** The signaling bits in this register are the states of the received A2 to D2 bits and the A17 to D17 bits in the receive signaling buffer. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 2 (Time Slot 2) and 17 (Time Slot 18). Bit 7 is the A2 signaling bit value. Please note that a receive signaling state is written into the receive signaling buffer when the corresponding channel enable bit RSEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position in this register represents the last value written into the buffer. The microprocessor can write the state of the outgoing signaling bits to the receive signaling highway for channels 2 and 17 in this register.

Address (Hex)	Bit	Symbol	Description
X+83	7-4 3-0	RA3-RD3 RA18-RD18	**Receive A3-D3 and A18-D18 Signaling Bits:** The signaling bits in this register are the states of the received A3 to D3 bits and the A18 to D18 bits in the receive signaling buffer. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 3 (Time Slot 3) and 18 (Time Slot 19). Bit 7 is the A3 signaling bit value. Please note that a receive signaling state is written into the receive signaling buffer when the corresponding channel enable bit RSEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position in this register represents the last value written into the buffer. The microprocessor can write the state of the outgoing signaling bits to the receive signaling highway for channels 3 and 18 in this register.
X+84	7-4 3-0	RA4-RD4 RA19-RD19	**Receive A4-D4 and A19-D19 Signaling Bits:** The signaling bits in this register are the states of the received A4 to D4 bits and the A19 to D19 bits in the receive signaling buffer. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 4 (Time Slot 4) and 19 (Time Slot 20). Bit 7 is the A4 signaling bit value. Please note that a receive signaling state is written into the receive signaling buffer when the corresponding channel enable bit RSEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position in this register represents the last value written into the buffer. The microprocessor can write the state of the outgoing signaling bits to the receive signaling highway for channels 4 and 19 in this register.
X+85	7-4 3-0	RA5-RD5 RA20-RD20	**Receive A5-D5 and A20-D20 Signaling Bits:** The signaling bits in this register are the states of the received A5 to D5 bits and the A20 to D20 bits in the receive signaling buffer. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 5 (Time Slot 5) and 20 (Time Slot 21). Bit 7 is the A5 signaling bit value. Please note that a receive signaling state is written into the receive signaling buffer when the corresponding channel enable bit RSEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position in this register represents the last value written into the buffer. The microprocessor can write the state of the outgoing signaling bits to the receive signaling highway for channels 5 and 20 in this register.
X+86	7-4 3-0	RA6-RD6 RA21-RD21	**Receive A6-D6 and A21-D21 Signaling Bits:** The signaling bits in this register are the states of the received A6 to D6 bits and the A21 to D21 bits in the receive signaling buffer. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 6 (Time Slot 6) and 21 (Time Slot 22). Bit 7 is the A6 signaling bit value. Please note that a receive signaling state is written into the receive signaling buffer when the corresponding channel enable bit RSEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position in this register represents the last value written into the buffer. The microprocessor can write the state of the outgoing signaling bits to the receive signaling highway for channels 6 and 21 in this register.

Address (Hex)	Bit	Symbol	Description
X+87	7-4 3-0	RA7-RD7 RA22-RD22	**Receive A7-D7 and A22-D22 Signaling Bits:** The signaling bits in this register are the states of the received A7 to D7 bits and the A22 to D22 bits in the receive signaling buffer. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 7 (Time Slot 7) and 22 (Time Slot 23). Bit 7 is the A7 signaling bit value. Please note that a receive signaling state is written into the receive signaling buffer when the corresponding channel enable bit RSEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position in this register represents the last value written into the buffer. The microprocessor can write the state of the outgoing signaling bits to the receive signaling highway for channels 7 and 22 in this register.
X+88	7-4 3-0	RA8-RD8 RA23-RD23	**Receive A8-D8 and A23-D23 Signaling Bits:** The signaling bits in this register are the states of the received A8 to D8 bits and the A23 to D23 bits in the receive signaling buffer. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 8 (Time Slot 8) and 23 (Time Slot 24). Bit 7 is the A8 signaling bit value. Please note that a receive signaling state is written into the receive signaling buffer when the corresponding channel enable bit RSEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position in this register represents the last value written into the buffer. The microprocessor can write the state of the outgoing signaling bits to the receive signaling highway for channels 8 and 23 in this register.
X+89	7-4 3-0	RA9-RD9 RA24-RD24	**Receive A9-D9 and A24-D24 Signaling Bits:** The signaling bits in this register are the states of the received A9 to D9 bits and the A24 to D24 bits in the receive signaling buffer. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 9 (Time Slot 9) and 24 (Time Slot 25). Bit 7 is the A9 signaling bit value. Please note that a receive signaling state is written into the receive signaling buffer when the corresponding channel enable bit RSEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position in this register represents the last value written into the buffer. The microprocessor can write the state of the outgoing signaling bits to the receive signaling highway for channels 9 and 24 in this register.
X+8A	7-4 3-0	RA10-RD10 RA25-RD25	**Receive A10-D10 and A25-D25 Signaling Bits:** The signaling bits in this register are the states of the received A10 to D10 bits and the A25 to D25 bits in the receive signaling buffer. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 10 (Time Slot 10) and 25 (Time Slot 26). Bit 7 is the A10 signaling bit value. Please note that a receive signaling state is written into the receive signaling buffer when the corresponding channel enable bit RSEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position in this register represents the last value written into the buffer. The microprocessor can write the state of the outgoing signaling bits to the receive signaling highway for channels 10 and 25 in this register.

Address (Hex)	Bit	Symbol	Description
X+8B	7-4 3-0	RA11-RD11 RA26-RD26	**Receive A11-D11 and A26-D26 Signaling Bits:** The signaling bits in this register are the states of the received A11 to D11 bits and the A26 to D26 bits in the receive signaling buffer. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 11 (Time Slot 11) and 26 (Time Slot 27). Bit 7 is the A11 signaling bit value. Please note that a receive signaling state is written into the receive signaling buffer when the corresponding channel enable bit RSEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position in this register represents the last value written into the buffer. The microprocessor can write the state of the outgoing signaling bits to the receive signaling highway for channels 11 and 26 in this register.
X+8C	7-4 3-0	RA12-RD12 RA27-RD27	**Receive A12-D12 and A27-D27 Signaling Bits:** The signaling bits in this register are the states of the received A12 to D12 bits and the A27 to D27 bits in the receive signaling buffer. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 12 (Time Slot 12) and 27 (Time Slot 28). Bit 7 is the A12 signaling bit value. Please note that a receive signaling state is written into the receive signaling buffer when the corresponding channel enable bit RSEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position in this register represents the last value written into the buffer. The microprocessor can write the state of the outgoing signaling bits to the receive signaling highway for channels 12 and 27 in this register.
X+8D	7-4 3-0	RA13-RD13 RA28-RD28	**Receive A13-D13 and A28-D28 Signaling Bits:** The signaling bits in this register are the states of the received A13 to D13 bits and the A28 to D28 bits in the receive signaling buffer. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 13 (Time Slot 13) and 28 (Time Slot 29). Bit 7 is the A13 signaling bit value. Please note that a receive signaling state is written into the receive signaling buffer when the corresponding channel enable bit RSEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position in this register represents the last value written into the buffer. The microprocessor can write the state of the outgoing signaling bits to the receive signaling highway for channels 13 and 28 in this register.
X+8E	7-4 3-0	RA14-RD14 RA29-RD29	**Receive A14-D14 and A29-D29 Signaling Bits:** The signaling bits in this register are the states of the received A14 to D14 bits and the A29 to D29 bits in the receive signaling buffer. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 14 (Time Slot 14) and 29 (Time Slot 30). Bit 7 is the A14 signaling bit value. Please note that a receive signaling state is written into the receive signaling buffer when the corresponding channel enable bit RSEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position in this register represents the last value written into the buffer. The microprocessor can write the state of the outgoing signaling bits to the receive signaling highway for channels 14 and 29 in this register.

Address (Hex)	Bit	Symbol	Description
X+8F	7-4 3-0	RA15-RD15 RA30-RD30	**Receive A15-D15 and A30-D30 Signaling Bits:** The signaling bits in this register are the states of the received A15 to D15 bits and the A30 to D30 bits in the receive signaling buffer. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 15 (Time Slot 15) and 30 (Time Slot 31). Bit 7 is the A15 signaling bit value. Please note that a receive signaling state is written into the receive signaling buffer when the corresponding channel enable bit RSEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position in this register represents the last value written into the buffer. The microprocessor can write the state of the outgoing signaling bits to the receive signaling highway for channels 15 and 30 in this register.

Receive Signaling State Registers (Active Buffer 1)

This is one of two active buffers used for signaling debounce. The contents are valid if control bit SIGDB is set to a 1. This buffer contains the most recent signaling nibble received from the E1 line.

Address (Hex)	Bit	Symbol	Description
X+137	7-4	RRSIGMAS	**Received Signaling Multiframe Alignment Signal:** The bits in this register contain the temporary states of the received multiframe alignment pattern (Time Slot 16 (bits 1-4) in frame 0) in the receive signaling buffer. This pattern is normally 0000. Bit 7 is received bit 1.
	3-0	RRX0, RRY, RRX1, RRX2	**Received Signaling Spare Bits and Remote Alarm Bit:** Bits 3, 1 and 0 in this register contain the temporary states of the received X0, X1, X2 bits (spare bits) in Time Slot 16, which correspond to bits 5, 7, and 8 in frame 0 of the Time Slot 16 multiframe. The RRY bit (bit 2) is defined as the loss of multiframe indication bit and is carried in bit 6 in frame 0 of the Time Slot 16 multiframe.
X+138	7-4 3-0	RRA1-RRD1 RRA16-RRD16	**Receive A1-D1 and A16-D16 Signaling Bits:** The signaling bits in this register are the states of the received A1 to D1 bits and the A16 to D16 bits in the receive signaling buffer. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 1 (Time Slot 1) and 16 (Time Slot 17). Bit 7 is the A1 signaling bit value. Please note that a receive signaling state is written into the receive signaling buffer when the corresponding channel enable bit RSEc is written with a 1 (where c is the channel number, from 1 to 30). When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position in this register represents the last value written into the buffer. The microprocessor can write the state of the outgoing signaling bits to the receive signaling highway for channels 1 and 16 in this register.

Address (Hex)	Bit	Symbol	Description
X+139	7-4 3-0	RRA2-RRD2 RRA17-RRD17	**Receive A2-D2 and A17-D17 Signaling Bits:** The signaling bits in this register are the states of the received A2 to D2 bits and the A17 to D17 bits in the receive signaling buffer. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 2 (Time Slot 2) and 17 (Time Slot 18). Bit 7 is the A2 signaling bit value. Please note that a receive signaling state is written into the receive signaling buffer when the corresponding channel enable bit RSEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position in this register represents the last value written into the buffer. The microprocessor can write the state of the outgoing signaling bits to the receive signaling highway for channels 2 and 17 in this register.
X+13A	7-4 3-0	RRA3-RRD3 RRA18-RRD18	**Receive A3-D3 and A18-D18 Signaling Bits:** The signaling bits in this register are the states of the received A3 to D3 bits and the A18 to D18 bits in the receive signaling buffer. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 3 (Time Slot 3) and 18 (Time Slot 19). Bit 7 is the A3 signaling bit value. Please note that a receive signaling state is written into the receive signaling buffer when the corresponding channel enable bit RSEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position in this register represents the last value written into the buffer. The microprocessor can write the state of the outgoing signaling bits to the receive signaling highway for channels 3 and 18 in this register.
X+13B	7-4 3-0	RRA4-RRD4 RRA19-RRD19	**Receive A4-D4 and A19-D19 Signaling Bits:** The signaling bits in this register are the states of the received A4 to D4 bits and the A19 to D19 bits in the receive signaling buffer. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 4 (Time Slot 4) and 19 (Time Slot 20). Bit 7 is the A4 signaling bit value. Please note that a receive signaling state is written into the receive signaling buffer when the corresponding channel enable bit RSEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position in this register represents the last value written into the buffer. The microprocessor can write the state of the outgoing signaling bits to the receive signaling highway for channels 4 and 19 in this register.
X+13C	7-4 3-0	RRA5-RRD5 RRA20-RRD20	**Receive A5-D5 and A20-D20 Signaling Bits:** The signaling bits in this register are the states of the received A5 to D5 bits and the A20 to D20 bits in the receive signaling buffer. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 5 (Time Slot 5) and 20 (Time Slot 21). Bit 7 is the A5 signaling bit value. Please note that a receive signaling state is written into the receive signaling buffer when the corresponding channel enable bit RSEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position in this register represents the last value written into the buffer. The microprocessor can write the state of the outgoing signaling bits to the receive signaling highway for channels 5 and 20 in this register.

Address (Hex)	Bit	Symbol	Description
X+13D	7-4 3-0	RRA6-RRD6 RRA21-RRD21	**Receive A6-D6 and A21-D21 Signaling Bits:** The signaling bits in this register are the states of the received A6 to D6 bits and the A21 to D21 bits in the receive signaling buffer. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 6 (Time Slot 6) and 21 (Time Slot 22). Bit 7 is the A6 signaling bit value. Please note that a receive signaling state is written into the receive signaling buffer when the corresponding channel enable bit RSEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position in this register represents the last value written into the buffer. The microprocessor can write the state of the outgoing signaling bits to the receive signaling highway for channels 6 and 21 in this register.
X+13E	7-4 3-0	RRA7-RRD7 RRA22-RRD22	**Receive A7-D7 and A22-D22 Signaling Bits:** The signaling bits in this register are the states of the received A7 to D7 bits and the A22 to D22 bits in the receive signaling buffer. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 7 (Time Slot 7) and 22 (Time Slot 23). Bit 7 is the A7 signaling bit value. Please note that a receive signaling state is written into the receive signaling buffer when the corresponding channel enable bit RSEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position in this register represents the last value written into the buffer. The microprocessor can write the state of the outgoing signaling bits to the receive signaling highway for channels 7 and 22 in this register.
X+13F	7-4 3-0	RRA8-RRD8 RRA23-RRD23	**Receive A8-D8 and A23-D23 Signaling Bits:** The signaling bits in this register are the states of the received A8 to D8 bits and the A23 to D23 bits in the receive signaling buffer. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 8 (Time Slot 8) and 23 (Time Slot 24). Bit 7 is the A8 signaling bit value. Please note that a receive signaling state is written into the receive signaling buffer when the corresponding channel enable bit RSEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position in this register represents the last value written into the buffer. The microprocessor can write the state of the outgoing signaling bits to the receive signaling highway for channels 8 and 23 in this register.
X+140	7-4 3-0	RRA9-RRD9 RRA24-RRD24	**Receive A9-D9 and A24-D24 Signaling Bits:** The signaling bits in this register are the states of the received A9 to D9 bits and the A24 to D24 bits in the receive signaling buffer. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 9 (Time Slot 9) and 24 (Time Slot 25). Bit 7 is the A9 signaling bit value. Please note that a receive signaling state is written into the receive signaling buffer when the corresponding channel enable bit RSEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position in this register represents the last value written into the buffer. The microprocessor can write the state of the outgoing signaling bits to the receive signaling highway for channels 9 and 24 in this register.

Address (Hex)	Bit	Symbol	Description
X+141	7-4 3-0	RRA10-RRD10 RRA25-RRD25	**Receive A10-D10 and A25-D25 Signaling Bits:** The signaling bits in this register are the states of the received A10 to D10 bits and the A25 to D25 bits in the receive signaling buffer. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 10 (Time Slot 10) and 25 (Time Slot 26). Bit 7 is the A10 signaling bit value. Please note that a receive signaling state is written into the receive signaling buffer when the corresponding channel enable bit RSEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position in this register represents the last value written into the buffer. The microprocessor can write the state of the outgoing signaling bits to the receive signaling highway for channels 10 and 25 in this register.
X+142	7-4 3-0	RRA11-RRD11 RRA26-RRD26	**Receive A11-D11 and A26-D26 Signaling Bits:** The signaling bits in this register are the states of the received A11 to D11 bits and the A26 to D26 bits in the receive signaling buffer. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 11 (Time Slot 11) and 26 (Time Slot 27). Bit 7 is the A11 signaling bit value. Please note that a receive signaling state is written into the receive signaling buffer when the corresponding channel enable bit RSEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position in this register represents the last value written into the buffer. The microprocessor can write the state of the outgoing signaling bits to the receive signaling highway for channels 11 and 26 in this register.
X+143	7-4 3-0	RRA12-RRD12 RRA27-RRD27	**Receive A12-D12 and A27-D27 Signaling Bits:** The signaling bits in this register are the states of the received A12 to D12 bits and the A27 to D27 bits in the receive signaling buffer. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 12 (Time Slot 12) and 27 (Time Slot 28). Bit 7 is the A12 signaling bit value. Please note that a receive signaling state is written into the receive signaling buffer when the corresponding channel enable bit RSEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position in this register represents the last value written into the buffer. The microprocessor can write the state of the outgoing signaling bits to the receive signaling highway for channels 12 and 27 in this register.
X+144	7-4 3-0	RRA13-RRD13 RRA28-RRD28	**Receive A13-D13 and A28-D28 Signaling Bits:** The signaling bits in this register are the states of the received A13 to D13 bits and the A28 to D28 bits in the receive signaling buffer. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 13 (Time Slot 13) and 28 (Time Slot 29). Bit 7 is the A13 signaling bit value. Please note that a receive signaling state is written into the receive signaling buffer when the corresponding channel enable bit RSEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position in this register represents the last value written into the buffer. The microprocessor can write the state of the outgoing signaling bits to the receive signaling highway for channels 13 and 28 in this register.

Address (Hex)	Bit	Symbol	Description
X+145	7-4 3-0	RRA14-RRD14 RRA29-RRD29	**Receive A14-D14 and A29-D29 Signaling Bits:** The signaling bits in this register are the states of the received A14 to D14 bits and the A29 to D29 bits in the receive signaling buffer. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 14 (Time Slot 14) and 29 (Time Slot 30). Bit 7 is the A14 signaling bit value. Please note that a receive signaling state is written into the receive signaling buffer when the corresponding channel enable bit RSEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position in this register represents the last value written into the buffer. The microprocessor can write the state of the outgoing signaling bits to the receive signaling highway for channels 14 and 29 in this register.
X+146	7-4 3-0	RRA15-RRD15 RRA30-RRD30	**Receive A15-D15 and A30-D30 Signaling Bits:** The signaling bits in this register are the states of the received A15 to D15 bits and the A30 to D30 bits in the receive signaling buffer. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 15 (Time Slot 15) and 30 (Time Slot 31). Bit 7 is the A15 signaling bit value. Please note that a receive signaling state is written into the receive signaling buffer when the corresponding channel enable bit RSEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position in this register represents the last value written into the buffer. The microprocessor can write the state of the outgoing signaling bits to the receive signaling highway for channels 15 and 30 in this register.

Receive Signaling State Match Count Registers

This is one of two active buffers used for signaling debounce. The contents are valid if control bit SIGDB is set to a 1. This buffer contains the four bit current match count (saturating) for each of the 30 signaling nibbles.

Address (Hex)	Bit	Symbol	Description
X+147	7-0		**Reserved:** Indeterminate value.
X+148	7-4 3-0	RSNM1 RSNM16	**Match Counts for Signaling Nibbles for Telephone Channel 1 and 16:** This register contains two four bit saturating counters, RSNM1 and RSNM16. RSNM1 is set to 0H if signaling is not enabled (RSE1, bit 0 in register X+E8H is set to a 0) or the signaling nibble just received does not match the value stored in the Signaling State Active Buffer 1 RRA1-RRD1 (bits 7-4 of register X+138H). RSNM1 is incremented if the signaling nibble just received matches the value stored in the Signaling State Active Buffer 1. If RSNM1 is equal to or greater than global threshold DEBVAL(3-0) (bits 3-0) in register 0FEH, the nibble stored in the Signaling State Active Buffer 1 is transferred to the Signaling State Debounce Buffer RA1-RD1 (bits 7-4 of register X+81H). RSNM16 is set to 0H if signaling is not enabled (RSE16, bit 7 of register X+E9H is set to a 0) or the signaling nibble just received does not match the value stored in the Signaling State Active Buffer 1 RRA16-RRD16 (bits 3-0 of register X+138H). RSNM16 is incremented if the signaling nibble just received matches the value stored in the Signaling State Active Buffer 1. If RSNM16 is equal to or greater than global threshold DEBVAL(3-0) (bits 3-0) in register 0FEH, the nibble stored in the Signaling State Active Buffer 1 is transferred to the Signaling State Debounce Buffer RA16 - RD16 (bits 3 -0 of register X+81H).
X+149	7-4 3-0	RSNM2 RSNM17	**Match Counts for Signaling Nibbles for Telephone Channel 2 and 17:** This register contains two four bit saturating counters, RSNM2 and RSNM17. RSNM2 is set to 0H if signaling is not enabled (RSE2, bit 1 in register X+E8H is set to a 0) or the signaling nibble just received does not match the value stored in the Signaling State Active Buffer 1 RRA2-RRD2 (bits 7-4 of register X+139H). RSNM2 is incremented if the signaling nibble just received matches the value stored in the Signaling State Active Buffer 1. If RSNM2 is equal to or greater than global threshold DEBVAL(3-0) (bits 3-0) in register 0FEH, the nibble stored in the Signaling State Active Buffer 1 is transferred to the Signaling State Debounce Buffer RA2-RD2 (bits 7-4 of register X+82H). RSNM17 is set to 0H if signaling is not enabled (RSE17, bit 0 in register X+EAH is set to a 0) or the signaling nibble just received does not match the value stored in the Signaling State Active Buffer 1 RRA17 - RRD17 (bits 3-0 of register X+139H). RSNM17 is incremented if the signaling nibble just received matches the value stored in the Signaling State Active Buffer 1. If RSNM17 is equal to or greater than global threshold DEBVAL(3-0) (bits 3-0) in register 0FEH, the nibble stored in the Signaling State Active Buffer 1 is transferred to the Signaling State Debounce Buffer RA17-RD17 (bits 3-0 of register X+82H).

Address (Hex)	Bit	Symbol	Description
X+14A	7-4 3-0	RSNM3 RSNM18	**Match Counts for Signaling Nibbles for Telephone Channel 3 and 18:** This register contains two four bit saturating counters, RSNM3 and RSNM18. RSNM3 is set to 0H if signaling is not enabled (RSE3, bit 2 in register X+E8H is set to a 0) or the signaling nibble just received does not match the value stored in the Signaling State Active Buffer 1 RRA3-RRD3 (bits 7-4 of register X+13AH). RSNM3 is incremented if the signaling nibble just received matches the value stored in the Signaling State Active Buffer 1. If RSNM3 is equal to or greater than global threshold DEBVAL(3-0) (bits 3-0) in register 0FEH, the nibble stored in the Signaling State Active Buffer 1 is transferred to the Signaling State Debounce Buffer RA3-RD3 (bits 7-4 of register X+83H). RSNM18 is set to 0H if signaling is not enabled (RSE18, bit 1 in register X+EAH is set to a 0) or the signaling nibble just received does not match the value stored in the Signaling State Active Buffer 1 RRA18-RRD18 (bits 3-0 of register X+13AH). RSNM18 is incremented if the signaling nibble just received matches the value stored in the Signaling State Active Buffer 1. If RSNM18 is equal to or greater than global threshold DEBVAL(3-0) (bits 3-0) in register 0FEH, the nibble stored in the Signaling State Active Buffer 1 is transferred to the Signaling State Debounce Buffer RA18-RD18 (bits 3-0 of register X+83H).
X+14B	7-4 3-0	RSNM4 RSNM19	**Match Counts for Signaling Nibbles for Telephone Channel 4 and 19:** This register contains two four bit saturating counters, RSNM4 and RSNM19. RSNM4 is set to 0H if signaling is not enabled (RSE4, bit 3 in register X+E8H is set to a 0) or the signaling nibble just received does not match the value stored in the Signaling State Active Buffer 1 RRA4-RRD4 (bits 7-4 of register X+13BH). RSNM4 is incremented if the signaling nibble just received matches the value stored in the Signaling State Active Buffer 1. If RSNM4 is equal to or greater than global threshold DEBVAL(3-0) (bits 3-0) in register 0FEH, the nibble stored in the Signaling State Active Buffer 1 is transferred to the Signaling State Debounce Buffer RA4-RD4 (bits 7-4 of register X+84H). RSNM19 is set to 0H if signaling is not enabled (RSE19, bit 2 in register X+EAH is set to a 0) or the signaling nibble just received does not match the value stored in the Signaling State Active Buffer 1 RRA19 - RRD19 (bits 3- 0 of register X+13BH). RSNM19 is incremented if the signaling nibble just received matches the value stored in the Signaling State Active Buffer 1. If RSNM19 is equal to or greater than global threshold DEBVAL(3-0) (bits 3-0) in register 0FEH, the nibble stored in the Signaling State Active Buffer 1 is transferred to the Signaling State Debounce Buffer RA19-RD19 (bits 3-0 of register X+84H).

Address (Hex)	Bit	Symbol	Description
X+14C	7-4 3-0	RSNM5 RSNM20	**Match Counts for Signaling Nibbles for Telephone Channel 5 and 20:** This register contains two four bit saturating counters, RSNM5 and RSNM20. RSNM5 is set to 0H if signaling is not enabled (RSE5, bit 4 in register X+E8H is set to a 0) or the signaling nibble just received does not match the value stored in the Signaling State Active Buffer 1 RRA5-RRD5 (bits 7-4 of register X+13CH). RSNM5 is incremented if the signaling nibble just received matches the value stored in the Signaling State Active Buffer 1. If RSNM5 is equal to or greater than global threshold DEBVAL(3-0) (bits 3-0) in register 0FEH, the nibble stored in the Signaling State Active Buffer 1 is transferred to the Signaling State Debounce Buffer RA5-RD5 (bits 7-4 of register X+85H). RSNM20 is set to 0H if signaling is not enabled (RSE20, bit 3 in register X+EAH is set to a 0) or the signaling nibble just received does not match the value stored in the Signaling State Active Buffer 1 RRA20-RRD20 (bits 3-0 of register X+13CH). RSNM20 is incremented if the signaling nibble just received matches the value stored in the Signaling State Active Buffer 1. If RSNM20 is equal to or greater than global threshold DEBVAL(3-0) (bits 3-0) in register 0FEH, the nibble stored in the Signaling State Active Buffer 1 is transferred to the Signaling State Debounce Buffer RA20-RD20 (bits 3-0 of register X+85H).
X+14D	7-4 3-0	RSNM6 RSNM21	**Match Counts for Signaling Nibbles for Telephone Channel 6 and 21:** This register contains two four bit saturating counters, RSNM6 and RSNM21. RSNM6 is set to 0H if signaling is not enabled (RSE6, bit 5 in register X+E8H is set to a 0) or the signaling nibble just received does not match the value stored in the Signaling State Active Buffer 1 RRA6-RRD6 (bits 7-4 of register X+13DH). RSNM6 is incremented if the signaling nibble just received matches the value stored in the Signaling State Active Buffer 1. If RSNM6 is equal to or greater than global threshold DEBVAL(3-0) (bits 3-0) in register 0FEH, the nibble stored in the Signaling State Active Buffer 1 is transferred to the Signaling State Debounce Buffer RA6-RD6 (bits 7-4 of register X+86H). RSNM21 is set to 0H if signaling is not enabled (RSE21, bit 4 in register X+EAH is set to a 0) or the signaling nibble just received does not match the value stored in the Signaling State Active Buffer 1 RRA2 -RRD21 (bits 3- 0 of register X+13DH). RSNM21 is incremented if the signaling nibble just received matches the value stored in the Signaling State Active Buffer 1. If RSNM21 is equal to or greater than global threshold DEBVAL(3-0) (bits 3-0) in register 0FEH, the nibble stored in the Signaling State Active Buffer 1 is transferred to the Signaling State Debounce Buffer RA21-RD21 (bits 3-0 of register X+86H).

Address (Hex)	Bit	Symbol	Description
X+14E	7-4 3-0	RSNM7 RSNM22	**Match Counts for Signaling Nibbles for Telephone Channel 7 and 22:** This register contains two four bit saturating counters, RSNM7 and RSNM22. RSNM7 is set to 0H if signaling is not enabled (RSE7, bit 6 in register X+E8H is set to a 0) or the signaling nibble just received does not match the value stored in the Signaling State Active Buffer 1 RRA7-RRD7 (bits 7-4 of register X+13EH). RSNM7 is incremented if the signaling nibble just received matches the value stored in the Signaling State Active Buffer 1. If RSNM7 is equal to or greater than global threshold DEBVAL(3-0) (bits 3-0) in register 0FEH, the nibble stored in the Signaling State Active Buffer 1 is transferred to the Signaling State Debounce Buffer RA7-RD7 (bits 7-4 of register X+87H). RSNM22 is set to 0H if signaling is not enabled (RSE22, bit 5 in register X+EAH is set to a 0) or the signaling nibble just received does not match the value stored in the Signaling State Active Buffer 1 RRA22-RRD22 (bits 3-0 of register X+13EH). RSNM22 is incremented if the signaling nibble just received matches the value stored in the Signaling State Active Buffer 1. If RSNM22 is equal to or greater than global threshold DEBVAL(3-0) (bits 3-0) in register 0FEH, the nibble stored in the Signaling State Active Buffer 1 is transferred to the Signaling State Debounce Buffer RA22-RD22 (bits 3-0 of register X+87H).
X+14F	7-4 3-0	RSNM8 RSNM23	**Match Counts for Signaling Nibbles for Telephone Channel 8 and 23:** This register contains two four bit saturating counters, RSNM8 and RSNM23. RSNM8 is set to 0H if signaling is not enabled (RSE8, bit 7 in register X+E8H is set to a 0) or the signaling nibble just received does not match the value stored in the Signaling State Active Buffer 1 RRA8-RRD8 (bits 7-4 of register X+13FH). RSNM8 is incremented if the signaling nibble just received matches the value stored in the Signaling State Active Buffer 1. If RSNM8 is equal to or greater than global threshold DEBVAL(3-0) (bits 3-0) in register 0FEH, the nibble stored in the Signaling State Active Buffer 1 is transferred to the Signaling State Debounce Buffer RA8 - RD8 (bits 7-4 of register X+88H). RSNM23 is set to 0H if signaling is not enabled (RSE23, bit 6 in register X+EAH is set to a 0) or the signaling nibble just received does not match the value stored in the Signaling State Active Buffer 1 RRA23-RRD23 (bits 3-0 of register X+13FH). RSNM23 is incremented if the signaling nibble just received matches the value stored in the Signaling State Active Buffer 1. If RSNM23 is equal to or greater than global threshold DEBVAL(3-0) (bits 3-0) in register 0FEH, the nibble stored in the Signaling State Active Buffer 1 is transferred to the Signaling State Debounce Buffer RA23-RD23 (bits 3-0 of register X+88H).

Address (Hex)	Bit	Symbol	Description
X+150	7-4 3-0	RSNM9 RSNM24	**Match Counts for Signaling Nibbles for Telephone Channel 9 and 24:** This register contains two four bit saturating counters, RSNM9 and RSNM24. RSNM9 is set to 0H if signaling is not enabled (RSE9, bit 0 in register X+E9H is set to a 0) or the signaling nibble just received does not match the value stored in the Signaling State Active Buffer 1 RRA9-RRD9 (bits 7-4 of register X+140H). RSNM9 is incremented if the signaling nibble just received matches the value stored in the Signaling State Active Buffer 1. If RSNM9 is equal to or greater than global threshold DEBVAL(3-0) (bits 3-0) in register 0FEH, the nibble stored in the Signaling State Active Buffer 1 is transferred to the Signaling State Debounce Buffer RA9-RD9 (bits 7-4 of register X+89H). RSNM24 is set to 0H if signaling is not enabled (RSE24, bit 7 in register X+EAH is set to a 0) or the signaling nibble just received does not match the value stored in the Signaling State Active Buffer 1 RRA24-RRD24 (bits 3-0 of register X+140H). RSNM24 is incremented if the signaling nibble just received matches the value stored in the Signaling State Active Buffer 1. If RSNM24 is equal to or greater than global threshold DEBVAL(3-0) (bits 3-0) in register 0FEH, the nibble stored in the Signaling State Active Buffer 1 is transferred to the Signaling State Debounce Buffer RA24-RD24 (bits 3-0 of register X+89H).
X+151	7-4 3-0	RSNM10 RSNM25	**Match Counts for Signaling Nibbles for Telephone Channel 10 and 25:** This register contains two four bit saturating counters, RSNM10 and RSNM25. RSNM10 is set to 0H if signaling is not enabled (RSE10, bit 1 in register X+E9H is set to a 0) or the signaling nibble just received does not match the value stored in the Signaling State Active Buffer 1 RRA10-RRD10 (bits 7-4 of register X+141H). RSNM10 is incremented if the signaling nibble just received matches the value stored in the Signaling State Active Buffer 1. If RSNM10 is equal to or greater than global threshold DEBVAL(3-0) (bits 3-0) in register 0FEH, the nibble stored in the Signaling State Active Buffer 1 is transferred to the Signaling State Debounce Buffer RA10-RD10 (bits 7-4 of register X+8AH). RSNM25 is set to 0H if signaling is not enabled (RSE25, bit 0 in register X+EBH is set to a 0) or the signaling nibble just received does not match the value stored in the Signaling State Active Buffer 1 RRA25-RRD25 (bits 3-0 of register X+141H). RSNM25 is incremented if the signaling nibble just received matches the value stored in the Signaling State Active Buffer 1. If RSNM25 is equal to or greater than global threshold DEBVAL(3-0) (bits 3-0) in register 0FEH, the nibble stored in the Signaling State Active Buffer 1 is transferred to the Signaling State Debounce Buffer RA25-RD25 (bits 3-0 of register X+8AH).

Address (Hex)	Bit	Symbol	Description
X+152	7-4 3-0	RSNM11 RSNM26	**Match Counts for Signaling Nibbles for Telephone Channel 11 and 26:** This register contains two four bit saturating counters, RSNM11 and RSNM26. RSNM11 is set to 0H if signaling is not enabled (RSE11, bit 2 in register X+E9H is set to a 0) or the signaling nibble just received does not match the value stored in the Signaling State Active Buffer 1 RRA11-RRD11 (bits 7-4 of register X+142H). RSNM11 is incremented if the signaling nibble just received matches the value stored in the Signaling State Active Buffer 1. If RSNM11 is equal to or greater than global threshold DEBVAL(3-0) (bits 3-0) in register 0FEH, the nibble stored in the Signaling State Active Buffer 1 is transferred to the Signaling State Debounce Buffer RA11-RD11 (bits 7-4 of register X+8BH). RSNM26 is set to 0H if signaling is not enabled (RSE26, bit 1 in register X+EBH is set to a 0) or the signaling nibble just received does not match the value stored in the Signaling State Active Buffer 1 RRA26-RRD26 (bits 3-0 of register X+142H). RSNM26 is incremented if the signaling nibble just received matches the value stored in the Signaling State Active Buffer 1. If RSNM26 is equal to or greater than global threshold DEBVAL(3-0) (bits 3-0) in register 0FEH, the nibble stored in the Signaling State Active Buffer 1 is transferred to the Signaling State Debounce Buffer RA26-RD26 (bits 3-0 of register X+8BH).
X+153	7-4 3-0	RSNM12 RSNM27	**Match Counts for Signaling Nibbles for Telephone Channel 12 and 27:** This register contains two four bit saturating counters, RSNM12 and RSNM27. RSNM12 is set to 0H if signaling is not enabled (RSE12, bit 3 in register X+E9H is set to a 0) or the signaling nibble just received does not match the value stored in the Signaling State Active Buffer 1 RRA12-RRD12 (bits 7-4 of register X+143H). RSNM12 is incremented if the signaling nibble just received matches the value stored in the Signaling State Active Buffer 1. If RSNM12 is equal to or greater than global threshold DEBVAL(3-0) (bits 3-0) in register 0FEH, the nibble stored in the Signaling State Active Buffer 1 is transferred to the Signaling State Debounce Buffer RA12-RD12 (bits 7-4 of register X+8CH). RSNM27 is set to 0H if signaling is not enabled (RSE27, bit 2 in register X+EBH is set to a 0) or the signaling nibble just received does not match the value stored in the Signaling State Active Buffer 1 RRA27-RRD27 (bits 3-0 of register X+143H). RSNM27 is incremented if the signaling nibble just received matches the value stored in the Signaling State Active Buffer 1. If RSNM27 is equal to or greater than global threshold DEBVAL(3-0) (bits 3-0) in register 0FEH, the nibble stored in the Signaling State Active Buffer 1 is transferred to the Signaling State Debounce Buffer RA27-RD27 (bits 3-0 of register X+8CH).

Address (Hex)	Bit	Symbol	Description
X+154	7-4 3-0	RSNM13 RSNM28	**Match Counts for Signaling Nibbles for Telephone Channel 13 and 28:** This register contains two four bit saturating counters, RSNM13 and RSNM28. RSNM13 is set to 0H if signaling is not enabled (RSE13, bit 4 in register X+E9H is set to a 0) or the signaling nibble just received does not match the value stored in the Signaling State Active Buffer 1 RRA13-RRD13 (bits 7-4 of register X+144H). RSNM13 is incremented if the signaling nibble just received matches the value stored in the Signaling State Active Buffer 1. If RSNM13 is equal to or greater than global threshold DEBVAL(3-0) (bits 3-0) in register 0FEH, the nibble stored in the Signaling State Active Buffer 1 is transferred to the Signaling State Debounce Buffer RA13-RD13 (bits 7-4 of register X+8DH). RSNM28 is set to 0H if signaling is not enabled (RSE28, bit 3 in register X+EBH is set to a 0) or the signaling nibble just received does not match the value stored in the Signaling State Active Buffer 1 RRA28-RRD28 (bits 3-0 of register X+144H). RSNM28 is incremented if the signaling nibble just received matches the value stored in the Signaling State Active Buffer 1. If RSNM28 is equal to or greater than global threshold DEBVAL(3-0) (bits 3-0) in register 0FEH, the nibble stored in the Signaling State Active Buffer 1 is transferred to the Signaling State Debounce Buffer RA28-RD28 (bits 3-0 of register X+8DH).
X+155	7-4 3-0	RSNM14 RSNM29	**Match Counts for Signaling Nibbles for Telephone Channel 14 and 29:** This register contains two four bit saturating counters, RSNM14 and RSNM29. RSNM14 is set to 0H if signaling is not enabled (RSE14, bit 5 in register X+E9H is set to a 0) or the signaling nibble just received does not match the value stored in the Signaling State Active Buffer 1 RRA14-RRD14 (bits 7-4 of register X+145H). RSNM14 is incremented if the signaling nibble just received matches the value stored in the Signaling State Active Buffer 1. If RSNM14 is equal to or greater than global threshold DEBVAL(3-0) (bits 3-0) in register 0FEH, the nibble stored in the Signaling State Active Buffer 1 is transferred to the Signaling State Debounce Buffer RA14-RD14 (bits 7-4 of register X+8EH). RSNM29 is set to 0H if signaling is not enabled (RSE29, bit 4 in register X+EBH is set to a 0) or the signaling nibble just received does not match the value stored in the Signaling State Active Buffer 1 RRA29-RRD29 (bits 3-0 of register X+145H). RSNM29 is incremented if the signaling nibble just received matches the value stored in the Signaling State Active Buffer 1. If RSNM29 is equal to or greater than global threshold DEBVAL(3-0) (bits 3-0) in register 0FEH, the nibble stored in the Signaling State Active Buffer 1 is transferred to the Signaling State Debounce Buffer RA29-RD29 (bits 3-0 of register X+8EH).

Address (Hex)	Bit	Symbol	Description
X+156	7-4 3-0	RSNM15 RSNM30	**Match Counts for Signaling Nibbles for Telephone Channel 15 and 30:** This register contains two four bit saturating counters, RSNM15 and RSNM30. RSNM15 is set to 0H if signaling is not enabled (RSE15, bit 6 in register X+E9H is set to a 0) or the signaling nibble just received does not match the value stored in the Signaling State Active Buffer 1 RRA15-RRD15 (bits 7-4 of register X+146H). RSNM15 is incremented if the signaling nibble just received matches the value stored in the Signaling State Active Buffer 1. If RSNM15 is equal to or greater than global threshold DEBVAL(3-0) (bits 3-0) in register 0FEH, the nibble stored in the Signaling State Active Buffer 1 is transferred to the Signaling State Debounce Buffer RA15-RD15 (bits 7-4 of register X+8FH). RSNM30 is set to 0H if signaling is not enabled (RSE30, bit 5 in register X+EBH is set to a 0) or the signaling nibble just received does not match the value stored in the Signaling State Active Buffer 1 RRA30-RRD30 (bits 3-0 of register X+146H). RSNM30 is incremented if the signaling nibble just received matches the value stored in the Signaling State Active Buffer 1. If RSNM30 is equal to or greater than global threshold DEBVAL(3-0) (bits 3-0) in register 0FEH, the nibble stored in the Signaling State Active Buffer 1 is transferred to the Signaling State Debounce Buffer RA30-RD30 (bits 3-0 of register X+8FH).

Transmit Signaling Control Registers

The bits in these read/write registers control the transmit signaling for telephone channels 1 through 30.

Address (Hex)	Bit	Symbol	Description
X+EC	7-0	TSE8-TSE1	**Transmit Signaling Enable for Channels 8-1:** When a bit in this register is set to 1, the transmit signaling bits for the corresponding telephone channel are enabled. The ABCD signaling bits are written into the transmit signaling buffers from the transmit signaling highway, and are inserted into the transmit line. When set to 0, the signaling states in the transmit signaling buffer are frozen. The ability to internally write the signaling bits from the transmit signaling highway into the transmit signaling buffers is disabled. This enables the microprocessor to write the signaling states into the transmit signaling registers. Bit 7 is the enable bit for channel 8. Signaling information for telephone channel c is carried in Time Slot c.
X+ED	7-0	TSE16-TSE9	**Transmit Signaling Enable for Channels 16-9:** When a bit in this register is set to 1, the transmit signaling bits for the corresponding telephone channel are enabled. The ABCD signaling bits are written into the transmit signaling buffers from the transmit signaling highway, and are inserted into the transmit line. When set to 0, the signaling states in the transmit signaling buffer are frozen. The ability to internally write the signaling bits from the transmit signaling highway into the transmit signaling buffers is disabled. This enables the microprocessor to write the signaling states into the transmit signaling registers. Bit 7 is the enable bit for channel 16. Signaling information for telephone channel c is carried in Time Slot c, except for channel 16, which is carried in Time Slot 17.

Address (Hex)	Bit	Symbol	Description
X+EE	7-0	TSE24-TSE17	**Transmit Signaling Enable for Channels 24-17:** When a bit in this register is set to 1, the transmit signaling bits for the corresponding telephone channel are enabled. The ABCD signaling bits are written into the transmit signaling buffers from the transmit signaling highway, and are inserted into the transmit line. When set to 0, the signaling states in the transmit signaling buffer are frozen. The ability to internally write the signaling bits from the transmit signaling highway into the transmit signaling buffers is disabled. This enables the microprocessor to write the signaling states into the transmit signaling registers. Bit 7 is the enable bit for channel 24. Signaling information for telephone channel c is carried in Time Slot c+1.
X+EF	7-6		**Reserved:** Write these bits to 0.
	5-0	TSE30-TSE25	**Transmit Signaling Enable for Channels 30-25:** When a bit in this register is set to 1, the transmit signaling bits for the corresponding telephone channel are enabled. The ABCD signaling bits are written into the transmit signaling buffers from the transmit signaling highway, and are inserted into the transmit line. When set to 0, the signaling states in the transmit signaling buffer are frozen. The ability to internally write the signaling bits from the transmit signaling highway into the transmit signaling buffers is disabled. This enables the microprocessor to write the signaling states into the transmit signaling registers. Bit 5 is the enable bit for channel 30. Signaling information for telephone channel c is carried in Time Slot c+1.

Transmit Signaling State Registers

These read/write registers contain the transmit signaling nibbles for telephone channels 1 through 30, plus the Time Slot 16 multiframe bits and the spare/remote alarm bits.

Address (Hex)	Bit	Symbol	Description
X+D0	7-4	TSIGMAS	**Transmit Signaling Multiframe Alignment Signal:** The bits in this register contain the states of the transmit multiframe alignment pattern (Time Slot 16 bits 1-4 in frame 0) in the transmit signaling buffer. This pattern is normally 0000. Bit 7 is transmitted bit 1.
	3-0	TX0, TY, TX1, TX2	**Transmit Signaling Spare Bits and Remote Alarm Bit:** Bits 3, 1 and 0 in this register contain the states of the transmit X0, X1, X2 bits (spare bits) in Time Slot 16, which are carried in bits 5, 7, and 8 of frame 0 in the multiframe. The TY bit (bit 2) is defined as the loss of multiframe indication bit and is carried in bit 6 in frame 0 of the multiframe.
X+D1	7-4 3-0	TA1-TD1 TA16-TD16	**Transmit A1-D1 and A16-D16 Signaling Bits:** The signaling bits in this register are the A1 to D1 and A16 to D16 signaling bits written into the signaling buffer from the transmit signaling highway. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 1 (Time Slot 1) and 16 (Time Slot 17). Bit 7 is the A1 signaling bit value. Please note that a transmit signaling state is written into the signaling buffer when the corresponding channel enable bit TSEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position represents the last value written into the buffer. The microprocessor can write the state of the transmitted signaling bits that correspond to channels 1 and 16 in this register.
X+D2	7-4 3-0	TA2-TD2 TA17-TD17	**Transmit A2-D2 and A17-D17 Signaling Bits:** The signaling bits in this register are the A2 to D2 and A17 to D17 signaling bits written into the signaling buffer from the transmit signaling highway. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 2 (Time Slot 2) and 17 (Time Slot 18). Bit 7 is the A2 signaling bit value. Please note that a transmit signaling state is written into the signaling buffer when the corresponding enable bit TSEc is written with a 1. When the corresponding channel enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position represents the last value written into the buffer. The microprocessor can write the state of the transmitted signaling bits that correspond to channels 2 and 17 in this register.
X+D3	7-4 3-0	TA3-TD3 TA18-TD18	**Transmit A3-D3 and A18-D18 Signaling Bits:** The signaling bits in this register are the A3 to D3 and A18 to D18 signaling bits written into the signaling buffer from the transmit signaling highway. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 3 (Time Slot 3) and 18 (Time Slot 19). Bit 7 is the A3 signaling bit value. Please note that a transmit signaling state is written into the signaling buffer when the corresponding channel enable bit TSEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position represents the last value written into the buffer. The microprocessor can write the state of the transmitted signaling bits that correspond to channels 3 and 18 in this register.

Address (Hex)	Bit	Symbol	Description
X+D4	7-4 3-0	TA4-TD4 TA19-TD19	**Transmit A4-D4 and A19-D19 Signaling Bits:** The signaling bits in this register are the A4 to D4 and A19 to D19 signaling bits written into the signaling buffer from the transmit signaling highway. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 4 (Time Slot 4) and 19 (Time Slot 20). Bit 7 is the A4 signaling bit value. Please note that a transmit signaling state is written into the signaling buffer when the corresponding channel enable bit TSEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position represents the last value written into the buffer. The microprocessor can write the state of the transmitted signaling bits that correspond to channels 4 and 19 in this register.
X+D5	7-4 3-0	TA5-TD5 TA20-TD20	**Transmit A5-D5 and A20-D20 Signaling Bits:** The signaling bits in this register are the A5 to D5 and A20 to D20 signaling bits written into the signaling buffer from the transmit signaling highway. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 5 (Time Slot 5) and 20 (Time Slot 21). Bit 7 is the A5 signaling bit value. Please note that a transmit signaling state is written into the signaling buffer when the corresponding channel enable bit TSEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position represents the last value written into the buffer. The microprocessor can write the state of the transmitted signaling bits that correspond to channels 5 and 20 in this register.
X+D6	7-4 3-0	TA6-TD6 TA21-TD21	**Transmit A6-D6 and A21-D21 Signaling Bits:** The signaling bits in this register are the A6 to D6 and A21 to D21 signaling bits written into the signaling buffer from the transmit signaling highway. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 6 (Time Slot 6) and 21 (Time Slot 22). Bit 7 is the A6 signaling bit value. Please note that a transmit signaling state is written into the signaling buffer when the corresponding channel enable bit TSEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position represents the last value written into the buffer. The microprocessor can write the state of the transmitted signaling bits that correspond to channels 6 and 21 in this register.
X+D7	7-4 3-0	TA7-TD7 TA22-TD22	**Transmit A7-D7 and A22-D22 Signaling Bits:** The signaling bits in this register are the A7 to D7 and A22 to D22 signaling bits written into the signaling buffer from the transmit signaling highway. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 7 (Time Slot 7) and 22 (Time Slot 23). Bit 7 is the A7 signaling bit value. Please note that a transmit signaling state is written into the signaling buffer when the corresponding channel enable bit TSEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position represents the last value written into the buffer. The microprocessor can write the state of the transmitted signaling bits that correspond to channels 7 and 22 in this register.

Address (Hex)	Bit	Symbol	Description
X+D8	7-4 3-0	TA8-TD8 TA23-TD23	**Transmit A8-D8 and A23-D23 Signaling Bits:** The signaling bits in this register are the A8 to D8 and A23 to D23 signaling bits written into the signaling buffer from the transmit signaling highway. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 8 (Time Slot 8) and 23 (Time Slot 24). Bit 7 is the A8 signaling bit value. Please note that a transmit signaling state is written into the signaling buffer when the corresponding channel enable bit TSEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position represents the last value written into the buffer. The microprocessor can write the state of the transmitted signaling bits that correspond to channels 8 and 23 in this register.
X+D9	7-4 3-0	TA9-TD9 TA24-TD24	**Transmit A9-D9 and A24-D24 Signaling Bits:** The signaling bits in this register are the A9 to D9 and A24 to D24 signaling bits written into the signaling buffer from the transmit signaling highway. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 9 (Time Slot 9) and 24 (Time Slot 25). Bit 7 is the A9 signaling bit value. Please note that a transmit signaling state is written into the signaling buffer when the corresponding channel enable bit TSEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position represents the last value written into the buffer. The microprocessor can write the state of the transmitted signaling bits that correspond to channels 9 and 24 in this register.
X+DA	7-4 3-0	TA10-TD10 TA25-TD25	**Transmit A10-D10 and A25-D25 Signaling Bits:** The signaling bits in this register are the A10 to D10 and A25 to D25 signaling bits written into the signaling buffer from the transmit signaling highway. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 10 (Time Slot 10) and 25 (Time Slot 26). Bit 7 is the A10 signaling bit value. Please note that a transmit signaling state is written into the signaling buffer when the corresponding channel enable bit TSEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position represents the last value written into the buffer. The microprocessor can write the state of the transmitted signaling bits that correspond to channels 10 and 25 in this register.
X+DB	7-4 3-0	TA11-TD11 TA26-TD26	**Transmit A11-D11 and A26-D26 Signaling Bits:** The signaling bits in this register are the A11 to D11 and A26 to D26 signaling bits written into the signaling buffer from the transmit signaling highway. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 11 (Time Slot 11) and 26 (Time Slot 27). Bit 7 is the A11 signaling bit value. Please note that a transmit signaling state is written into the signaling buffer when the corresponding channel enable bit TSEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position represents the last value written into the buffer. The microprocessor can write the state of the transmitted signaling bits that correspond to channels 11 and 26 in this register.

Address (Hex)	Bit	Symbol	Description
X+DC	7-4 3-0	TA12-TD12 TA27-TD27	**Transmit A12-D12 and A27-D27 Signaling Bits:** The signaling bits in this register are the A12 to D12 and A27 to D27 signaling bits written into the signaling buffer from the transmit signaling highway. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 12 (Time Slot 12) and 27 (Time Slot 28). Bit 7 is the A12 signaling bit value. Please note that a transmit signaling state is written into the signaling buffer when the corresponding channel enable bit TSEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position represents the last value written into the buffer. The microprocessor can write the state of the transmitted signaling bits that correspond to channels 12 and 27 in this register.
X+DD	7-4 3-0	TA13-TD13 TA28-TD28	**Transmit A13-D13 and A28-D28 Signaling Bits:** The signaling bits in this register are the A13 to D13 and A28 to D28 signaling bits written into the signaling buffer from the transmit signaling highway. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 13 (Time Slot 13) and 28 (Time Slot 29). Bit 7 is the A13 signaling bit value. Please note that a transmit signaling state is written into the signaling buffer when the corresponding channel enable bit TSEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position represents the last value written into the buffer. The microprocessor can write the state of the transmitted signaling bits that correspond to channels 13 and 28 in this register.
X+DE	7-4 3-0	TA14-TD14 TA29-TD29	**Transmit A14-D14 and A29-D29 Signaling Bits:** The signaling bits in this register are the A14 to D14 and A29 to D29 signaling bits written into the signaling buffer from the transmit signaling highway. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 14 (Time Slot 14) and 29 (Time Slot 30). Bit 7 is the A14 signaling bit value. Please note that a transmit signaling state is written into the signaling buffer when the corresponding channel enable bit TSEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position represents the last value written into the buffer. The microprocessor can write the state of the transmitted signaling bits that correspond to channels 14 and 29 in this register.
X+DF	7-4 3-0	TA15-TD15 TA30-TD30	**Transmit A15-D15 and A30-D30 Signaling Bits:** The signaling bits in this register are the A15 to D15 and A30 to D30 signaling bits written into the signaling buffer from the transmit signaling highway. The bits correspond to the ABCD signaling bits carried in Time Slot 16 for channels 15 (Time Slot 15) and 30 (Time Slot 31). Bit 7 is the A15 signaling bit value. Please note that a transmit signaling state is written into the signaling buffer when the corresponding channel enable bit TSEc is written with a 1. When the corresponding enable bit is written with a 0, a signaling freeze occurs, and the value read in a bit position represents the last value written into the buffer. The microprocessor can write the state of the transmitted signaling bits that correspond to channels 15 and 30 in this register.

E1 Line Status Registers

These registers are read/write, except for registers X+10H and X+164H, which are read-only unlatched. The status bits in the X+11H and X+165H registers represent the latched status indications generated by the channel alarms. The bits latch on either the positive transition, the negative transition, or both transitions of the current status or interrupt request event bits in register X+10H/X+164H as defined by the RISE/FALL control bits (bits 7 and 6) in the Global Configuration Register 00BH. A latched bit will cause a hardware interrupt indication when the global interrupt mask bit GIM (bit 5) in register 00BH, and the corresponding mask bit in the mask registers, X+14H and X+166H are both written with a 0 and the associated global mask bits in registers 012H and 01BH are set to 0. The bits in register X+10H and X+165H represent the current (unlatched) alarm status. A latched status bit is reset by writing a 0 into the latched bit position, or by the rising edge of the one-second pulse (from SREGT, BPOSC or RCLKn) when the performance monitoring/fault monitoring feature is enabled. This feature activates the shadow registers X+12H, X+13H, X+167H and X+168H, and it is enabled by writing a 1 to control bit SRGEN (bit 3) in the Global Configuration register 00BH.

Address (Hex)	Bit	Symbol	Description
X+10	7	LOS	**Loss Of Signal Alarm Indication:** This bit position is used to indicate a unlatched line loss of signal alarm indication. A 1 is a true state. When control bit RAIL (bit 7) in register X+00H is set to a 1 loss of signal is a consecutive string of bit periods when no pulses are detected on either lead RPOSn or lead RNEGn as defined by control bits LOSI7-LOSI0 in register 02AH, OND5-OND0 and ENLOSI in register 02BH. In addition, LOS may also be generated in NRZ mode (RAIL = 0) as controlled by control bits EXLOS and ELOSN (bits 3 and 2) in register X+00H and RXFS (bit 1) in register X+1FFH by a signal on RSCANn input lead.
	6	AIS	**AIS Alarm Indication (Unlatched):** A 1 indicates that a line Alarm Indication Signal (AIS) (and/or an AIS in Time Slot 16 if control bit TS16EIC is set to a 1) has been detected. Control bit ENLAIS enables a line AIS alarm. Control bit E16AIS enables a Receive Time Slot 16 AIS alarm. Control bit ENAISI (bit 5) in register 00CH determines the detection criteria for AIS. When ENAISI is set to 0,a line AIS is detected when the received line signal has two or less zeros in each of two consecutive double-frame periods (512 bits). Recovery occurs when each of two consecutive double-frame periods contain three or more zeros after frame alignment has been detected. This is ITU-T G.775 compliant. When ENAISI is set to 1,a line AIS is detected when the received line signal has two or less zeros in a single double-frame period (512 bits). Recovery occurs when a single double-frame period contains three or more zeros after frame alignment has been detected. An AIS in Time Slot 16 is detected when the received time slot has detected three or less zeros in each of two consecutive multiframe periods. Recovery occurs when each of two consecutive multiframe periods contains four or more zeros or when the multiframe alignment signal has been detected.
	5	OOF	**Out Of Frame (OOF) Alarm (Unlatched):** A 1 indicates that an Out Of Frame alarm has been detected. The alarm is programmed using the OOF1 and OOF0 control (bits 2 and 1) in register X+01H. The E1Fx8 supports two recovery schemes, with or without the CRC-4 check. See the Operations section for more details.

Address (Hex)	Bit	Symbol	Description
X+10 (cont.)	4	RAI	**Remote Alarm Indication (RAI) (Unlatched):** A 1 indicates that the received RAI bit is a 1 for four or more consecutive frames in which it is carried. The RAI bit is bit 3 in Time Slot 0, in those alternate (NFAS) frames that are not carrying the frame alignment pattern. If control bit TS16EIC (bit 0) in register X+00H is set to a 1, the occurrence of three of the Y-bits of Time Slot 16 set to a 1 will also cause this bit to be set. Recovery occurs when the RAI bit is 0 for four (NFAS) or three (Y-bit) or more consecutive frames in which it is carried.
	3	CFA	**Change In Frame Alignment (CFA) Indication (Unlatched):** A 1 indicates that the frame alignment circuit has detected a change in the frame alignment pattern, only after frame alignment has been regained.
	2	OOFM	**Out Of Multiframe Alignment (OOFM) Alarm (Unlatched):** A 1 indicates that Time Slot 16 multiframe alignment has been lost (if control bit TS16EIC (bit 0) in register X+00H is set to a 1) and/or a CRC-4 multiframe alignment has also been lost. Control bit EOOCRC (bit 2) in register X+03H enables a loss of CRC-4 multiframe alignment alarm. Control bit EOO16M (bit 1) in register X+03H enables a TS16 multiframe alarm.
	1	SLIP	**Slip Indication (Unlatched):** This bit reflects the current status of the transmit/receive slip buffer with respect to a slip being executed in the previous 125 microseconds. A 1 is true state.
	0	SCHG	**Signaling Change of State Indication:** This bit position is used to indicate a change of state of any signaling bit when control bit SIGIEN (bit 3) in register X+134H is set to a 1. A 1 is a true state.
X+11	7	LLOS	**Latched Loss Of Signal (LOS):** This bit position latches when there is a transition in the unlatched bit LOS in register X+10H. This bit is set on the transition set by the RISE and FALL bits in register 00BH. A 1 is true state. If not masked by the corresponding mask bit, the GIM bit in the global control register or corresponding global mask bit, an interrupt is generated. This bit is cleared by writing a 0 into this bit position or by the one-second pulse, if the shadow register feature is enabled (global control bit SRGEN set to a 1).
	6	LAIS	**Latched AIS:** This bit position latches when there is a transition in the unlatched bit AIS in register X+10H. This bit is set on the transition set by the RISE and FALL bits in register 00BH. A 1 is true state. If not masked by the corresponding mask bit, the GIM bit in the global control register or corresponding global mask bit, an interrupt is generated. This bit is cleared by writing a 0 into this bit position or by the one-second pulse, if the shadow register feature is enabled (global control bit SRGEN set to a 1).
	5	LOOF	**Latched Out Of Frame (OOF):** This bit position latches when there is a transition in the unlatched bit OOF in register X+10H. This bit is set on the transition set by the RISE and FALL bits in register 00BH. A 1 is true state. If not masked by the corresponding mask bit, the GIM bit in the global control register or corresponding global mask bit, an interrupt is generated. This bit is cleared by writing a 0 into this bit position or by the one-second pulse, if the shadow register feature is enabled (global control bit SRGEN set to a 1).

Address (Hex)	Bit	Symbol	Description
X+11 (cont.)	4	LRAI	**Latched Remote Alarm Indication (RAI):** This bit position latches when there is a transition in the unlatched bit RAI in register X+10H. This bit is set on the transition set by the RISE and FALL bits in register 00BH. A 1 is true state. If not masked by the corresponding mask bit, the GIM bit in the global control register or corresponding global mask bit, an interrupt is generated. This bit is cleared by writing a 0 into this bit position or by the one-second pulse, if the shadow register feature is enabled (global control bit SRGEN set to a 1).
	3	LCFA	**Latched Change In Frame Alignment Alarm:** This bit position latches when there is a transition in the unlatched bit CFA in register X+10H. This bit is set on the transition set by the RISE bit in register 00BH. A 1 is true state. If not masked by the corresponding mask bit, the GIM bit in the Global control register or corresponding global mask bit, an interrupt is generated. This bit is cleared by writing a 0 into this bit position or by the one-second pulse, if the shadow register feature is enabled (global control bit SRGEN set to a 1).
	2	LOOFM	**Latched Out Of Multiframe Alignment (OOFM):** This bit position latches when there is a transition in the unlatched bit OOFM in register X+10H. This bit is set on the transition set by the RISE and FALL bits in register 00BH. A 1 is true state. If not masked by the corresponding mask bit, the GIM bit in the Global control register or corresponding global mask bit, an interrupt is generated. This bit is cleared by writing a 0 into this bit position or by the one-second pulse, if the shadow register feature is enabled (global control bit SRGEN set to a 1).
	1	LSLIP	**Latched Slip Indication:** This bit position latches when there is a transition in the unlatched bit SLIP in register X+10H. This bit is set on the transition set by the RISE and FALL bits in register 00BH. A 1 is true state. If not masked by the corresponding mask bit, the GIM bit in the Global control register or corresponding global mask bit, an interrupt is generated. This bit is cleared by writing a 0 into this bit position or by the one-second pulse, if the shadow register feature is enabled (global control bit SRGEN set to a 1).
	0	LSCHG	**Latched Signaling Change of State Indication:** This bit position latches when there is a transition in the unlatched bit SCHG in register X+10H. This bit is set on the transition set by the RISE bit in register 00BH. If not masked by the corresponding mask bit, the GIM bit in the Global control register or corresponding global mask bit, an interrupt is generated. This bit is cleared by writing a 0 into this bit position or by the one-second pulse, if the shadow register feature is enabled (global control bit SRGEN set to a 1).

Address (Hex)	Bit	Symbol	Description
X+12	7	PLOS	**Loss Of Signal Alarm One-second Error Indication:** Enabled when control bit SRGEN (bit 3) in register 00BH is a 1, otherwise this bit is held to 0. This bit is set to 1 when a loss of signal alarm indication has been detected in the last one-second interval.
	6	PAIS	**AIS One-second Error Indication:** Enabled when control bit SRGEN is a 1, otherwise this bit is held to 0. This bit is set to 1 when an AIS alarm indication in register X+10H has been detected in the last one-second interval.
	5	POOF	**Out Of Frame One-second Error Indication:** Enabled when control bit SRGEN is a 1, otherwise this bit is held to 0. This bit is set to 1 when an out of frame alarm indication in register X+10H has been detected in the last one-second interval.
	4	PRAI	**RAI (Yellow) Alarm One-second Error Indication:** Enabled when control bit SRGEN is a 1, otherwise this bit is held to 0. This bit is set to 1 when a RAI (Yellow) alarm indication in register X+10H has been detected in the last one-second interval.
	3	PCFA	**Change In Frame Alignment Indication:** Enabled when control bit SRGEN is a 1, otherwise this bit is held to 0. This bit is set to 1 when a change in frame alignment indication in register X+10H has been detected in the last one-second interval.
	2	POOFM	**Out Of Multiframe Alignment (OOFM) One-second Error:** Enabled when control bit SRGEN is a 1, otherwise this bit is held to 0. This bit is set to 1 when an Out Of Multiframe Alignment indication in register X+10H has been detected in the last one-second interval.
	1	PSLIP	**Transmit or Receive Slip One-second Error Indication:** Enabled when control bit SRGEN is a 1, otherwise this bit is held to 0. This bit is set to 1 when a slip indication in register X+10H has been detected in the last one-second interval.
	0	PSCHG	**Signaling Change of State One-second Error Indication:** Enabled when control bit SRGEN is a 1, otherwise this bit is held to 0. This bit is set to 1 when a signaling change of state indication in register X+10H has been detected in the last one-second interval.

Address (Hex)	Bit	Symbol	Description
X+13	7	FLOS	**Loss Of Signal Alarm Persistent One-second Error Indication:** Enabled when control bit SRGEN is a 1, otherwise this bit is held to 0. This bit is set to 1 when a loss of signal alarm indication is active, but did not become active in the last one-second interval.
	6	FAIS	**AIS Persistent One-second Error Indication:** Enabled when control bit SRGEN is a 1, otherwise this bit is held to 0. This bit is set to 1 for a one-second interval when an AIS alarm indication is active, but did not become active in the last one-second interval.
	5	FOOF	**Out Of Frame Persistent One-second Error Indication:** Enabled when control bit SRGEN is a 1, otherwise this bit is held to 0. This bit is set to 1 for a one-second interval when an out of frame alarm indication in register X+10H is active, but did not become active in the last one-second interval.
	4	FRAI	**RAI (Yellow) Alarm Persistent One-second Error Indication:** Enabled when control bit SRGEN is a 1, otherwise this bit is held to 0. This bit is set to 1 for a one-second interval when a RAI (Yellow) alarm indication in register X+10H is active, but did not become active in the last one-second interval.
	3	FCFA	**Change In Frame Alignment Persistent One-second Error Indication:** Enabled when control bit SRGEN is a 1, otherwise this bit is held to 0. This bit is set to 1 for a one-second interval when a change in frame alignment alarm indication in register X+10H is active, but did not become active in the last one-second interval.
	2	FOOFM	**Out Of Multiframe Alignment (OOFM) Persistent One-second Error Indication:** Enabled when control bit SRGEN is a 1, otherwise this bit is held to 0. This bit is set to 1 for a one-second interval if the OOFM alarm in register X+10H is active, but did not become active in the last one-second interval.
	1	FSLIP	**Transmit or Receive Slip Persistent One-second Error Indication:** Enabled when control bit SRGEN is a 1, otherwise this bit is held to 0. This bit is set to 1 for a one-second interval when a slip is active, but did not become active in the last one-second interval.
	0	FSCHG	**Transmit Slip Persistent One-second Error Indication:** Enabled when control bit SRGEN is a 1, otherwise this bit is held to 0. This bit is set to 1 for a one-second interval when a signaling change of state in register X+10H is active, but did not become active in the last one-second interval.

Address (Hex)	Bit	Symbol	Description
X+14	7	MLOS	**Loss Of Signal Alarm Indication Interrupt Mask Bit:** When set to 1, the latched loss of signal alarm indication is masked from providing a hardware interrupt.
	6	MAIS	**AIS Alarm Indication Interrupt Mask Bit:** When set to 1, the latched AIS alarm indication is masked from providing a hardware interrupt.
	5	MOOF	**Out Of Frame Alarm Indication Interrupt Mask Bit:** When set to 1, the latched out of frame alarm indication is masked from providing a hardware interrupt.
	4	MRAI	**RAI (Yellow) Alarm Indication Interrupt Mask Bit:** When set to 1, the latched RAI (Yellow) alarm indication is masked from providing a hardware interrupt.
	3	MCFA	**Change In Frame Alignment Indication Interrupt Mask Bit:** When set to 1, the latched change in frame alarm indication is masked from providing a hardware interrupt.
	2	MOOFM	**Out Of Multiframe Alignment (OOFM) Mask Bit:** When set to 1, detection of an out of multiframe alarm is masked from providing a hardware interrupt.
	1	MSLIP	**Transmit or Receive Slip Indication Interrupt Mask Bit:** When set to 1, a slip indication is masked from providing a hardware interrupt.
	0	MSCHG	**Signaling Change of State Indication Interrupt Mask Bit:** When set to 1, a change of signaling state indication is masked from providing a hardware interrupt.
X+164	7		**Reserved:** Write this bit to 0.
	6	AIS16	**TS16 AIS Alarm Indication:** This bit position is used to indicate an unlatched Time Slot 16 AIS indication. A 1 is true state. An AIS in Time Slot 16 is detected when the received time slot has detected three or less zeros in each of two consecutive multiframe periods. Recovery occurs when each of two consecutive multiframe periods contains four or more zeros or when the multiframe alignment signal has been detected.
	5	ECRCE	**Receive Excessive CRC-4 Alarm Error Indication:** A 1 indicates that 915 or more of the last 1000 CRC-4 received were in error. A 0 indicates that the number of CRC-4 errors was below this level.
	4	RAI16	**TS16 RAI (Yellow) Alarm Indication:** This bit position is used to indicate an unlatched Time Slot 16 RAI (Yellow) alarm condition from the distant end; a 1 in bit position 6 of the Time Slot 16 multiframe for frame 0 indicates the alarm; three occurrences in a row will set this alarm. A 1 is a true state.
	3		**Reserved:** Write this bit to 0.

Address (Hex)	Bit	Symbol	Description
X+164 (cont.)	2	OO16M	**Out Of TS16 Multiframe Alignment Alarm:** A 1 indicates that Time Slot 16 multiframe alignment has been lost. Control bit EOO16M bit 1 in register X+03H enables a Time Slot 16 multiframe alarm. A Time Slot 16 multiframe alarm may be caused by two or more consecutive frame 0 of Time Slot 16 with the first four bits not being 0000, Time Slot 16 is all zeros for 16 consecutive frames, or basic frame alignment is lost.
	1		**Reserved:** Write this bit to 0.
	0	AUXP	**Auxiliary Pattern Alarm Indication:** A 1 indicates that an unframed alternating binary “10” pattern has been received 254 or more times on lead RPOSn/RNEGn or lead RNRZn for 250 microseconds. A 0 indicates either that framing has been detected or that less than 254 unframed alternating binary “10” patterns have been detected for 250 microseconds. Control bit ENRXAUXP must be set to a 1 for this signal to be detected.
X+165	7		**Reserved:** Write this bit to 0.
	6	LAIS16	**Latched TS16 AIS Alarm Indication:** This bit position latches when there is a transition in the unlatched bit AIS16 in register X+164H. This bit is set on the transition set by the RISE and FALL bits in register 00BH. A 1 is true state. If not masked by the corresponding mask bit, the GIM bit in the global control register or corresponding global mask bit, an interrupt is generated. This bit is cleared by writing a 0 into this bit position or by the one-second pulse, if the shadow register feature is enabled (global control bit SRGEN set to a 1).
	5	LECRCE	**Latched Receive Excessive CRC-4 Error Indication:** This bit position latches when there is a transition in the unlatched bit ECRCE in register X+164H. This bit is set on the transition set by the RISE and FALL bits in register 00BH. A 1 is true state. If not masked by the corresponding mask bit, the GIM bit in the global control register or corresponding global mask bit, an interrupt is generated. This bit is cleared by writing a 0 into this bit position or by the one-second pulse, if the shadow register feature is enabled (global control bit SRGEN set to a 1).
	4	LRAI16	**Latched TS16 RAI (Yellow) Alarm Indication:** This bit position latches when there is a transition in the unlatched bit RAI16 in register X+164H. This bit is set on the transition set by the RISE and FALL bits in register 00BH. A 1 is true state. If not masked by the corresponding mask bit, the GIM bit in the global control register or corresponding global mask bit, an interrupt is generated. This bit is cleared by writing a 0 into this bit position or by the one-second pulse, if the shadow register feature is enabled (global control bit SRGEN set to a 1).
	3		**Reserved:** Write this bit to 0.

Address (Hex)	Bit	Symbol	Description
X+165 (cont.)	2	LOO16M	**Latched Out Of TS16 Multiframe Alignment Alarm:** This bit position latches when there is a transition in the unlatched bit OO16M in register X+164H. This bit is set on the transition set by the RISE and FALL bits in register 00BH. A 1 is true state. If not masked by the corresponding mask bit, the GIM bit in the global control register or corresponding global mask bit, an interrupt is generated. This bit is cleared by writing a 0 into this bit position or by the one-second pulse, if the shadow register feature is enabled (global control bit SRGEN set to a 1).
	1		**Reserved:** Write this bit to 0.
	0	LAUXP	**Latched Auxiliary Pattern Alarm Indication:** This bit position latches when there is a transition in the unlatched bit AUXP in register X+164H. This bit is set on the transition set by the RISE and FALL bits in register 00BH. A 1 is true state. If not masked by the corresponding mask bit, the GIM bit in the global control register or corresponding global mask bit, an interrupt is generated. This bit is cleared by writing a 0 into this bit position or by the one-second pulse, if the shadow register feature is enabled (global control bit SRGEN set to a 1).
X+166	7		**Reserved:** Write this bit to 0.
	6	MAIS16	**TS16 AIS Alarm Indication Interrupt Mask Bit:** When set to 1, the latched TS16 AIS alarm indication in register X+165H is masked from providing a hardware interrupt.
	5	MECRCE	**Receive Excessive CRC-4 Error Indication Interrupt Mask Bit:** When set to 1, the latched Received Excessive CRC-4 Error (LECRCE) alarm indication in register X+165H is masked from providing a hardware interrupt.
	4	MRAI16	**TS16 RAI (Yellow) Alarm Indication Interrupt Mask Bit:** When set to 1, the latched TS16 RAI (Yellow) alarm indication in register X+165H is masked from providing a hardware interrupt.
	3		**Reserved:** Write this bit to 0.
	2	MOO16M	**Out Of TS16 Multiframe Alignment (OO16M) Mask Bit:** When set to 1, the latched Out Of TS16 multiframe alarm indication in register X+165H is masked from providing a hardware interrupt.
	1		**Reserved:** Write this bit to 0.
	0	MAUXP	**Auxiliary Pattern Alarm Indication Interrupt Mask Bit:** When set to 1, the latched AUXP alarm indication in register X+165H is masked from providing a hardware interrupt.

Address (Hex)	Bit	Symbol	Description
X+167	7		**Reserved:** Write this bit to 0.
	6	PAIS16	**TS16 AIS One-second Error Indication:** Enabled when control bit SRGEN bit 3 in register 00BH is a 1, otherwise this bit is held to 0. This bit is set to 1 when an AIS alarm indication has been detected in the last one-second interval.
	5	PECRCE	**Excessive CRC-4 Error One-second Error Indication:** Enabled when control bit SRGEN is a 1, otherwise this bit is held to 0. This bit is set to 1 when an excessive CRC-4 error alarm indication has been detected in the last one-second interval.
	4	PRA16	**TS16 RAI (Yellow) Alarm One-second Error Indication:** Enabled when control bit SRGEN is a 1, otherwise this bit is held to 0. This bit is set to 1 when a TS16 RAI alarm indication has been detected in the last one-second interval.
	3		**Reserved:** Write this bit to 0.
	2	POO16M	**Out Of TS16 Multiframe Alignment (OO16M):** Enabled when control bit SRGEN is a 1, otherwise this bit is held to 0. This bit is set to 1 when an OO16M alarm indication has been detected in the last one-second interval.
	1		**Reserved:** Write this bit to 0.
	0	PAUXP	**Auxiliary Pattern Alarm:** Enabled when control bit SRGEN is a 1, otherwise this bit is held to 0. This bit is set to 1 when an AUXP alarm indication has been detected in the last one-second interval.
X+168	7		**Reserved:** Write this bit to 0.
	6	FAIS16	**TS16 AIS Persistent One-second Error Indication:** Enabled when control bit SRGEN is a 1, otherwise this bit is held to 0. This bit is set to 1 for a one-second interval when an TS16 AIS alarm indication is active, but did not become active in the last one-second interval.
	5	FECRCE	**Excessive CRC-4 Error Persistent One-second Error Indication:** Enabled when control bit SRGEN is a 1, otherwise this bit is held to 0. This bit is set to 1 for a one-second interval when an ECECE alarm indication is active, but did not become active in the last one-second interval.
	4	FRAI16	**TS16 RAI (Yellow) Alarm Persistent One-second Error Indication:** Enabled when control bit SRGEN is a 1, otherwise this bit is held to 0. This bit is set to 1 for a one-second interval when a TS16 RAI (Yellow) alarm indication is active, but did not become active in the last one-second interval.
	3		**Reserved:** Write this bit to 0.
	2	FOO16M	**Out Of TS16 Multiframe Alignment (OO16M) Persistent One-second Error Indication:** Enabled when control bit SRGEN is a 1, otherwise this bit is held to 0. This bit is set to 1 for a one-second interval when an OO16M alarm indication has been detected in the last one-second interval.
	1		**Reserved:** Write this bit to 0.

Address (Hex)	Bit	Symbol	Description
X+168 (cont.)	0	FAUXP	**Auxiliary Pattern Alarm Persistent One-second Error Indication:** Enabled when control bit SRGEN is a 1, otherwise this bit is held to 0. This bit is set to 1 for a one-second interval when an AUXP alarm indication is active, but did not become active in the last one-second interval.

Non-Interrupt Status Registers

These registers are read only except register X+19H which is a read to clear register. The status indications are not latched (except X+19H) and do not generate interrupts.

Address (Hex)	Bit	Symbol	Description
X+17	7-6		**Reserved:** Write these bits to 0.
	5	TABIT	**Transmit A-Bits Indication:** Enabled for the Transmission interface only. A 1 indicates that the transmit signaling highway A-bits are set to 1 (external AIS indication).
	4	TYBIT	**Transmit Y-Bit Indication:** Enabled for the Transmission interface only. A 1 indicates that the transmit signaling highway RAI, R-bit (bit 3 of Time Slot 0 odd frames on lead TTSIGn) is set to 1 (external RAI indication).
	3-2		**Reserved:** Write these bits to 0.
	1	RXSF	**Receive Signaling Freeze Indication:** A 1 indicates that the receive signaling bits in the signaling buffer are frozen due to loss of signal, out of frame, or the RXSFZ (bit 1) in register X+134H is a 1.
	0	TXSF	**Transmit Signaling Freeze Indication:** A 1 indicates that the transmit signaling bits in the signaling buffer are frozen due to the A-bits in the signaling highway for the transmission interface are 1, or the TXSFZ (bit 0) in register X+134H is a 1.
X+18	7	NCRC4	**Non-CRC-4 Interworking:** A 1 indicates that a CRC-4 to non-CRC-4 interworking has been established. When 0, this bit indicates that a CRC-4 interworking has been established. The status of this bit should be disregarded when control bit CRCA is 0.
	6-5		**Reserved:** Indeterminate value.
	4	TS16ME	**Time Slot 16 Multiframe Error.** A 1 indicates an error has occurred in the Time Slot 16 multiframe pattern (bits 1 - 4 normally equal to 0000). This alarm will persist for one Time Slot multiframe period. This bit is set to a 0 if the channel is out of Time Slot 16 multiframe (status bit OO16M set to a 1).
	3-0		**Reserved:** Indeterminate value.
X+19	7-0	SIGACT7-SIGACT0	**Signaling Activity:** This read to clear register holds signaling change status indicators. Each bit covers four channels. For example, SIGACT0 is set to a 1, if a signaling change of state has been detected for telephone channels 1, 2, 16 or 17. SIGACT1 covers channels 3, 4, 18 and 19. SIGACT7 covers channels 29 and 30 only.

Address (Hex)	Bit	Symbol	Description
X+175	7-6		**Reserved:** Write these bits to 0.
	5	S6X	**Sa6 Unknown Code:** A 1 indicates that the Sa6 code debounced for three sub multiframes is a code that does not correspond to any other code in this register. Control bit ENRXNBR (bit 3) in register X+03H must be set to a 1.
	4	S6F	**Sa6 F Code:** A 1 indicates that the Sa6 code debounced for three sub multiframes is a 1111 code. Control bit ENRXNBR (bit 3) in register X+03H must be set to a 1.
	3	S6E	**Sa6 E Code:** A 1 indicates that the Sa6 code debounced for three sub multiframes is a 1110 code. Control bit ENRXNBR (bit 3) in register X+03H must be set to a 1.
	2	S6C	**Sa6 C Code:** A 1 indicates that the Sa6 code debounced for three sub multiframes is a 1100 code. Control bit ENRXNBR (bit 3) in register X+03H must be set to a 1.
	1	S6A	**Sa6 A Code:** A 1 indicates that the Sa6 code debounced for three sub multiframes is a 1010 code. Control bit ENRXNBR (bit 3) in register X+03H must be set to a 1.
	0	S68	**Sa6 8 Code:** A 1 indicates that the Sa6 code debounced for three sub multiframes is a 1000 code. Control bit ENRXNBR (bit 3) in register X+03H must be set to a 1.

Transmit Sa4 - Sa8 Code Registers

The contents of these read/write registers may be sent in CRC-4 mode for the National bits.

Address (Hex)	Bit	Symbol	Description
X+169	7-0	XSA47-XSA40	**Transmit Sa4 Byte:** This register contains the Sa4 byte to be transmitted for the case where control bit TSA4S (bit 4) in register X+E3H is set to a 0 and control bit SA4 (bit 4) in register X+0CH is set to a 0. Bit number 7 is transmitted in frame 2 of the multiframe and bit 0 is transmitted in frame 16 of the multiframe.
X+16A	7-0	XSA57-XSA50	**Transmit Sa5 Byte:** This register contains the Sa5 byte to be transmitted for the case where control bit TSA5S (bit 3) in register X+E3H is set to a 0 and control bit SA5 (bit 3) in register X+0CH is set to a 0. Bit number 7 is transmitted in frame 2 of the multiframe and bit 0 is transmitted in frame 16 of the multiframe.
X+16B	7-0	XSA67-XSA60	**Transmit Sa6 Byte:** This register contains the Sa6 byte to be transmitted for the case where control bit TSA6S (bit 2) in register X+E3H is set to a 0 and control bit SA6 (bit 2) in register X+0CH is set to a 0. Bit number 7 is transmitted in frame 2 of the multiframe and bit 0 is transmitted in frame 16 of the multiframe.

Address (Hex)	Bit	Symbol	Description
X+16C	7-0	XSA77-XSA70	**Transmit Sa7 Byte:** This register contains the Sa7 byte to be transmitted for the case where control bit TSA7S (bit 1) in register X+E3H is set to a 0 and control bit SA7 (bit 1) in register X+0CH is set to a 0. Bit number 7 is transmitted in frame 2 of the multiframe and bit 0 is transmitted in frame 16 of the multiframe.
X+16D	7-0	XSA87-XSA80	**Transmit Sa8 Byte:** This register contains the Sa8 byte to be transmitted for the case where control bit TSA8S (bit 0) in register X+E3H is set to a 0 and control bit SA8 (bit 0) in register X+0CH is set to a 0. Bit number 7 is transmitted in frame 2 of the multiframe and bit 0 is transmitted in frame 16 of the multiframe.

Receive Sa4 - Sa8 Code Registers

These read only registers contain the most recently received 8 bits for each National bit synchronized to the Time Slot 0 multiframe. Control bit ENRXNBR (bit 3) in register X+03H must be set to a 1 for data to be loaded into these registers.

Address (Hex)	Bit	Symbol	Description
X+16F	7-0	RSA47-RSA40	**Receive Sa4 Byte:** This register contains the Sa4 byte received for the case where control bits CRCMD1 and CRCMD0 (bits 3 and 2) in register X+07H are set to X0 or 11 (CRC-4 operating modes). Bit number 7 is received in frame 2 of the multiframe and bit 0 is received in frame 16 of the multiframe.
X+170	7-0	RSA57-RSA50	**Receive Sa5 Byte:** This register contains the Sa5 byte received for the case where control bits CRCMD1 and CRCMD0 (bits 3 and 2) in register X+07H are set to X0 or 11 (CRC-4 operating modes). Bit number 7 is received in frame 2 of the multiframe and bit 0 is received in frame 16 of the multiframe.
X+171	7-0	RSA67-RSA60	**Receive Sa6 Byte:** This register contains the Sa6 byte received for the case where control bits CRCMD1 and CRCMD0 (bits 3 and 2) in register X+07H are set to X0 or 11 (CRC-4 operating modes). Bit number 7 is received in frame 2 of the multiframe and bit 0 is received in frame 16 of the multiframe. Sa6 has additional processing functions associated with it; see registers X+175H for Sa6 code detectors and registers X+177H through X+17EH for Sa6 error code counters.
X+172	7-0	RSA77-RSA70	**Receive Sa7 Byte:** This register contains the Sa7 byte received for the case where control bits CRCMD1 and CRCMD0 (bits 3 and 2) in register X+07H are set to X0 or 11 (CRC-4 operating modes). Bit number 7 is received in frame 2 of the multiframe and bit 0 is received in frame 16 of the multiframe.
X+173	7-0	RSA87-RSA80	**Receive Sa8 Byte:** This register contains the Sa8 byte received for the case where control bits CRCMD1 and CRCMD0 (bits 3 and 2) in register X+07H are set to X0 or 11 (CRC-4 operating modes). Bit number 7 is received in frame 2 of the multiframe and bit 0 is received in frame 16 of the multiframe.

Performance Counters and Counter Shadow Registers

The E1Fx8 provides performance counter and counter shadow read/write registers for E-bit errors, CRC-4 bit errors, coding violations, framing bit errors, Sa6 bit errors and out of lock indications from the PRBS Analyzer. The counter shadow registers provide the microprocessor with an error count for the previous one-second interval. A counter and the corresponding counter shadow register (and their overflow bits) are cleared when the microprocessor writes 0 to their bits. The rising edges of a one-second interval pulse also clears the counters (and the overflow bits, if set). The shadow registers for the various counters are also updated at one-second intervals by the selected one-second clock (see control bits S1SEXTB, S1SINT and S1YNC2-S1YNC0). Please note that when reading unlatched counters of greater than 8 bits, the counters must be read in two consecutive read operations with the even numbered register read first.

Address (Hex)	Bit	Symbol	Description
X+F0	7-0	LCRC7-LCRC0	**Latched CRC-4 Error Counter Shadow Register:** This register contains the lower 8 bits of the 10-bit shadow register assigned for holding the CRC-4 error count that occurred in the previous one-second interval. This location is updated from CRC7-CRC0 with a new count at one-second intervals on the rising edges of the one-second clock if control bit SRGEN is set to a 1. Bit 0 is the LSB of the 10-bit count.
X+F1	7	LCRCO	**Latched CRC-4 Error Counter Overflow Bit:** This bit contains the overflow indication associated with the 10-bit shadow register LCRC9-LCRC0 assigned for holding the CRC-4 error count that occurred in the previous one-second interval. This location is updated from CRCO at one-second intervals on the rising edges of the one-second clock if control bit SRGEN is set to a 1.
	6-2		**Reserved:** Write these bits to 0.
	1-0	LCRC9-LCRC8	**Latched CRC-4 Error Counter Shadow Register:** This register contains the upper two bits of the 10-bit shadow register assigned for holding the CRC-4 error count that occurred in the previous one-second interval. This location is updated from CRC9-CRC8 with a new count at one-second intervals on the rising edges of the one-second clock if control bit SRGEN is set to a 1. Bit 1 is the MSB of the 10-bit count.
X+F2	7-0	CRC7-CRC0	**CRC-4 Error Counter:** This register contains the lower 8 bits of the 10-bit CRC-4 error counter. This location is cleared at one-second intervals on the rising edges of the one-second clock if control bit SRGEN is set to a 1. Bit 0 is the LSB of the 10-bit count.
X+F3	7	CRCO	**CRC-4 Error Counter Overflow Bit:** This bit contains the overflow indication associated with the 10-bit CRC-4 counter CRC9-CRC0. This bit sets when the 10-bit counter overflows. It will remain set until the microprocessor writes a 0 into this location. This location is also cleared at one-second intervals on the rising edges of the one-second clock if control bit SRGEN is set to a 1.
	6-2		**Reserved:** Write these bits to 0.
	1-0	CRC9-CRC8	**CRC-4 Error Counter:** This register contains the upper 2 bits of the 10-bit CRC-4 error counter. This location is cleared at one-second intervals on the rising edges of the one-second clock if control bit SRGEN is set to a 1. Bit 1 is the MSB of the 10-bit count.

Address (Hex)	Bit	Symbol	Description
X+F4	7-0	LCV7-LCV0	**Latched Coding Violation Error Counter Shadow Register:** This register contains the lower 8 bits of the 16-bit shadow register assigned for holding the HDB3 coding violation count that occurred in the previous one-second interval. This location is updated from CV7-CV0 with a new count at one-second intervals on the rising edges of the one-second clock if control bit SRGEN is set to a 1. Bit 0 is the LSB of the 16-bit count.
X+F5	7-0	LCV15-LCV8	**Latched Coding Violation Error Counter Shadow Register:** This register contains the upper 8 bits of the 16-bit shadow register assigned for holding the HDB3 coding violation count that occurred in the previous one-second interval. This location is updated from CV15-CV8 with a new count at one-second intervals on the rising edges of the one-second clock if control bit SRGEN is set to a 1. Bit 7 is the MSB of the 16-bit count.
X+F6	7	LCVO	**Latched Coding Violation Error Counter Overflow Bit:** This bit contains the overflow indication associated with the 16-bit shadow register LCV15-LCV0 assigned for holding the Coding Violation count that occurred in the previous one-second interval. This location is updated from CVO at one-second intervals on the rising edges of the one-second clock if control bit SRGEN is set to a 1.
	6-0		**Reserved:** Write these bits to 0.
X+F7	7-0	CV7-CV0	**Coding Violation Counter:** This register contains the lower 8 bits of the 16-bit HDB3 coding violation counter. This location is cleared at one-second intervals on the rising edges of the one-second clock if control bit SRGEN is set to a 1. Bit 0 is the LSB of the 16-bit count.
X+F8	7-0	CV15-CV8	**Coding Violation Counter:** This register contains the upper 8 bits of the 16-bit HDB3 coding violation counter. This location is cleared at one-second intervals on the rising edges of the one-second clock if control bit SRGEN is set to a 1. Bit 7 is the MSB of the 16-bit count.
X+F9	7	CVO	**Coding Violation Counter Overflow Bit:** This bit contains the overflow indication associated with the 16-bit coding violation counter CV15-CV0. This bit sets when the 16-bit counter overflows. It will remain set until the microprocessor writes a 0 into this location. This location is also cleared at one-second intervals on the rising edges of the one-second clock if control bit SRGEN is set to a 1.
	6-0		**Reserved:** Write these bits to 0.
X+FA	7-0	LFBE7-LFBE0	**Latched Framing Word Error Counter Shadow Register:** This register contains 8 bit shadow register assigned for holding the framing word errors that occurred in the previous one-second interval. This location is updated from FBE7-FBE0 with a new count at one-second intervals on the rising edges of the one-second clock if control bit SRGEN is set to a 1. This counter may be used to determine BER thresholds for ITU-T G.732.

Address (Hex)	Bit	Symbol	Description
X+FB	7	LFBEO	**Latched Framing Bit Error Counter Overflow Bit:** This bit contains the overflow indication associated with the 8-bit shadow register LFBE7-LFBE0 assigned for holding the framing word error count that occurred in the previous one-second interval. This location is updated from FBEO at one-second intervals on the rising edges of the one-second clock if control bit SRGEN is set to a 1.
	6-0		**Reserved:** Write these bits to 0.
X+FC	7-0	FBE7-FBE0	**Framing Word Error Counter:** This register contains the 8 bit framing word error counter. A framing word error is counted as either an incorrect FAS pattern in Time Slot 0 (FAS frames) or bit 2 of Time Slot 0 (NFAS frames) not being a 1. This location is cleared at one-second intervals on the rising edges of the one-second clock if control bit SRGEN is set to a 1.
X+FD	7	FBEO	**Framing Bit Error Counter Overflow Bit:** This bit contains the overflow indication associated with the 8-bit framing bit error counter FBE7-FBE0. This bit sets when the 8-bit counter overflows. It will remain set until the microprocessor writes a 0 into this location. This location is also cleared at one-second intervals on the rising edges of the one-second clock if control bit SRGEN is set to a 1.
	6-0		**Reserved:** Write these bits to 0.
X+FE	7-0	LEBE7-LEBE0	**Latched E-Bit Error Counter Shadow Register:** This register contains the lower 8 bits of the 10-bit shadow register assigned for holding the E-bit error count that occurred in the previous one-second interval. This location is updated from EBE7-EBE0 with a new count at one-second intervals on the rising edges of the one-second clock if control bit SRGEN is set to a 1. Bit 0 is the LSB of the 10-bit count.
X+FF	7	LEBEO	**Latched E-Bit Error Counter Overflow Bit:** This bit contains the overflow indication associated with the 10-bit shadow register LEBE9-LEBE0 assigned for holding the E-bit error count that occurred in the previous one-second interval. This location is updated from EBEO at one-second intervals on the rising edges of the one-second clock if control bit SRGEN is set to a 1.
	6-2		**Reserved:** Write these bits to 0.
	1-0	LEBE9-LEBE8	**Latched E-Bit Error Counter Shadow Register:** This register contains the upper two bits of the 10-bit shadow register assigned for holding the E-bit error count that occurred in the previous one-second interval. This location is updated from EBE9-EBE8 with a new count at one-second intervals on the rising edges of the one-second clock if control bit SRGEN is set to a 1. Bit 1 is the MSB of the 10-bit count.
X+100	7-0	EBE7-EBE0	**E-Bit Error Counter:** This register contains the lower 8 bits of the 10-bit E-bit error counter; when the E1Fx8 framer is in multiframe alignment, each E-bit received as a 0 is counted in this counter. This location is cleared at one-second intervals between the rising and falling edges of the one-second clock if control bit SRGEN is set to a 1. Bit 0 is the LSB of the 10-bit count.

Address (Hex)	Bit	Symbol	Description
X+101	7	EBEO	**E-Bit Error Counter Overflow Bit:** This bit contains the overflow indication associated with the 10-bit E-bit counter EBE9-EBE0. This bit sets when the 10-bit counter overflows. It will remain set until the microprocessor writes a 0 into this location. This location is also cleared at one-second intervals on the rising edges of the one-second clock if control bit SRGEN is set to a 1.
	6-2		**Reserved:** Write these bits to 0.
	1-0	EBE9-EBE8	**E-Bit Error Counter:** This register contains the upper 2 bits of the 10-bit E-bit error counter; when the E1Fx8 framer is in multiframe alignment, each E-bit received as a 0 is counted in this counter. This location is cleared at one-second intervals on the rising edges of the one-second clock if control bit SRGEN is set to a 1. Bit 1 is the MSB of the 10-bit count.
X+157	7-0	LTESTP7-LTESTP0	**Latched Time Slot Test Pattern Out Of Lock Counter Shadow Register:** This register holds the lower 8 bits of the 15 bit register used for the out of lock indications.
X+158	7	LTSTPO	**Latched Time Slot Test Pattern Out Of Lock Counter Overflow Bit Shadow Register:** This register holds the overflow bit of the 15 bit register used for the out of lock indications.
	6-0	LTESTP14-LTESTP8	**Latched Time Slot Test Pattern Out Of Lock Counter Shadow Register:** This register holds the upper 7 bits of the 15 bit register used for the out of lock indications.
X+159	7-0	TESTP7-TESTP0	**Time Slot Test Pattern Out Of Lock Counter:** This register holds the lower 8 bits of the 15 bit register used for the out of lock indications from the PRBS/ Code Word Analyzer.
X+15A	7	TESTPO	**Time Slot Test Pattern Out Of Lock Counter Overflow Bit:** This register holds the overflow bit of the 15 bit register used for the out of lock indications.
	6-0	TESTP14-TESTP8	**Time Slot Test Pattern Out Of Lock Counter:** This register holds the upper 7 bits of the 15 bit register used for the out of lock indications from the PRBS/ Code Word Analyzer.
X+177	7-0	LSA617-LSA610	**Latched Sa6-Bit Error Counter #1 Shadow Register:** This register contains the lower 8 bits of the 10-bit shadow register assigned for holding the Sa6-bit error count that occurred in the previous one-second interval. This location is updated from SA617-SA610 in register X+179H with a new count at one-second intervals on the rising edges of the one-second clock if control bit SRGEN is set to a 1. Bit 0 is the LSB of the 10-bit count.

Address (Hex)	Bit	Symbol	Description
X+178	7	LSA61O	**Latched Sa6-Bit Error Counter #1 Overflow Bit:** This bit contains the overflow indication associated with the 10-bit shadow register LSA619-LSA610 assigned for holding the Sa6 error count that occurred in the previous one-second interval. This location is updated from SA61O at one-second intervals on the rising edges of the one-second clock if control bit SRGEN is set to a 1.
	6-2		**Reserved:** Write these bits to 0.
	1-0	LSA619-LSA618	**Latched Sa6-Bit Error Counter #1 Shadow Register:** This register contains the upper two bits of the 10-bit shadow register assigned for holding the Sa6-bit error count that occurred in the previous one-second interval. This location is updated from SA619 and SA618 with a new count at one-second intervals on the rising edges of the one-second clock if control bit SRGEN is set to a 1. Bit 1 is the MSB of the 10-bit count.
X+179	7-0	SA617-SA610	**Sa6-Bit Error Counter #1:** This register contains the lower 8 bits of the 10-bit Sa6 error counter that counts alarms from Terminal Equipment; Sa6 codes of 0001 or 0011 in every received sub multiframe are counted in this counter if control bit ENRXNBR is set to a 1. This location is cleared at one-second intervals between the rising and falling edges of the one-second clock if control bit SRGEN is set to a 1. Bit 0 is the LSB of the 10-bit count.
X+17A	7	SA61O	**Sa6-Bit Error Counter #1 Overflow Bit:** This bit contains the overflow indication associated with the 10-bit Sa6 bit error counter SA619-SA610. This bit sets when the 10-bit counter overflows. It will remain set until the microprocessor writes a 0 into this location. This location is also cleared at one-second intervals on the rising edges of the one-second clock if control bit SRGEN is set to a 1.
	6-2		**Reserved:** Write these bits to 0.
	1-0	SA619-SA618	**Sa6-Bit Error Counter #1:** This register contains the upper 2 bits of the 10-bit Sa6 error counter that counts alarms from Terminal Equipment; Sa6 codes of 0001 or 0011 in every received sub multiframe are counted in this counter if control bit ENRXNBR is set to a 1. This location is cleared at one-second intervals on the rising edges of the one-second clock if control bit SRGEN is set to a 1. Bit 1 is the MSB of the 10-bit count.
X+17B	7-0	LSA627-LSA620	**Latched Sa6-Bit Error Counter #2 Shadow Register:** This register contains the lower 8 bits of the 10-bit shadow register assigned for holding the Sa6-bit error count that occurred in the previous one-second interval. This location is updated from SA627 - SA620 with a new count at one-second intervals on the rising edges of the one-second clock if control bit SRGEN is set to a 1. Bit 0 is the LSB of the 10-bit count.

Address (Hex)	Bit	Symbol	Description
X+17C	7	LSA62O	**Latched Sa6-Bit Error Counter #2 Overflow Bit:** This bit contains the overflow indication associated with the 10-bit shadow register LSA629-LSA620 assigned for holding the Sa6 error count that occurred in the previous one-second interval. This location is updated from SA62O at one-second intervals on the rising edges of the one-second clock if control bit SRGEN is set to a 1.
	6-2		**Reserved:** Write these bits to 0.
	1-0	LSA629-LSA628	**Latched Sa6-Bit Error Counter #2 Shadow Register:** This register contains the upper two bits of the 10-bit shadow register assigned for holding the Sa6-bit error count that occurred in the previous one-second interval. This location is updated from SA629 and SA628 with a new count at one-second intervals on the rising edges of the one-second clock if control bit SRGEN is set to a 1. Bit 1 is the MSB of the 10-bit count.
X+17D	7-0	SA627-SA620	**Sa6-Bit Error Counter #2:** This register contains the lower 8 bits of the 10-bit Sa6 error counter that counts alarms from the T Reference Point; Sa6 codes of 0010 or 0011 in every received sub multiframe are counted in this counter if control bit ENRXNBR is set to a 1. This location is cleared at one-second intervals between the rising and falling edges of the one-second clock if control bit SRGEN is set to a 1. Bit 0 is the LSB of the 10-bit count.
X+17E	7	SA62O	**Sa6-Bit Error Counter #2 Overflow Bit:** This bit contains the overflow indication associated with the 10-bit Sa6 bit error counter SA629-SA620. This bit sets when the 10-bit counter overflows. It will remain set until the microprocessor writes a 0 into this location. This location is also cleared at one-second intervals on the rising edges of the one-second clock if control bit SRGEN is set to a 1.
	6-2		**Reserved:** Write these bits to 0.
	1-0	SA629-SA628	**Sa6-Bit Error Counter #2:** This register contains the upper 2 bits of the 10-bit Sa6 error counter that counts alarms from the T Reference Point; Sa6 codes of 0010 or 0011 in every received sub multiframe are counted in this counter if control bit ENRXNBR is set to a 1. This location is cleared at one-second intervals on the rising edges of the one-second clock if control bit SRGEN is set to a 1. Bit 1 is the MSB of the 10-bit count.

Test Generation Registers

These read/write registers control error insertion, PRBS generator/analyzer at the E1 level and loopback at the E1 level.

Address (Hex)	Bit	Symbol	Description
X+106	7	CRCE	**Generate a CRC-4 Error:** This feature is enabled when control bits CRCMD1 and CRCMD0 are equal to X0, or 11 (i.e., this enables the CRC-4 feature). When CRCE is set to 1, the CRC-4 bits in Time Slot 0 are transmitted in the inverted state once. To send another CRC-4 error, this bit must be first written with a 0, and then a 1.
	6	FRME	**Transmit Framing Error:** When set to a 1, a single FAS framing word including the International bit is transmitted inverted for one frame. The microprocessor must write a 0 into this bit position before another framing error can be transmitted.
	5	BPVE	**Transmit Bipolar Violation Error:** When the rail interface is selected, a 1 causes a single BPV error to be sent. The microprocessor must write a 0 into this bit position before another BPV error can be transmitted.
	4	NFASE	**Transmit NFAS Error:** When set to a 1, bit 2 in Time Slot 0 for a non frame alignment frame (NFAS) is sent as a 0 for a single frame. The microprocessor must write a 0 into this bit position before another NFAS framing error can be transmitted.
	3-2		**Reserved:** Write these bits to 0.
	1	PRBRE	**PRBS Receiver Enable:** When this bit is set to 1, the internal PRBS Analyzer is enabled for analyzing a PRBS pattern present at the output of the AMI/HDB3 Decoder. Control bits TPRN2- 0 (bits 4-2) in register X+109H determine the pattern expected and control bit RTFM (bit 7) in register X+01H when set to 1 enables the PRBS Analyzer to search over all of the bits including Time Slot 0. If RTFM is set to a 0, Time Slot 0 is considered as don't care. The PRBS Analyzer provides an output to status bit TPLOL (bit 5) in register X+129H as well as counter TESTP0-TESTP14 in registers X+159H and X+15AH. Control bit SPRBRE (bit 1) in register X+107H must be set to a 0.
	0	INPRBS	**Insert PRBS:** When set to 1, PRBS is inserted in place of the data from the transmit data highway. Control bit TTFM (bit 6) in register X+01H when set to a 0 causes Time Slot 0 to overwrite the pattern. Control bit SINSPRBS (bit 0) in register X+107H must be set to a 0.

<table>
<tr><th>Address (Hex)</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td rowspan="8">X+107</td><td>7</td><td>LLP</td><td>Local Loopback Enable: A 1 enables the loopback feature. Transmit data, after the codec is looped back as received data. When control bit TXLAIS is a 1, AIS is transmitted in place of test data.</td></tr>
<tr><td>6</td><td>TXLAIS</td><td>Transmit AIS in Local Loopback: When set to a 1, AIS is transmitted on the line only while local loopback is enabled (control bit LLP is set to a 1) When set to a 0 the signal being looped back is also sent to the line.</td></tr>
<tr><td>5</td><td>RLP</td><td>Remote Line Loopback Enable: A 1 enables the remote line loopback feature. Receive line data prior to the codec but after the dejitter buffer is looped back as the transmit line data. When both LLP and RLP are set to a 1, a bidirectional loopback is enabled; the dejitter buffer is not included in the bidirectional loopback (where X=don’t care).
<table>
<tr><th>BYPASS</th><th>LLP</th><th>RLP</th><th>Loopback</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>None without dejitter buffer in RX path</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>None with dejitter buffer in RX path</td></tr>
<tr><td>X</td><td>1</td><td>0</td><td>Local without dejitter buffer</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Remote without dejitter buffer in RX path</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Remote with dejitter buffer in RX path</td></tr>
<tr><td>X</td><td>1</td><td>1</td><td>Bi-directional without dejitter buffer</td></tr>
</table></td></tr>
<tr><td>4</td><td>PLP</td><td>Payload Loopback Enable: A 1 enables the payload loopback feature. The receive System data stream is looped back as the transmit data stream. The transmit framing pattern is not overwritten by the received signal. The relationship between a received time slot and the received Time Slot 0 is not maintained (either time slot number or bit position) when the payload is looped back.</td></tr>
<tr><td>3-2</td><td></td><td>Reserved: Write these bits to 0.</td></tr>
<tr><td>1</td><td>SPRBRE</td><td>System side PRBS Receiver Enable: When this bit is set to 1, the internal PRBS Analyzer is enabled for analyzing a PRBS pattern present at the input of the Transmit Slip Buffer. Control bits TPRN2- 0 (bits 4-2) in register X+109H determine the pattern expected. The PRBS Analyzer provides an output to status bit TPLOL (bit 5) in register X+129H as well as counter TESTP0 -14 in registers X+159H and X+15AH. Control bit PRBRE (bit 1) in register X+106H must be set to a 0.</td></tr>
<tr><td>0</td><td>SINPRBS</td><td>System side PRBS Insertion: When set to 1, PRBS is inserted in place of the data to the receive data highway. Control bit INSPRBS (bit 0) in register X+106H must be set to a 0.</td></tr>
</table>

Time Slot/DS0 Loopback, Test Pattern Status and DPLL Status Registers

These registers provide the status and control for the DS0 loopback activate and deactivate sequences as well as providing the N x DS0 PRBS and DPLL status. Register X+129H is read-only, the rest are read/write.

Address (Hex)	Bit	Symbol	Description
X+129	7	DS0ACT	**DS0 Receive Remote Loopback Activation Request:** An unlatched indication that indicates that the DS0 receive remote loopback activation request has been received on the time slots defined by control bits TSLL32-TSLL1 in registers X+12DH, X+12EH, X+12FH and X+130H when control bit TSRLOP (bit 7 in register X+109H) is set to a 0 and control bit RLPEN (bit 0 in register X+109H) is set to a 1. The activation request signal is a 2^7-1 PRBS pattern applied for 2 seconds followed by 2 seconds of all ones as defined in ANSI T1.403-1998.
	6	DS0DCT	**DS0 Receive Remote Loopback Deactivation Request:** An unlatched indication that indicates that the DS0 receive remote loopback deactivation request has been received on the time slots defined by control bits TSLL32-TSLL1 in registers X+12DH, X+12EH, X+12FH and X+130H when control bit TSRLOP (bit 7 in register X+109H) is set to a 0 and control bit RLPEN (bit 0 in register X+109H) is set to a 1. The deactivation request signal is a 2^7-1 PRBS pattern inverted applied for 2 seconds followed by 2 seconds of all ones as defined in ANSI T1.403-1998.
	5	TPLOL	**Receive Out Of Lock Indication:** An unlatched indication that indicates that the time slot or E1 PRBS test pattern out of lock occurred or a mismatch has occurred against the microprocessor written DS0 code word value. For this indication to be valid, the received signal and analyzer must be in the same mode (framed or unframed). The status of the out of lock indication for the PRBS analyzer is checked on a bit-by-bit basis when set for a PRBS pattern. A code word is checked on a byte-by-byte basis and is assumed to be contiguous. Control bits TPRN2, TPRN1 and TPRN0 (bits 4, 3 and 2 in register X+109H) determine the pattern to be detected. For code words, the pattern is held in registers X+15BH through X+15EH; Control bits RTPAE or SRTPAE (bit 2 and 0 in register X+131H) must be set to a 1 to enable the analyzer for Nx time slot analysis, while control bit PRBRE or SPRBRE (bits 1 in registers X+106H or X+107H) must be set to a 1 for E1 analysis.
	4	DS0TXC	**DS0 Transmit Remote Loopback Activation or Deactivation Request completed:** An unlatched indication that indicates that the DS0 transmit remote loopback activation/deactivation request of four-second duration has been completely transmitted. Control bit TRDSLP (bit 5 in register X+109H) is set to 1 to send the entire sequence of 2 seconds of the PRBS pattern followed by 2 seconds of all ones on the time slots selected by TSRL32-TSRL1 in registers X+10DH, X+10CH, X+10BH and X+10AH and enabled by TSRLOP (bit 7 in register X+109H) set to a 1. Control bit DS0DA (bit 6 in register X+109H) set to 0 selects an Activation Request or set to 1 selects a Deactivation Request.

Address (Hex)	Bit	Symbol	Description
X+129 (cont.)	3	INTACT	**Intermediate Indication for DS0 Receive Remote Loopback Activate Request:** A 1 in this bit position indicates that the DS0 loopback code activate PRBS pattern (2^7-1) has been detected for n frames where control bits SRTT7-SRTT0 in register X+12CH determine the value n and when the fraction being monitored is determined by control bits TSLL32-TSLL1 in registers X+130H, X+12FH, X+12EH, and X+12DH. Control bit TSRLOP (bit 7 in register X+109H) must be set to a 0 and control bit RLPEN (bit 0 in register X+109H) must be set to a 1 for detection to take place.
	2	INTDCT	**Intermediate Indication for DS0 Receive Remote Loopback Deactivate Request:** A 1 in this bit position indicates that the DS0 loopback code deactivate PRBS pattern (2^7-1 inverted) has been detected for n frames where control bits SRTT7- SRTT0 in register X+12CH determine the value n and when the fraction being monitored is determined by control bits TSLL32-TSLL1 in registers X+130H, X+12FH, X+12EH, and X+12DH. Control bit TSRLOP (bit 7 in register X+109H) must be set to a 0 and control bit RLPEN (bit 0 in register X+109H) must be set to a 1 for detection to take place.
	1	OVERF	**DPLL FIFO Overflow Indication:** This bit position indicates when a specific framer has detected a DPLL FIFO overflow. This bit position is cleared when the corresponding framer indication is cleared
	0	UNDERF	**DPLL FIFO Underflow Indication:** This bit position indicates when a specific framer has detected a DPLL FIFO underflow. This bit position is cleared when the corresponding framer indication is cleared
X+12A	7	LDS0ACT	**Latched DS0 Receive Remote Loopback Activation Request:** A latched indication that indicates that the DS0 receive remote loopback activation request was received. This bit is set only on the positive transition of status bit DS0ACT (bit 7) in register X+129.
	6	LDS0DCT	**Latched DS0 Receive Remote Loopback Deactivation Request:** A latched indication that indicates that the DS0 receive remote loopback deactivation request was received. This bit is set only on the positive transition of status bit DS0DCT (bit 6) in register X+129.
	5	LTPLOL	**Latched Receive Out Of Lock Indication.** A latched indication that indicates that the time slot or E1 PRBS test pattern out of lock occurred or a mismatch has occurred against the microprocessor written code word value. This bit is set only on the positive transition of status bit TPLOL (bit 5) in register X+129.
	4	LDS0TXC	**Latched DS0 Transmit Remote Loopback Activation or Deactivation Request Completed:** A latched indication that indicates that the DS0 transmit remote loopback activation/deactivation request has been transmitted. This bit is set only on the positive transition of status bit DS0TXC (bit 4) in register X+129.
	3	LINTACT	**Latched Intermediate Indication for DS0 Receive Remote Loopback Activate Request:** A latched indication that indicates that the intermediate DS0 receive remote loopback activate PRBS pattern has been received. This bit is set only on the positive transition of status bit INTACT (bit 3) in register X+129.

Address (Hex)	Bit	Symbol	Description
X+12A (cont.)	2	LINTDCT	**Latched Intermediate Indication for DS0 Receive Remote Loopback Deactivate Request:** A latched indication that indicates that the intermediate DS0 receive remote loopback deactivate PRBS pattern has been received. This bit is set only on the positive transition of status bit INTDCT (bit 2) in register X+129.
	1	LOVERF	**Latched DPLL FIFO Overflow Indication:** This bit position latches when there is a transition in the unlatched bit OVERF in register X+129H. A 1 is true state. If not masked by the corresponding mask bit or the GIM bit, an interrupt is generated. This bit is cleared by writing a 0 into this bit position. This bit is set only on the positive transition of status bit OVERF (bit 1) in register X+129.
	0	LUNDERF	**Latched DPLL FIFO Underflow Indication:** This bit position latches when there is a transition in the unlatched bit UNDERF in register X+129H. A 1 is true state. If not masked by the corresponding mask bit or the GIM bit, an interrupt is generated. This bit is cleared by writing a 0 into this bit position.This bit is set only on the positive transition of status bit UNDERF (bit 0) in register X+129.
X+12B	7	MDACT	**Mask DS0 Receive Remote Loopback Activation Request Indication:** A 1 will mask a remote loopback activation request from generating an interrupt indication.
	6	MDDCT	**Mask DS0 Receive Remote Loopback Deactivation Request Indication:** A 1 will mask a remote loopback deactivation request from generating an interrupt indication.
	5	MTPLOL	**Mask Receive Out Of Lock Indication:** A 1 will mask a DS0 test pattern out of lock from generating an interrupt indication.
	4	MDS0TXC	**Mask DS0 Transmit Remote Loopback Activation/ Deactivation Request Completed Indication:** A 1 will mask the transmit remote loopback activation/deactivation request completed indication from generating an interrupt indication.
	3	MINTACT	**Mask Intermediate Indication for DS0 Receive Remote Loopback Activate Request:** A 1 will mask a remote loopback activate PRBS pattern from generating an interrupt indication.
	2	MINTDCT	**Mask Intermediate Indication for DS0 Receive Remote Loopback Deactivate Request:** A 1 will mask a remote loopback deactivate PRBS pattern from generating an interrupt indication.
	1	MOVERF	**Mask DPLL FIFO Overflow Indication:** A 1 will mask a DPLL FIFO overflow from generating an interrupt indication.
	0	MUNDERF	**Mask DPLL FIFO Underflow Indication:** A 1 will mask a DPLL FIFO underflow from generating an interrupt indication.

Time Slot/DS0 Test Pattern Control Registers

These registers provide the status and control for the DS0 loopback activate and deactivate sequences as well as providing the N x Time Slot controls and PRBS controls. These registers are read/write.

Address (Hex)	Bit	Symbol	Description
X+109	7	TSRLOP	**Time Slot Remote Loopback Enable:** A 1 enables the ANSI Remote DS0 loopback feature, and also enables the time slot mode in the PRBS generator. The local loopback control bits are now used for sending the remote loopback sequence for the designated time slots. A 0 enables a remote time slot loopback as determined by control bits TSRL32-TSRL1 in registers X+10AH through X+10DH.
	6	DS0DA	**DS0 Remote Loopback Activation Request:** A 1 sets the DS0 remote loopback sequence generator for transmitting the four-second long DS0 remote loopback deactivation request. A 0 sets the DS0 remote loopback sequence generator for transmitting the four-second long DS0 remote loopback activation request. See ANSI T1.403-1998 for the specific pattern.
	5	TRDSLP	**Transmit DS0 Remote Loopback Activation or Deactivation Request:** A 1 written to this bit position causes a DS0 deactivation sequence to be transmitted when control bit DS0DA in this register is a 1 or an activation sequence to be transmitted when control bit DS0DA is a 0. The DS0 channel in which the sequence is to be transmitted is determined by control bits TSRL32-TSRL1in registers X+10AH through X+10DH. To send another sequence this bit must be first written with a 0, followed by a 1.
	4-2	TPRN2-TPRN0	**Time Slot Test Pattern Selection:** The Time Slot test pattern is selected according to the following table (where X=don't care). **TPRN2 TPRN1 TPRN0 Action** X 0 0 Not Used 0 0 1 2^{20}-1 (QRSS) 0 1 0 2^{15}-1 1 0 1 2^{11}-1 1 1 0 2^{23}-1 X 1 1 Register test word
	1	TSLLP	**Time Slot Local Loopback Enable:** A 1 enables the time slot local loopback feature and the time slots selected for local loopback are determined by control bits TSLL32-TSLL1.
	0	RLPEN	**Receive DS0 Remote Loopback Detection Enabled:** A 1 enables the DS0 remote loopback detector for detecting the activate and deactivate sequence.
X+10A	7-0	TSRL8-TSRL1	**Time Slot 7 to 0 Remote Loopback Control:** A 1 written to one or more control bits in this register causes the designated time slots to be remotely looped back, transmitted with the payload, or a selected test pattern. Control bit TDEn in register X+E4H corresponding to the time slot to be looped back must be set to a 1 even if control bit TXSBE (bit 5) in register X+11CH is set to a 0. For framing enabled (TTFM control bit in register X+01H not equal to 1), Time Slot 0 is not looped back.

Address (Hex)	Bit	Symbol	Description
X+10B	7-0	TSRL16-TSRL9	**Time Slot 15 to 8 Remote Loopback Control:** A 1 written to one or more control bits in this register causes the designated time slots to be remotely looped back, transmitted with the payload, or a selected test pattern. Control bit TDEn in register X+E5H corresponding to the time slot to be looped back must be set to a 1 even if control bit TXSBE (bit 5) in register X+11CH is set to a 0. For signaling enabled (TYP1, TYP0 control bits in register X+134H not equal to 00), Time Slot 16 is not looped back.
X+10C	7-0	TSRL24-TSRL17	**Time Slot 23 to 16 Remote Loopback Control:** A 1 written to one or more control bits in this register causes the designated time slots to be remotely looped back, transmitted with the payload, or a selected test pattern. Control bit TDEn in register X+E6H corresponding to the time slot to be looped back must be set to a 1 even if control bit TXSBE (bit 5) in register X+11CH is set to a 0.
X+10D	7-0	TSRL32-TSRL25	**Time Slot 31 to 24 Remote Loopback Control:** A 1 written to one or more control bits in this register causes the designated time slots to be remotely looped back, transmitted with the payload, or a selected test pattern. Control bit TDEn in register X+E7H corresponding to the time slot to be looped back must be set to a 1 even if control bit TXSBE (bit 5) in register X+11CH is set to a 0.
X+12C	7 - 0	SRTT7-SRTT0	**Select Frame Count for Receive Activation and Deactivation Indication:** The value written into this register determines the number of frames after lock is acquired before the activation or deactivation indication is acceptable. Value must be non zero.
X+12D	7-0	TSLL8-TSLL1	**Time Slot 7 to 0 Local Loopback Control:** A 1 written to one or more control bits in this register causes the designated time slots to be locally looped back, transmitted with the payload, or a selected test pattern. Control bit TDEn in register X+E4H corresponding to the time slot to be looped back must be set to a 1 even if control bit TXSBE (bit 5) in register X+11CH is set to a 0.
X+12E	7-0	TSLL16-TSLL9	**Time Slot 15 to 8 Local Loopback Control:** A 1 written to one or more control bits in this register causes the designated time slots to be locally looped back, transmitted with the payload, or a selected test pattern. Control bit TDEn in register X+E5H corresponding to the time slot to be looped back must be set to a 1 even if control bit TXSBE (bit 5) in register X+11CH is set to a 0.
X+12F	7-0	TSLL24-TSLL17	**Time Slot 23 to 16 Local Loopback Control:** A 1 written to one or more control bits in this register causes the designated time slots to be locally looped back, transmitted with the payload, or a selected test pattern. Control bit TDEn in register X+E6H corresponding to the time slot to be looped back must be set to a 1 even if control bit TXSBE (bit 5) in register X+11CH is set to a 0.
X+130	7-0	TSLL32-TSLL25	**Time Slot 31 to 24 Local Loopback Control:** A 1 written to one or more control bits in this register causes the designated time slots to be locally looped back, transmitted with the payload, or a selected test pattern. Control bit TDEn in register X+E7H corresponding to the time slot to be looped back must be set to a 1 even if control bit TXSBE (bit 5) in register X+11CH is set to a 0.

Address (Hex)	Bit	Symbol	Description
X+131	7-4		**Reserved:** Write these bits to 0.
	3	SPRN	**Send Time Slot Test Pattern:** A 1 sends the test pattern selected by control bits TPRN2, TPRN1 and TPRN0, for the time slots selected by control bits TSRLn.
	2	RTPAE	**Receive Test Pattern Detector Enabled:** A 1 enables the time slot test pattern detector. The time slots analyzed are selected by control bits TSLL32-TSLL1 in registers X+12DH through X+130H and the pattern searched for is selected by control bits TPRN2 - TPRN0 in this register. The out of lock indication is given in status bit TPLOL (bit 5 in register X+129H) with a latched value in bit LTPLOL (bit 5 in register X+12AH). Out of locks are counted as TESTP14 - TESTP0 with overflow bit TESTPO in registers X+159H and X+15AH. Shadow registers LTEST14 - LTEST0 with overflow bit LTESTO are provided in X+157H and X+158H.
	1	SSPRN	**Send System Side Time Slot Test Pattern:** A 1 sends the test pattern selected by control bits TPRN2, TPRN1 and TPRN0, for the channels selected by control bits TSLLn.
	0	SRTPAE	**System Side Receive Test Pattern Detector Enabled:** A 1 enables the time slot test pattern detector. The time slots analyzed are selected by control bits TSRL32- TSRL1 in registers X+10AH through X+10DH and the pattern searched for is selected by control bits TPRN2-TPRN0 in this register. The out of lock indication is given in status bit TPLOL (bit 5 in register X+129H) with a latched value in bit LTPLOL (bit 5 in register X+12AH). Out of locks are counted as TESTP14-TESTP0 with overflow bit TESTPO in registers X+159H and X+15AH. Shadow registers LTEST14-LTEST0 with overflow bit LTESTO are provided in X+157H and X+158H.
X+15B	7-0	Test Word Byte 1	**Time Slot Test Word Register Byte 1:** This register is used for sending a microprocessor test pattern when control bits TPRN1 and TPRN0 are equal to 11. This word is transmitted first. Bit 7 is transmitted first.
X+15C	7-0	Test Word Byte 2	**Time Slot Test Word Register Byte 2:** This register is used for sending a microprocessor test pattern when control bits TPRN1 and TPRN0 are equal to 11. This word is transmitted second. Bit 7 is transmitted first.
X+15D	7-0	Test Word Byte 3	**Time Slot Test Word Register Byte 3:** This register is used for sending a microprocessor test pattern when control bits TPRN1 and TPRN0 are equal to 11. This word is transmitted third. Bit 7 is transmitted first.
X+15E	7-0	Test Word Byte 4	**Time Slot Test Word Register Byte 4:** This register is used for sending a microprocessor test pattern when control bits TPRN1 and TPRN0 are equal to 11. This word is transmitted forth. Bit 7 is transmitted first.

Test Registers

Address (Hex)	Bit	Symbol	Description
X+1FF	7-3		**Reserved:** Write these bits to 0.
	2	OBLOL	**Observe Out Of Lock:** This bit is for testing purposes and must be set to 0 for normal operation. When set to 1, status bit TPLOL is substituted for the normal signal on lead RTAUXn. with a high indicating out of lock.
	1	RXFS	**Receive Fast Sync Enable:** This bit used for testing purposes and for externally synchronizing the framer. It must be a 0 for normal framing detection. If control bit RAIL (bit 7 in register X+00H) is set to 0, control bit EXLOS (bit 3 in register X+00H) is set to a 1, and this bit is set to a 1, a positive, single RCLKn clock cycle wide pulse on lead RSCANn will force the framer to interpret the next bit as the first bit of a multiframe.
	0		**Reserved:** Write this bit to 0.

APPLICATION DIAGRAMS

The E1Fx8 can be used in a wide range of telecommunication and data communication applications:

- Internet access equipment with E1 and fractional E1 ports
- DCS, digital central office or remote digital terminals (exchange terminations and access nodes)
- SDH terminal or add/drop multiplexers supporting E1 byte-synchronous operation or E1monitoring with G.706 annex C

The following diagram illustrates typical applications using the E1Fx8.

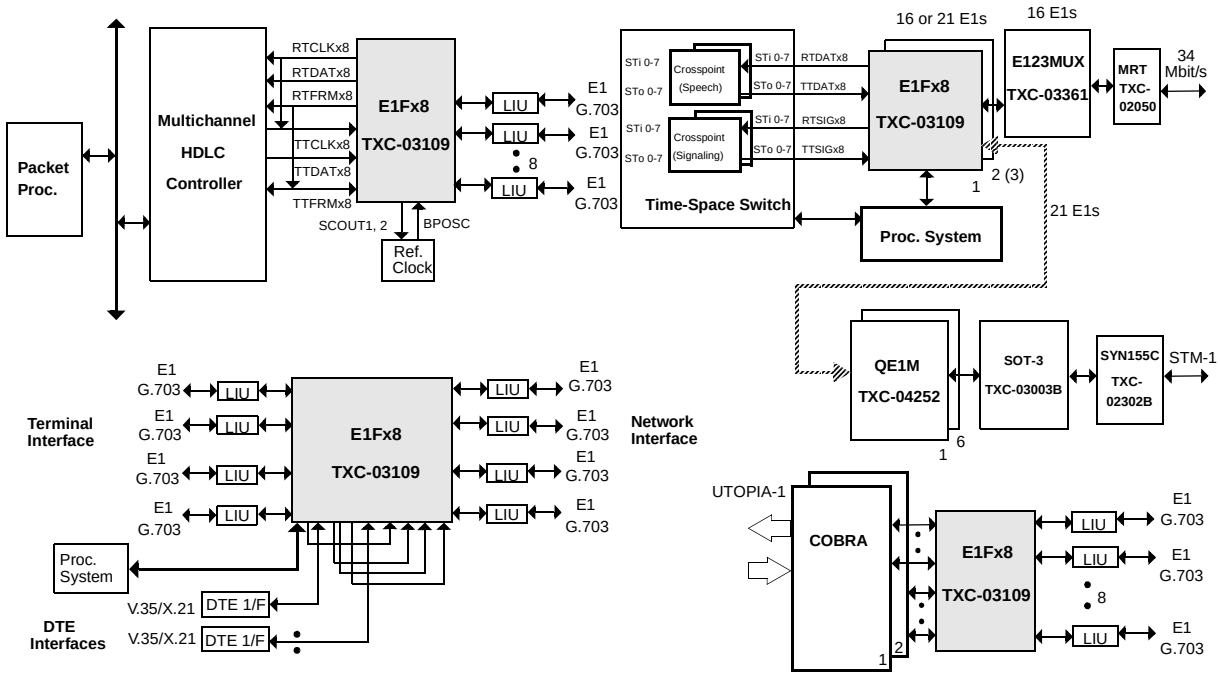
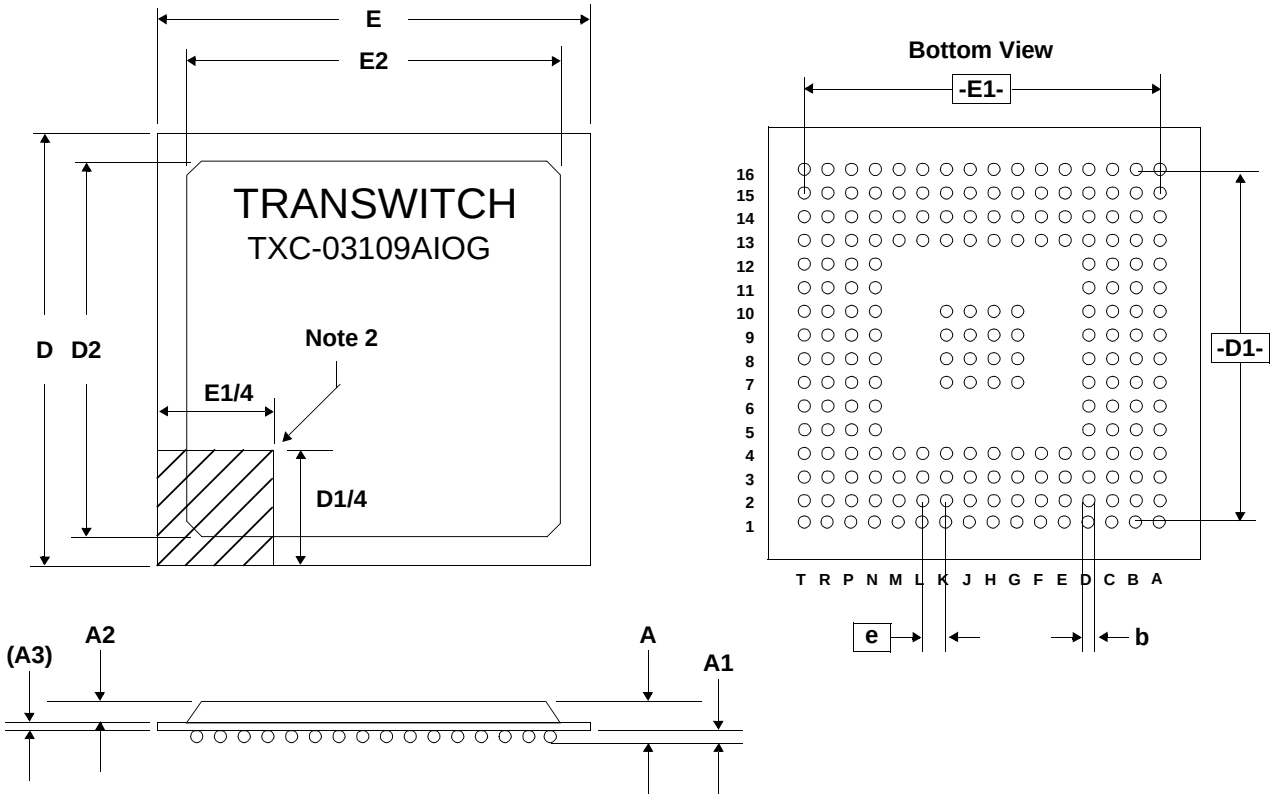


Figure 66. Typical Applications using the E1Fx8

The application diagram in Figure 66 shows four different uses for the E1Fx8. For a frame relay application the E1Fx8 is connected to a multi-channel HDLC controller. The E1Fx8 is also shown above being used as an SDH/STM-1 add/drop async multiplexer application, quad fractional E1 CSU/DSU application and ATM switch UNI or IMA application.

PACKAGE INFORMATION

The E1Fx8 device is available in two package formats. One is a 208-lead plastic ball grid array package suitable for surface mounting, as illustrated in Figure 67. The other is a 256-lead plastic ball grid array package suitable for surface mounting, as illustrated in Figure 68.

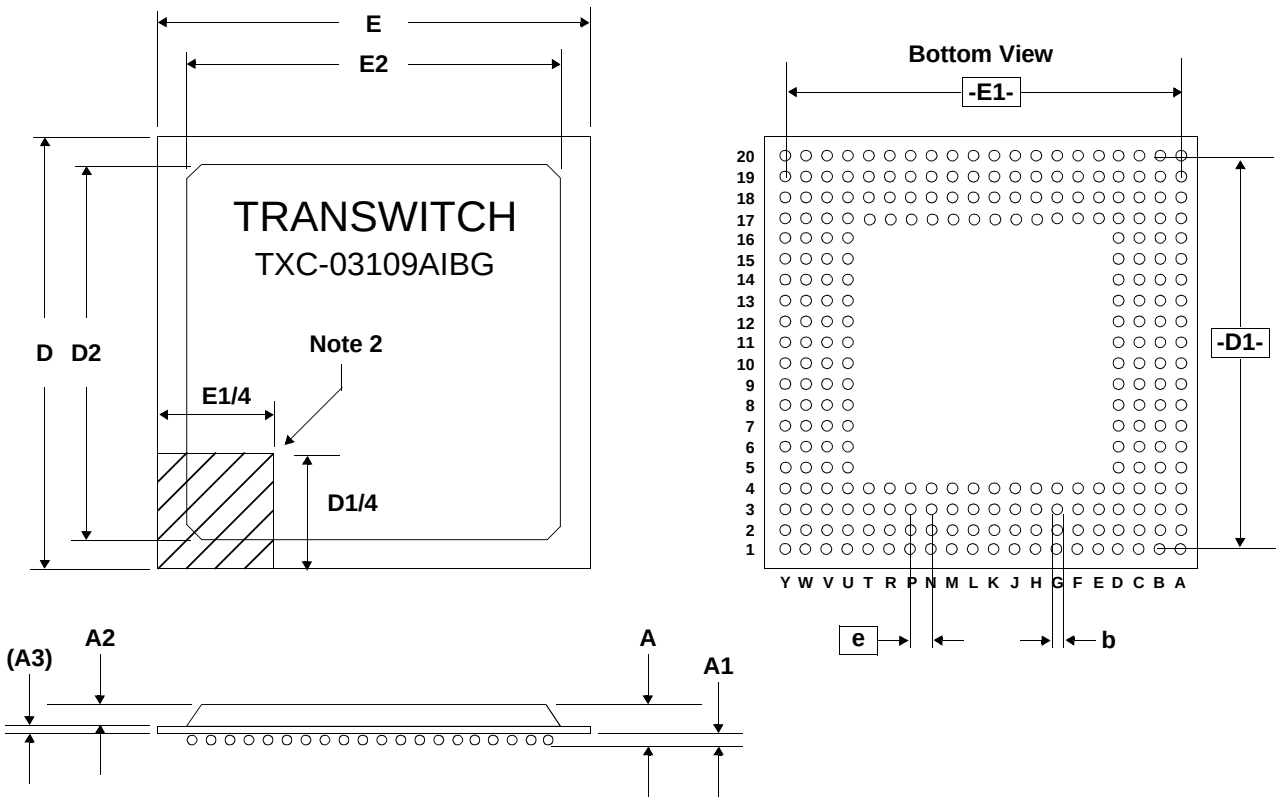


Notes:

1. All dimensions are in millimeters. Values shown are for reference only.
2. Identification of the solder ball A1 corner is contained within this shaded zone. This package corner may be a 90° angle, or chamfered for A1 identification.
3. Size of array: 16 x 16, JEDEC code MO-151-AAF-1

Dimension (Note 1)	Min	Max
A A1 A2	1.35 0.30 0.75	1.75 0.50 0.85
A3 (Ref.)	0.36	
b	0.40	0.60
D	17.00	
D1 (BSC)	15.00	
D2	15.00	15.70
E	17.00	
E1 (BSC)	15.00	
E2	15.00	15.70
e (BSC)	1.00	

Figure 67. E1Fx8 TXC-03109 208-Lead Plastic Ball Grid Array Package Diagram



Notes:

1. All dimensions are in millimeters. Values shown are for reference only.
2. Identification of the solder ball A1 corner is contained within this shaded zone. This package corner may be a 90° angle, or chamfered for A1 identification.
3. Size of array: 20 x 20, JEDEC code MO-151-BAL-2.

Dimension (Note 1)	Min	Max
A	1.92	2.32
A1	0.50	0.70
A2	1.12	1.22
A3 (Ref.)	0.36	
b	0.60	0.90
D	27.00	
D1 (BSC)	24.13	
D2	23.50	24.70
E	27.00	
E1 (BSC)	24.13	
E2	23.50	24.70
e (BSC)	1.27	

Figure 68. E1Fx8 TXC-03109 256-Lead Plastic Ball Grid Array Package Diagram

ORDERING INFORMATION

Part Number: TXC-03109AIOG	208-lead Plastic Ball Grid Array Package
Part Number: TXC-03109AIBG	256-lead Plastic Ball Grid Array Package

RELATED PRODUCTS

TXC-02050, MRT Multi-Rate Line Interface device. The MRT directly interfaces with the E123MUX device and provides the functions for terminating ITU-T-specified 8448 kbit/s (E2) and 34368 kbit/s (E3) line rate signals, or 6312 kbit/s (JT2) line signals specified in the Japanese NTT Technical Reference for High Speed Digital Leased Circuits. An optional HDB3 codec is provided for the two ITU-T line rates.

TXC-02302B, SYN155C VLSI Device (155-Mbit/s Synchronizer, Clock and Data Output). Transmits and receives at STS-3/STM-1 rates. Provides the complete STS-3/STM-1 frame synchronization function. Connects directly to optical fiber interface components.

TXC-03003B, SOT-3 VLSI Device (STM-1/STS-3/STS-3c Overhead Terminator). This device performs section, line and path overhead processing for STM-1/STS-3/STS-3c signals. Compliant with ANSI and ITU-T standards.

TXC-03011, SOT-1E VLSI Device (SONET STS-1 Overhead Terminator). This device provides extended features relative to the 84-lead TXC-03001 and TXC-03001B SOT-1 devices, and it has a 144-lead package.

TXC-03108, T1Fx8 VLSI Device (8-Channel T1 Framer). An 8-channel framer for voice and data communications applications. This device handles all logical interfacing functionality to a T1 line and operates from a power supply of 3.3 volts.

TXC-03114, QE1F-*Plus* VLSI Device (Quad E1 Framer-*Plus*). The QE1F-*Plus* is a 4-channel E1 (2048 kbit/s) framer designed for voice and data communications applications. A dual unipolar or NRZ line interface is supported with full alarm detection and generation per ITU-T G.703 and operates from a power supply of 3.3 or 5 volts.

TXC-03361, E123MUX VLSI Device (E1/E2/E3 Mux/Demux). The E123MUX is a CMOS VLSI device that provides the E13 functions needed to multiplex and demultiplex 16 independent E1 signals to and from an E3 signal that conforms to the ITU-T G.751 Recommendation. The E123MUX can also be configured to operate as an E12 or E23 multiplexer and demultiplexer.

TXC-04252, QE1M VLSI Device (Quad E1 to AU-4/VT2 or TU-12 Async Mapper-Desync). Interconnects four E1 signals with any four asynchronous mode VT2 or TU-12 tributaries carried in SDH AU-4/AU-3 rate payload interface.

TXC-04216, E1Mx16 VLSI Device (Sixteen channel E1 to AU-4/VT2 or TU-12 Async Mapper-Desync). Interconnects sixteen E1 signals with any sixteen asynchronous mode VT2 or TU-12 tributaries carried in SDH AU-4/AU-3 rate payload interface.

TXC-05101C, HDLC VLSI Device (HDLC Controller, 36-Bit Terminal I/O). High Speed High Level Data Link Controller that sends and receives packets at line rates up to 51.84 Mbit/s using either a nibble, byte-parallel, or serial interface.

TXC-05150, CDB VLSI Device (Cell Delineation Block). Provides cell delineation for ATM cells carried in a physical line at rates of 1.544 to 155 Mbit/s.

TXC-05427C, COBRA VLSI Device (Constant Bit Rate ATM Adaptation Layer 1). Provides ATM AAL1 Structured and Unstructured service for four T1, E1 or n x 64k constant bit rate interfaces. This device is not recommended for use in new designs.

TXC-06101, PHAST-1 VLSI Device (SONET STS-1 Overhead Terminator). This device provides the same features as the TXC-03011B SOT-1E device in the same package with the same pin outs, except it operates from a power supply of 3.3 volts.

TXC-06103, PHAST-3N VLSI Device (SONET/SDH STM-1, STS-3 or STS-3c Overhead Terminator) This PHAST-3N VLSI device provides a COMBUS interface for downstream devices and operates from a power supply of 3.3 volts.

TXC-06112, PHAST-12 VLSI Device (SONET/SDH STM-1, STM-4 STS-12 or STS-3c Section and Line Overhead Terminator) This PHAST-12 VLSI device provides a COMBUS interface for downstream devices and operates from a power supply of 3.3 volts.

TXC-06125, XBERT VLSI Device (Bit Error Rate Generator/Receiver). Programmable multi-rate test pattern generator and receiver in a single chip with serial, nibble, or byte interface capability.

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute
11 West 42nd Street
New York, New York 10036

Tel: 212-642-4900
Fax: 212-302-1286
Web: www.ansi.org

The ATM Forum (U.S.A., Europe, Asia):

2570 West El Camino Real
Suite 304
Mountain View, CA 94040

Tel: 650-949-6700
Fax: 650-949-6705
Web: www.atmforum.org

ATM Forum Europe Office

Av. De Tervueren 402
1150 Brussels
Belgium

Tel: 2 761 66 77
Fax: 2 761 66 79
Web: www.euroinfo@atmforum.ocm

ATM Forum Asia-Pacific Office

Hamamatsucho Suzuki Building 3F
1-2-11, Hamamatsucho, Minato-ku
Tokyo 105-0013, Japan

Tel: 3 3438 3694
Fax: 3 3438 3698
Web: www.apinfo@atmforum.com

Bellcore (See Telcordia)

CCITT (See ITU-T)

EIA (U.S.A.):

Electronic Industries Association
Global Engineering Documents
7730 Carondelet Avenue, Suite 407
Clayton, MO 63105-3329

Tel: 800-854-7179 (within U.S.A.)
Tel: 314-726-0444 (outside U.S.A.)
Fax: 314-726-6418
Web: www.global.ihs.com

ETSI (Europe):

European Telecommunications Standards Institute
650 route des Lucioles
06921 Sophia Antipolis Cedex
France

Tel: 4 92 94 42 22
Fax: 4 92 94 43 33
Web: www.etsi.org

GO-MVIP (U.S.A.):

The Global Organization for Multi-Vendor Integration Protocol (GO-MVIP)
3220 N Street NW, Suite 360
Washington, DC 20007

Tel: 800-669-6857 (within U.S.A.)
Tel: 903-769-3717 (outside U.S.A.)
Fax: 508-650-1375
Web: www.mvip.org

ITU-T (International):

Publication Services of International Telecommunication Union
Telecommunication Standardization Sector
Place des Nations, CH 1211
Geneve 20, Switzerland

Tel: 22 730 5111
Fax: 22 733 7256
Web: www.itu.int

MIL-STD (U.S.A.):

DODSSP Standardization Documents Ordering Desk
Building 4 / Section D
700 Robbins Avenue
Philadelphia, PA 19111-5094

Tel: 215-697-2179
Fax: 215-697-1462
Web: www.dodssp.daps.mil

PCI SIG (U.S.A.):

PCI Special Interest Group
2575 NE Kathryn Street #17
Hillsboro, OR 97124

Tel: 800-433-5177 (within U.S.A.)
Tel: 503-693-6232 (outside U.S.A.)
Fax: 503-693-8344
Web: www.pcisig.com

Telcordia (U.S.A.):

Telcordia Technologies, Inc.
Attention - Customer Service
8 Corporate Place
Piscataway, NJ 08854

Tel: 800-521-CORE (within U.S.A.)
Tel: 908-699-5800 (outside U.S.A.)
Fax: 908-336-2559
Web: www.telcordia.com

TTC (Japan):

TTC Standard Publishing Group of the
Telecommunications Technology Committee
2nd Floor, Hamamatsucho - Suzuki Building,
1 2-11, Hamamatsu-cho, Minato-ku, Tokyo

Tel: 3 3432 1551
Fax: 3 3432 1553
Web: www.ttc.or.jp

LIST OF DATA SHEET CHANGES

This change list identifies those areas within this updated E1Fx8 Data Sheet that have significant differences relative to the previous and now superseded E1Fx8 Data Sheet:

Updated E1Fx8 Data Sheet:	*PRELIMINARY* Ed. 3, January 2001
Previous E1Fx8 Data Sheet:	*PRELIMINARY* Ed. 2, February 2000

The page numbers indicated below of this updated Data Sheet include changes relative to the previous Data Sheet.

Page Number of Updated Data Sheet	Summary of the Change
All	Changed edition number and date.
42	Deleted “Component Temperature x Time” row from the first table.
55	Added pulse width of RTFRMn signal as Symbol t_{PW} in Figure 14 diagram and table. Added Note 2 to table.
56	Added pulse width of TTFRMn signal as Symbol t_{PW} in Figure 15 diagram and table. Added Note 2 to table.
58	Added pulse width of RTFRMn signal as Symbol t_{PW} in Figure 17 diagram and table. Added Note 2 to table.
59	Added pulse width of TTFRMn signal as Symbol t_{PW} in Figure 18 diagram and table. Added Note 2 to table.
279	Replaced List of Data Sheet Changes.

- NOTES -

- NOTES -

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