- **Organization . . . 1048576 By 8 Bits**
  524288 By 16 Bits
- **Array-Blocking Architecture**
  - **Two 8K-Byte/4K-Word Parameter Blocks**
  - **One 96K-Byte/48K-Word Main Block**
  - **Seven 128K-Byte/64K-Word Main Blocks**
  - **One 16K-Byte/8K-Word Protected Boot Block**
  - **Top or Bottom Boot Locations**
- **All Inputs/Outputs TTL-Compatible**
- **Maximum Access/Minimum Cycle Time**

	5-V V_{CC}	3-V V_{CC}
'28F008Axy70	70 ns	100 ns
'28F008Axy80	80 ns	120 ns
'28F800Axy70	70 ns	100 ns
'28F800Axy80	80 ns	120 ns

  (See Table 1 for V_{CC}/V_{PP} Voltage Configuration)
- **100000- and 10000-Program/Erase Cycle Versions**
- **Three Temperature Ranges**
  - **Commercial . . . 0°C to 70°C**
  - **Extended . . . – 40°C to 85°C**
  - **Automotive . . . – 40°C to 125°C**
- **Embedded Program/Erase Algorithms**
  - **Automated Byte Programming**
  - **Automated Word Programming**
  - **Automated Block Erase**
  - **Erase Suspend/Erase Resume**
- **Automatic Power-Saving Mode**
- **JEDEC Standards Compatible**
  - **Compatible With JEDEC Byte/Word Pinouts**
  - **Compatible With JEDEC EEPROM Command Set**
- **Fully Automated On-Chip Erase and Byte/Word Program Operations**
- **Package Options**
  - **44-Pin Plastic Small-Outline Package (PSOP) (DBJ Suffix)**
  - **40-Pin Thin Small-Outline Package (TSOP) (DCD Suffix)**
  - **48-Pin TSOP (DCD Suffix)**
  - **48-Ball Micro Ball Grid Array (μBGA™) available**
- **Low Power Dissipation (V_{CC} = 5.5 V)**
  - **Active Write . . . 330 mW (Byte Write)**
  - **Active Read . . . 220 mW (Byte Read)**
  - **Active Write . . . 330 mW (Word Write)**
  - **Active Read . . . 275 mW (Word Read)**
  - **Block Erase . . . 330 mW**
  - **Standby . . . 0.55 mW (CMOS-Input Levels)**
  - **Deep Power-Down Mode . . . 0.044 mW**
- **Write-Protection for Boot Block**
- **Industry Standard Command-State Machine (CSM)**
  - **Erase Suspend/Resume**
  - **Algorithm-Selection Identifier**
- **Flexible V_{PP}/Supply Voltage Combination**

PIN NOMENCLATURE

A0–A18	Address Inputs
A0–A19	Address Inputs (for 40-pin TSOP only)
$\overline{BYTE}$	Byte Enable
DQ0–DQ14	Data In/Out
DQ15/A_{-1}	Data In/Out (word-wide mode), Low-Order Address (byte-wide mode)
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{NC}$	No Internal Connection
$\overline{RP}$	Reset/Deep Power Down
V_{CC}	Power Supply
V_{PP}	Power Supply for Program/Erase
V_{SS}	Ground
$\overline{WE}$	Write Enable
$\overline{WP}$	Write Protect (for 40-pin and 48-pin TSOP only)

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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Table of Contents

description

The TMS28F800Axy is a 8388608-bit, boot-block flash memory that can be electrically block-erased and reprogrammed. The TMS28F800Axy is organized in a blocked architecture consisting of:

- One 16K-byte/8K-word protected boot block
- Two 8K-byte/4K-word parameter blocks
- One 96K-byte/48K-word main block
- Seven 128K-byte/64K-word main blocks

The device can be ordered in four different voltage configurations (see Table 1). Operation as a 1024K-byte (8-bit) or a 512K-word (16-bit) organization is user-definable.

Embedded program and block-erase functions are fully automated by the on-chip write-state machine (WSM), simplifying these operations and relieving the system microcontroller of these secondary tasks. WSM status can be monitored by an on-chip status register to determine progress of program/erase tasks. The device features user-selectable block erasure.

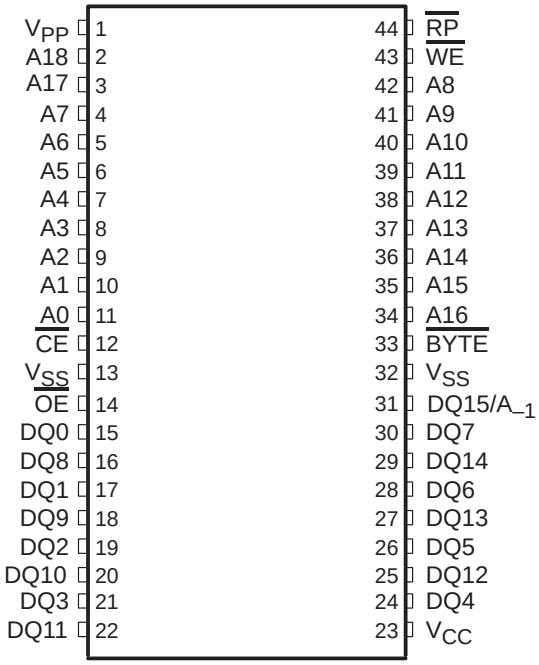
The TMS28F800AEy configuration allows the user to perform memory reads using 2.7–3.6-V V_{CC} and 5-V V_{CC} for optimum power consumption. Erasing or programming the device can be accomplished with V_{PP} = 3 V, 5 V, or 12-V. This configuration is offered in the commercial temperature range (0°C to 70°C) and the extended temperature range (–40°C to 85°C). Also, TMS28F800ASy offers V_{CC} = 3 – 3.6 V and V_{CC} = 5 V for optimum power consumption. The TMS28F800ALy configuration allows performance of memory reads using V_{CC} = 3.0 – 3.6 V for optimum power consumption. The TMS28F800AVy configuration allows performance of memory reads using V_{CC} = 2.7–3.6 V for optimum power consumption.

The TMS28F800AZy configuration offers a 5-V memory read with a 3-V/5-V/12-V program and erase. This configuration is offered in three temperature ranges: 0°C to 70°C, – 40°C to 85°C, – 40°C to 125°C.

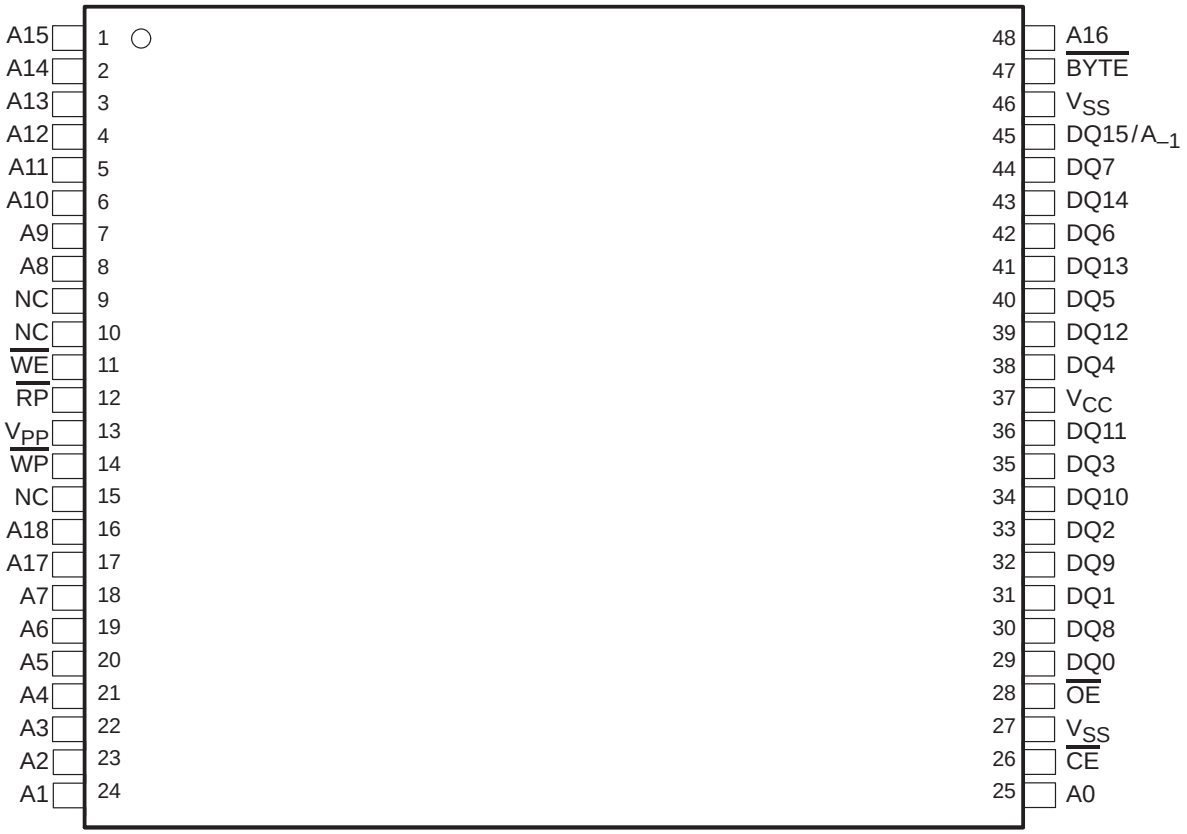
The TMS28F800Axy is offered in a 44-pin plastic small-outline package (PSOP) and a 48-pin thin small-outline package (TSOP) organized as 16-bit or 8-bit.

The TMS28F008 is functionally equivalent to the ’F800 except that it is organized only as a 8-bit configuration, and it is offered only in a 40-pin TSOP.

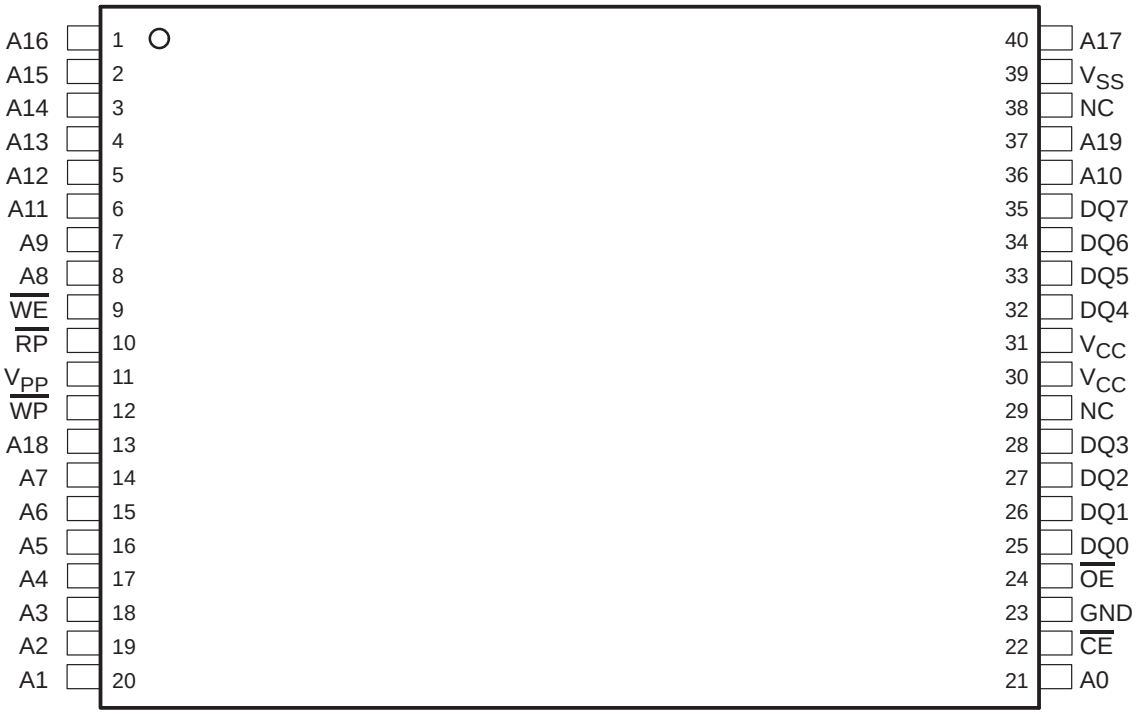
TMS28F800Axy
44-PIN PSOP (DBJ)
(TOP VIEW)



TMS28F800Axy
48-PIN TSOP (DCD)
(TOP VIEW)



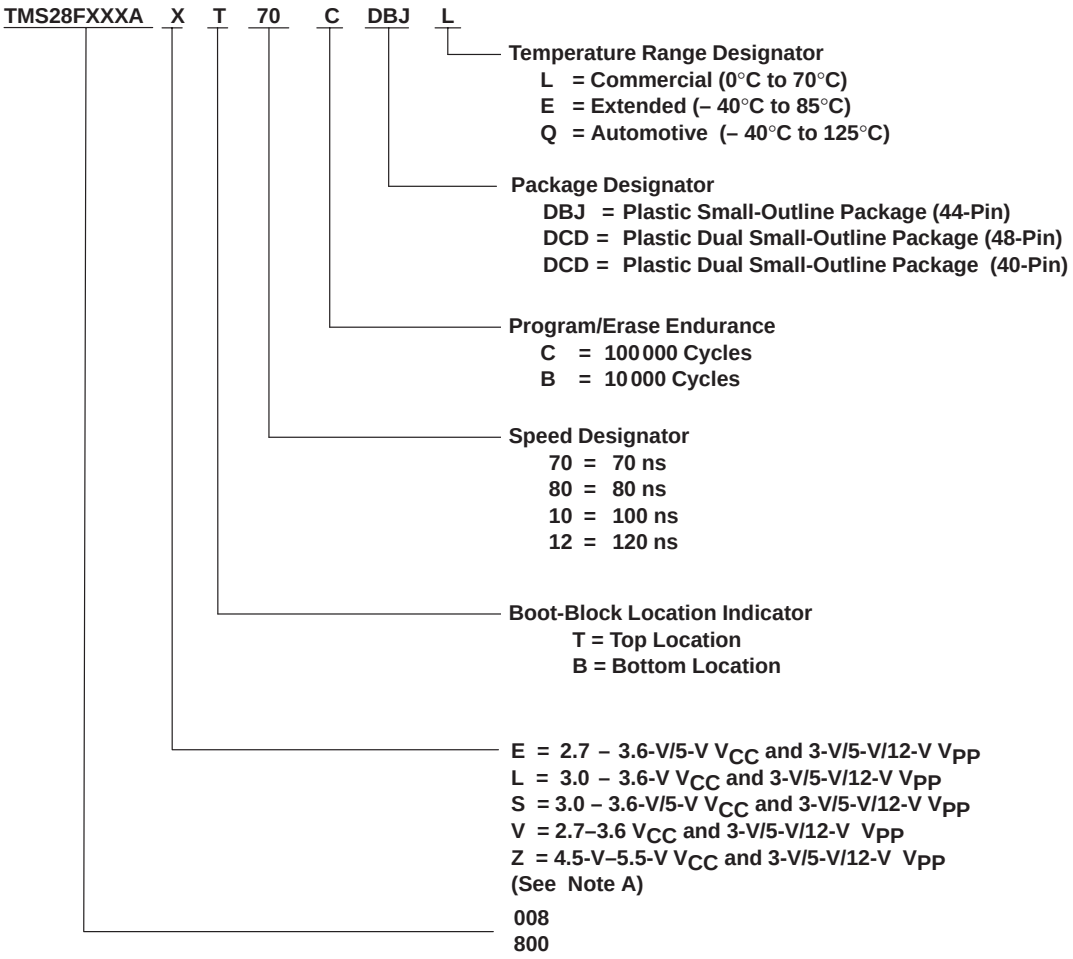
TMS28F008Axy
40-PIN TSOP (DCD)
(TOP VIEW)



TMS28F800Axy
48-BALL μBGA
(TOP VIEW)

	1	2	3	4	5	6	7	8
A	A13	A11	A8	V_{PP}	$\overline{WP}$	NC	A7	A4
B	A14	A10	$\overline{WE}$	$\overline{RP}$	A18	A17	A5	A2
C	A15	A12	A9	NC	NC	A6	A3	A1
D	A16	D14	D5	D11	D2	D8	$\overline{CE}$	A0
E	$\overline{BYTE}$	D15	D6	D12	D3	D9	D0	V_{SS}
F	V_{SS}	D7	D13	D4	V_{CC}	D10	D1	$\overline{OE}$

device symbol nomenclature

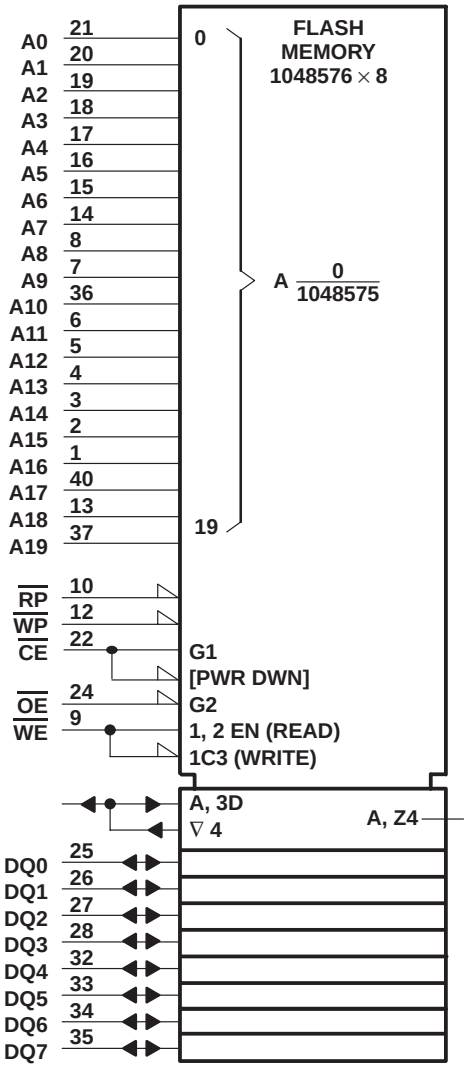


NOTE A: V_{CC} and V_{PP} are nominal unless otherwise stated.

Table 1. V_{CC}/V_{PP} Voltage Configurations

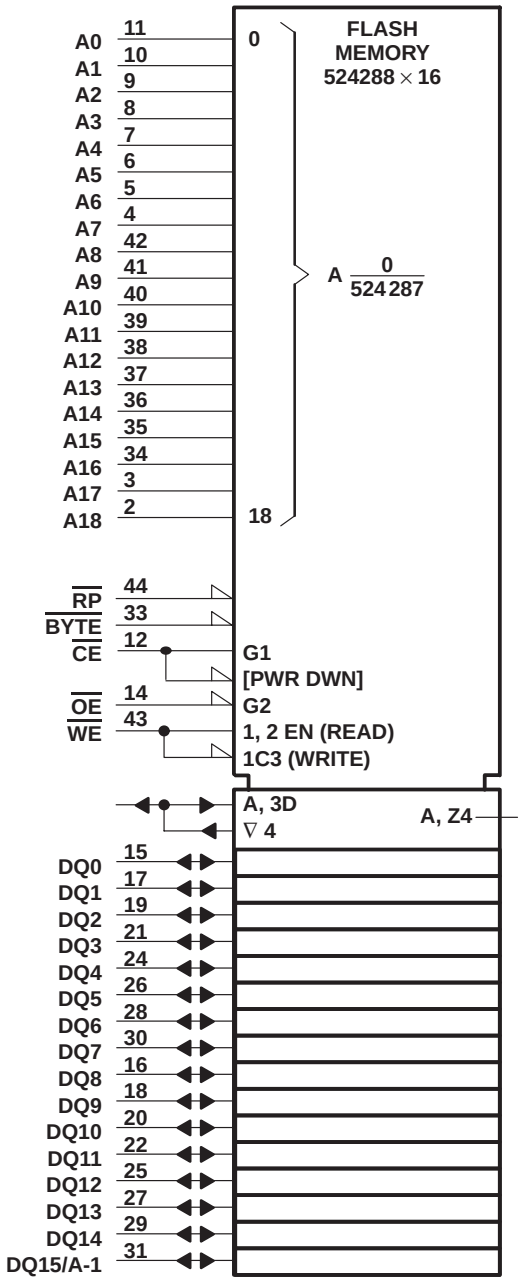
DEVICE CONFIGURATION	READ VOLTAGE (V_{CC})	PROGRAM/ERASE VOLTAGE (V_{PP})
TMS28F800AEy	2.7 V to 3.6 V/5 V ± 10 %	3 V/5 V ± 10% or 12 V ± 5%
TMS28F800AZy	5 V ± 10 %	3 V/5 V ± 10% or 12 V ± 5 %
TMS28F008AEy	2.7 V to 3.6 V/5 V ± 10 %	3 V/5 V ± 10% or 12 V ± 5%
TMS28F008AZy	5 V ± 10 %	3 V/5 V ± 10% or 12 V ± 5%
TMS28F800ASy	3.3 V/5 V ± 10 %	3 V/5 V ± 10% or 12 V ± 5%
TMS28F008ASy	3.3 V/5 V ± 10 %	3 V/5 V ± 10% or 12 V ± 5%
TMS28F800AVy	2.7 V to 3.6 V	3 V/5 V ± 10% or 12 V ± 5%
TMS28F008AVy	2.7 V to 3.6 V	3 V/5 V ± 10% or 12 V ± 5%
TMS28F800ALy	3.3 V ± 10 %	3 V/5 V ± 10% or 12 V ± 5%
TMS28F008ALy	3.3 V± 10 %	3 V/5 V ± 10% or 12 V ± 5%

logic symbol for the TMS28F008Axy 40-pin package†



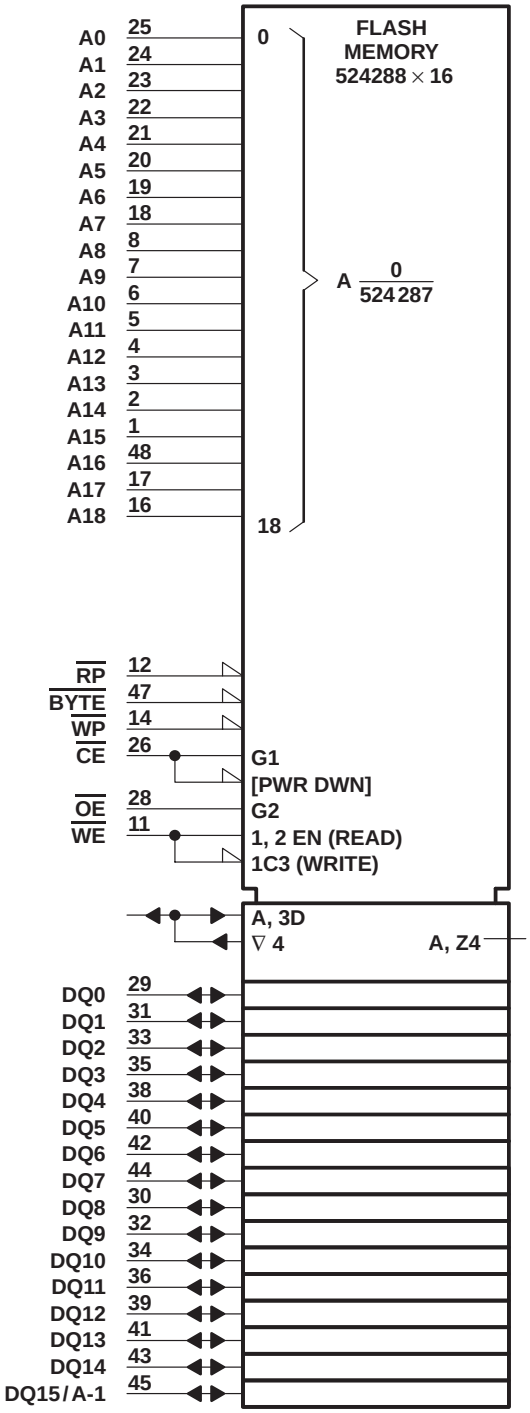
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DCD package.

logic symbol for TMS28F800Axy 44-pin package†



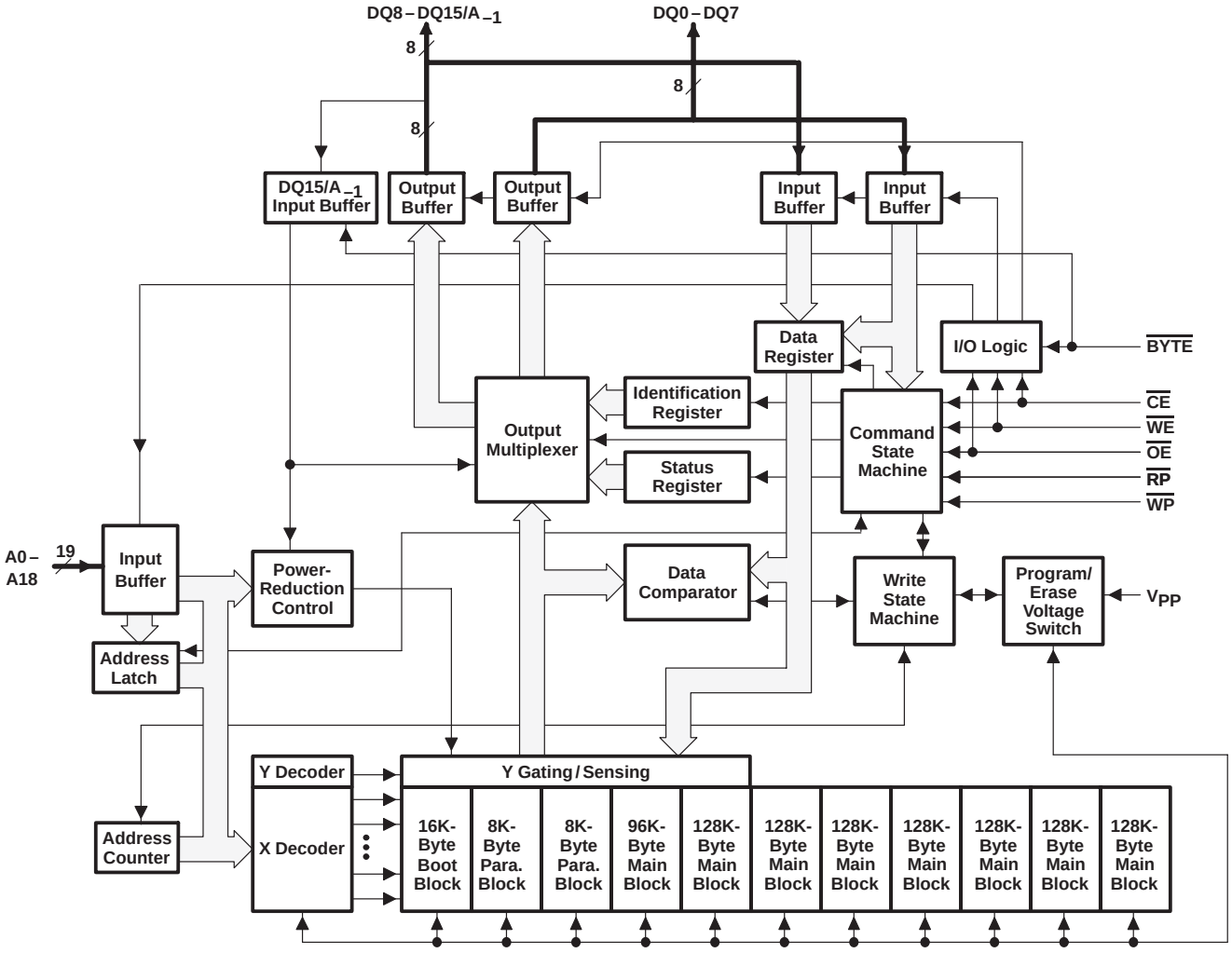
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DBJ package.

logic symbol for TMS28F800Axy 48-pin package†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DCD package.

functional block diagram



architecture

The TMS28F008Axy and TMS28F800Axy use a blocked architecture to allow independent erasure of selected memory blocks. The block to be erased is selected by using any valid address within that block.

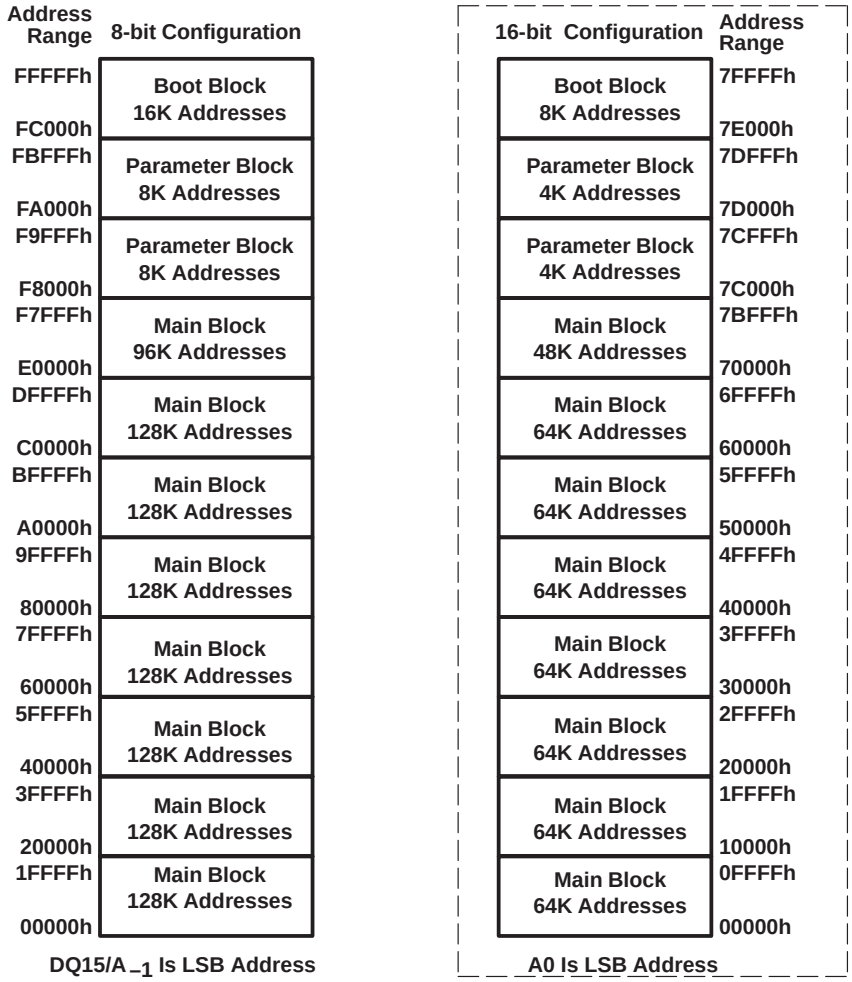
block memory maps (’28F800Axy 16-bit configuration)

The TMS28F800Axy is available with the block architecture mapped in either of two configurations: the boot block located at the top or at the bottom of the memory array, as required by different microprocessors. The TMS28F800AxB (bottom boot block) is mapped with the 8K-word boot block located at the low-order address range (00000h to 01FFFh). The TMS28F800AxT (top boot block) is inverted with respect to the TMS28F800AxB with the boot block located at the high-order address range (7E000h to 7FFFFh). Both of these address ranges are for word-wide mode. Figure 1 and Figure 2 show the memory maps for these configurations.

block memory maps (’28F008Axy and ’28F800Axy 8-bit configuration)

The TMS28F008Axy and TMS28F800Axy are available with the block architecture mapped in either of two configurations: the boot block located at the top (e.g., TMS28F008AxT) or at the bottom (e.g., TMS28F008AxB) of the memory array, as required by different microprocessors. The ’28F008AxB and ’28F800AxB (8-bit) are mapped with 16K-byte boot block located at the low-order address range (00000h to 03FFFh). The TMS28F008AxT and TMS28F800AxT (8-bit) are inverted with respect to the TMS28F008AxB models with the boot block located at the higher-order address range (FC000h to FFFFFh).

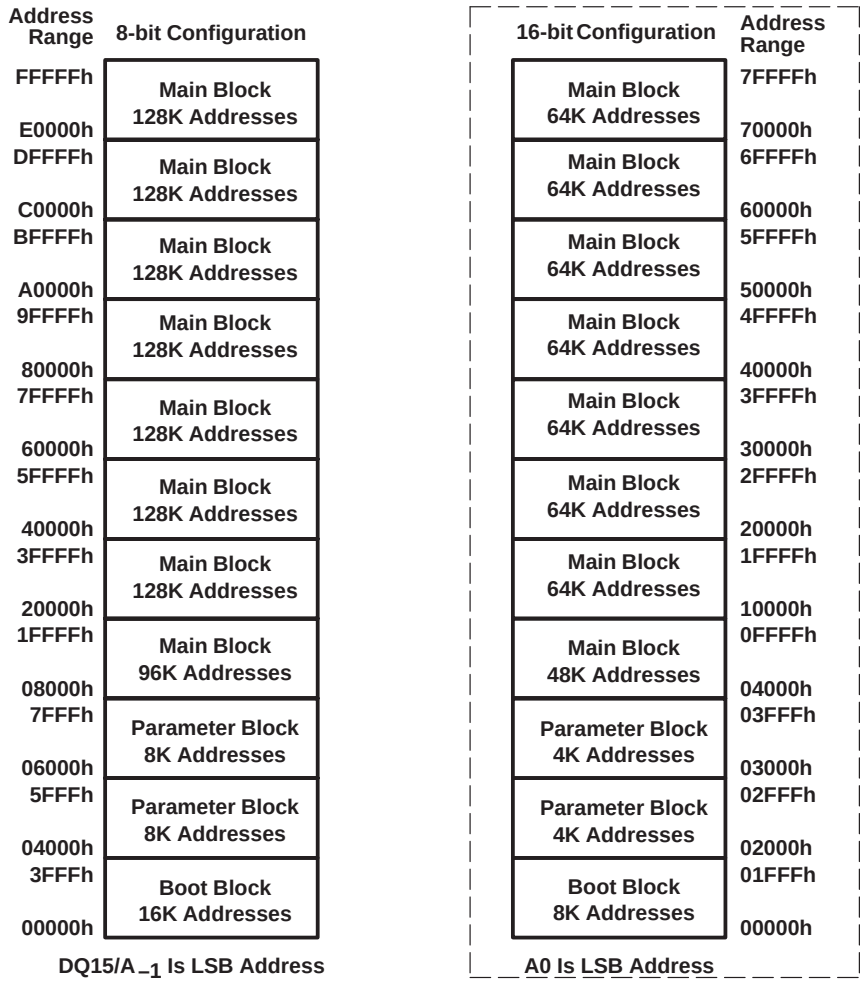
block memory maps (continued)



NOTE A: ’28F008Axy is offered in a 40-pin TSOP package, 8-bit configuration only, and A0 is the LSB address.

Figure 1. TMS28F008AxT and TMS28F800AxT (Top Boot Block) Memory Map

block memory maps (continued)



NOTE A: '28F008Axy is offered in a 40-pin TSOP package, 8-bit configuration only, and A0 is LSB adddress.

Figure 2. TMS28F008AxB and TMS28F800AxB (Bottom Boot Block) Memory Map

boot-block data protection

The 16K-byte boot block can be used to store key system data that is seldom changed in normal operation. Data in this block can be secured by using different combinations of the reset/deep power-down pin ($\overline{RP}$), the write protect pin ($\overline{WP}$) and V_{PP} supply levels. Table 2 provides a list of these combinations.

parameter block

Two parameter blocks of 8K bytes each can be used like a scratch pad to store frequently updated data. Alternatively, the parameter blocks can be used for additional boot- or main-block data. If a parameter block is used to store additional boot-block data, caution must be exercised because the parameter block does not have the boot-block data-protection safety feature.

main block

Primary memory on the TMS28F800Axy is located in eight main blocks. Seven of the blocks have storage capacity for 128K bytes and the eighth block has storage capacity for 96K bytes.

data protection

Data is secured or unsecured by using different combinations of the reset/deep power-down pin ($\overline{RP}$), the write protect pin ($\overline{WP}$) and V_{PP} supply levels. See to Table 2 for a listing of these combinations.

There are two configurations to secure the entire memory against inadvertant alteration of data. The V_{PP} supply pin can be held below the V_{PP} lock-out voltage level (V_{PPLK}) or the $\overline{RP}$ can be pulled to a logic-low level. If $\overline{RP}$ is held low, the device resets, which means it powers down and, therefore, cannot be read. Typically, this pin is tied to the system reset for additional protection during system power up.

The boot-block sector has an additional security feature through the $\overline{WP}$ pin. When the $\overline{RP}$ pin is at a logic-high level, the $\overline{WP}$ pin controls whether the boot-block sector is protected. When $\overline{WP}$ is held at the logic-low level, the boot block is protected. When $\overline{WP}$ is held at the logic-high level, the boot block is unprotected along with the rest of the other sectors. Alternatively, the entire memory can be unprotected by pulling the $\overline{RP}$ pin to V_{HH} (12 V).

Table 2. Data-Protection Combinations (see Note 1)

DATA PROTECTION PROVIDED	V_{PP}	$\overline{RP}$	$\overline{WP}$
All blocks locked	$\le V_{PPLK}$	X	X
All blocks locked (reset)	$\ge V_{PPLK}$	V_{IL}	X
All blocks unlocked	$\ge V_{PPLK}$	V_{HH}	X
Only boot block locked	$\ge V_{PPLK}$	V_{IH}	V_{IL}
All blocks unlocked	$\ge V_{PPLK}$	V_{IH}	V_{IH}

NOTE 1: For TMS28F008AZy and TMS28F800AZy (12-V V_{PP}) products, the $\overline{WP}$ pin is disabled and can be left floating. To unlock blocks, $\overline{RP}$ must be at V_{HH}.

command-state machine (CSM)

Commands are issued to the CSM using standard microprocessor write timings. The CSM acts as an interface between the external microprocessor and the internal WSM. Table 1 lists the CSM codes and device modes, and Table 4 lists the data for the bus cycle. When a program or erase command is issued to the CSM, the WSM controls the internal sequences and the CSM responds only to status reads. After the WSM completes its task, the WSM status bit (SB7) is set to a 1, allowing the CSM to respond to the full command set again.

operation

Device operations are selected by entering standard JEDEC 8-bit command codes with conventional microprocessor timing into an on-chip CSM through I/O pins DQ0–DQ7. When the device is powered up, internal reset circuitry initializes the chip to a read-array mode of operation. Changing the mode of operation requires that a command code be entered into the CSM. Table 1 lists the CSM codes for all modes of operation.

The on-chip status register allows the progress of various operations to be monitored. The status register is interrogated by entering a read-status-register command into the CSM (cycle 1) and reading the register data on I/O pins DQ0–DQ7 (cycle 2). Status-register bits SB0 through SB7 correspond to DQ0 through DQ7.

operation (continued)

Table 3. CSM Codes for Device-Mode Selection

COMMAND CODE ON DQ0–DQ7†	DEVICE MODE
00h	Invalid/Reserved
10h	Alternate Program Setup
20h	Block-Erase Setup
40h	Program Setup
50h	Clear Status Register
70h	Read Status Register
90h	Algorithm Selection
B0h	Erase-Suspend
D0h	Erase-Resume/Block-Erase Confirm
FFh	Read Array

† DQ0 is the least significant bit. DQ8–DQ15 can be any valid 2-state level.

command definition

Once a specific command code has been entered, the WSM executes an internal algorithm generating the necessary timing signals to program, erase, and verify data. See Table 4 for the CSM command definitions and data for each of the bus cycles.

Table 4. Command Definitions

COMMAND	BUS CYCLES REQUIRED	FIRST BUS CYCLE			SECOND BUS CYCLE		
		OPERATION	ADDRESS	DATA INPUT	OPERATION	ADDRESS	DATA IN/OUT
Read Operations							
Read Array	1	Write	X	FFh	Read	X	Data Out
Read Algorithm-Selection Code	3	Write	X	90h	Read	A0	M/D
Read Status Register	2	Write	X	70h	Read	X	SRB
Clear Status Register	1	Write	X	50h			
Program Mode							
Program Setup/Program (byte/word)	2	Write	PA	40h or 10h	Write	PA	PD
Erase Operations							
Block-Erase Setup/ Block-Erase Confirm	2	Write	BEA	20h	Write	BEA	D0h
Erase Suspend/ Erase Resume	2	Write	X	B0h	Write	X	D0h

Legend:

BEA Block-erase address. Any address selected within a block selects that block for erase.
M/D Manufacturer-equivalent/device-equivalent code
PA Address to be programmed
PD Data to be programmed at PA
SRB Status-register data byte that can be found on DQ0–DQ7
X Don't care

status register

The status register can be used to determine whether the state of a program/erase operation is pending or complete. The status register is monitored by writing a read-status command to the CSM and reading the resulting status code on I/O pins DQ0–DQ7. This is valid for operations in either the byte-wide or word-wide mode. When writing to the CSM in word-wide mode, the high-order I/O pins (DQ8–DQ15) can be set to any valid 2-state level. When reading the status bits during a word-wide read operation, the high-order I/O pins (DQ8–DQ15) are set to 00h internally, so the user needs to interpret only the low-order I/O pins (D0–DQ7).

After a read-status command has been given, the data appearing on DQ0–DQ7 remains as status register data until a new command is issued to the CSM. To return the device to other modes of operation, a new command must be issued to the CSM.

Register data is updated on the falling edge of $\overline{OE}$ or $\overline{CE}$. The latest falling edge of either of these two signals updates the latch within a given read cycle. Latching the data prevents errors from occurring should the register input change during a status-register read. To ensure that the status-register output contains updated status data, $\overline{CE}$ or $\overline{OE}$ must be toggled for each subsequent status read.

The status register provides the internal state of the WSM to the external microprocessor. During periods when the WSM is active, the status register can be polled to determine the WSM status. Table 5 defines the status-register bits and their functions.

Table 5. Status-Register Bit Definitions and Functions

STATUS BIT	FUNCTION	DATA	COMMENTS
SB7	Write-state-machine status (WSMS)	1 = Ready 0 = Busy	If SB7 = 0 (busy), the WSM has not completed an erase or programming operation. If SB7 = 1 (ready), other polling operations can be performed. Until this occurs, the other status bits are not valid. If the WSM status bit shows busy (0), the user must toggle $\overline{CE}$ or $\overline{OE}$ periodically to determine when the WSM has completed an operation (SB7 = 1) since SB7 is not updated automatically at the completion of a WSM task.
SB6	Erase-suspend status (ESS)	1 = Erase suspended 0 = Erase in progress or completed	When an erase-suspend command is issued, the WSM halts execution and sets the ESS bit high (SB6 = 1), indicating that the erase operation has been suspended. The WSMS bit also is set high (SB7 = 1), indicating that the erase-suspend operation has been completed successfully. The ESS bit remains at a logic-high level until an erase-resume command is input to the CSM (code D0h).
SB5	Erase status (ES)	1 = Block-erase error 0 = Block-erase good	SB5 = 0 indicates that a successful block erasure has occurred. SB5 = 1 indicates that an erase error has occurred. In this case, the WSM has completed the maximum allowed erase pulses determined by the internal algorithm, but this was insufficient to erase the device completely.
SB4	Program status (PS)	1 = Byte/word-program error 0 = Byte/word-program good	SB4 = 0 indicates successful programming has occurred at the addressed block location. SB4 = 1 indicates that the WSM was unable to program the addressed block location correctly.
SB3	V_{PP} status (VPPS)	1 = Program abort: V_{PP} range error 0 = V_{PP} good	SB3 provides information on the status of V_{PP} during programming. If V_{PP} is lower than V_{PPL} after a program or erase command has been issued, SB3 is set to a 1, indicating that the programming operation is aborted. If V_{PP} is between V_{PPH} and V_{PPL}, SB3 is not set.
SB2–SB0	Reserved		These bits must be masked out when reading the status register.

byte-wide or word-wide mode selection

The memory array is divided into two parts: an upper-half that outputs data through I/O pins DQ8–DQ15, and a lower-half that outputs data through DQ0–DQ7. Device operation in either byte-wide or word-wide mode is user-selectable and is determined by the logic state of $\overline{BYTE}$. When $\overline{BYTE}$ is at a logic-high level, the device is in the word-wide mode and data is written to, or read from, I/O pins DQ0–DQ15. When $\overline{BYTE}$ is at a logic-low level, the device is in the byte-wide mode and data is written to or read from I/O pins DQ0–DQ7. In the byte-wide mode, I/O pins DQ8–DQ14 are placed in the high-impedance state and DQ15/A_{-1} becomes the low-order address pin and selects either the upper- or lower-half of the array. Array data from the upper half (DQ8–DQ15) and the lower half (DQ0–DQ7) are multiplexed to appear on DQ0–DQ7. Table 6 and Table 7 summarize operations for word-wide mode and byte-wide mode, respectively. Table 8 summarizes the operation for ’28F008Axy.

Table 6. Operation Modes for Word-Wide Mode ($\overline{BYTE}$ = V_{IH}) (’28F800Axy) (see Note 2)

MODE	$\overline{WP}$	$\overline{CE}$	$\overline{OE}$	$\overline{RP}$	$\overline{WE}$	A9	A0	V_{PP}	DQ0–DQ15
Read	X	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	X	X	Data out
Algorithm-selection mode	X	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{ID}	V_{IL}	X	Manufacturer-equivalent code 0089h
	X	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{ID}	V_{IH}	X	Device-equivalent code 889Ch (top boot block)
									Device-equivalent code 889Dh (bottom boot block)
Output disable	X	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	X	Hi-Z
Standby	X	V_{IH}	X	V_{IH}	X	X	X	X	Hi-Z
Reset/deep power down	X	X	X	V_{IL}	X	X	X	X	Hi-Z
Write (see Note 3)	V_{IL} or V_{IH}	V_{IL}	V_{IH}	V_{IH} or V_{HH}	V_{IL}	X	X	V_{PPL}or V_{PPH}	Data in

Table 7. Operation Modes for Byte-Wide Mode ($\overline{BYTE}$ = V_{IL}) (’28F800Axy) (see Note 2)

MODE	$\overline{WP}$	$\overline{CE}$	$\overline{OE}$	$\overline{RP}$	$\overline{WE}$	A9	A0	V_{PP}	DQ15/A_{-1}	DQ8–DQ14	DQ0–DQ7
Read lower byte	X	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	X	X	V_{IL}	Hi-Z	Data out
Read upper byte	X	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	X	X	V_{IH}	Hi-Z	Data out
Algorithm-selection mode	X	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{ID}	V_{IL}	X	X	Hi-Z	Manufacturer-equivalent code 89h
	X	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{ID}	V_{IH}	X	X	Hi-Z	Device-equivalent code 9Ch (top boot block)
											Device-equivalent code 9Dh (bottom boot block)
Output disable	X	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	X	X	Hi-Z	Hi-Z
Standby	X	V_{IH}	X	V_{IH}	X	X	X	X	X	Hi-Z	Hi-Z
Reset/deep power down	X	X	X	V_{IL}	X	X	X	X	X	Hi-Z	Hi-Z
Write (see Note 3)	V_{IL} or V_{IH}	V_{IL}	V_{IH}	V_{IH} or V_{HH}	V_{IL}	X	X	V_{PPL} or V_{PPH}	X	Hi-Z	Data in

NOTES: 2. X = don’t care
3. When writing commands to the ’28F008Axy and the ’28F800Axy, V_{PP} must be in the appropriate V_{PP} voltage range (as shown in the recommended operating conditions table for a specific product) for block-erase or program commands to be executed. Also, depending on the combination of $\overline{RP}$ and $\overline{WP}$, the boot block can be secured and, therefore, is not programmable (see Table 2 for a list of the combinations).

byte-wide or word-wide mode selection (continued)

Table 8. Operation Modes for Byte-Wide Mode (’28F008Axy) (see Note 2)

MODE	$\overline{WP}$	$\overline{CE}$	$\overline{OE}$	$\overline{RP}$	$\overline{WE}$	A9	A0	V_{PP}	DQ0 – DQ7
Read	X	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	X	X	Data out
Algorithm-selection mode	X	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{ID}	V_{IL}	X	Manufacturer-equivalent code 89h
	X	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{ID}	V_{IH}	X	Device-equivalent code 98 (top boot block)
									Device-equivalent code 99 (bottom boot block)
Output disable	X	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	X	Hi-Z
Standby	X	V_{IH}	X	V_{IH}	X	X	X	X	Hi-Z
Reset/deep power down	X	X	X	V_{IL}	X	X	X	X	Hi-Z
Write (see Note 3)	V_{IL} or V_{IH}	V_{IL}	V_{IH}	V_{IH} or V_{HH}	V_{IL}	X	X	V_{PPL} or V_{PPH}	Data in

NOTES: 2. X = don’t care

3. When writing commands to the ’28F008Axy and the ’28F800Axy, V_{PP} must be in the appropriate V_{PP} voltage range (as shown in the recommended operating conditions table for a specific product) for block-erase or program commands to be executed. Also, depending on the combination of $\overline{RP}$ and $\overline{WP}$, the boot block can be secured and, therefore, is not programmable (see Table 2 for a list of the combinations).

command-state machine (CSM) operations

The CSM decodes instructions for read, read algorithm-selection code, read-status register, clear-status register, program, erase, erase-suspend, and erase-resume. The 8-bit command code is input to the device on DQ0–DQ7 (see Table 1 for CSM codes). During a program or erase cycle, the CSM informs the WSM that a program or erase cycle has been requested. During a program cycle, the WSM controls the program sequences and the CSM responds only to status reads.

During an erase cycle, the CSM responds to status-read and erase-suspend commands. When the WSM has completed its task, the WSM status bit (SB7) is set to a logic-high level and the CSM responds to the full command set. The CSM stays in the current command state until the microprocessor issues another command.

The WSM successfully initiates an erase or program operation only when V_{PP} is within its correct voltage range. For data protection, it is recommended that $\overline{RP}$ be held at a logic-low level during a CPU reset.

clear status register

The internal circuitry can set only the V_{PP} status bit (SB3), the program status bit (SB4), and the erase status bit (SB5) of the status register. The clear-status-register command (50h) allows the external microprocessor to clear these status bits and synchronize to internal operations. When the status bits are cleared, the device returns to the read-array mode.

read operations

There are three read operations available: read array, read algorithm-selection code, and read status register.

- read array

  The array level is read by entering the command code FFh on DQ0–DQ7. Control pins $\overline{CE}$ and $\overline{OE}$ must be at a logic-low level (V_{IL}) and $\overline{WE}$ and $\overline{RP}$ must be at a logic-high level (V_{IH}) to read data from the array. Data is available on DQ0–DQ15 (word-wide mode) or DQ0–DQ7 (byte-wide mode). Any valid address within any of the blocks selects that block and allows data to be read from the block.

- read algorithm-selection code

  Algorithm-selection codes are read by entering command code 90h on DQ0–DQ7. Two bus cycles are required for this operation: the first to enter the command code and a second to read the device-equivalent code. Control pins $\overline{CE}$ and $\overline{OE}$ must be at a logic-low level (V_{IL}) and $\overline{WE}$ and $\overline{RP}$ must be at a logic-high level (V_{IH}). Two identifier bytes are accessed by toggling A0. The manufacturer-equivalent code is obtained on DQ0–DQ7 with A0 at a logic-low level (V_{IL}). The device-equivalent code is obtained when A0 is set to a logic-high level (V_{IH}). Alternatively, the manufacturer- and device-equivalent codes can be read by applying V_{ID} (nominally 12 V) to A9 and selecting the desired code by toggling A0 high or low. All other addresses are “don’t cares” (see Table 4, Table 6, and Table 7).

- read status register

  The status register is read by entering the command code 70h on DQ0–DQ7. Control pins $\overline{CE}$ and $\overline{OE}$ must be at a logic-low level (V_{IL}) and $\overline{WE}$ and $\overline{RP}$ must be at a logic-high level (V_{IH}). Two bus cycles are required for this operation: one to enter the command code and a second to read the status register. In a given read cycle, status register contents are updated on the falling edge of $\overline{CE}$ or $\overline{OE}$, whichever occurs last within the cycle.

programming operations

There are two CSM commands for programming: program setup and alternate program setup (see Table 1). After the desired command code is entered, the WSM takes over and correctly sequences the device to complete the program operation. During this time, the CSM responds only to status reads until the program operation has been completed, after which all commands to the CSM become valid again. Once a program command has been issued, the WSM normally cannot be interrupted until the program algorithm is completed (see Figure 3 and Figure 4).

Taking $\overline{RP}$ to V_{IL} during programming aborts the program operation. During programming, V_{PP} must remain in the appropriate V_{PP} voltage range as shown in the recommended operating conditions table. Different combinations of $\overline{RP}$, $\overline{WP}$, and V_{PP} pin voltage levels ensure that data in certain blocks are secured, and, therefore, cannot be programmed (see Table 2 for a list of combinations). Only 0s are written and compared during a program operation. If 1s are programmed, the memory cell contents do not change and no error occurs.

A program-setup command can be aborted by writing FFh (in byte-wide mode) or FFFFh (in word-wide mode) during the second cycle. After writing all 1s during the second cycle, the CSM responds only to status reads. When the WSM status bit (SB7) is set to a logic-high level, signifying the nonprogram operation is terminated, all commands to the CSM become valid again.

erase operations

There are two erase operations that can be performed by the TMS28F008Axy and TMS28F800Axy devices: block erase and erase suspend/erase resume. An erase operation must be used to initialize all bits in an array block to 1s. After block-erase confirm is issued, the CSM responds only to status reads or erase-suspend commands until the WSM completes its task.

- block erasure

  Block erasure inside the memory array sets all bits within the addressed block to logic 1s. Erasure is accomplished only by blocks; data at single address locations within the array cannot be erased individually. The block to be erased is selected by using any valid address within that block. Note that different combinations of $\overline{RP}$, $\overline{WP}$ and V_{PP} pin voltage levels ensure that data in certain blocks are secure and, therefore, cannot be erased (see Table 2 for a list of combinations). Block erasure is initiated by a command sequence to the CSM: block-erase setup (20h) followed by block-erase confirm (D0h) (see Figure 5). A two-command erase sequence protects against accidental erasure of memory contents.

  Erase-setup and erase-confirm commands are latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs first. Block addresses are latched during the block-erase-confirm command on the rising edge of $\overline{CE}$ or $\overline{WE}$ (see Figure 15 and Figure 16). When the block-erase-confirm command is complete, the WSM automatically executes a sequence of events to complete the block erasure. During this sequence, the block is programmed with logic 0s, data is verified, all bits in the block are erased, and finally, verification is performed to ensure that all bits are erased correctly. Monitoring of the erase operation is possible through the status register (see “read status register” in the subsection “read operations”).

- erase suspend/erase resume

  During the execution of an erase operation, the erase-suspend command (B0h) can be entered to direct the WSM to suspend the erase operation. Once the WSM has reached the suspend state, it allows the CSM to respond only to the read-array, read-status-register, and erase-resume commands. During the erase-suspend operation, array data should be read from a block other than the one being erased. To resume the erase operation, an erase-resume command (D0h) must be issued to cause the CSM to clear the suspend state previously set (see Figure 5 and Figure 6).

automatic power-saving mode

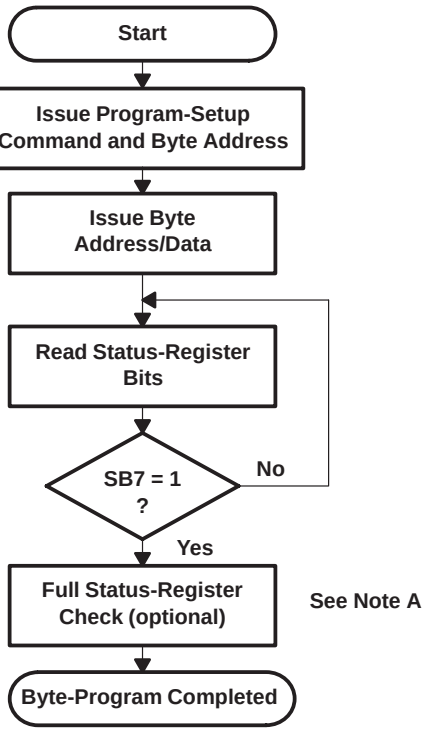
Substantial power savings are realized during periods when the array is not being read. During this time, the device switches to the automatic power-saving (APS) mode. When the device switches to this mode, I_{CC} reduces by an order of magnitude. For example, for a 5 V port, I_{CC} typically reduces from 40 mA to 1 mA. The low level of power is maintained until another read operation is initiated. In this mode, the I/O pins retain the data from the last memory address read until a new address is read. This mode is entered automatically if no new address is accessed within a 200-ns time-out period.

reset/deep power-down mode

Very low levels of power consumption can be attained by using a special pin, $\overline{RP}$, to disable internal device circuitry. When $\overline{RP}$ is at a CMOS logic-low level of 0.0 V ± 0.2 V, a much lower I_{CC} value or power is achievable. This is important in portable applications where extended battery life is of major concern.

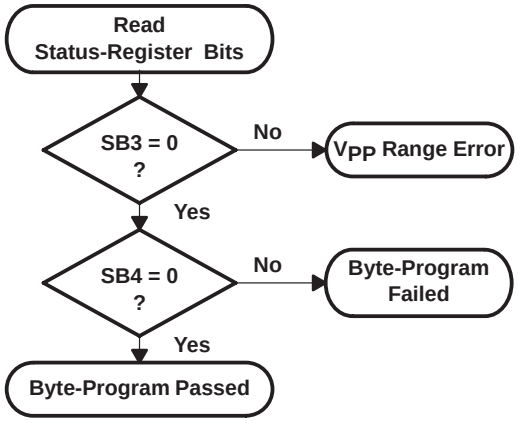
A recovery time is required when exiting from deep power-down mode. For a read-array operation, a minimum of $t_{d(RP)}$ is required before data is valid, and a minimum of $t_{rec(RPHE)}$ and $t_{rec(RPHW)}$ in deep power-down mode is required before data input to the CSM can be recognized. With $\overline{RP}$ at ground, the WSM is reset and the status register is cleared, effectively eliminating accidental programming to the array during system reset. After restoration of power, the device does not recognize any operation command until $\overline{RP}$ is returned to a V_{IH} or V_{HH} level.

Should $\overline{RP}$ go low during a program or erase operation, the device powers down and, therefore, becomes nonfunctional. Data being written or erased at that time becomes invalid or indeterminate, requiring that the operation be performed again after power restoration.



BUS OPERATION	COMMAND	COMMENTS
Write	Write program setup	Data = 40h or 10h Addr = Address of byte to be programmed
Write	Write data	Data = Byte to be programmed Addr = Address of byte to be programmed
Read		Status-register data. Toggle $\overline{OE}$ or $\overline{CE}$ to update status register
Standby		Check SB7 1 = Ready, 0 = Busy
Repeat for subsequent bytes. Write FFh after the last byte-programming operation to reset the device to read-array mode		

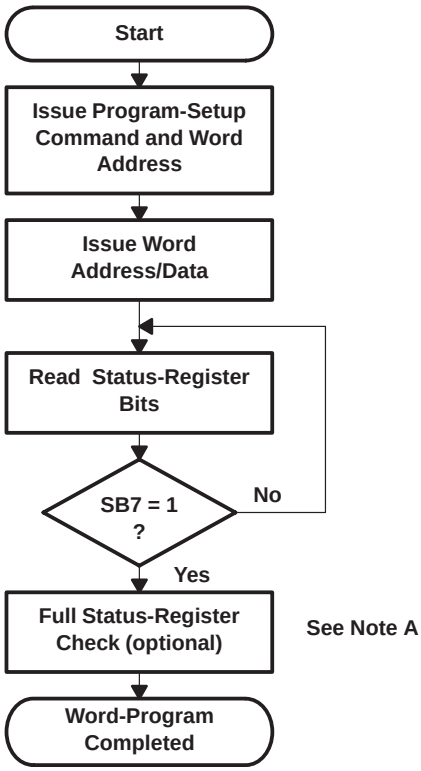
FULL STATUS-REGISTER-CHECK FLOW



BUS OPERATION	COMMAND	COMMENTS
Standby		Check SB3 1 = Detect V_{PP} low (see Note B)
Standby		Check SB4 1 = Byte-program error (see Note C)

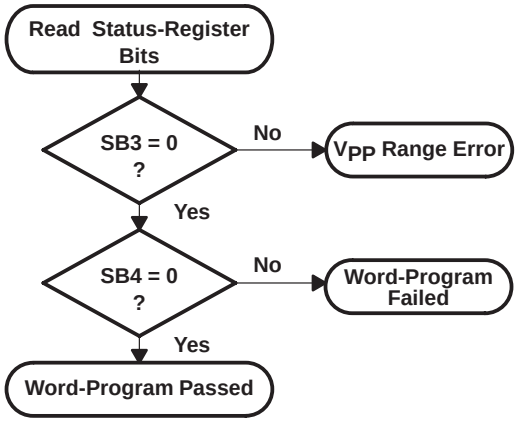
NOTES: A. Full status-register check can be done after each byte or after a sequence of bytes.
B. SB3 must be cleared before attempting additional program/erase operations.
C. SB4 is cleared only by the clear-status-register command, but it does not prevent additional program operation attempts.

Figure 3. Automated Byte-Programming Flow Chart



BUS OPERATION	COMMAND	COMMENTS
Write	Write program setup	Data = 40h or 10h Addr = Address of word to be programmed
Write	Write data	Data = Word to be programmed Addr = Address of word to be programmed
Read		Status-register data. Toggle $\overline{OE}$ or $\overline{CE}$ to update status register.
Standby		Check SB7 1 = Ready, 0 = Busy
Repeat for subsequent words. Write FFh after the last word-programming operation to reset the device to read-array mode.		

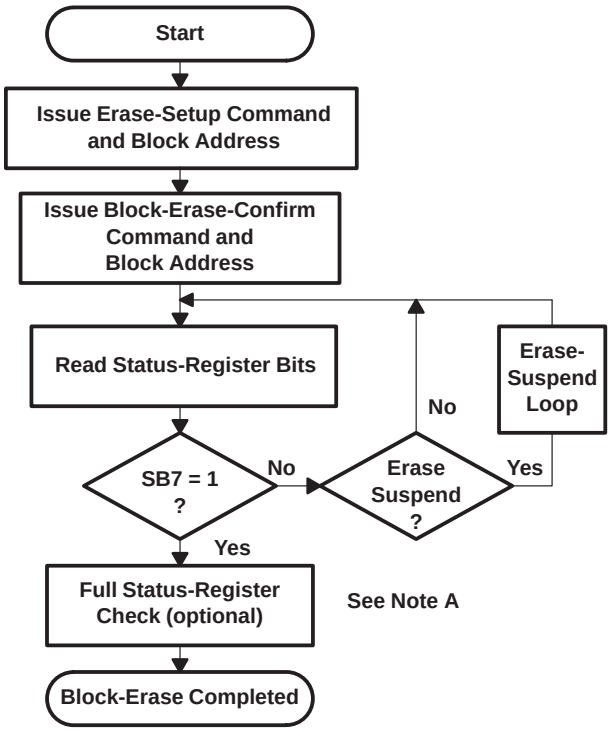
FULL STATUS-REGISTER-CHECK FLOW



BUS OPERATION	COMMAND	COMMENTS
Standby		Check SB3 1 = Detect V_{PP} low (see Note B)
Standby		Check SB4 1 = Word-program error (see Note C)

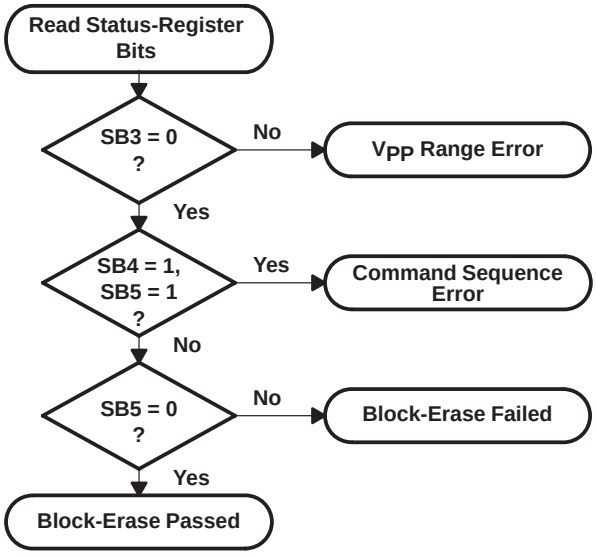
NOTES: A. Full status-register check can be done after each word or after a sequence of words.
B. SB3 must be cleared before attempting additional program/erase operations.
C. SB4 is cleared only by the clear-status-register command, but it does not prevent additional program operation attempts.

Figure 4. Automated Word-Programming Flow Chart



BUS OPERATION	COMMAND	COMMENTS
Write	Write erase setup	Data = 20h Block Addr = Address within block to be erased
Write	Erase	Data = D0h Block Addr = Address within block to be erased
Read		Status-register data. Toggle $\overline{OE}$ or $\overline{CE}$ to update status register
Standby		Check SB7 1 = Ready, 0 = Busy
Repeat for subsequent blocks. Write FFh after the last block-erase operation to reset the device to read-array mode		

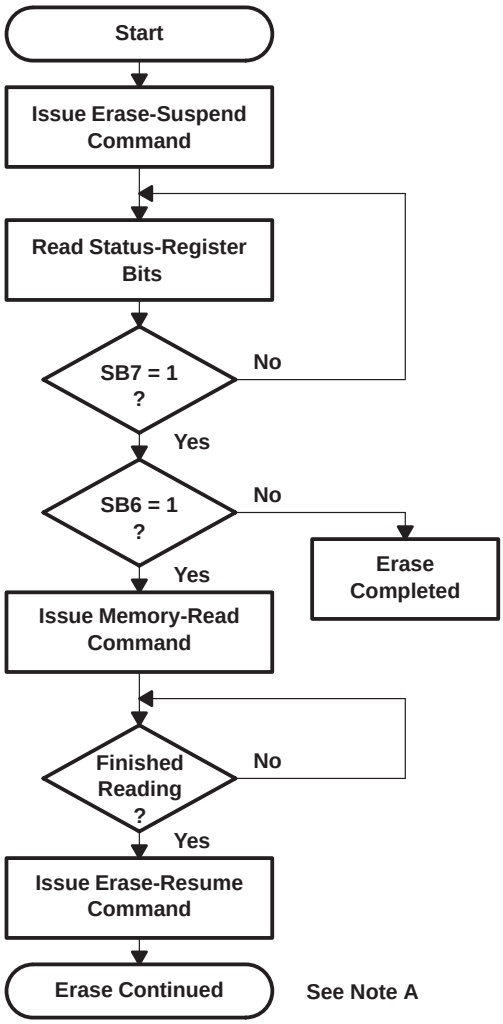
FULL STATUS-REGISTER-CHECK FLOW



BUS OPERATION	COMMAND	COMMENTS
Standby		Check SB3 1 = Detect V_{PP} low (see Note B)
Standby		Check SB4 and SB5 1 = Block-erase error
Standby		Check SB5 1 = Block-erase error (see Note C)

NOTES: A. Full status-register check can be done after each block or after a sequence of blocks.
B. SB3 must be cleared before attempting additional program/erase operations.
C. SB5 is cleared only by the clear-status-register command in cases where multiple blocks are erased before full status is checked.

Figure 5. Automated Block-Erase Flow Chart



BUS OPERATION	COMMAND	COMMENTS
Write	Erase suspend	Data = B0h
Read		Status-register data. Toggle $\overline{OE}$ or $\overline{CE}$ to update status register
Standby		Check SB7 1 = Ready
Standby		Check SB6 1 = Suspended
Write	Read memory	Data = FFh
Read		Read data from block other than that being erased.
Write	Erase resume	Data = D0h

NOTE A: See block-erase flow chart for complete erasure procedure

Figure 6. Erase-Suspend/Erase-Resume Flow Chart

absolute maximum ratings over ambient temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 4) . . . . . – 0.6 V to 7 V
Supply voltage range, V_{PP} (see Note 4) . . . . . – 0.6 V to 14 V
Input voltage range: All inputs except A9, $\overline{RP}$ . . . . . – 0.6 V to V_{CC} + 1 V
$\overline{RP}$, A9 (see Note 5) . . . . . – 0.6 V to 13.5 V
Output voltage range (see Note 6) . . . . . – 0.6 V to V_{CC} + 1 V
Ambient temperature range, T_A, during read/erase/program: L suffix . . . . . 0°C to 70°C
E suffix . . . . . – 40°C to 85°C
Storage temperature range, T_{stg} . . . . . – 65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 4. All voltage values are with respect to V_{SS}.
5. The voltage on any input or output can undershoot to – 2 V for periods of less than 20 ns. See Figure 7.
6. The voltage on any input or output can overshoot to 2 V for periods of less than 20 ns. See Figure 8.

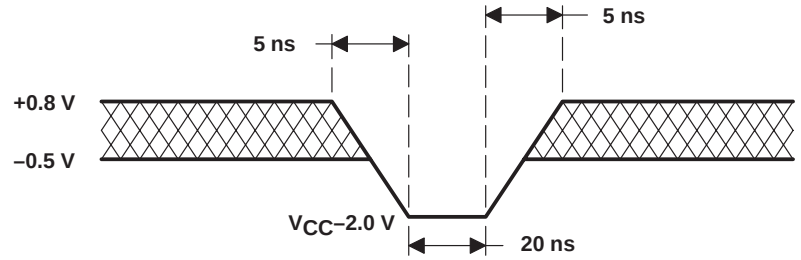


Figure 7. Maximum Negative Overshoot Waveform

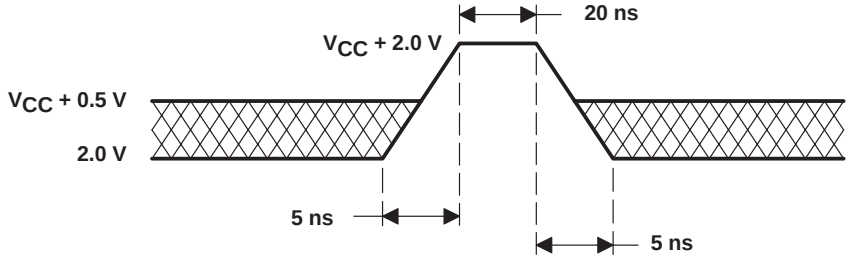
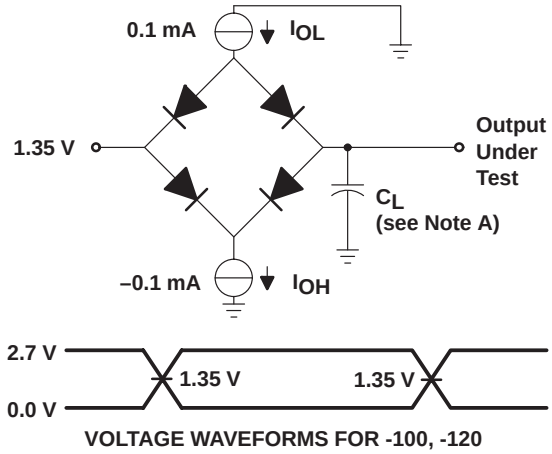


Figure 8. Maximum Positive Overshoot Waveform

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS FOR -100, -120

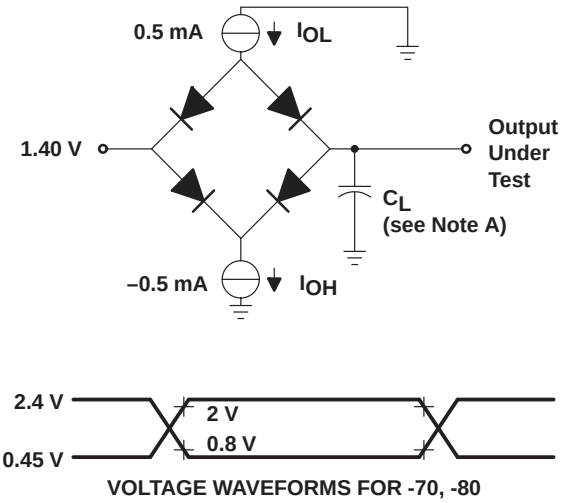
Conditions: V_{IH} = 2.7 V
V_{IL} = 0 V
C_L = 30 pF

Measurements taken at: 1.35 V for logic high
1.35 V for logic low

Input rise and fall = <5 ns

NOTES: A. C_L includes probe and fixture capacitance.
B. Each device should have a 0.1-µF ceramic capacitor connected between V_{CC} and V_{SS}, as closely as possible to the device pins.

Figure 9. 3-V Testing Load Circuit and Voltage Waveform



VOLTAGE WAVEFORMS FOR -70, -80

Conditions: V_{IH} = 2.45 V
V_{IL} = 0.45 V
C_L = 100 pF

Measurements taken at: 2.0 V for logic high
0.8 V for logic low

Input rise and fall = <20 ns

NOTES: A. C_L includes probe and fixture capacitance.
B. Each device should have a 0.1-µF ceramic capacitor connected between V_{CC} and V_{SS}, as closely as possible to the device pins.

Figure 10. 5-V Testing Load Circuit and Voltage Waveform

recommended operating conditions

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	During write/read/erase/erase suspend	3 V_{CC}	2.7	3	3.6	V
			3.3 V_{CC}	3	3.3	3.6	
			5 V_{CC}	4.5	5	5.5	
V_{PP}	Supply voltage	During read only (V_{PPL})		0		6.5	V
		During write/erase/erase suspend, V_{PP} can have V_{CC} as MIN or NOM	3 V_{PP}	3.0	3.3	3.6	V
			5 V_{PP}	4.5	5	5.5	
			12 V_{PP}	11.4	12	12.6	
V_{IH}	High-level dc input voltage		TTL	2		V_{CC} + 0.5	V
			CMOS	V_{CC} – 0.2		V_{CC} + 0.2	
V_{IL}	Low-level dc input voltage		TTL	– 0.5		0.8	V
			CMOS	V_{SS} – 0.2		V_{SS} + 0.2	
V_{LKO}	V_{CC} lock-out voltage from write/erase (see Note 7)			1.2			V
V_{HH}	$\overline{RP}$ unlock voltage			11.4	12	13	V
V_{PPLK}	V_{PP} lock-out voltage from write/erase (see Note 7)			0		1.5	V
T_A	Ambient temperature during read/erase/program:		L Suffix	0		70	°C
			E Suffix	–40		85	°C

NOTE 7: Typical values shown are at T_A = 25°C.

word/byte typical write and block-erase performance (see Notes 7 and 8)

	MIN	TYP	MAX	UNIT
Main-block erase time		2.4		s
Main-block byte-program time		1.7		s
Main-block word-program time		1.1		s
Parameter/boot-block erase time		0.84		s

NOTES: 7. Typical values shown are at T_A = 25°C.
8. Excludes system-level overhead (all times in seconds)

electrical characteristics over recommended ranges of supply voltage and ambient temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		TMS28F800AEy AND TMS28008AEy TMS28F800ASyAND TMS28F008ASy				UNIT
					TMS28F800AVy TMS28F008AVy		TMS28F800AZy TMS28F008AZy		
					3 V/3.3 V		5 V		
					MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	TTL	V_{CC} = V_{CC} MIN, I_{OH} = – 2.5 mA (5 V) V_{CC} = V_{CC} MIN, I_{OH} = –2 µA (3 V)		2.4		2.4		V
		CMOS	V_{CC} = V_{CC} MIN, I_{OH} = – 100 µA		V_{CC} – 0.4	0.55 V_{CC}	V_{CC} – 0.4	0.55 V_{CC}	
V_{OL}	Low-level output voltage		V_{CC} = V_{CC} MIN, I_{OL} = 5.8 mA			0.45		0.45	V
V_{ID}	A9 selection-code voltage		During read algorithm-selection mode		11.4	12.6	11.4	12.6	V
I_I	Input current (leakage), except for A9 when A9 = V_{ID} (see Note 9)		V_{CC} = V_{CC} MAX, V_I = 0 V to V_{CC} MAX,			±1		±1	µA
I_{ID}	A9 selection-code current		A9 = V_{ID}			500		500	µA
I_{RP}	$\overline{RP}$ boot-block unlock current		$\overline{RP}$ = V_{HH}			500		500	µA
I_O	Output current (leakage)		V_{CC} = V_{CC} MAX, V_O = 0 V to V_{CC} MAX			±10		±10	µA
I_{PPR}	V_{PP} read current		V_{PP} ≥ V_{PPH}[2] (at 12 V)			200		200	µA
I_{PPS}	V_{PP} standby current (standby)		V_{PP} ≤ V_{CC}			10		10	µA
I_{PPL}	V_{PP} supply current (reset/deep power-down mode)		$\overline{RP}$ = V_{SS} ± 0.2 V, V_{PP} ≤ V_{CC}			5		5	µA
I_{PP1}	V_{PP} supply current (active read)		V_{PP} ≥ V_{CC}			200		200	µA
I_{PP2}	V_{PP} supply current (active byte-write) (see Notes 10 and 11)		Programming in progress			30		30	mA
I_{PP3}	V_{PP} supply current (active word-write) (see Notes 10 and 11)		Programming in progress			30		30	mA
I_{PP4}	V_{PP} supply current (block-erase) (see Notes 10 and 11)		Block-erase in progress			30		30	mA
I_{PP5}	V_{PP} supply current (erase-suspend) (see Notes 10 and 11)		Block-erase suspended			200		200	µA
I_{CCS}	V_{CC} supply current (standby)	TTL-input level	V_{CC} = V_{CC} MAX $\overline{CE}$ = $\overline{RP}$ = V_{IH}			1.5		2	mA
		CMOS-input level	V_{CC} = V_{CC} MAX, $\overline{CE}$ = $\overline{RP}$ = V_{CC} ± 0.2 V			110		130	µA
I_{CCL}	V_{CC} supply current (reset/deep power-down mode)		$\overline{RP}$ = V_{SS} ± 0.2 V	0°C to 70°C		8		8	µA
				– 40°C to 85°C		8		8	

NOTES: 9. DQ15/A_{-1} is tested for output leakage only.
10. Characterization data available
11. All ac current values are RMS unless otherwise noted.

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electrical characteristics over recommended ranges of supply voltage and ambient temperature (unless otherwise noted) (continued)

PARAMETER			TEST CONDITIONS		TMS28F800AEy AND TMS28008AEy TMS28F800ASy AND TMS28F008ASy				UNIT
					TMS28F800AVy TMS28F008AVy		TMS28F800AZy TMS28F008AZy		
					3 V/3.3 V		5 V		
					MIN	MAX	MIN	MAX	
I_{CC1}	V_{CC} supply current (active read)	TTL-input level	V_{CC} MAX, $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH} = 5 MHz (3 V)	I_{OUT} = 0 mA, 10 MHz (5 V)		30		30	mA
		CMOS-input level	V_{CC} MAX, $\overline{CE}$ = GND, f = 5 MHz (3 V)	I_{OUT} = 0 mA, $\overline{OE}$ = V_{CC} 10 MHz (5 V)		30		30	mA
I_{CC2}	V_{CC} supply current (active byte-write) (see Notes 9, 10, and 11)		V_{CC} = V_{CC} MAX,	Programming in progress		60		60	mA
I_{CC3}	V_{CC} supply current (active word-write) (see Notes 9, 10, and 11)		V_{CC} = V_{CC} MAX,	Programming in progress		60		60	mA
I_{CC4}	V_{CC} supply current (block-erase) (see Notes 9, 10, and 11)		V_{CC} = V_{CC} MAX,	Block-erase in progress		60		60	mA
I_{CC5}	V_{CC} supply current (erase-suspend) (see Notes 9 and 10)		V_{CC} = V_{CC} MAX,	Block-erase suspended		8		8	mA

NOTES: 9. DQ15/A_{-1} is tested for output leakage only.
10. Characterization data available
11. All ac current values are RMS unless otherwise noted.

power-up and reset switching characteristics for TMS28F008ASy or ’AEy and TMS28F800ASy or ’AEy over recommended ranges of supply voltage (commercial and extended temperature ranges) (see Notes 10, 11, and 12)

PARAMETER		ALT. SYMBOL	’28F008AEy70 ’28F800AEy70 ’28F008ASy70 ’28F800ASy70				’28F008AEy80 ’28F800AEy80 ’28F008ASy80 ’28F800ASy80				UNIT
			3 V/3.3-V V_{CC} RANGE		5-V V_{CC} RANGE		3 V/3.3-V V_{CC} RANGE		5-V V_{CC} RANGE		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{su(VCC)}$	Setup time, $\overline{RP}$ low to V_{CC} at 3 V MIN or 3.6 V MAX) (see Note 13)	t_{PL5V} t_{PL3V}	0		0		0		0		ns
$t_{a(DV)}$	Address valid to data valid	t_{AVQV}		100		70		120		80	ns
$t_{su(DV)}$	Setup time, $\overline{RP}$ high to data valid	t_{PHQV}		800		450		800		450	ns
$t_{h(RP5)}$	Hold time, V_{CC} at 4.5 V (MIN) to $\overline{RP}$ high	t_{5VPH}	2		2		2		2		µs
$t_{h(RP3)}$	Hold time, V_{CC} at 3 V (MIN) to $\overline{RP}$ high	t_{3VPH}	2		2		2		2		µs

NOTES: 10. Characterization data available
11. All ac current values are RMS unless otherwise noted.
12. $\overline{E}$ and $\overline{G}$ are switched low after power up.
13. The power supply can switch low concurrently with $\overline{RP}$ going low.

switching characteristics for TMS28F008ASy or 'AEy and TMS28F800ASy or 'AEy over recommended ranges of supply voltage (commercial and extended temperature ranges)

read operations

PARAMETER		ALT. SYMBOL	'28F008ASy70 '28F800ASy70		'28F008AEy70 '28F800AEy70		'28F008ASy80 '28F800ASy80		'28F008AEy80 '28F800AEy80		UNIT
			3 V		5 V		3 V		5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time, from A0–A18 (see Note 14)	t_{AVQV}		100		70		120		80	ns
$t_{a(E)}$	Access time, from $\overline{CE}$	t_{ELQV}		100		70		120		80	ns
$t_{a(G)}$	Access time, from $\overline{OE}$	t_{GLQV}		65		35		65		40	ns
$t_{c(R)}$	Cycle time, read	t_{AVAV}	100		70		120		80		ns
$t_{d(E)}$	Delay time, $\overline{CE}$ low to low-impedance output	t_{ELQX}	0		0		0		0		ns
$t_{d(G)}$	Delay time, $\overline{OE}$ low to low-impedance output	t_{GLQX}	0		0		0		0		ns
$t_{dis(E)}$	Disable time, $\overline{CE}$ to high-impedance output	t_{EHQZ}		55		25		55		30	ns
$t_{dis(G)}$	Disable time, $\overline{OE}$ to high-impedance output	t_{GHQZ}		45		25		45		30	ns
$t_{h(D)}$	Hold time, DQ valid from A0–A17, $\overline{CE}$, or $\overline{OE}$, whichever occurs first (see Note 14)	t_{AXQX}	0		0		0		0		ns
$t_{su(EB)}$	Setup time, $\overline{BYTE}$ from $\overline{CE}$ low	t_{ELFL} t_{ELFH}		7		5		5		5	ns
$t_{d(RP)}$	Delay time, output from $\overline{RP}$ high	t_{PHQV}		800		450		800		450	ns
$t_{dis(BL)}$	Disable time, $\overline{BYTE}$ low to DQ8–DQ15 in the high-impedance state	t_{FLQZ}		100		70		120		80	ns
$t_{a(BH)}$	Access time, from $\overline{BYTE}$ going high	t_{FHQV}		100		70		120		80	ns

NOTE 14: For 28F800 (8-bit configuration) A_{-1}, A_{-1}–A18 with A_{-1} as LSB address. For 28F008 (16-bit configuration): A0–A19 with A0 as LSB address.

timing requirements for TMS28F008ASy or ’AEy and TMS28F800ASy or ’AEy (commercial and extended temperature ranges)

write/erase operations — $\overline{WE}$-controlled writes

		ALT. SYMBOL	’28F008ASy70 ’28F800ASy70		’28F008AEy70 ’28F800AEy70		’28F008ASy80 ’28F800ASy80		’28F008AEy80 ’28F800AEy80		UNIT
			3 V		5 V		3 V		5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(W)}$	Cycle time, write	t_{AVAV}	100		70		120		80		ns
$t_{c(W)OP}$	Cycle time, duration of programming operation	t_{WHQV1}	6		6		6		6		µs
$t_{c(W)ERB}$	Cycle time, erase operation (boot block)	t_{WHQV2}	0.3		0.3		0.3		0.3		s
$t_{c(W)ERP}$	Cycle time, erase operation (parameter block)	t_{WHQV3}	0.3		0.3		0.3		0.3		s
$t_{c(W)ERM}$	Cycle time, erase operation (main block)	t_{WHQV4}	0.6		0.6		0.6		0.6		s
$t_{d(RPR)}$	Delay time, boot-block relock	t_{PHBR}		200		100		200		100	ns
$t_{h(A)}$	Hold time, A0–A18 (see Note 14)	t_{WHAX}	0		0		0		0		ns
$t_{h(D)}$	Hold time, DQ valid	t_{WHDX}	0		0		0		0		ns
$t_{h(E)}$	Hold time, $\overline{CE}$	t_{WHEH}	0		0		0		0		ns
$t_{h(VPP)}$	Hold time, V_{PP} from valid status-register bit	t_{QVVL}	0		0		0		0		ns
$t_{h(RP)}$	Hold time, $\overline{RP}$ at V_{HH} from valid status-register bit	t_{QVPH}	0		0		0		0		ns
$t_{h(WP)}$	Hold time, $\overline{WP}$ from valid status-register bit	t_{WHPL}	0		0		0		0		ns
$t_{su(WP)}$	Setup time, $\overline{WP}$ before write operation	t_{ELPH}	90		50		100		50		ns
$t_{su(A)}$	Setup time, A0–A17 (see Note 14)	t_{AVWH}	90		50		100		50		ns
$t_{su(D)}$	Setup time, DQ	t_{DVWH}	90		50		100		50		ns
$t_{su(E)}$	Setup time, $\overline{CE}$ before write operation	t_{ELWL}	0		0		0		0		ns
$t_{su(RP)}$	Setup time, $\overline{RP}$ at V_{HH} to $\overline{WE}$ going high	t_{PHHWH}	200		100		100		100		ns
$t_{su(VPP)1}$	Setup time, V_{PP} to $\overline{WE}$ going high	t_{VPWH}	200		100		100		100		ns
$t_{w(W)}$	Pulse duration, $\overline{WE}$ low	t_{WLWH}	90		50		100		50		ns
$t_{w(WH)}$	Pulse duration, $\overline{WE}$ high	t_{WLWL}	20		10		30		30		ns
$t_{rec(RPHW)}$	Recovery time, $\overline{RP}$ high to $\overline{WE}$ going low	t_{PHWL}	1.5		450		1.5		450		µs

NOTE 14: For 28F800 (8-bit configuration) A_{-1}, A_{-1}–A18 with A_{-1} as LSB address. For 28F008 (16-bit configuration): A0–A19 with A0 as LSB address.

timing requirements for TMS28F008ASy or 'AEy and TMS28F800ASy or 'AEy (commercial and extended temperature ranges)

write/erase operations — $\overline{CE}$-controlled writes

		ALT. SYMBOL	'28F008ASy70 '28F800ASy70		'28F008AEy70 '28F800AEy70		'28F008ASy80 '28F800ASy80		'28F008AEy80 '28F800AEy80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(E)}$	Cycle time, write	t_{AVAV}	100		70		120		80		ns
$t_{c(E)OP}$	Cycle time, duration of programming operation	t_{EHQV1}	6		6		6		6		µs
$t_{c(E)ERB}$	Cycle time, erase operation (boot block)	t_{EHQV2}	0.3		0.3		0.3		0.3		s
$t_{c(E)ERP}$	Cycle time, erase operation (parameter block)	t_{EHQV3}	0.3		0.3		0.3		0.3		s
$t_{c(E)ERM}$	Cycle time, erase operation (main block)	t_{EHQV4}	0.6		0.6		0.6		0.6		s
$t_{d(RPR)}$	Delay time, boot-block relock	t_{PHBR}		200		100		200		100	ns
$t_{h(A)}$	Hold time, A0–A18 (see Note 14)	t_{EHAX}	0		0		0		0		ns
$t_{h(D)}$	Hold time, DQ valid	t_{EHDX}	0		0		0		0		ns
$t_{h(W)}$	Hold time, $\overline{WE}$	t_{EHWH}	0		0		0		0		ns
$t_{h(VPP)}$	Hold time, V_{PP} from valid status-register bit	t_{QVVL}	0		0		0		0		ns
$t_{h(RP)}$	Hold time, $\overline{RP}$ at V_{HH} from valid status-register bit	t_{QVPH}	0		0		0		0		ns
$t_{h(WP)}$	Hold time, $\overline{WP}$ from valid status-register bit	t_{WHPL}	0		0		0		0		ns
$t_{su(WP)}$	Setup time, $\overline{WP}$ before write operation	t_{ELPH}	90		50		100		50		ns
$t_{su(A)}$	Setup time, A0–A18 (see Note 14)	t_{AVEH}	90		50		100		50		ns
$t_{su(D)}$	Setup time, DQ	t_{DVEH}	90		50		100		50		ns
$t_{su(W)}$	Setup time, $\overline{WE}$ before write operation	t_{WLEL}	0		0		0		0		ns
$t_{su(RP)}$	Setup time, $\overline{RP}$ at V_{HH} to $\overline{CE}$ going high	t_{PHHEH}	200		100		100		100		ns
$t_{su(VPP)2}$	Setup time, V_{PP} to $\overline{CE}$ going high	t_{VPEH}	200		100		100		100		ns
$t_{w(E)}$	Pulse duration, $\overline{CE}$ low	t_{ELEH}	90		50		100		50		ns
$t_{w(EH)}$	Pulse duration, $\overline{CE}$ high	t_{EHEL}	20		10		30		30		ns
$t_{rec(RPHE)}$	Recovery time, $\overline{RP}$ high to $\overline{CE}$ going low	t_{PHEL}	1.5		450		1.5		450		µs

NOTE 14: For 28F800 (8-bit configuration) A_{-1}, A_{-1}–A18 with A_{-1} as LSB address. For 28F008 (16-bit configuration): A0–A19 with A0 as LSB address.

power-up and reset switching characteristics for TMS28F008AVy or 'ALy and TMS28F800AVy or 'ALy over recommended ranges of supply voltage (commercial and extended temperature ranges) (see Notes 10, 11, and 12)

PARAMETER		ALT. SYMBOL	'28F008AVy100 '28F800AVy100 '28F008ALy100 '28F800ALy100		'28F008AVy120 '28F800AVy120 '28F008ALy120 '28F800ALy120		UNIT
			3.3-V V_{CC} RANGE		3.3-V V_{CC} RANGE		
			MIN	MAX	MIN	MAX	
$t_{su(VCC)}$	Setup time, $\overline{RP}$ low to V_{CC} at 3 V MIN or 3.6 V MAX (see Note 13)	t_{PL5V} t_{PL3V}	0		0		ns
$t_{a(DV)}$	Access time, address valid to data valid	t_{AVQV}		100		120	ns
$t_{su(DV)}$	Setup time, $\overline{RP}$ high before data valid	t_{PHQV}		800		800	ns
$t_{h(RP3)}$	Hold time, V_{CC} at 3 V (MIN) to $\overline{RP}$ high	t_{3VPH}	2		2		µs

NOTES: 10. Characterization data available
11. All ac current values are RMS unless otherwise noted.
12. $\overline{E}$ and $\overline{G}$ are switched low after power up.
13. The power supply can switch low concurrently with $\overline{RP}$ going low.

switching characteristics for TMS28F008AVy or 'ALy and TMS28F800AV or 'ALy over recommended ranges of supply voltage (commercial and extended temperature ranges)

read operations

PARAMETER		ALT. SYMBOL	'28F008AVy100 '28F800AVy100 '28F008ALy100 '28F800ALy100		'28F008AVy120 '28F800AVy120 '28F008ALy120 '28F800ALy120		UNIT
			3 V		3 V		
			MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time, from A0–A18 (see Note 14)	t_{AVQV}		100		120	ns
$t_{a(E)}$	Access time, from $\overline{CE}$	t_{ELQV}		100		120	ns
$t_{a(G)}$	Access time, from $\overline{OE}$	t_{GLQV}		65		65	ns
$t_{c(R)}$	Cycle time, read	t_{AVAV}	100		120		ns
$t_{d(E)}$	Delay time, $\overline{CE}$ low to low-impedance output	t_{ELQX}	0		0		ns
$t_{d(G)}$	Delay time, $\overline{OE}$ low to low-impedance output	t_{GLQX}	0		0		ns
$t_{dis(E)}$	Disable time, $\overline{CE}$ to high-impedance output	t_{EHQZ}		55		55	ns
$t_{dis(G)}$	Disable time, $\overline{OE}$ to high-impedance output	t_{GHQZ}		45		45	ns
$t_{h(D)}$	Hold time, DQ valid from A0–A17, $\overline{CE}$, or $\overline{OE}$, whichever occurs first (see Note 14)	t_{AXQX}	0		0		ns
$t_{su(EB)}$	Setup time, $\overline{BYTE}$ from $\overline{CE}$ low	t_{ELFL} t_{ELFH}		7		5	ns
$t_{d(RP)}$	Delay time, output from $\overline{RP}$ high	t_{PHQV}		800		800	ns
$t_{dis(BL)}$	Disable time, $\overline{BYTE}$ low to DQ8–DQ15 in the high-impedance state	t_{FLQZ}		100		120	ns
$t_{a(BH)}$	Access time, from $\overline{BYTE}$ going high	t_{FHQV}		100		120	ns

NOTE 14: For 28F800 (8-bit configuration) A_{-1}, A_{-1}–A18 with A_{-1} as LSB address. For 28F008 (16-bit configuration): A0–A19 with A0 as LSB address.

timing requirements for TMS28F008AVy or ’ALy and TMS28F800AVy or ’ALy (commercial and extended temperature ranges)

write/erase operations — $\overline{WE}$-controlled writes

		ALT. SYMBOL	’28F008AVy100 ’28F800AVy100 ’28F008ALy100 ’28F800ALy100		’28F008AVy120 ’28F800AVy120 ’28F008ALy120 ’28F800ALy120		UNIT
			3 V		3 V		
			MIN	MAX	MIN	MAX	
$t_{c(W)}$	Cycle time, write	t_{AVAV}	100		120		ns
$t_{c(W)OP}$	Cycle time, duration of programming operation	t_{WHQV1}	6		6		µs
$t_{c(W)ERB}$	Cycle time, erase operation (boot block)	t_{WHQV2}	0.3		0.3		s
$t_{c(W)ERP}$	Cycle time, erase operation (parameter block)	t_{WHQV3}	0.3		0.3		s
$t_{c(W)ERM}$	Cycle time, erase operation (main block)	t_{WHQV4}	0.6		0.6		s
$t_{d(RPR)}$	Delay time, boot-block relock	t_{PHBR}		200		200	ns
$t_{h(A)}$	Hold time, A0–A18 (see Note 14)	t_{WHAX}	0		0		ns
$t_{h(D)}$	Hold time, DQ valid	t_{WHDX}	0		0		ns
$t_{h(E)}$	Hold time, $\overline{CE}$	t_{WHEH}	0		0		ns
$t_{h(VPP)}$	Hold time, V_{PP} from valid status-register bit	t_{QVVL}	0		0		ns
$t_{h(RP)}$	Hold time, $\overline{RP}$ at V_{HH} from valid status-register bit	t_{QVPH}	0		0		ns
$t_{h(WP)}$	Hold time, $\overline{WP}$ from valid status-register bit	t_{WHPL}	0		0		ns
$t_{su(WP)}$	Setup time, $\overline{WP}$ before write operation	t_{ELPH}	90		100		ns
$t_{su(A)}$	Setup time, A0–A17 (see Note 14)	t_{AVWH}	90		100		ns
$t_{su(D)}$	Setup time, DQ	t_{DVWH}	90		100		ns
$t_{su(E)}$	Setup time, $\overline{CE}$ before write operation	t_{ELWL}	0		0		ns
$t_{su(RP)}$	Setup time, $\overline{RP}$ at V_{HH} to $\overline{WE}$ going high	t_{PHHWH}	200		100		ns
$t_{su(VPP)1}$	Setup time, V_{PP} to $\overline{WE}$ going high	t_{VPWH}	200		100		ns
$t_{w(W)}$	Pulse duration, $\overline{WE}$ low	t_{WLWH}	90		100		ns
$t_{w(WH)}$	Pulse duration, $\overline{WE}$ high	t_{WLWL}	20		30		ns
$t_{rec(RPHW)}$	Recovery time, $\overline{RP}$ high to $\overline{WE}$ going low	t_{PHWL}	1.5		1.5		µs

NOTE 14: For 28F800 (8-bit configuration) A_{-1}, A_{-1}–A18 with A_{-1} as LSB address. For 28F008 (16-bit configuration): A0–A19 with A0 as LSB address.

timing requirements for TMS28F008AVy or ’ALy and TMS28F800AVy or ’ALy (commercial and extended temperature ranges) (continued)

write/erase operations — $\overline{CE}$-controlled writes

		ALT. SYMBOL	’28F008AVy100 ’28F800AVy100 ’28F008ALy100 ’28F800ALy100		’28F008AVy80 ’28F800AVy80 ’28F008ALy80 ’28F800ALy80		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(E)}$	Cycle time, write	t_{AVAV}	100		120		ns
$t_{c(E)OP}$	Cycle time, duration of programming operation	t_{EHQV1}	6		6		µs
$t_{c(E)ERB}$	Cycle time, erase operation (boot block)	t_{EHQV2}	0.3		0.3		s
$t_{c(E)ERP}$	Cycle time, erase operation (parameter block)	t_{EHQV3}	0.3		0.3		s
$t_{c(E)ERM}$	Cycle time, erase operation (main block)	t_{EHQV4}	0.6		0.6		s
$t_{d(RPR)}$	Delay time, boot-block relock	t_{PHBR}		200		200	ns
$t_{h(A)}$	Hold time, A0–A18 (see Note 14)	t_{EHAX}	0		0		ns
$t_{h(D)}$	Hold time, DQ valid	t_{EHDX}	0		0		ns
$t_{h(W)}$	Hold time, $\overline{WE}$	t_{EHWH}	0		0		ns
$t_{h(VPP)}$	Hold time, V_{PP} from valid status-register bit	t_{QVVL}	0		0		ns
$t_{h(RP)}$	Hold time, $\overline{RP}$ at V_{HH} from valid status-register bit	t_{QVPH}	0		0		ns
$t_{h(WP)}$	Hold time, $\overline{WP}$ from valid status-register bit	t_{WHPL}	0		0		ns
$t_{su(WP)}$	Setup time, $\overline{WP}$ before write operation	t_{ELPH}	90		100		ns
$t_{su(A)}$	Setup time, A0–A18 (see Note 14)	t_{AVEH}	90		100		ns
$t_{su(D)}$	Setup time, DQ	t_{DVEH}	90		100		ns
$t_{su(W)}$	Setup time, $\overline{WE}$ before write operation	t_{WLEL}	0		0		ns
$t_{su(RP)}$	Setup time, $\overline{RP}$ at V_{HH} to $\overline{CE}$ going high	t_{PHHEH}	200		100		ns
$t_{su(VPP)2}$	Setup time, V_{PP} to $\overline{CE}$ going high	t_{VPEH}	200		100		ns
$t_{w(E)}$	Pulse duration, $\overline{CE}$ low	t_{ELEH}	90		100		ns
$t_{w(EH)}$	Pulse duration, $\overline{CE}$ high	t_{EHEL}	20		30		ns
$t_{rec(RPHE)}$	Recovery time, $\overline{RP}$ high to $\overline{CE}$ going low	t_{PHEL}	1.5		1.5		µs

NOTE 14: For 28F800 (8-bit configuration) A_{-1}, A_{-1}–A18 with A_{-1} as LSB address. For 28F008 (16-bit configuration): A0–A19 with A0 as LSB address.

power-up and reset switching characteristics for TMS28F008AZy and TMS28F800AZy over recommended ranges of supply voltage (commercial and extended temperature ranges) (see Notes 10, 11, and 12)

PARAMETER		ALT. SYMBOL	'28F008AZy70 '28F800AZy70		'28F008AZy80 '28F800AZy80		UNIT
			MIN	MAX	MIN	MAX	
$t_{su(VCC)}$	Setup time, $\overline{RP}$ low to V_{CC} at 4.5 V MIN or 5.5 V MAX) (see Note 13)	t_{PL5V}	0		0		ns
$t_{a(DV)}$	Address valid to data valid	t_{AVQV}		70		80	ns
$t_{su(DV)}$	Setup time, $\overline{RP}$ high to data valid	t_{PHQV}		450		450	ns
$t_{h(RP5)}$	Hold time, V_{CC} at 4.5 V (MIN) to $\overline{RP}$ high	t_{5VPH}	2		2		µs

NOTES: 10. Characterization data available
11. All ac current values are RMS unless otherwise noted.
12. $\overline{E}$ and $\overline{G}$ are switched low after power up.
13. The power supply can switch low concurrently with $\overline{RP}$ going low.

switching characteristics for TMS28F008AZy and TMS28F800AZy over recommended ranges of supply voltage (commercial and extended temperature ranges)

read operations

PARAMETER		ALT. SYMBOL	'28F008AZy70 '28F800AZy70		'28F008AZy80 '28F800AZy80		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time, from A0–A18 (see Note 14)	t_{AVQV}		70		80	ns
$t_{a(E)}$	Access time, from $\overline{CE}$	t_{ELQV}		70		80	ns
$t_{a(G)}$	Access time, from $\overline{OE}$	t_{GLQV}		35		40	ns
$t_{c(R)}$	Cycle time, read	t_{AVAV}	70		80		ns
$t_{d(E)}$	Delay time, $\overline{CE}$ low to low-impedance output	t_{ELQX}	0		0		ns
$t_{d(G)}$	Delay time, $\overline{OE}$ low to low-impedance output	t_{GLQX}	0		0		ns
$t_{dis(E)}$	Disable time, $\overline{CE}$ to high-impedance output	t_{EHQZ}		25		30	ns
$t_{dis(G)}$	Disable time, $\overline{OE}$ to high-impedance output	t_{GHQZ}		25		30	ns
$t_{h(D)}$	Hold time, DQ valid from A0–A17, $\overline{CE}$, or $\overline{OE}$, whichever occurs first (see Note 14)	t_{AXQX}	0		0		ns
$t_{su(EB)}$	Setup time, $\overline{BYTE}$ from $\overline{CE}$ low	t_{ELFL} t_{ELFH}		5		5	ns
$t_{d(RP)}$	Delay time, output from $\overline{RP}$ high	t_{PHQV}		450		450	ns
$t_{dis(BL)}$	Disable time, $\overline{BYTE}$ low to DQ8–DQ15 in the high-impedance state	t_{FLQZ}		70		80	ns
$t_{a(BH)}$	Access time, from $\overline{BYTE}$ going high	t_{FHQV}		70		80	ns

NOTE 14: For 28F800 (8-bit configuration) A_{-1}, A_{-1}–A18 with A_{-1} as LSB address. For 28F008 (16-bit configuration): A0–A19 with A0 as LSB address.

timing requirements for TMS28F008AZy and TMS28F800AZy (commercial and extended temperature ranges)

write/erase operations — $\overline{WE}$-controlled writes

		ALT. SYMBOL	'28F008AZy70 '28F800AZy70		'28F008AZy80 '28F800AZy80		UNIT
			5 V		5 V		
			MIN	MAX	MIN	MAX	
$t_{c(W)}$	Cycle time, write	t_{AVAV}	70		80		ns
$t_{c(W)OP}$	Cycle time, duration of programming operation	t_{WHQV1}	6		6		µs
$t_{c(W)ERB}$	Cycle time, erase operation (boot block)	t_{WHQV2}	0.3		0.3		s
$t_{c(W)ERP}$	Cycle time, erase operation (parameter block)	t_{WHQV3}	0.3		0.3		s
$t_{c(W)ERM}$	Cycle time, erase operation (main block)	t_{WHQV4}	0.6		0.6		s
$t_{d(RPR)}$	Delay time, boot-block relock	t_{PHBR}		100		100	ns
$t_{h(A)}$	Hold time, A0–A18 (see Note 14)	t_{WHAX}	0		0		ns
$t_{h(D)}$	Hold time, DQ valid	t_{WHDX}	0		0		ns
$t_{h(E)}$	Hold time, $\overline{CE}$	t_{WHEH}	0		0		ns
$t_{h(VPP)}$	Hold time, V_{PP} from valid status-register bit	t_{QVVL}	0		0		ns
$t_{h(RP)}$	Hold time, $\overline{RP}$ at V_{HH} from valid status-register bit	t_{QVPH}	0		0		ns
$t_{h(WP)}$	Hold time, $\overline{WP}$ from valid status-register bit	t_{WHPL}	0		0		ns
$t_{su(WP)}$	Setup time, $\overline{WP}$ before write operation	t_{ELPH}	50		50		ns
$t_{su(A)}$	Setup time, A0–A17 (see Note 14)	t_{AVWH}	50		50		ns
$t_{su(D)}$	Setup time, DQ	t_{DVWH}	50		50		ns
$t_{su(E)}$	Setup time, $\overline{CE}$ before write operation	t_{ELWL}	0		0		ns
$t_{su(RP)}$	Setup time, $\overline{RP}$ at V_{HH} to $\overline{WE}$ going high	t_{PHHWH}	100		100		ns
$t_{su(VPP)1}$	Setup time, V_{PP} to $\overline{WE}$ going high	t_{VPWH}	100		100		ns
$t_{w(W)}$	Pulse duration, $\overline{WE}$ low	t_{WLWH}	50		50		ns
$t_{w(WH)}$	Pulse duration, $\overline{WE}$ high	t_{WLWL}	10		30		ns
$t_{rec(RPHW)}$	Recovery time, $\overline{RP}$ high to $\overline{WE}$ going low	t_{PHWL}	450		450		µs

NOTE 14: For 28F800 (8-bit configuration) A_{-1}, A_{-1}–A18 with A_{-1} as LSB address. For 28F008 (16-bit configuration): A0–A19 with A0 as LSB address.

timing requirements for TMS28F008AZy and TMS28F800AZy (commercial and extended temperature ranges)

write/erase operations — $\overline{CE}$-controlled writes

		ALT. SYMBOL	'28F008AZy70 '28F800AZy70		'28F008AZy80 '28F800AZy80		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(E)}$	Cycle time, write	t_{AVAV}	70		80		ns
$t_{c(E)OP}$	Cycle time, duration of programming operation	t_{EHQV1}	6		6		µs
$t_{c(E)ERB}$	Cycle time, erase operation (boot block)	t_{EHQV2}	0.3		0.3		s
$t_{c(E)ERP}$	Cycle time, erase operation (parameter block)	t_{EHQV3}	0.3		0.3		s
$t_{c(E)ERM}$	Cycle time, erase operation (main block)	t_{EHQV4}	0.6		0.6		s
$t_{d(RPR)}$	Delay time, boot-block relock	t_{PHBR}		100		100	ns
$t_{h(A)}$	Hold time, A0–A18 (see Note 14)	t_{EHAX}	0		0		ns
$t_{h(D)}$	Hold time, DQ valid	t_{EHDX}	0		0		ns
$t_{h(W)}$	Hold time, $\overline{WE}$	t_{EHWH}	0		0		ns
$t_{h(VPP)}$	Hold time, V_{PP} from valid status-register bit	t_{QVVL}	0		0		ns
$t_{h(RP)}$	Hold time, $\overline{RP}$ at V_{HH} from valid status-register bit	t_{QVPH}	0		0		ns
$t_{h(WP)}$	Hold time, $\overline{WP}$ from valid status-register bit	t_{WHPL}	0		0		ns
$t_{su(WP)}$	Setup time, $\overline{WP}$ before write operation	t_{ELPH}	50		50		ns
$t_{su(A)}$	Setup time, A0–A18 (see Note 14)	t_{AVEH}	50		50		ns
$t_{su(D)}$	Setup time, DQ	t_{DVEH}	50		50		ns
$t_{su(W)}$	Setup time, $\overline{WE}$ before write operation	t_{WLEL}	0		0		ns
$t_{su(RP)}$	Setup time, $\overline{RP}$ at V_{HH} to $\overline{CE}$ going high	t_{PHHEH}	100		100		ns
$t_{su(VPP)2}$	Setup time, V_{PP} to $\overline{CE}$ going high	t_{VPEH}	100		100		ns
$t_{w(E)}$	Pulse duration, $\overline{CE}$ low	t_{ELEH}	50		50		ns
$t_{w(EH)}$	Pulse duration, $\overline{CE}$ high	t_{EHEL}	10		30		ns
$t_{rec(RPHE)}$	Recovery time, $\overline{RP}$ high to $\overline{CE}$ going low	t_{PHEL}	450		450		µs

NOTE 14: For 28F800 (8-bit configuration) A_{-1}, A_{-1}–A18 with A_{-1} as LSB address. For 28F008 (16-bit configuration): A0–A19 with A0 as LSB address.

PARAMETER MEASUREMENT INFORMATION

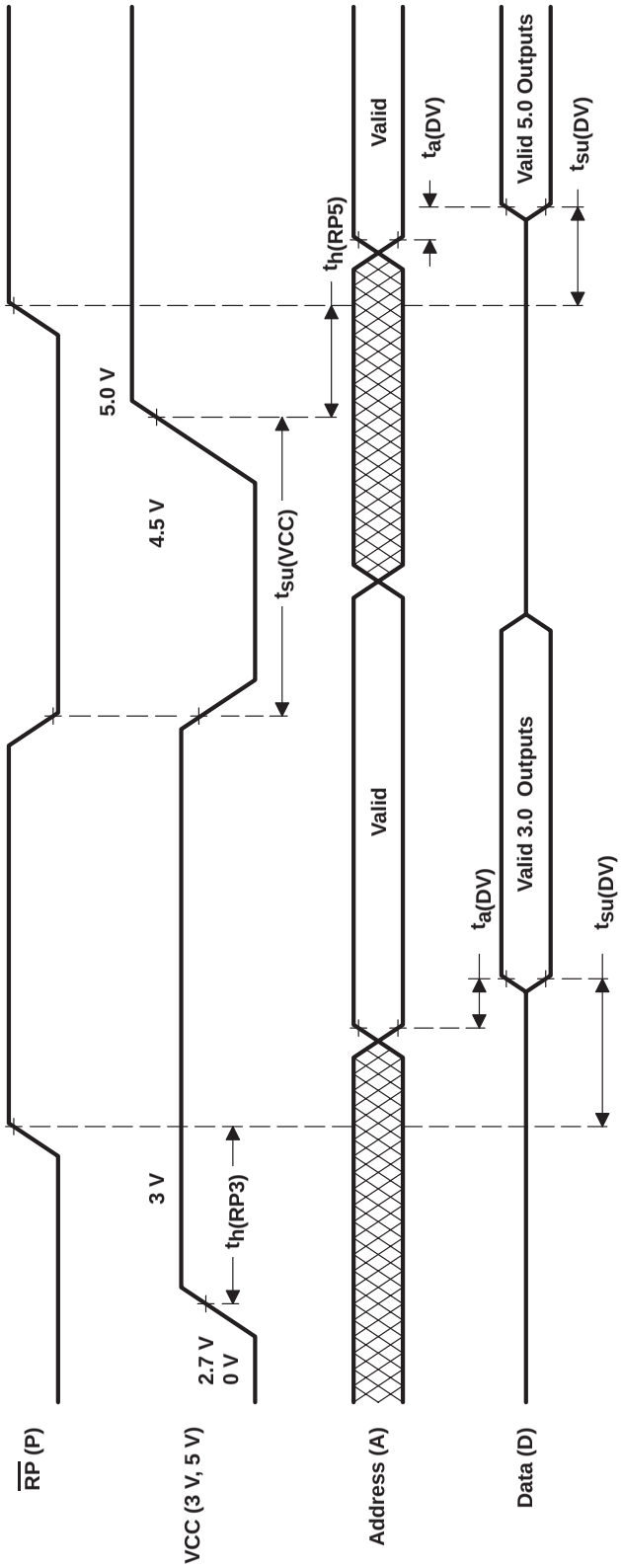


Figure 11. Power-Up Timing and Reset Switching

PARAMETER MEASUREMENT INFORMATION

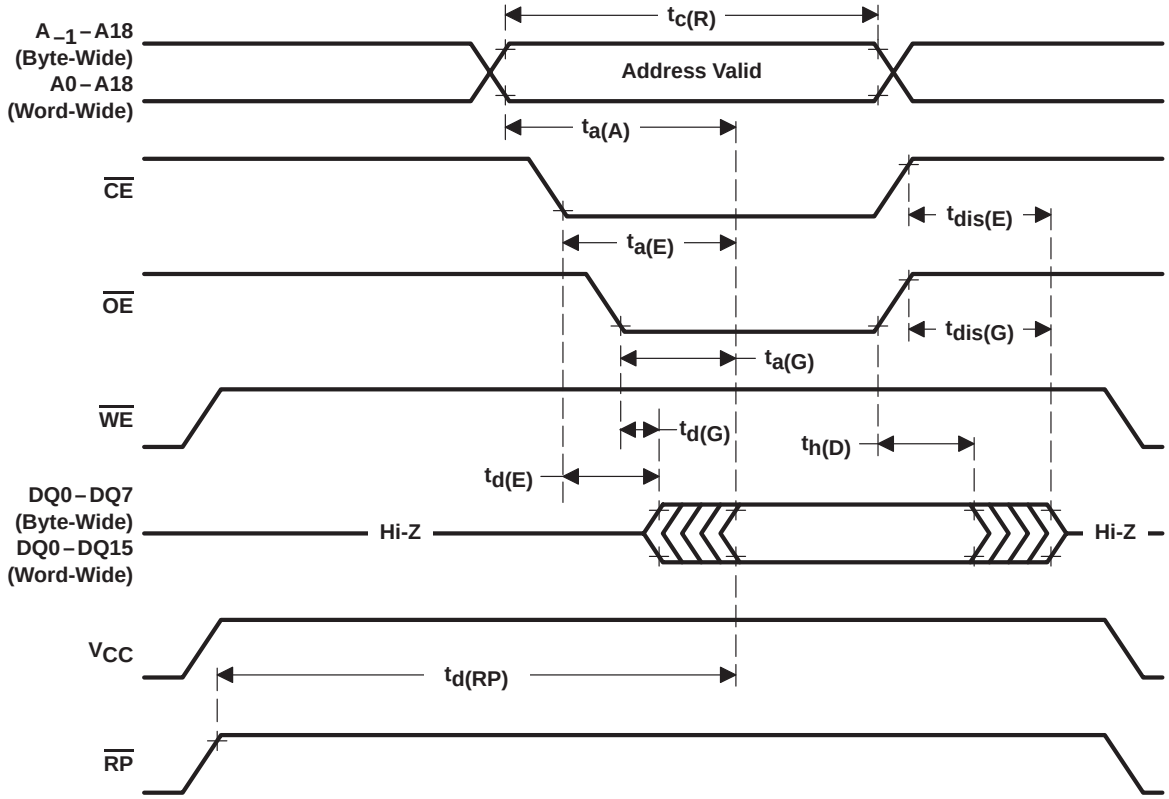


Figure 12. Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

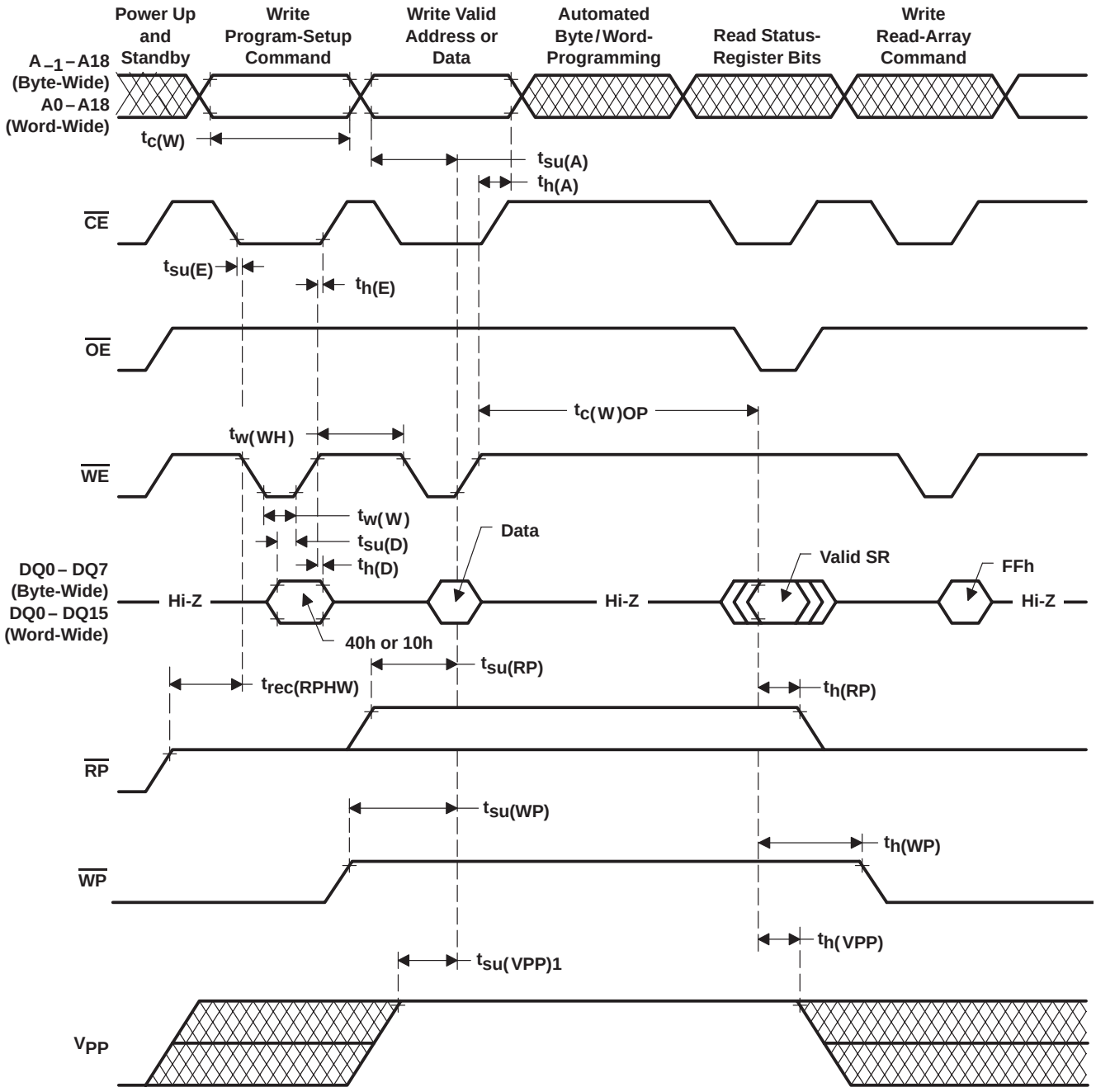


Figure 13. Write-Cycle Timing ($\overline{WE}$-Controlled Write)

PARAMETER MEASUREMENT INFORMATION

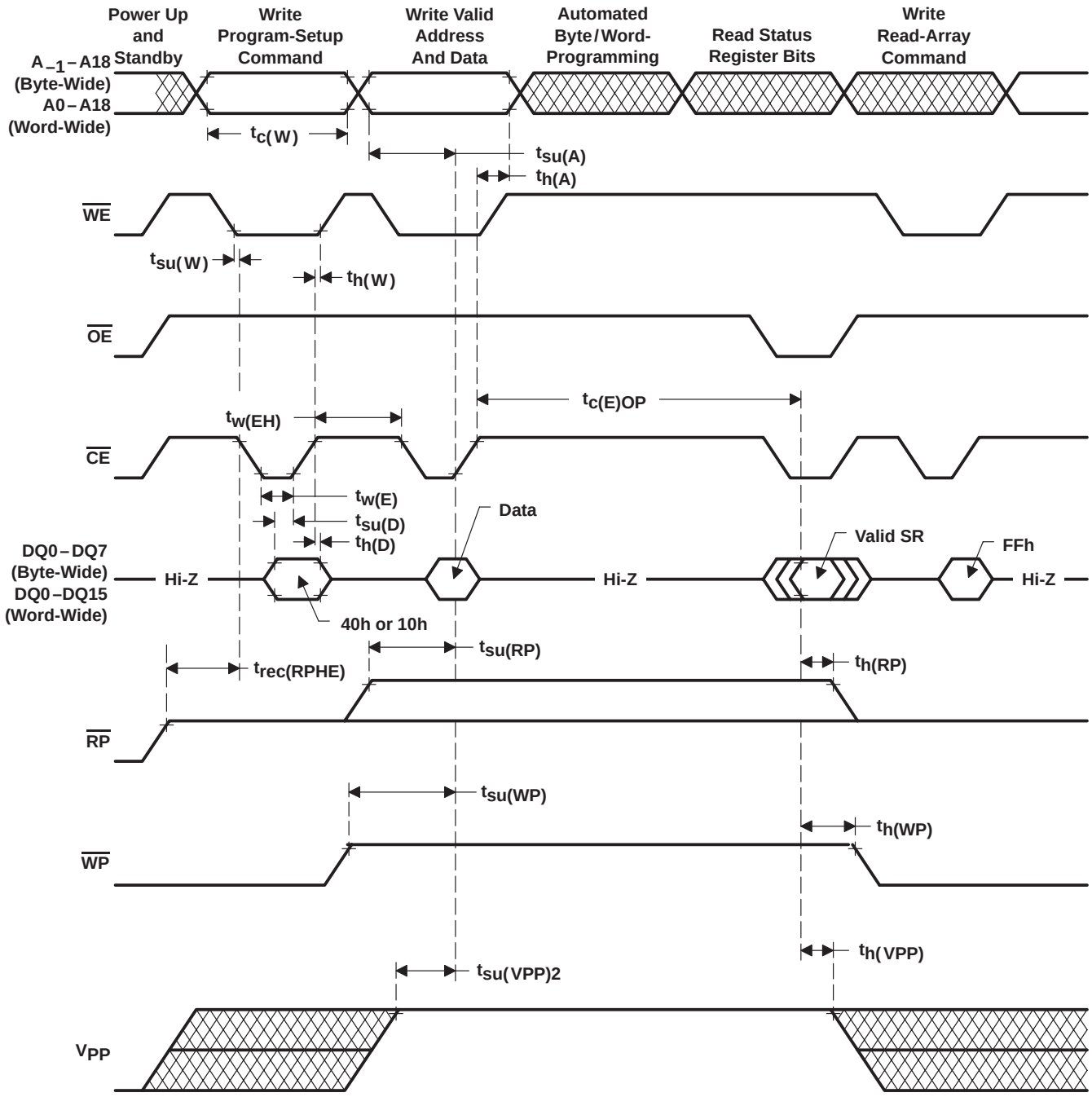


Figure 14. Write-Cycle Timing ($\overline{CE}$-Controlled Write)

PARAMETER MEASUREMENT INFORMATION

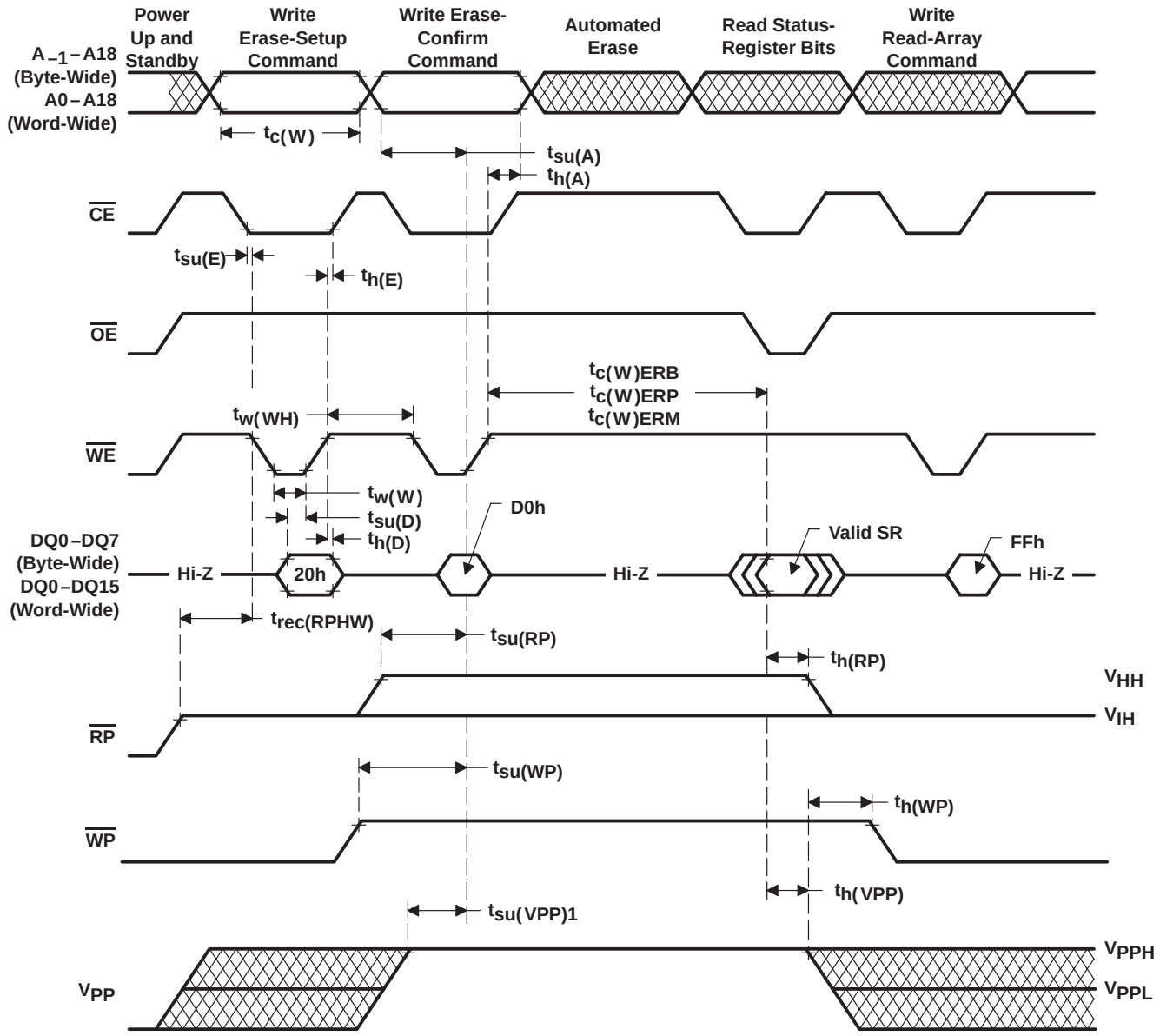


Figure 15. Erase-Cycle Timing ($\overline{WE}$-Controlled Write)

PARAMETER MEASUREMENT INFORMATION

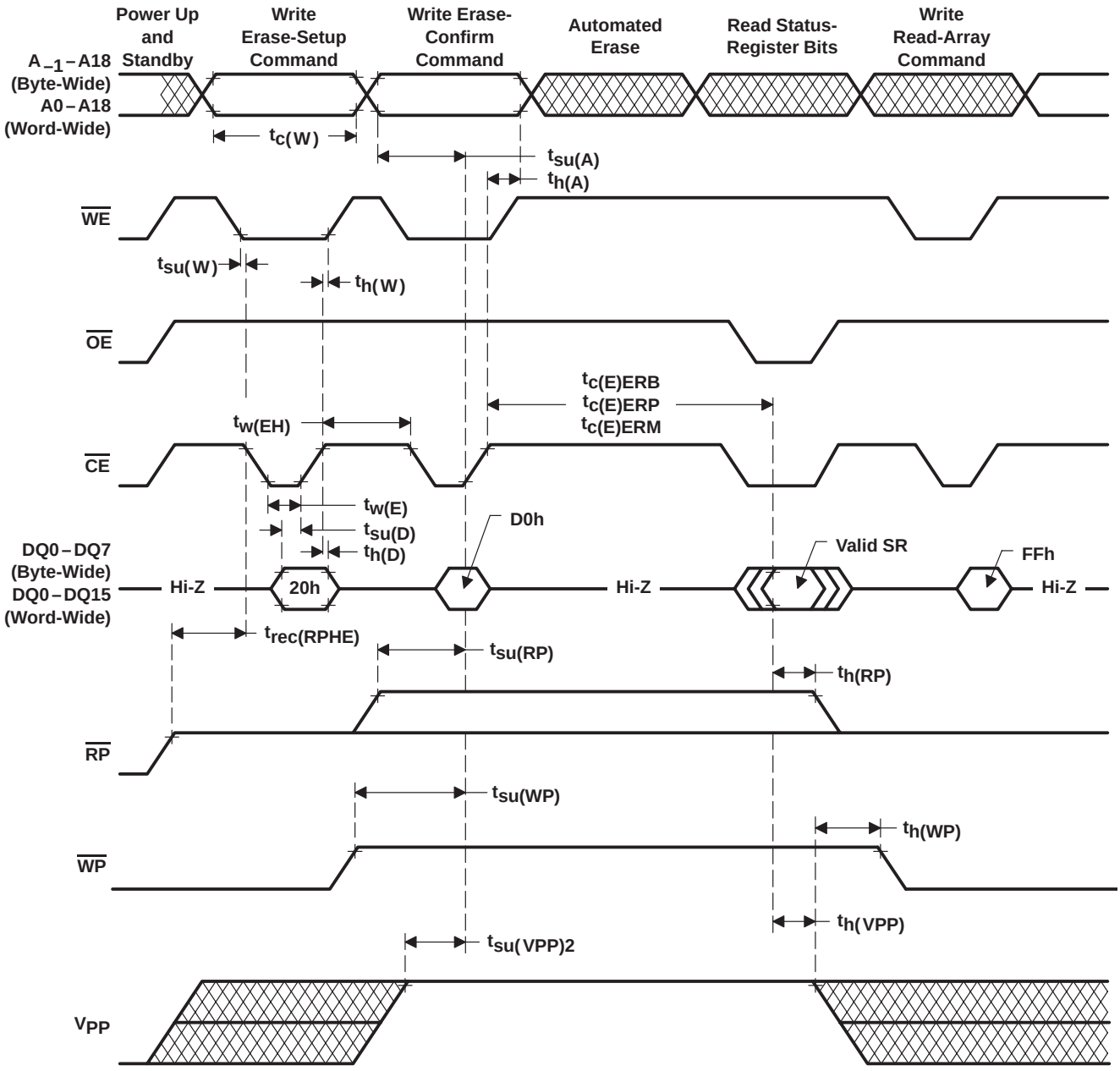


Figure 16. Erase-Cycle Timing ($\overline{CE}$-Controlled Write)

PARAMETER MEASUREMENT INFORMATION

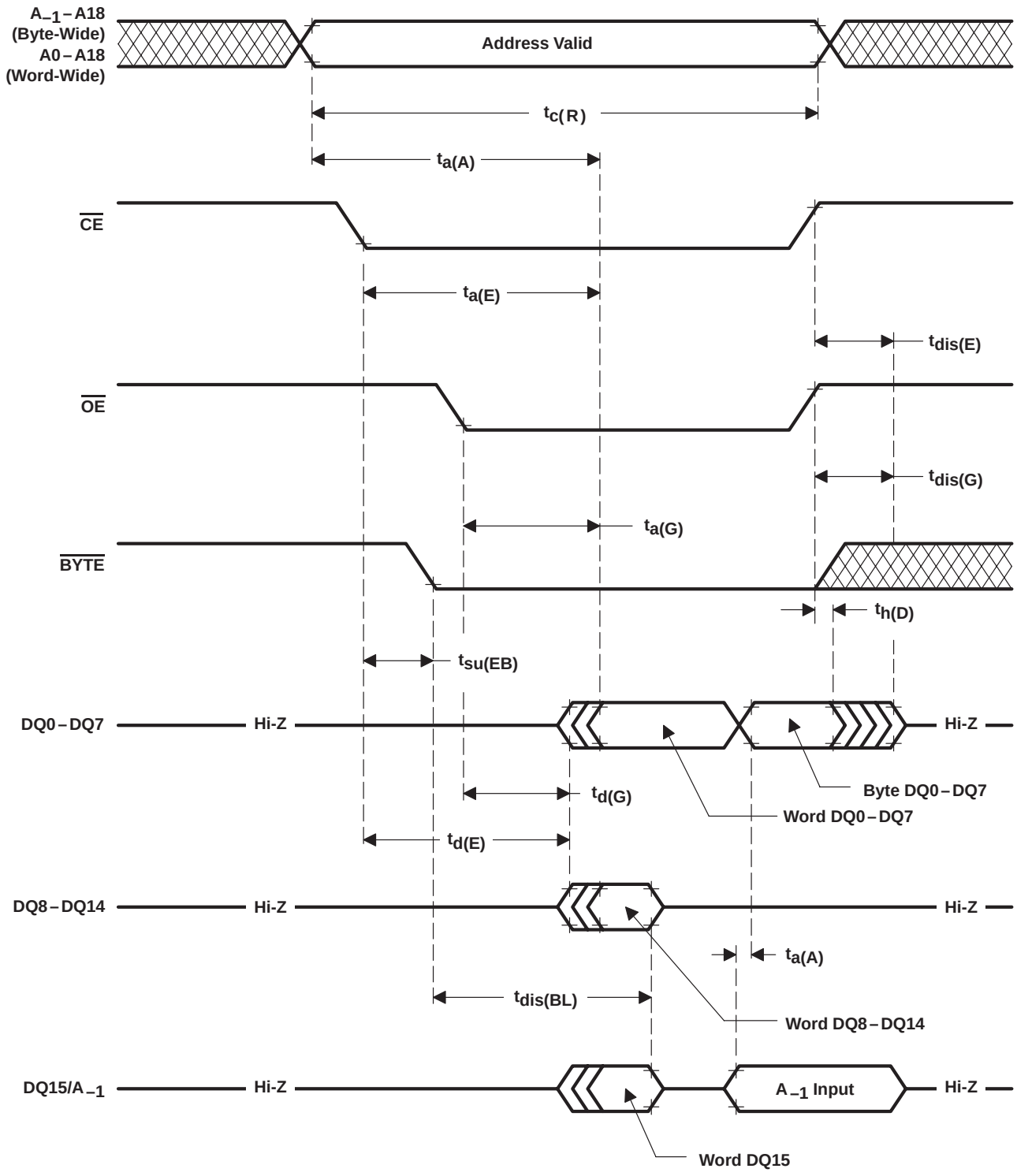


Figure 17. $\overline{\text{BYTE}}$ Timing, Changing From Word-Wide to Byte-Wide Mode

PARAMETER MEASUREMENT INFORMATION

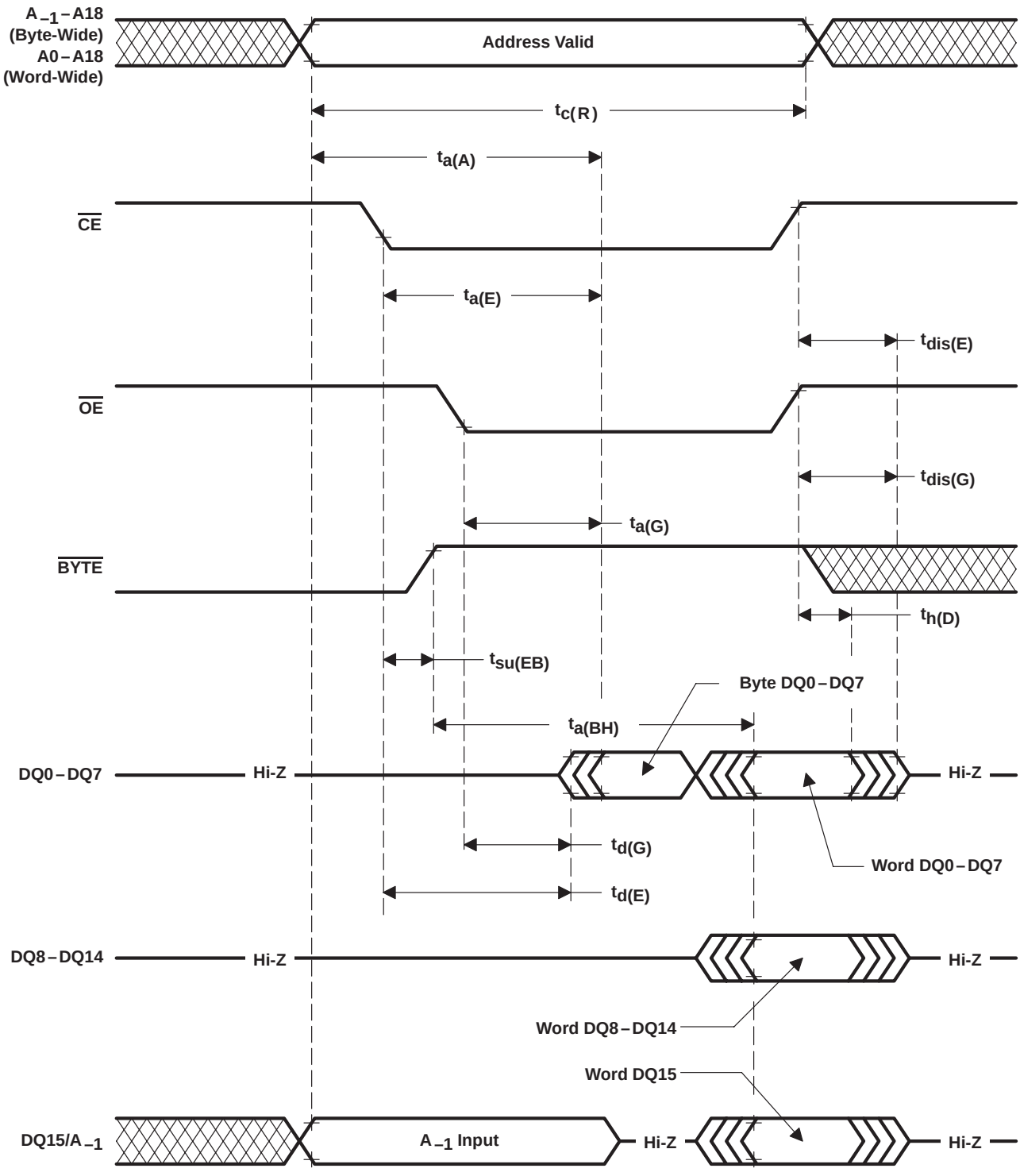
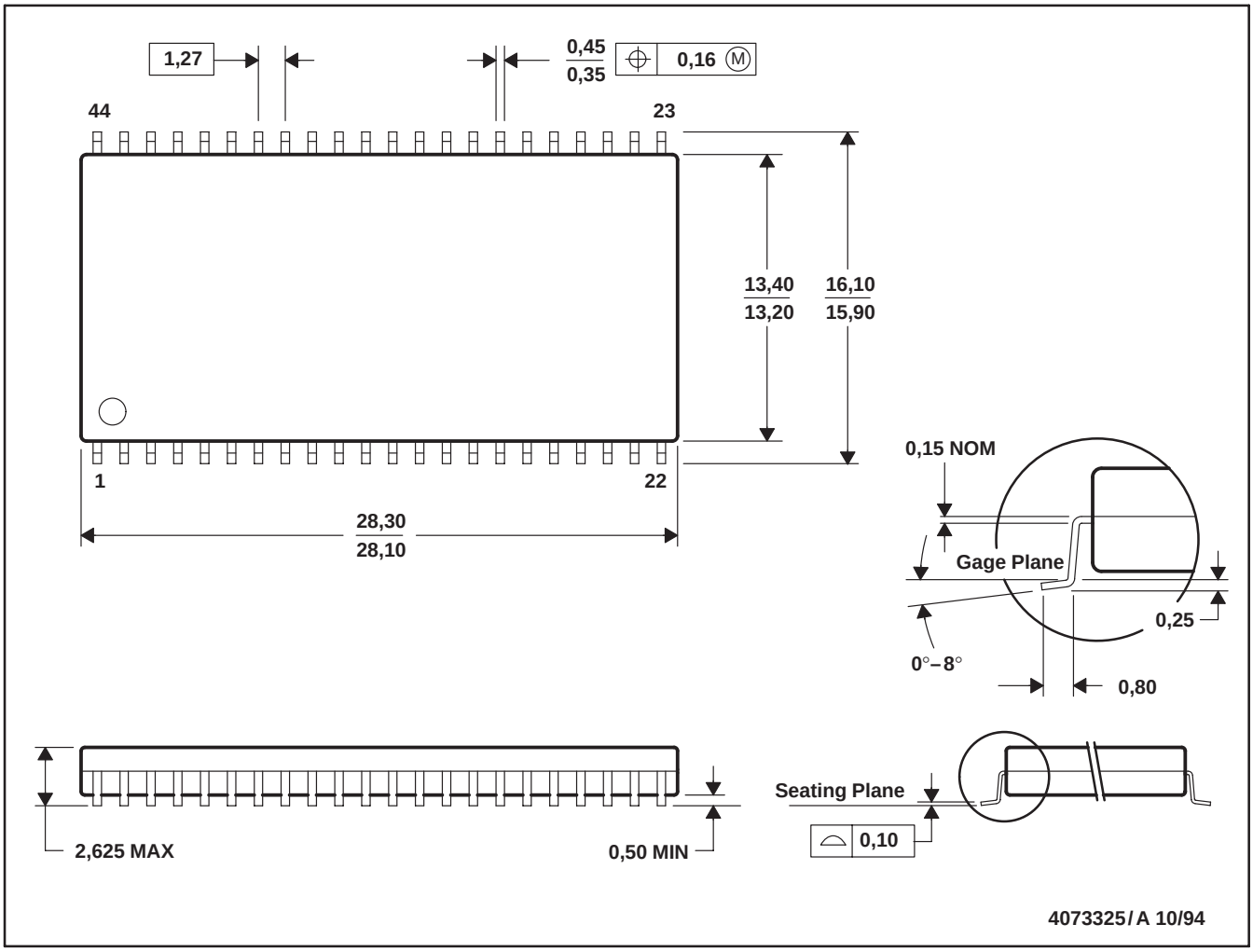


Figure 18. $\overline{\text{BYTE}}$ Timing, Changing From Byte-Wide to Word-Wide Mode

MECHANICAL DATA

DBJ (R-PDSO-G44) **PLASTIC SMALL-OUTLINE PACKAGE**

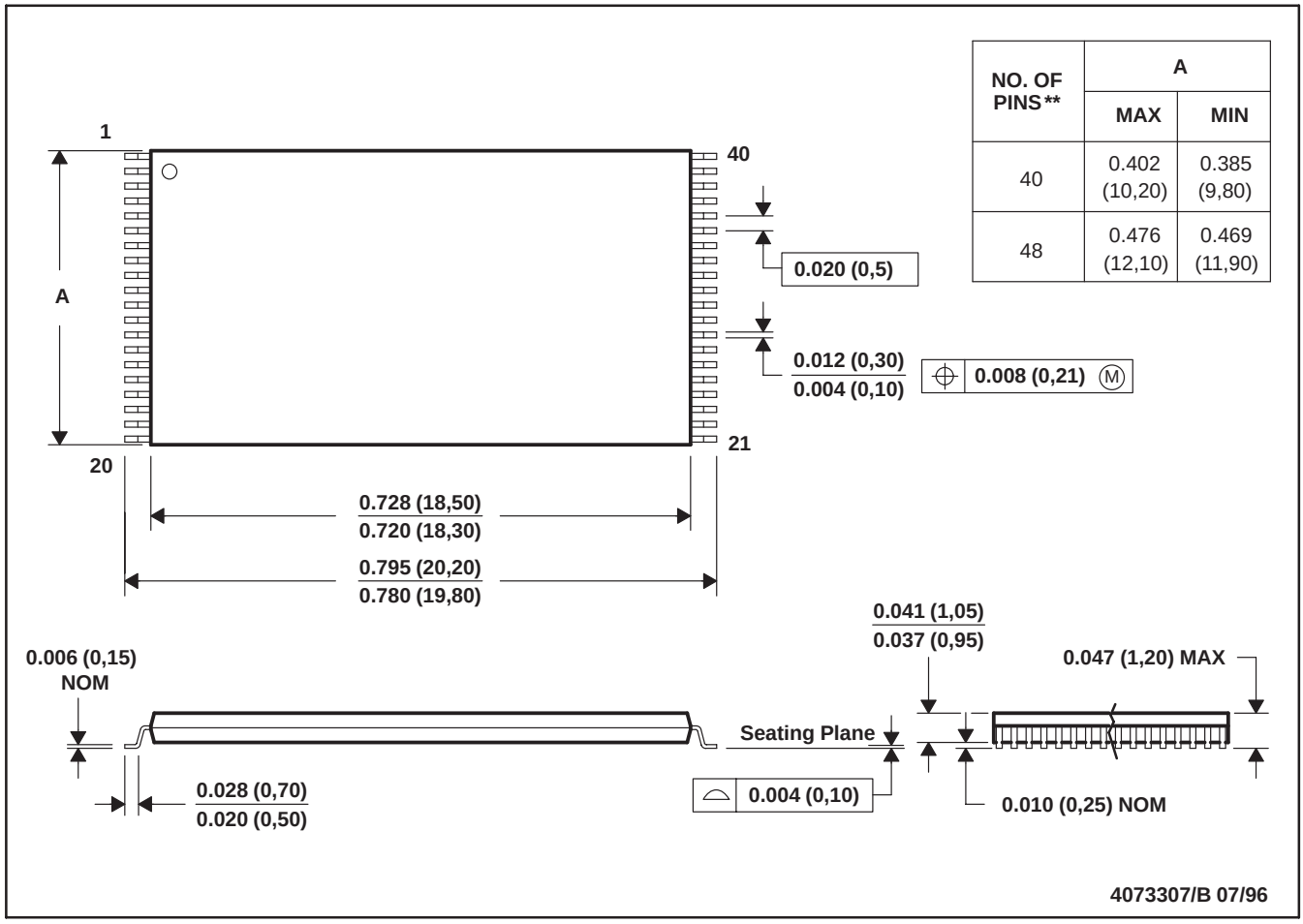


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.

MECHANICAL DATA

DCD (R-PDSO-G)** **PLASTIC DUAL SMALL-OUTLINE PACKAGE**

40 PIN SHOWN



NO. OF PINS**	A	
	MAX	MIN
40	0.402 (10,20)	0.385 (9,80)
48	0.476 (12,10)	0.469 (11,90)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

A

B

C

D

E

F

L

M

O

P

R

S

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