TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

4-MBIT (524,288 WORDS ×8 BITS / 262,144 WORDS ×16 BITS) CMOS FLASH MEMORY

DESCRIPTION

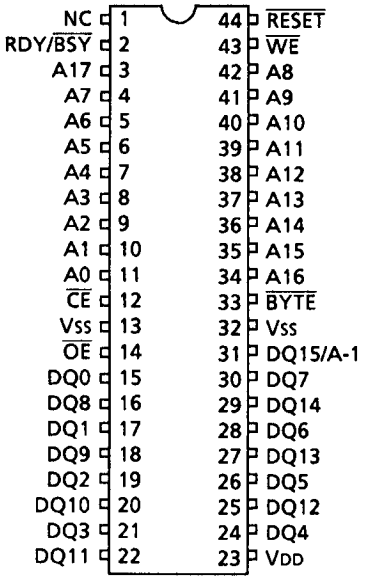
The TC58F400/401 is a 4,194,304-bit electrically erasable and programmable flash memory organized as 524,288 words × 8 bits or 262,144 words × 16 bits. The TC58F400/401 features commands for Read, Program and Erase operations to allow easy interfacing with microprocessors. The commands are based on the JEDEC standard. The Program and Erase operations are automatically executed in the chip. The device has Chip, Block and Multi-Block Erase capability.

The TC58F400/401 is available in either a 44-pin plastic SOP or a 48-pin TSOP package to suit a variety of design applications.

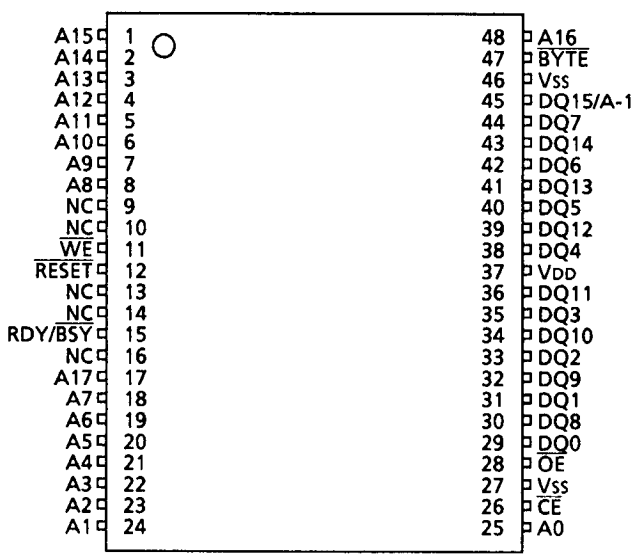
FEATURES

- Power Supply
  V_{DD} = 5.0 V ± 0.5 V
- Organization
  512K×8 bits / 256K×16 bits
- Modes
  Auto Program (byte / word)
  Auto Chip Erase
  Auto Block Erase
  Auto Multiple Block Erase
  Erase Suspend / Resume
  Block Protection
- Block Erase Architecture
  1×16 Kbytes / 2×8 Kbytes / 1×32 Kbytes / 7×64 Kbytes
- Boot Block Architecture
  TC58F400F/FT ····Bottom Boot Block
  TC58F401F/FT ····Top Boot Block
- Mode Control
  Compatible with JEDEC standard commands
- Data Polling, Toggle bit
- Erase / Program Cycles 10^5 Cycles typ.
- Access Time
  90 ns / 100 ns
- Power Dissipation
  1 mA (Standby TTL level)
  100 μA (Standby CMOS level)
  50 mA (Read operation)
  50 mA (Program / Erase operations)
- Packages
  TC58F400F/401F: SOP44 - P - 600 - 1.27
  (Weight: 1.9 g typ.)
  TC58F400FT/401FT: TSOP I 48 - P - 1220 - 0.50
  (Weight: 0.53 g typ.)

PIN ASSIGNMENT (TOP VIEW)



TC58F400F (SOP)
TC58F401F (SOP)

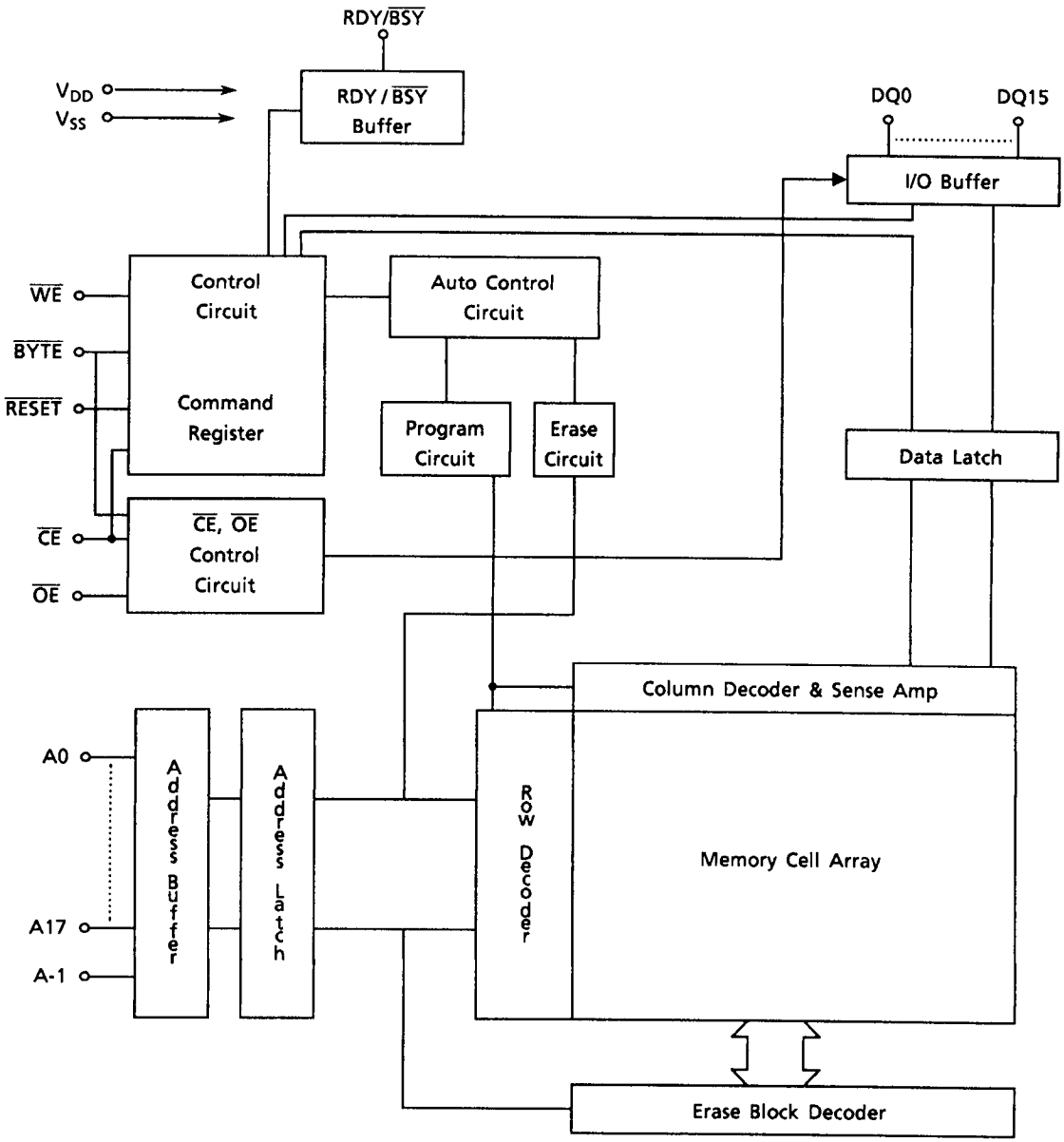


TC58F400FT / TC58F401FT (TSOP)

PIN NAMES

A0 to A17	Address Input
DQ0 toDQ14	Data Input / Output
DQ15/A-1	Output (Input) / Address Input
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{BYTE}$	Word/Byte Select Input
$\overline{WE}$	Write Enable Input
RDY/$\overline{BSY}$	Ready/Busy Output
$\overline{RESET}$	Hardware Reset Input
NC	No Connection
V_{DD}	Power Supply
V_{SS}	Ground

BLOCK DIAGRAM



MODE SELECTION

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0	A1	A6	A9	$\overline{RESET}$	$\overline{BYTE} = V_{IH}$ DQ0 to DQ15	$\overline{BYTE} = V_{IL}$ DQ0 to DQ7
Read	L	L	H	A0	A1	A6	A9	H	D_{OUT}	D_{OUT}
ID Read (1)	L	L	H	L	L	L	V_{ID}	H	Code	Code
ID Read (2)	L	L	H	H	L	L	V_{ID}	H	Code	Code
Standby	H	*	*	*	*	*	*	H	High-Z	High-Z
Output Disable	*	H	H	*	*	*	*	*	High-Z	High-Z
Write	L	H	L	A0	A1	A6	A9	H	D_{IN}	D_{IN}
Block Protect	L	V_{ID}	L	L	H	L	V_{ID}	H	*	*
Block Unprotect	L	V_{ID}	L	L	H	H	V_{ID}	H	*	*
Verify Block Protect	L	L	H	L	H	L	V_{ID}	H	Code	Code
Temporary Block Unprotect	*	*	*	*	*	*	*	V_{ID}	*	*
Reset	*	*	*	*	*	*	*	L	High-Z	High-Z

Notes : DQ8 to 15 are High-Z when $\overline{BYTE} = V_{IL}$

* : High or Low

ID Read (1) : Manufacturer Code

ID Read (2) : Device Code

The Address range is A17 : A-1 in if Byte Mode ($\overline{BYTE} = V_{IL}$)

The Address range is A17 : A0 in if Word Mode ($\overline{BYTE} = V_{IH}$)

ID CODE TABLE

CODE TYPE			A12 to A17	A6	A1	A0	CODE (HEX)
Manufacturer Code			*	V_{IL}	V_{IL}	V_{IL}	0098H
Device Code	TC58F400	Byte	*	V_{IL}	V_{IL}	V_{IH}	38H
		Word					0038H
	TC58F401	Byte	*	V_{IL}	V_{IL}	V_{IH}	68H
		Word					0068H
Verify Block Protect			BA (1)	V_{IL}	V_{IH}	V_{IL}	(2)

Notes: (1) BA: Block Address

(2) Protected Block = 01H (byte), 0001H (word)

Unprotected Block = 00H (byte), 0000H (word)

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	V_{CC} Supply Voltage [1]	−0.6 to 7.0	V
V_{IN}	Input Voltage [1]	−0.6 to V_{DD} + 0.5 (≤ 7.0)	V
V_{DQ}	Input / Output Voltage [1]	−0.6 to V_{DD} + 0.5 (≤ 7.0)	V
P_D	Power Dissipation	0.6	W
T_{SOLDER}	Soldering Temperature (10 s)	260	°C
T_{STG}	Storage Temperature	−55 to 150	°C
T_{OPR}	Operating Temperature	0 to 70	°C
N_{EW}	Erase / Program Cycling Capability	100,000	Cycles
V_{ID}	Maximum Input Voltage [2]	13.0	V
I_{OSHORT}	Output Short Circuit Current [3]	200	mA

1) Minimum DC Voltage is −0.5 V. During transitions, input may undershoot to −2.0 V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{DD} + 0.5 V, which may overshoot to V_{DD} + 2.0 V for periods of less than 20 ns.
2) Maximum voltage on A9, $\overline{OE}$ or $\overline{RESET}$ may overshoot to + 14.0 V for periods of less than 20 ns.
3) Output shorted for no more than one second. No more than one output may be shorted at a time.

CAPACITANCE (Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	CONDITION	TYP.	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	4	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	10	12	pF

* This parameter is periodically sampled and is not tested for every device.

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0 to 70°C)

SYMBOL	PARAMETER		MIN	MAX	UNIT
V_{DD}	V_{DD} Supply Voltage		4.50	5.50	V
V_{IH}	Input High Level Voltage	V_{DD} = 5.0 V ± 0.5 V	2.0	V_{DD} + 0.5	
V_{IL}	Input Low Level Voltage	V_{DD} = 5.0 V ± 0.5 V	−0.5 *1	0.8	
V_{ID}	Voltage for ID Read and Block Protect		11.4	12.6	

*1 Pulse width 20 ns (max)

DC CHARACTERISTICS (Ta = 0 to 70°C, V_{DD} = 5.0 V ± 0.5 V)

SYMBOL	PARAMETER	CONDITION		MIN	MAX	UNIT
I_{LI}	Input Leakage Current	0 V ≤ V_{IN} ≤ V_{DD}		–	± 1	μA
I_{LO}	Output Leakage Current	0 V ≤ V_{OUT} ≤ V_{DD}		–	± 1	
V_{OH1}	Output High Voltage (TTL)	I_{OH} = –2.5 mA		2.4	–	V
V_{OH2}	Output High Voltage (CMOS)	I_{OH} = –100 μA		V_{DD} –0.4	–	
		I_{OH} = –2.5 mA		0.85 V_{DD}	–	
V_{OL}	Output Low Voltage	I_{OL} = 4.0 mA		–	0.45	
I_{DDO1}	V_{DD} Average Read Current (Read)	V_{IN} = V_{IH} / V_{IL}, I_{OUT} = 0 mA, t_{CYCLE} = t_{RC} (min)	×8	–	40	mA
			×16	–	50	
I_{DDO2}	V_{DD} Average Program Current (Program)	V_{IN} = V_{IH} / V_{IL}, I_{OUT} = 0 mA	×8	–	40	
			×16	–	50	
I_{DDO3}	V_{DD} Average Erase Current (Erase)	V_{IN} = V_{IH} / V_{IL}, I_{OUT} = 0 mA		–	50	
I_{DDS1}	V_{DD} Standby Current (TTL)	$\overline{CE}$ = $\overline{RESET}$ = V_{IH} or $\overline{RESET}$ = V_{IL}		–	1	
I_{DDS2}	V_{DD} Standby Current (CMOS)	$\overline{CE}$ = $\overline{RESET}$ = V_{DD} ± 0.2 V or $\overline{RESET}$ = V_{SS} ± 0.2 V		–	100	μA
I_{ID}	High Voltage Input Current	11.4 V ≤ V_{ID} ≤ 12.6 V		–	50	
V_{LKO}	Low V_{DD} Lock-out Voltage			3.2	4.2	V

BLOCK ERASE ADDRESS TABLES

(TOP BOOT BLOCK: TC58F401): BYTE MODE

BLOCK #	A17	A16	A15	A14	A13	A12	ADDRESS RANGE	SIZE
BA0	0	0	0	×	×	×	00000H to 0FFFFH	64 Kbytes
BA1	0	0	1	×	×	×	10000H to 1FFFFH	64 Kbytes
BA2	0	1	0	×	×	×	20000H to 2FFFFH	64 Kbytes
BA3	0	1	1	×	×	×	30000H to 3FFFFH	64 Kbytes
BA4	1	0	0	×	×	×	40000H to 4FFFFH	64 Kbytes
BA5	1	0	1	×	×	×	50000H to 5FFFFH	64 Kbytes
BA6	1	1	0	×	×	×	60000H to 6FFFFH	64 Kbytes
BA7	1	1	1	0	×	×	70000H to 77FFFH	32 Kbytes
BA8	1	1	1	1	0	0	78000H to 79FFFH	8 Kbytes
BA9	1	1	1	1	0	1	7A000H to 7BFFFH	8 Kbytes
BA10	1	1	1	1	1	×	7C000H to 7FFFFH	16 Kbytes

(BOTTOM BOOT BLOCK: TC58F400): BYTE MODE

BLOCK #	A17	A16	A15	A14	A13	A12	ADDRESS RANGE	SIZE
BA0	0	0	0	0	0	×	00000H to 03FFFH	16 Kbytes
BA1	0	0	0	0	1	0	04000H to 05FFFH	8 Kbytes
BA2	0	0	0	0	1	1	06000H to 07FFFH	8 Kbytes
BA3	0	0	0	1	×	×	08000H to 0FFFFH	32 Kbytes
BA4	0	0	1	×	×	×	10000H to 1FFFFH	64 Kbytes
BA5	0	1	0	×	×	×	20000H to 2FFFFH	64 Kbytes
BA6	0	1	1	×	×	×	30000H to 3FFFFH	64 Kbytes
BA7	1	0	0	×	×	×	40000H to 4FFFFH	64 Kbytes
BA8	1	0	1	×	×	×	50000H to 5FFFFH	64 Kbytes
BA9	1	1	0	×	×	×	60000H to 6FFFFH	64 Kbytes
BA10	1	1	1	×	×	×	70000H to 7FFFFH	64 Kbytes

The Address range is A17 : A-1 in if Byte Mode ($\overline{BYTE}$ = V_{IL})

(TOP BOOT BLOCK: TC58F401): WORD MODE

BLOCK #	A17	A16	A15	A14	A13	A12	ADDRESS RANGE	SIZE
BA0	0	0	0	×	×	×	00000H to 07FFFH	32 Kwords
BA1	0	0	1	×	×	×	08000H to 0FFFFH	32 Kwords
BA2	0	1	0	×	×	×	10000H to 10FFFH	32 Kwords
BA3	0	1	1	×	×	×	18000H to 1FFFFH	32 Kwords
BA4	1	0	0	×	×	×	20000H to 27FFFH	32 Kwords
BA5	1	0	1	×	×	×	28000H to 2FFFFH	32 Kwords
BA6	1	1	0	×	×	×	30000H to 37FFFH	32 Kwords
BA7	1	1	1	0	×	×	38000H to 3BFFFH	16 Kwords
BA8	1	1	1	1	0	0	3C000H to 3CFFFH	4 Kwords
BA9	1	1	1	1	0	1	3D000H to 3DFFFH	4 Kwords
BA10	1	1	1	1	1	×	3E000H to 3FFFFH	8 Kwords

(BOTTOM BOOT BLOCK: TC58F400): WORD MODE

BLOCK #	A17	A16	A15	A14	A13	A12	ADDRESS RANGE	SIZE
BA0	0	0	0	0	0	×	00000H to 01FFFH	8 Kwords
BA1	0	0	0	0	1	0	02000H to 02FFFH	4 Kwords
BA2	0	0	0	0	1	1	03000H to 03FFFH	4 Kwords
BA3	0	0	0	1	×	×	04000H to 07FFFH	16 Kwords
BA4	0	0	1	×	×	×	08000H to 0FFFFH	32 Kwords
BA5	0	1	0	×	×	×	10000H to 17FFFH	32 Kwords
BA6	0	1	1	×	×	×	18000H to 1FFFFH	32 Kwords
BA7	1	0	0	×	×	×	20000H to 27FFFH	32 Kwords
BA8	1	0	1	×	×	×	28000H to 3FFFFH	32 Kwords
BA9	1	1	0	×	×	×	30000H to 37FFFH	32 Kwords
BA10	1	1	1	×	×	×	38000H to 3FFFFH	32 Kwords

The Address range is A17 : A0 in if Word Mode ($\overline{BYTE}$ = V_{IH})

COMMAND DEFINITIONS

COMMAND SEQUENCE		BUS WRITE CYCLES REQ'D	FIRST BUS WRITE CYCLE		SECOND BUS WRITE CYCLE		THIRD BUS WRITE CYCLE		FOURTH BUS READ/WRITE CYCLE		FIFTH BUS WRITE CYCLE		SIXTH BUS WRITE CYCLE	
			Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read/Reset		1	XXXXH	F0H										
Read/Reset	Word	3	5555H	AAH	2AAAH	55H	5555H	F0H	RA 1)	RD 2)				
	Byte		AAAAH		5555H		AAAAH							
ID Read/ Verify Block Protection	Word	3	5555H	AAH	2AAAH	55H	5555H	90H	IA 3)	ID 4)				
	Byte		AAAAH		5555H		AAAAH							
Program	Word	4	5555H	AAH	2AAAH	55H	5555H	A0H	PA 5)	PD 6)				
	Byte		AAAAH		5555H		AAAAH							
Chip Erase	Word	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
	Byte		AAAAH		5555H		AAAAH		AAAAH		5555H		AAAAH	
Block Erase	Word	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	BA 7)	30H
	Byte		AAAAH		5555H		AAAAH		AAAAH		5555H			
Block Protect	Word	6	5555H	AAH	2AAAH	55H	5555H	9AH	5555H	AAH	2AAAH	55H	5555H	9AH
	Byte		AAAAH		5555H		AAAAH		AAAAH		5555H		AAAAH	
Block Unprotect	Word	6	5555H	AAH	2AAAH	55H	5555H	6AH	5555H	AAH	2AAAH	55H	5555H	6AH
	Byte		AAAAH		5555H		AAAAH		AAAAH		5555H		AAAAH	
Block Erase Suspend			Erase can be suspended during Block Erase with Addr. : *** 8), Data: B0H.											
Block Erase Resume			Erase can be resumed after suspend with Addr. : *** 8), Data: 30H.											

Notes:
1. RA : Read Address
2. RD : Read Data
3. IA : ID Address (A6, A1, A0)
   0000H = Manufacturer code
   0001H = Device code
   0002H = Verify block protection (A17 to A12 = block address)
4. ID : ID Data
   (0098H - Manufacturer, 0038H - TC58F400, 0068H - TC58F401)
   For a protected block, data = 0001H,
   For an unprotected block, data = 0000H
5. PA : Program Address
6. PD : Program Data
7. BA : Block Address
8. *** : V_{IH} or V_{IL}
9. The system should generate the following address patterns:
   Word mode: 5555H or 2AAAH in addresses A0 to A14.
   Byte mode: AAAAH or 5555H in addresses A-1 to A14.
   The Address range is A17 : A-1 in if Byte Mode ($\overline{BYTE}$ = V_{IL})
   The Address range is A17 : A0 in if Word Mode ($\overline{BYTE}$ = V_{IH})

Table 12. HARDWARE STATUS FLAGS

	STATUS	DQ7	DQ6	DQ5	DQ3
In Progress	Auto - Programming	$\overline{DQ7}$	Toggle	0	0
	Program/Erase in Auto Erase	0	Toggle	0	1
Time Limits Exceeded	Auto - Programming	$\overline{DQ7}$	Toggle	1	1
	Program/Erase in Auto Erase	0	Toggle	1	1

Notes: 1. DQ0, DQ1, DQ2 are pins reserved for future use.
2. DQ8 to DQ15 = Don't care for x 16 mode.
3. DO4, DQ2 to DQ0: High - Z

AC CHARACTERISTICS AND OPERATING CONDITIONS

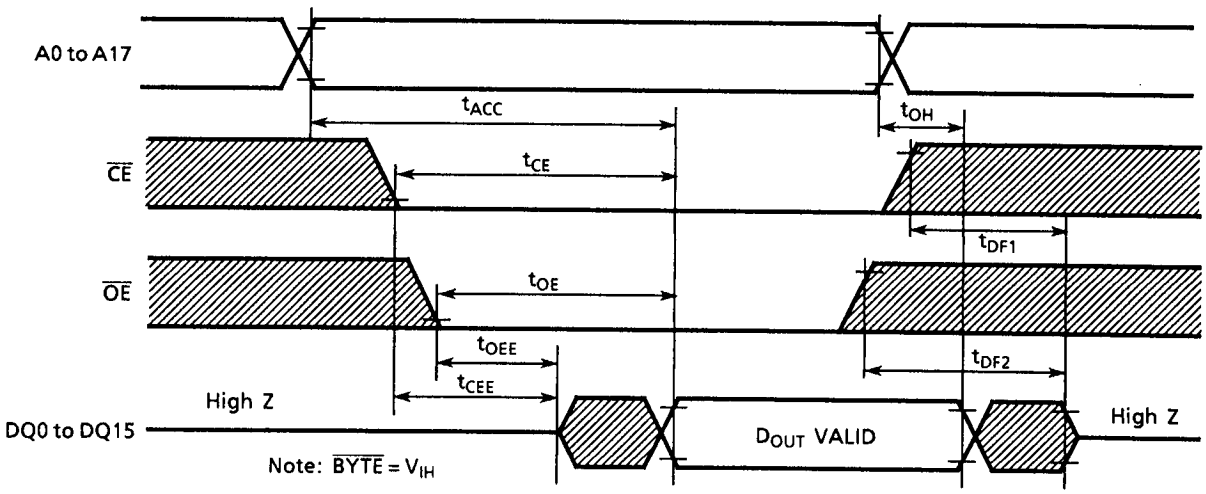
For Read-Only Characteristics (Ta = 0 to 70°C)

SYMBOL	PARAMETER	-90		-10		UNIT
		MIN	MAX	MIN	MAX	
t_{RC}	Read Cycle Time	90	–	100	–	ns
t_{ACC}	Address Access Time	–	90	–	100	ns
t_{CE}	$\overline{CE}$ Access Time	–	90	–	100	ns
t_{OE}	$\overline{OE}$ Access Time	–	35	–	40	ns
t_{CEE}	$\overline{CE}$ to Output Low Z	0	–	0	–	ns
t_{OEE}	$\overline{OE}$ to Output Low Z	0	–	0	–	ns
t_{OH}	Output Data Hold Time	0	–	0	–	ns
t_{DF1}	$\overline{CE}$ to Output High Z	–	20	–	30	ns
t_{DF2}	$\overline{OE}$ to Output High Z	–	20	–	30	ns
t_{READY}	$\overline{Reset}$ Pin Low to Read Mode	–	20	–	20	μs
t_{BTD}	$\overline{Byte}$ to Output High Z	–	30	–	30	ns

AC TEST CONDITIONS

PARAMETER	CONDITION
V_{DD}	5.0 V ± 10%
Output Load	1 TTL Gate + CL = 100 pF
Input Pulse Rise and Fall Time (between 10% and 90%)	5 ns Max
Input Pulse Level	0.6 V / 2.4 V
Timing Measurement Reference Level	Input 0.8 V / 2.0 V, Output 0.8 V / 2.0 V

TIMING DIAGRAM FOR READ OPERATION

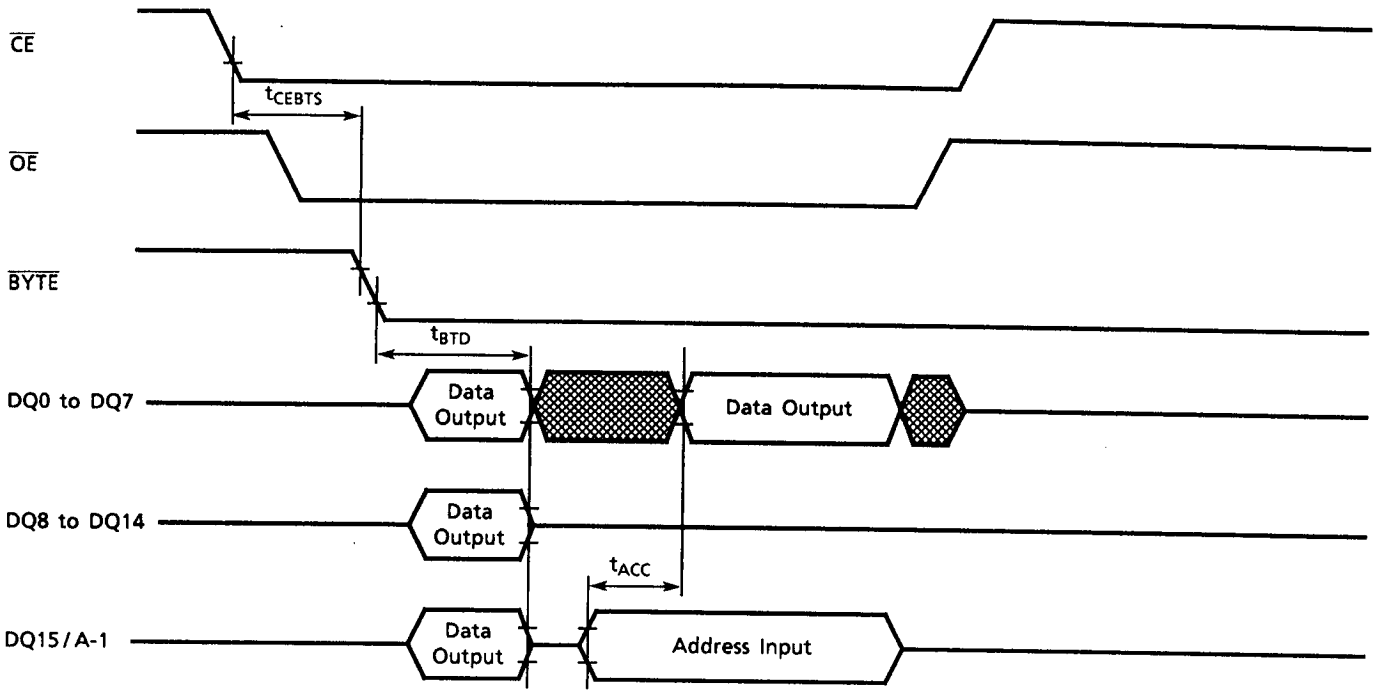


AC CHARACTERISTICS AND OPERATING CONDITIONS

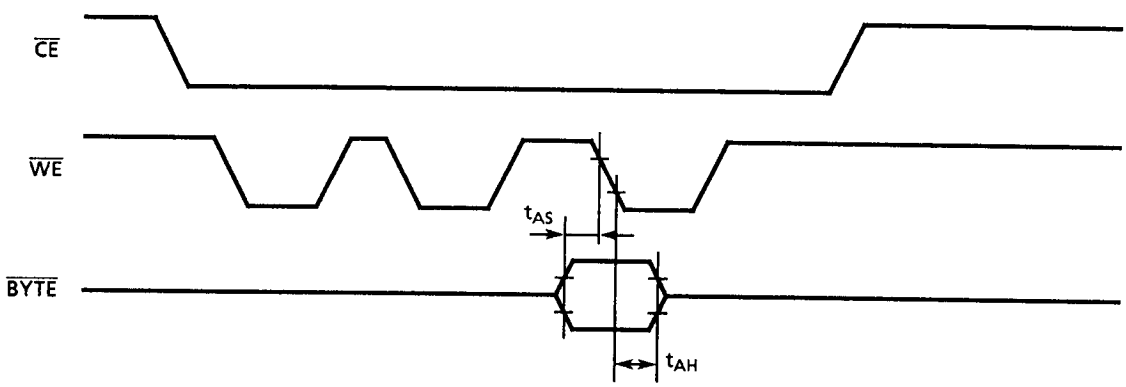
For Command Control Operations (Ta = 0 to 70°C)

SYMBOL	PARAMETER	-90		-10		UNIT
		MIN	MAX	MIN	MAX	
t_{CMD}	Command Write Cycle Time	90	–	100	–	ns
t_{AS}	Address Setup Time	0	–	0	–	ns
t_{AH}	Address Hold Time	45	–	50	–	ns
t_{DS}	Data Setup Time	45	–	50	–	ns
t_{DH}	Data Hold Time	0	–	0	–	ns
t_{CELH}	$\overline{CE}$ Low Level Hold TIme	50	–	55	–	ns
t_{WELH}	$\overline{WE}$ Low Level Hold Time	50	–	55	–	ns
t_{WEHH}	$\overline{WE}$ High Level Hold Time	20	–	20	–	ns
t_{CES}	$\overline{CE}$ Setup to $\overline{WE}$ Active	0	–	0	–	ns
t_{CEH}	$\overline{CE}$ Low Level Hold Time from $\overline{WE}$ High Level	0	–	0	–	ns
t_{OES}	$\overline{OE}$ Setup to $\overline{WE}$ Active	0	–	0	–	ns
t_{OEH}	$\overline{OE}$ High Level Hold Time	20	–	20	–	ns
t_{PPW}	Auto Program Time	16	–	16	–	μs
t_{PCEW}	Auto Chip Erase Time	1.5	–	1.5	–	s
t_{PBEW}	Auto Block Erase Time	1.5	–	1.5	–	s
t_{VDS}	V_{DD} Setup Time	50	–	50	–	μs
t_{VPS}	V_{ID} Setup Time	4	–	4	–	μs
t_{VPT}	V_{ID} Transition Time	4	–	4	–	μs
t_{OEHP}	$\overline{OE}$ High Level Hold Time for Toggle and Data Polling	10	–	10	–	ns
t_{PPLH}	Block Protect / $\overline{WE}$ Low Level Hold Time	100	–	100	–	μs
t_{PULH}	Block Unprotect / $\overline{WE}$ Low Level Hold Time	10	–	10	–	ms
t_{PAS}	Protect Address Setup Time	0	–	0	–	ns
t_{PAH}	Protect Address Hold Time	0	–	0	–	ns
t_{WEPHH}	$\overline{WE}$ High Level Hold Time for Protect/Unprotect	20	–	20	–	ns
t_{WEPRH}	$\overline{WE}$ High Level Hold Protect/Unprotect Recovery Time	4	–	4	–	μs
t_{RP}	$\overline{RESET}$ Low Level Hold Time	500	–	500	–	ns
t_{READY}	$\overline{RESET}$ Pin Low Level to Read Mode	–	20	–	20	μs
t_{ACC}	Address Access Time	–	90	–	100	ns
t_{CE}	$\overline{CE}$ Access Time	–	90	–	100	ns
t_{OE}	$\overline{OE}$ Access Time	–	35	–	40	ns
t_{CEE}	$\overline{CE}$ to Output Low Z	0	–	0	–	ns
t_{OEE}	$\overline{OE}$ to Output Low Z	0	–	0	–	ns
t_{OH}	Data Output Hold Time	0	–	0	–	ns
t_{DF1}	$\overline{CE}$ to Output High Z	–	20	–	30	ns
t_{DF2}	$\overline{OE}$ to Output High Z	–	20	–	30	ns
t_{BT}	$\overline{BYTE}$ to Output Valid	–	90	–	100	ns
t_{BTD}	$\overline{BYTE}$ to Output High Z	–	30	–	30	ns
t_{BUSY}	Program/Erase Valid to RDY/$\overline{BSY}$	35	–	40	–	ns
t_{CEBTS}	$\overline{CE}$ Setup to $\overline{BYTE}$ Transition	–	5	–	5	ns

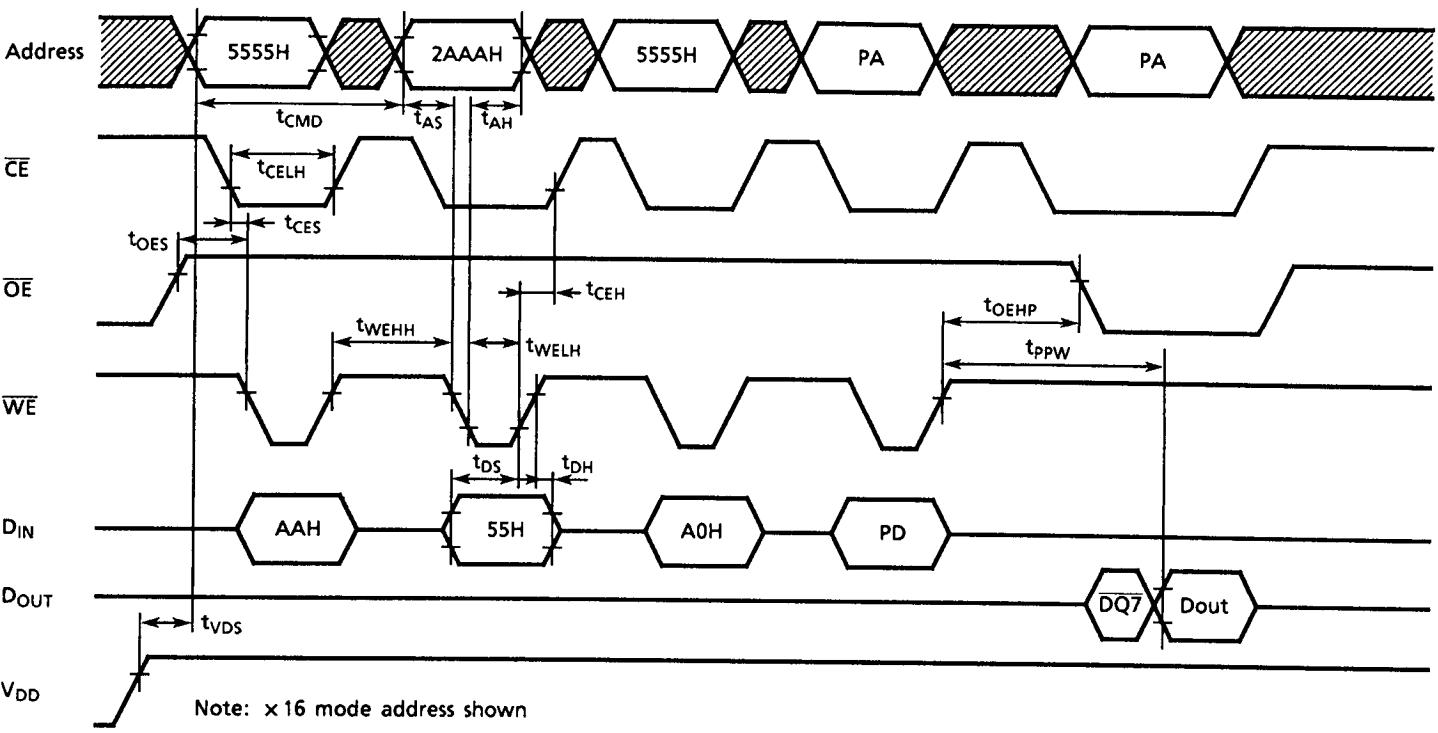
TIMING DIAGRAMS BYTE Timing Diagram for Read Operation



BYTE Timing Diagram for Write Operation

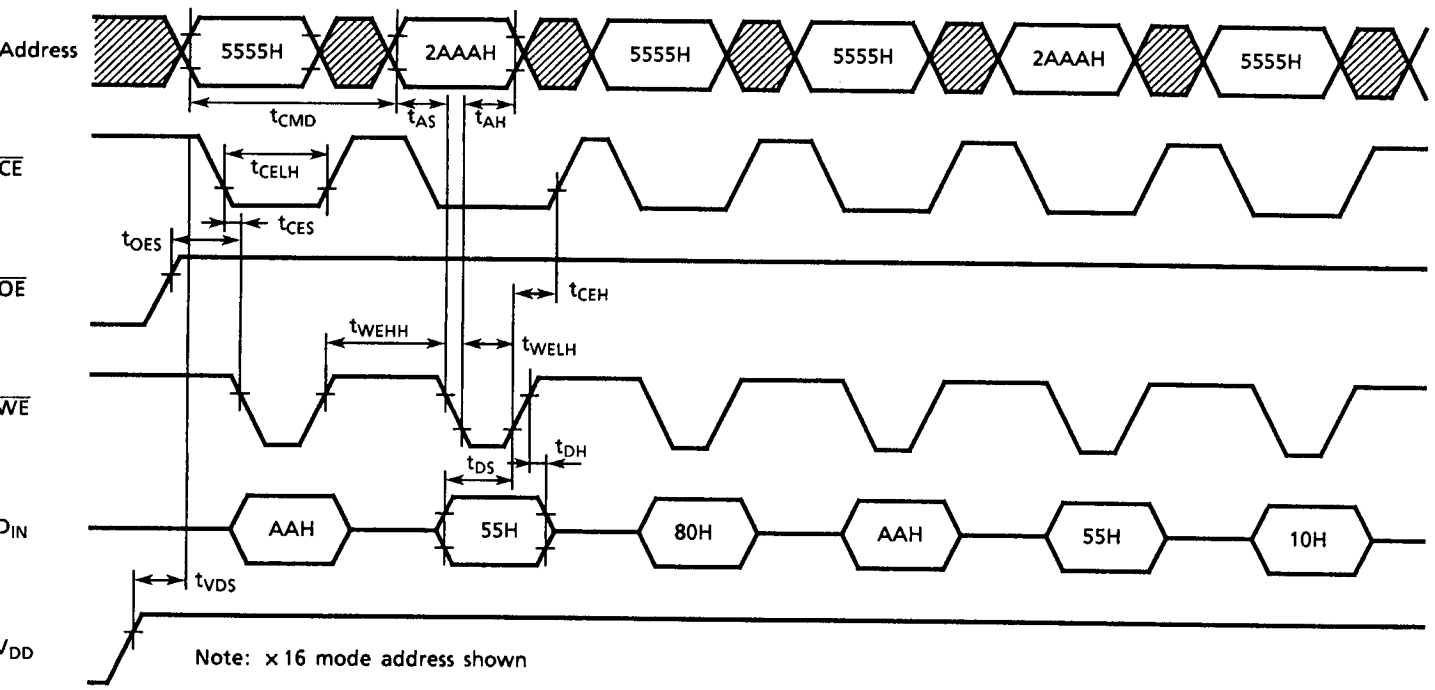


Timing Diagram for Program Operation



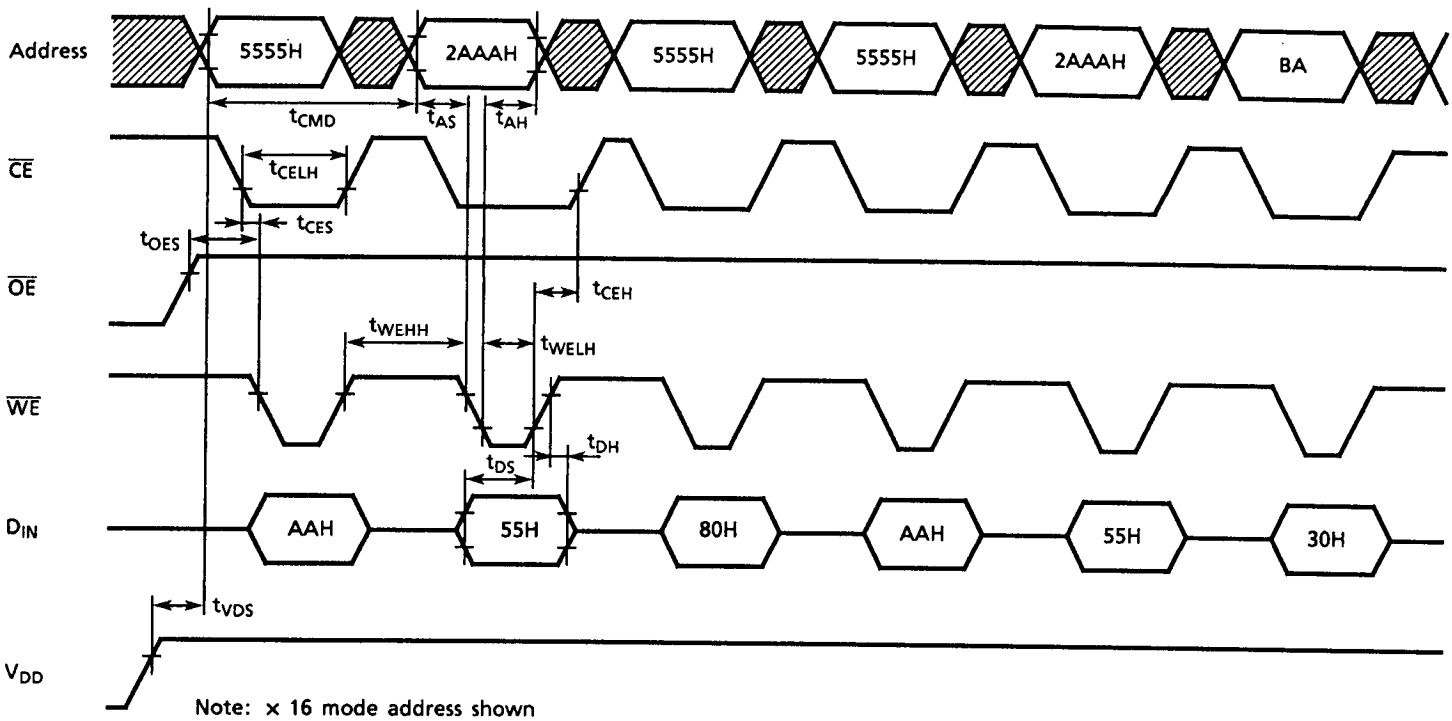
Note: x16 mode address shown

Timing diagram for Chip Erase Operation



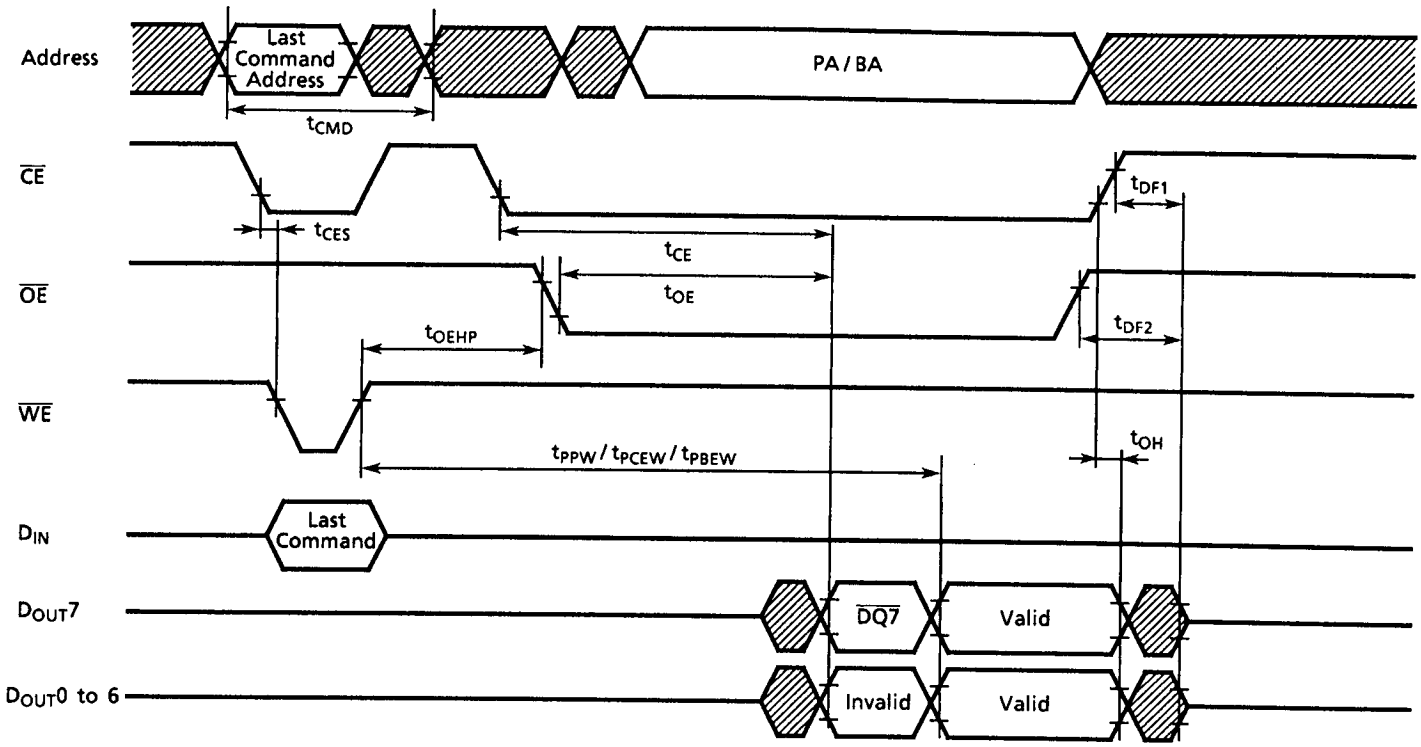
Note: x16 mode address shown

Timing Diagram for Block Erase Operation

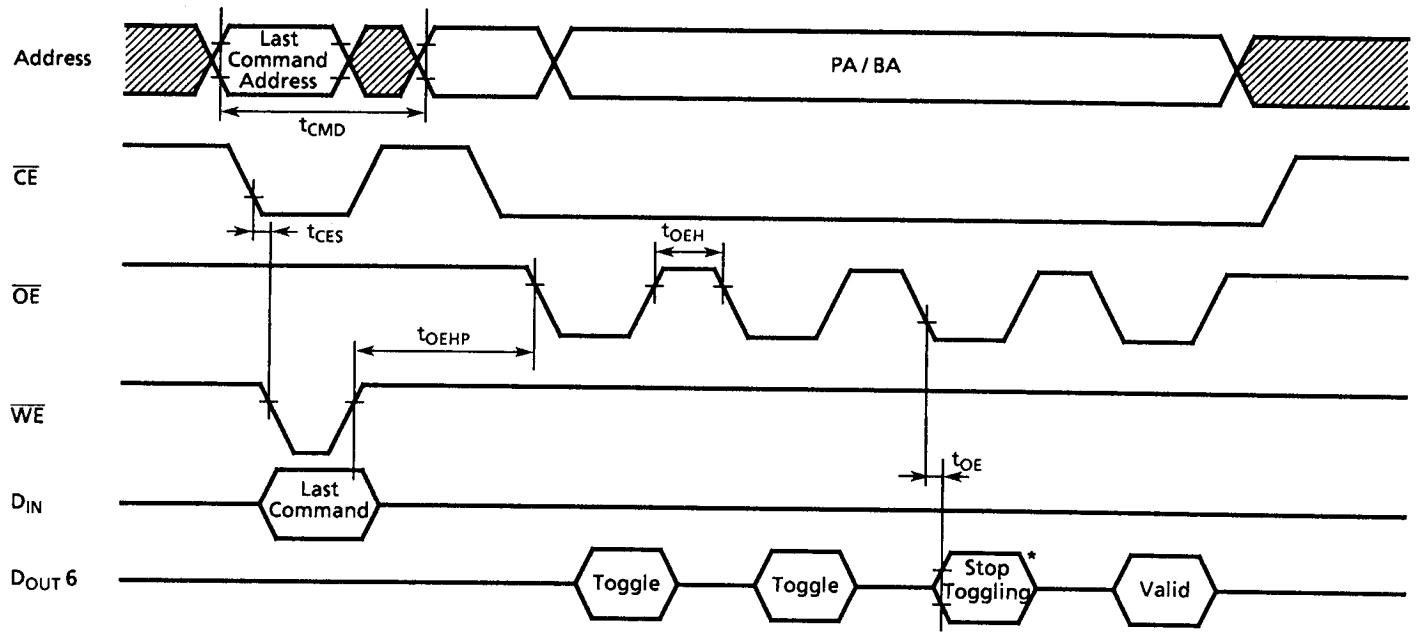


Note: x 16 mode address shown

Timing Diagram for Data Polling during Auto Algorithm Operation



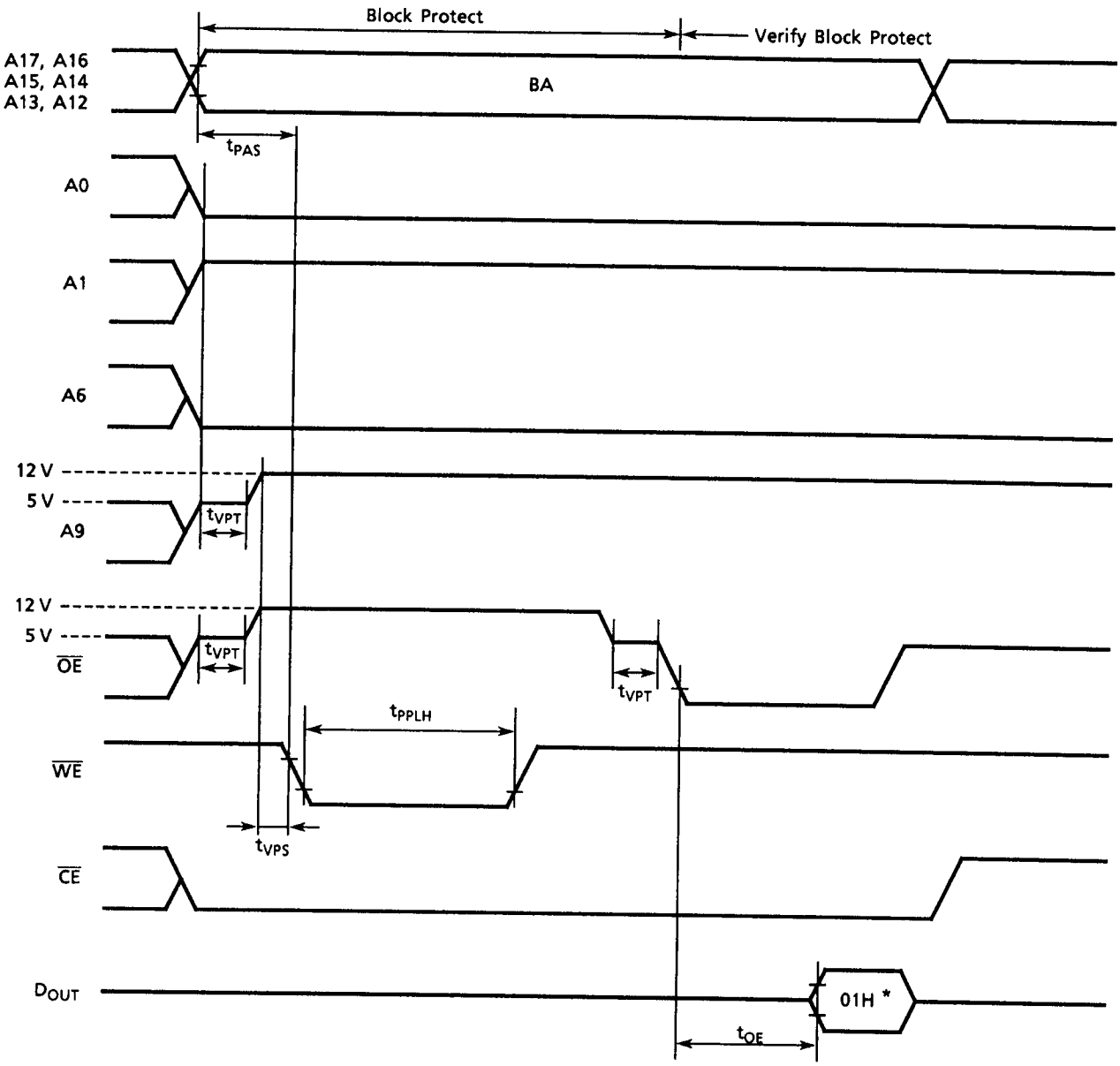
Timing Diagram for Toggle Bit during Auto Algorithm Operation



* D_{OUT} 6 stops toggling when the last command has been completed.

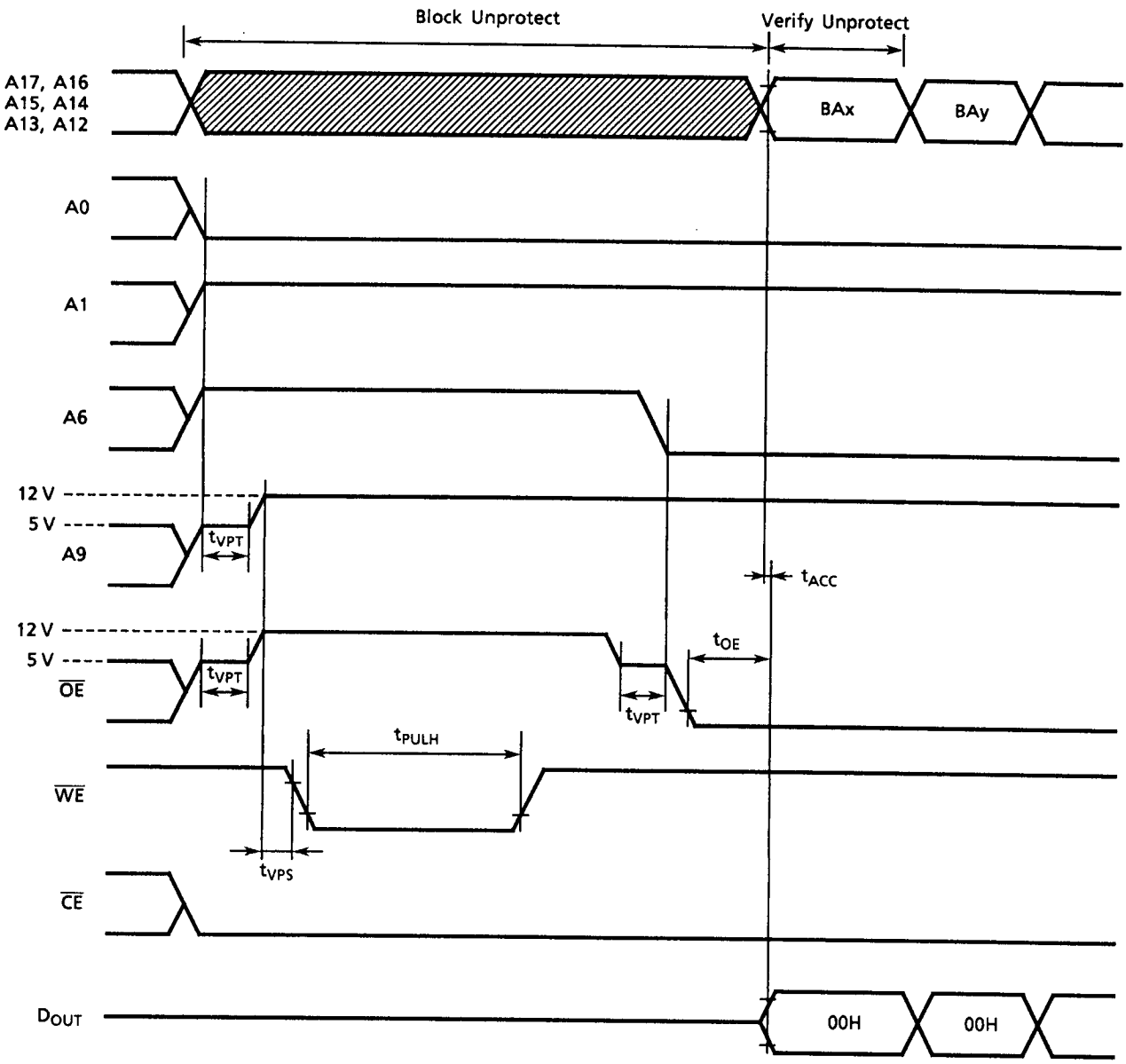
Note: PA = Program Address
BA = Block Address

Timing Diagram for Block Protection (Hardware)



Note: BA = Block Address
* 01H indicates block is protected.
* 00H indicates block is not protected.

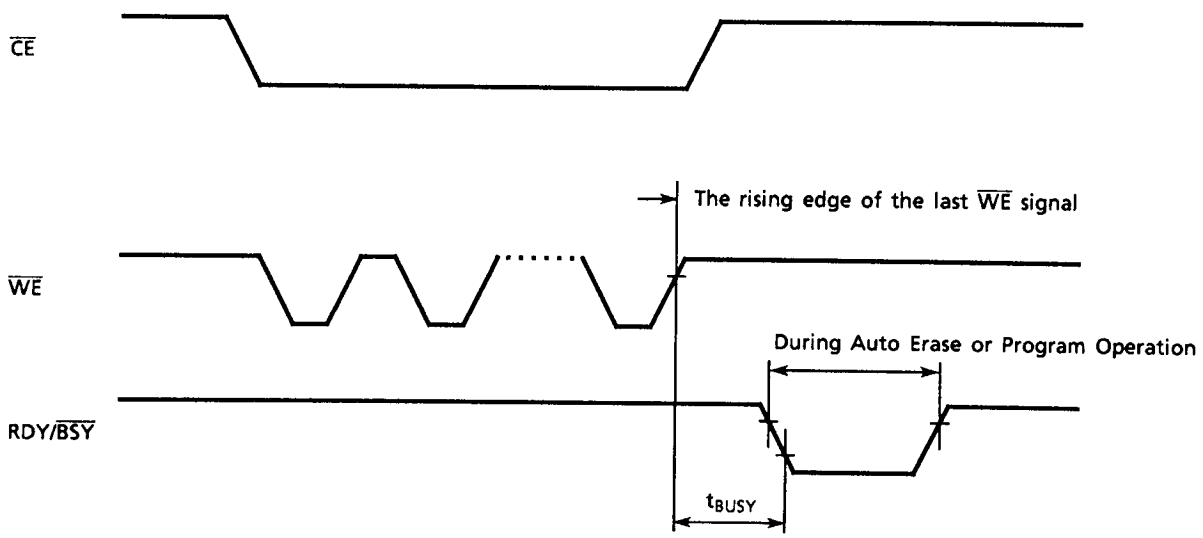
Timing Diagram for Block Unprotection (Hardware)



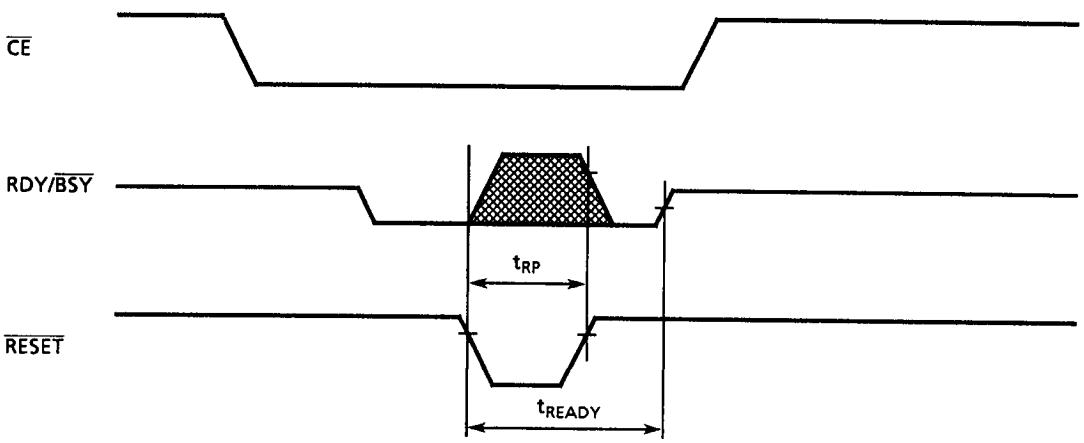
Note: BA = Block Address

* 00H indicates block is unprotected.
* 01H indicates block is protected.

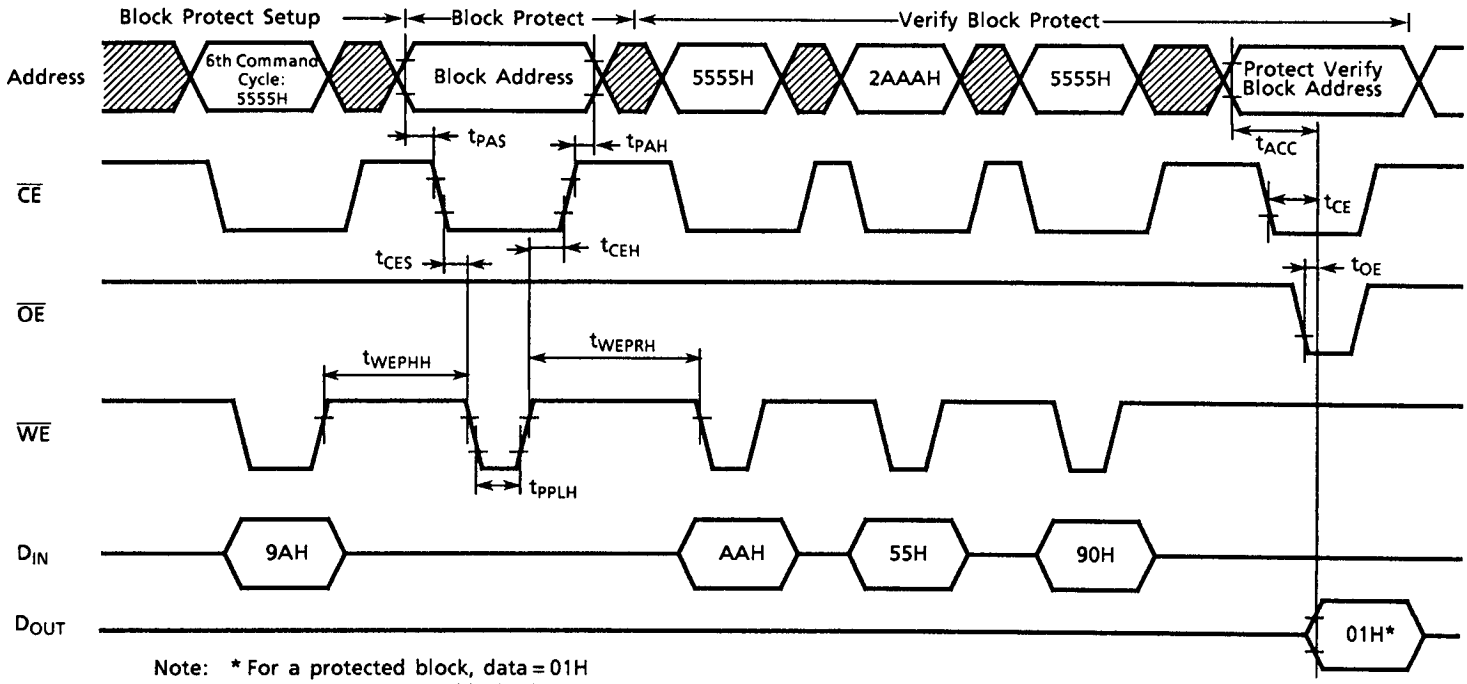
RDY/BSY Timing Diagram for Erase/Program Operation



RDY/BSY Timing Diagram for Erase/Program Operation



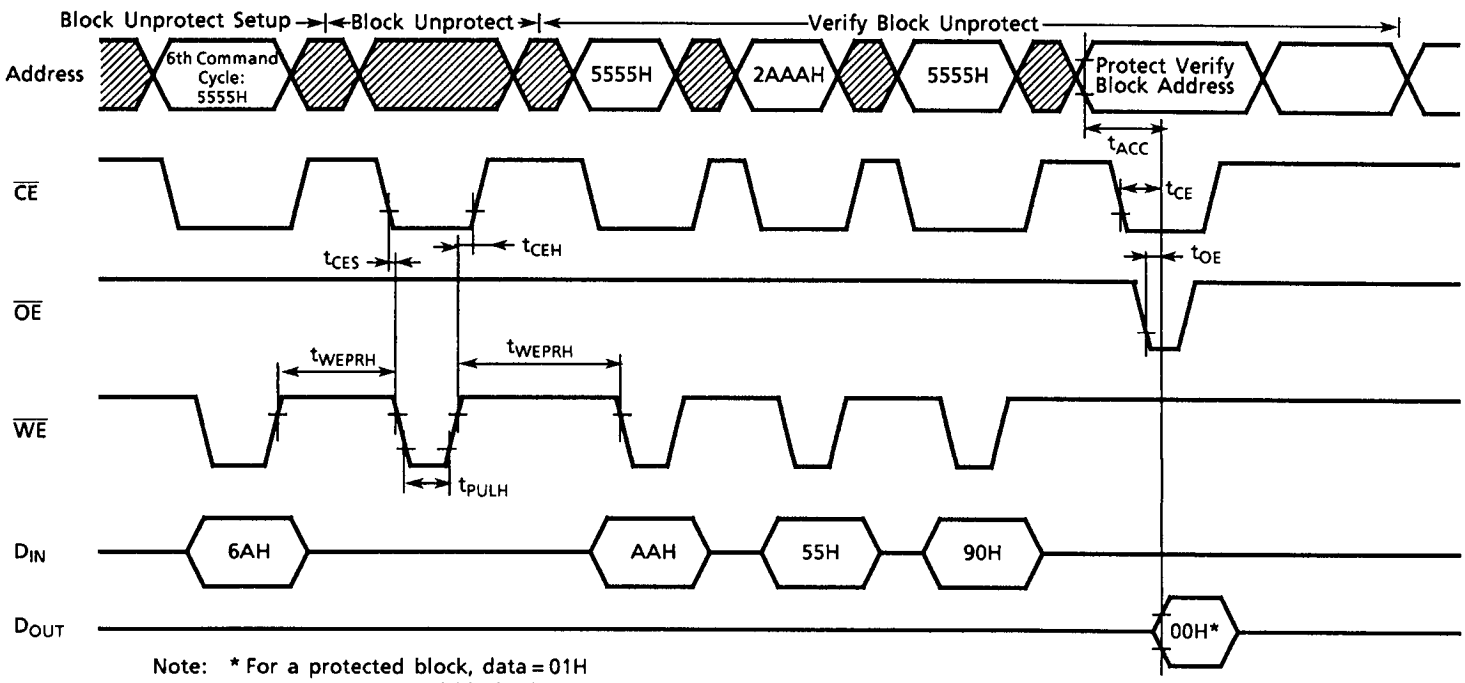
Timing Diagram for Software Block Protect Operation



Note: * For a protected block, data = 01H
For an unprotected block, data = 00H

x 16 mode address shown

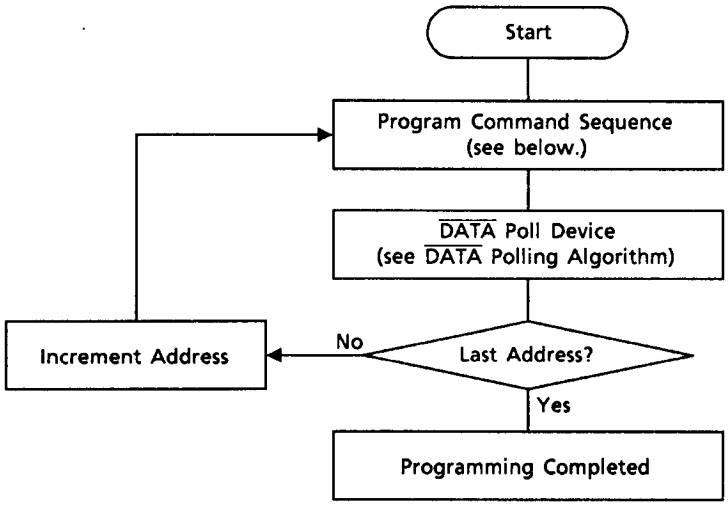
Timing Diagram for Software Block Unprotect Operation



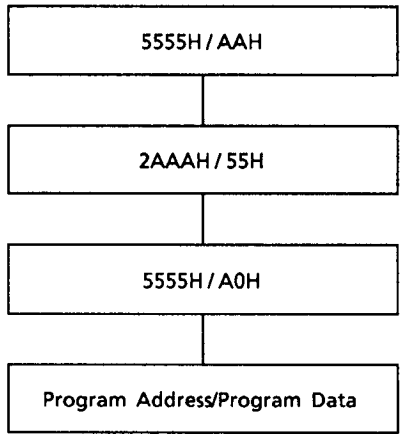
Note: * For a protected block, data = 01H
For an unprotected block, data = 00H

x 16 mode address shown
All blocks are unprotected.

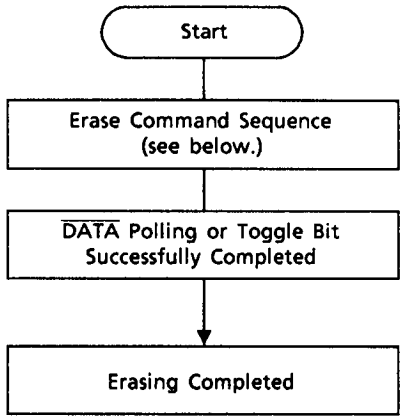
AUTO PROGRAM ALGORITHM



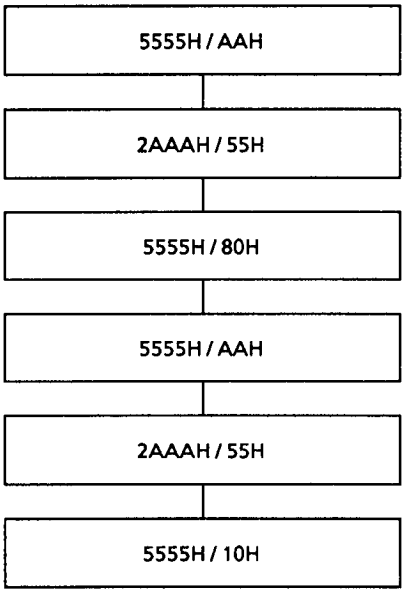
Program Command Sequence (Address/Command):



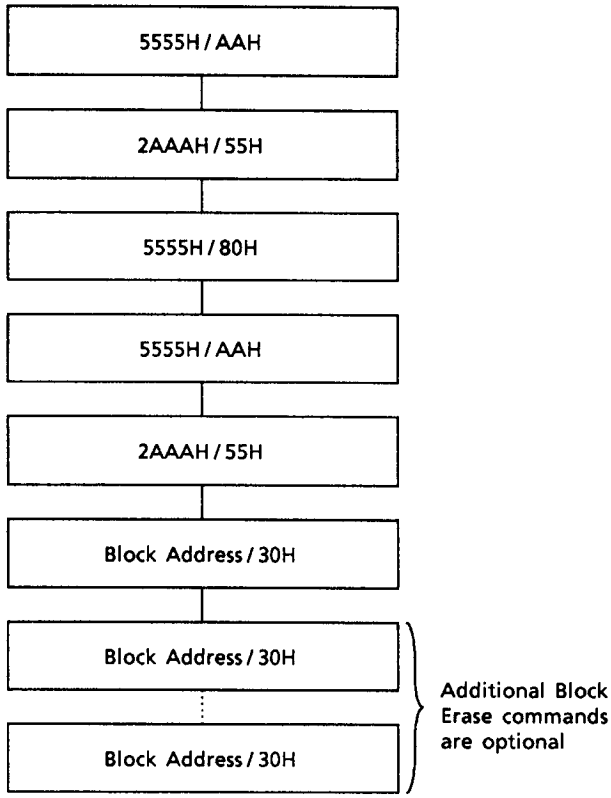
AUTO ERASE ALGORITHM



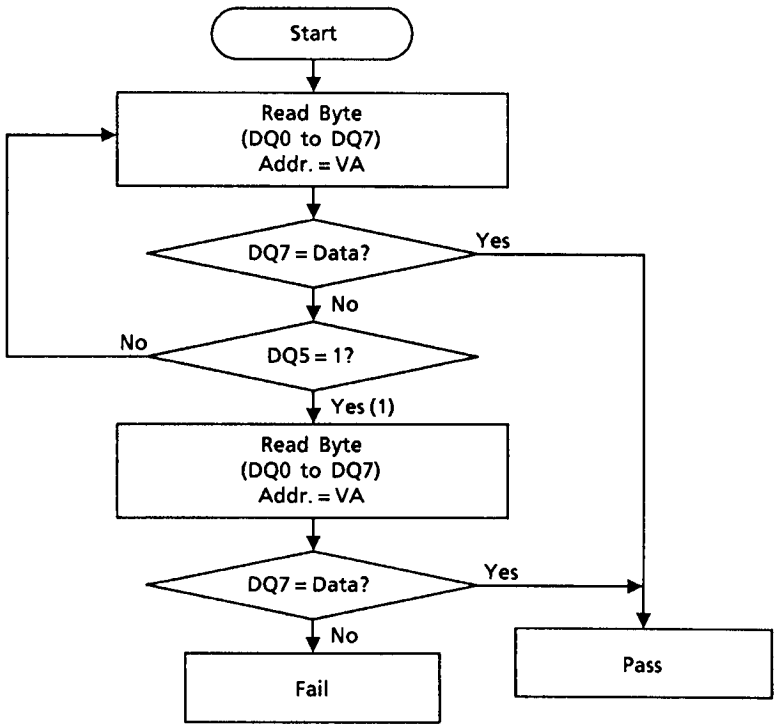
Chip Erase Command Sequence
(Address / Command):



Individual Block / Multiple Block
Erase Command Sequence (Address / Command):



DATA POLLING ALGORITHM

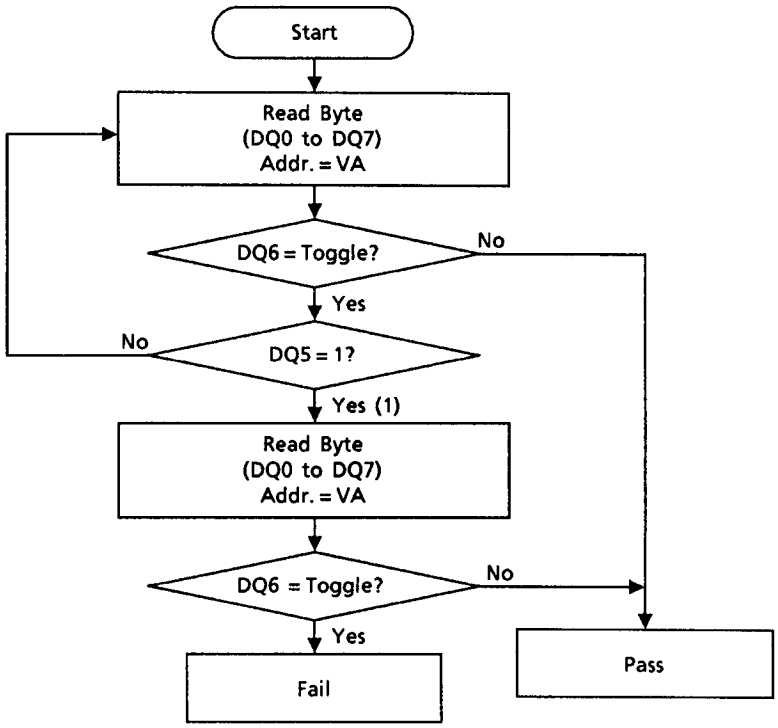


VA = Byte address for programming
VA = Any of the addresses within the block being erased during a Block Erase operation
VA = XXXXH during a Chip Erase operation

Note:

1. DQ7 must be rechecked even if DQ5 = 1 because DQ7 and DQ5 may change simultaneously.

TOGGLE BIT ALGORITHM

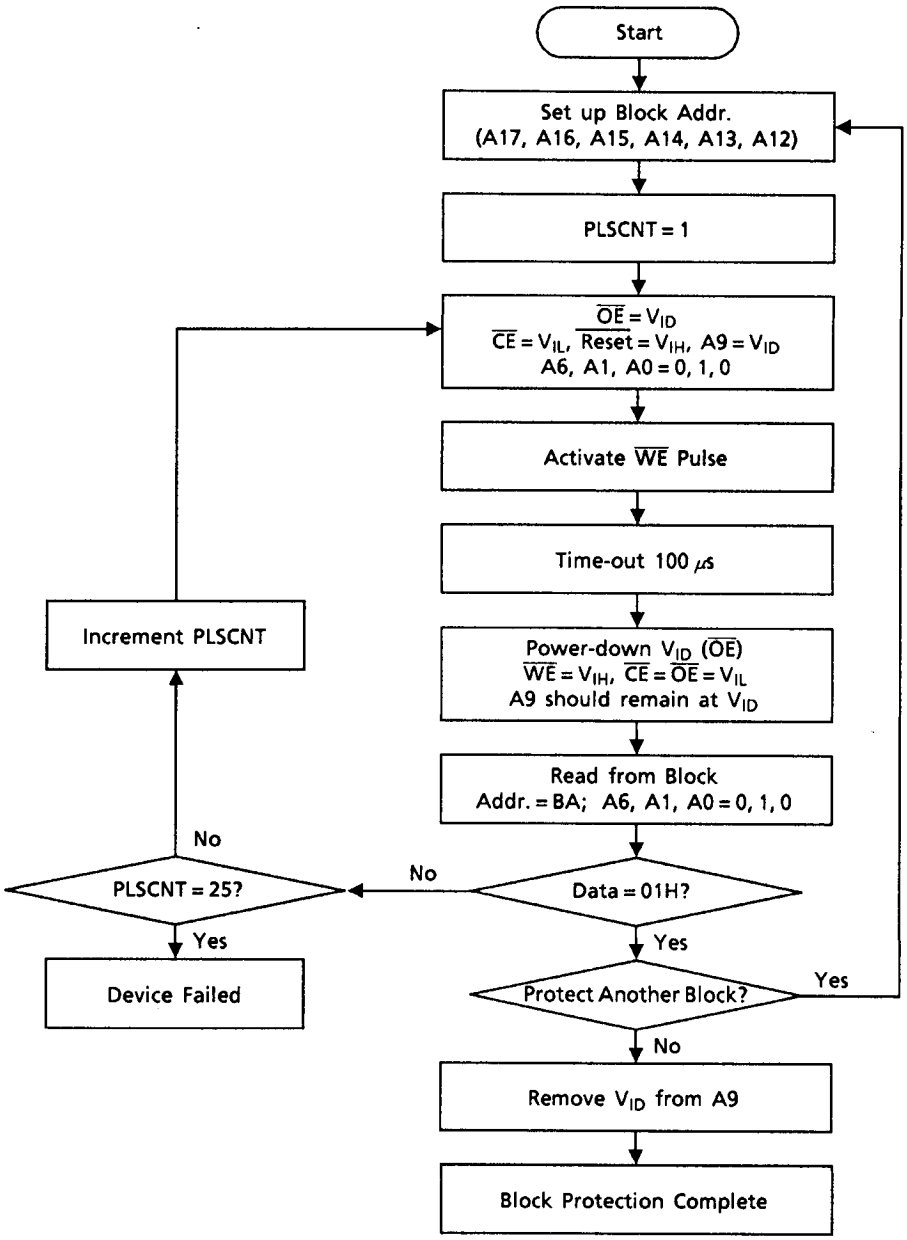


VA = Byte address for programming
VA = Any of the addresses within the block being erased during a Block Erase operation
VA = XXXXH during a Chip Erase operation
VA = Any address not within the block that was being erased during an Erase Suspend operation

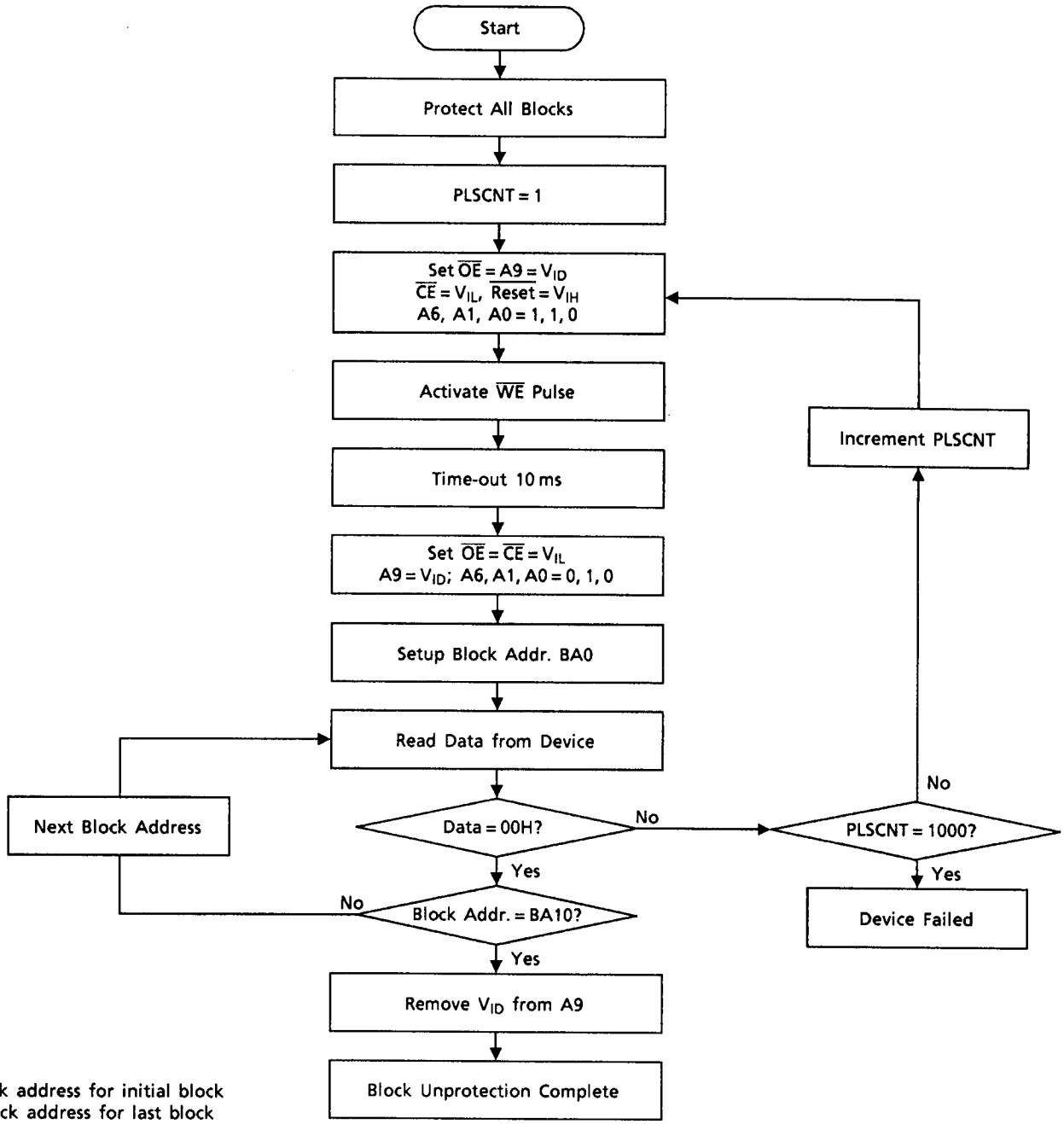
Note:

(1) DQ6 must be rechecked even if DQ5 = 1 because DQ6 may stop toggling at the same time that DQ5 changes to 1.

BLOCK PROTECTION ALGORITHM (HARDWARE)



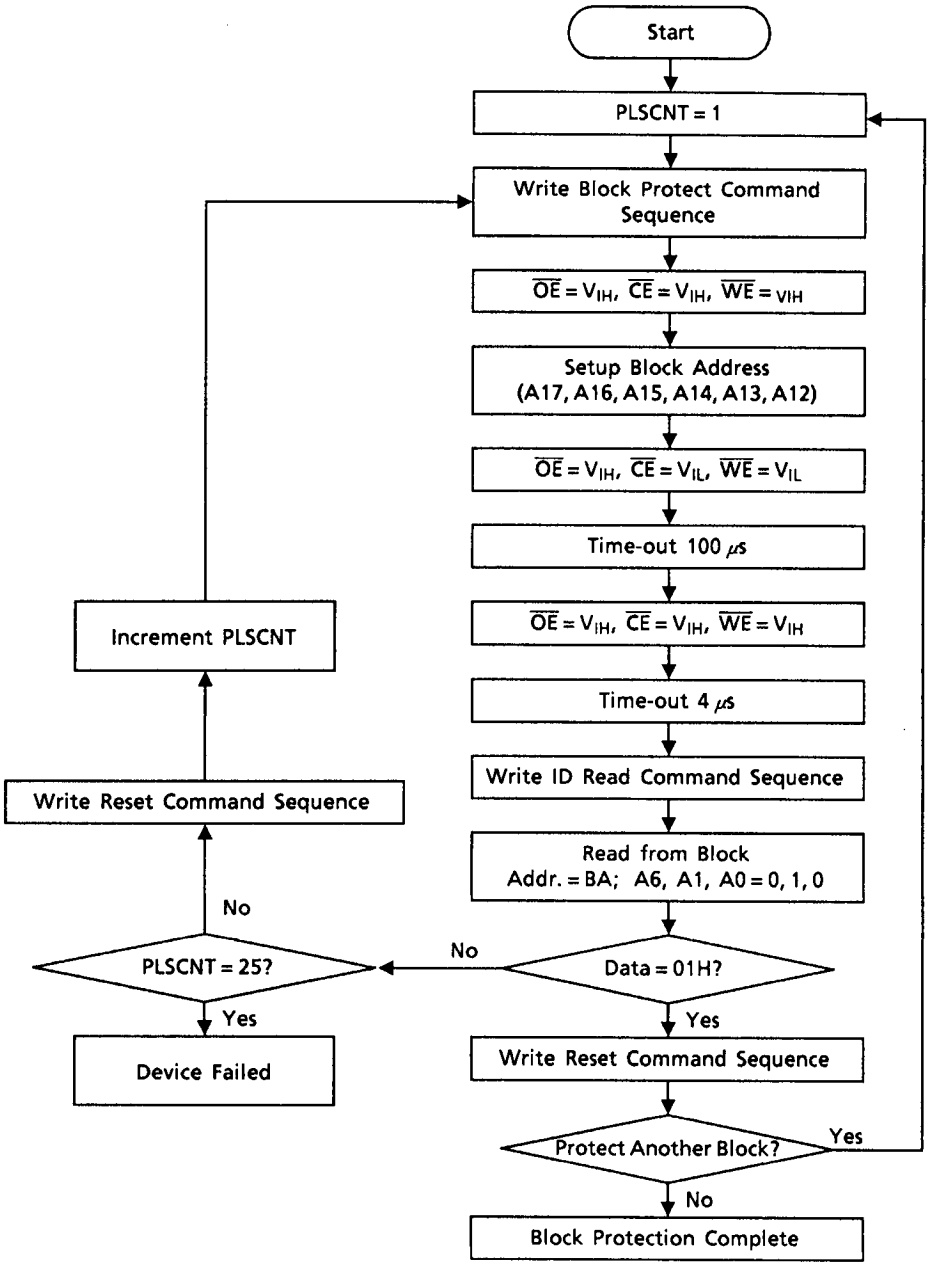
BLOCK UNPROTECTION ALGORITHM (HARDWARE)



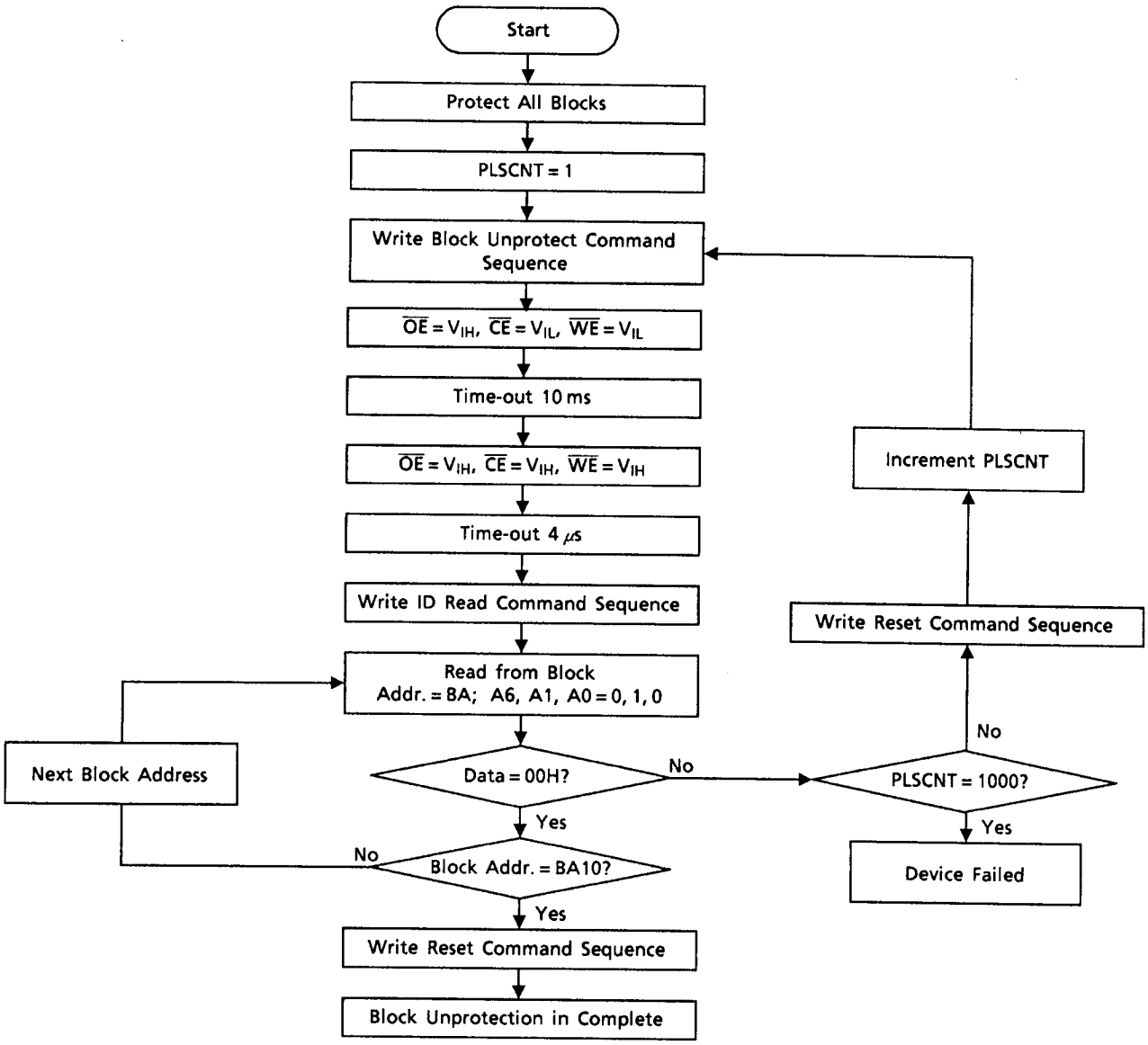
Notes:

BA0 = Block address for initial block
BA10 = Block address for last block

BLOCK PROTECTION ALGORITHM (SOFTWARE)



BLOCK UNPROTECTION ALGORITHM (SOFTWARE)



Notes:

BA0 = Block address for initial block
BA10 = Block address for last block

OPERATING MODES

The TC58F400/401 features a variety of operation modes: Read, ID Read, Auto Program / Verify, Auto Chip Erase / Verify, Auto Block Erase / Verify, Erase Suspend / Resume, Reset and Software Protection / Unprotection. Each mode is selected by a command input via the DQ pins.

READ MODE

When the device is set to Read mode, it acts as an asynchronous ROM with an access time of 90/100 ns (V_{DD} = 5 V ± 10%). Read mode is set by inputting the F0H command.

ID READ MODE

The ID Read mode is used to establish the device type. The ID Read mode is set either from the Command mode (1) or the EPROM mode (2).

(1) The ID Read mode can be set by inputting the 90H command (refer to Command Definitions). The data at address 0 is the manufacturer code (98H), while the data at address 1 is the device code (TC58F400 = 38H / TC58F401 = 68H). The access time of an ID Read is the same as that of a normal Read operation.

(2) The ID Read mode can also be set by applying V_{ID} to the A9 pin. The manufacturer code is read out when the address = 00H; the device code is read out when the address = 01H.

AUTO PROGRAM MODE

The Program mode is set by entering the Program command (refer to Command Definitions). Program operation is enabled on the rising edge of the $\overline{WE}$ signal in the fourth bus cycle. The Program and Verify operation is automatically executed in the chip. The device status can be determined either by $\overline{DATA}$ polling via DQ7 or by checking the toggle bit of the programmed address via DQ6. Commands are not recognized during program operation. The device allows the programming of 0s into 1 memory cells. The programming of a 1 into a 0 cell will fail. Erasing is necessary to turn a 0 into a 1.

AUTO CHIP ERASE MODE

The Chip Erase mode is set by entering the Chip Erase command (refer to Command Definitions). The Chip Erase operation is enabled in the sixth bus cycle. All memory cells are automatically pre-programmed to 0, erased and verified as erased by the chip. The device status can be determined by either $\overline{DATA}$ polling via DQ7 or by checking the toggle bit via DQ6. Commands are not recognized during a Chip Erase operation.

AUTO BLOCK ERASE MODE

The Auto Block Erase mode is set by entering the Block Erase command (refer to Command Definitions). The Auto Block Erase operation is enabled in the sixth bus cycle. The Block Erase is executed 80 μs (Block Erase Hold Time) after the rising edge of $\overline{WE}$ in the sixth cycle. The device is reset if any command other than a Block Erase command (30H) or a Suspend command is input during the Block Erase Hold Time. DQ3 is 0 during the Block Erase Hold Time. Once erasing starts, DQ3 becomes 1. The pre-programming of cells to 0 before erasing, and the Erase and Erase Verify operations are all automatically executed in the chip. The device status can be determined via DQ7 ($\overline{DATA}$ polling) or via DQ6 (bit toggling). The Erase Suspend command is only allowed during a Block Erase operation.

ERASE SUSPEND / RESUME MODE

The Erase Suspend mode is used to read data from a block that has not been selected for erasing. The Erase Suspend command (B0H) is allowed during a Block Erase operation; it is ignored in other operation modes. The Block Erase operation is also suspended if a Suspend command is issued during the Block Erase Hold Time. The device is reset if any command other than a Suspend is issued. A suspended device allows only a Read or Resume command. The Block Erase address is latched when the device is suspended, hence the device resumes operation without address input.

The device enters Suspend mode 0.1 μs to 15 μs after the Erase Suspend command is issued. Then the device enters a pseudo-Read mode. The data can be read out from an unselected block, however, the data is invalid if the address is set to a block selected for erasing. The device status can be determined from DQ6. DQ6 stops toggling once the device has entered the pseudo-Read mode. The host processor must track the current device mode since there is no indication whether the device is in pseudo-or normal Read mode.

The device restarts the Block Erase operation after receiving a Resume command. The Erase Suspend command is recognized after the Block Erase operation has restarted. (DQ6 outputs the toggle signal after block erasing resumes.)

BLOCK PROTECT

The TC58F400/401 has a block protection feature to prevent erasing of protected blocks. Block protection is enabled by either hardware protection (1)or a software command mode (2). The device is shipped with all blocks unprotected.

(1) A block is protected when: A9 = $\overline{OE}$ = V_{ID} (the maximum input voltage), $\overline{CE}$ = V_{IL}, A1 = V_{IH}, and A0 = A6 = V_{IL}; the block address is set using A12 to A17 (refer to Block Erase Address Tables). The block protect data must be programmed in the protection circuit while $\overline{WE}$ is Low (refer to Timming Diagram for Block Protection (Hardware) and Block Protection Algorithm (hardware)). Block protection is verified if 01H (in ×8 mode) or 0001H (in ×16 mode) is returned by the protected block when A9 = V_{ID}, $\overline{CE}$ and $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, A1 = V_{IH}, and A0 = A6 = V_{IL}. The address of the protected block is held in A12 to A17.

(2) A block can also be protected using software commands (refer to Command Definitions). Block protection is verified by a subsequent Verify Block Protect command which also terminates the Block Protect operation. When a Verify Block Protect command is executed, with A1 = V_{IH} and A0 = A6 = V_{IL}, a protected block will return the result 01H (in ×8 mode) or 0001H (in ×16 Mode). The address of the protected block is held in A12 to A17 (refer to Software Block Protect Operation and Block Protection Algorithm (Software)).

TEMPORARY BLOCK UNPROTECTION

The TC58F400/401 has a temporary block unprotection feature which disables block protection for all protected blocks. Unprotection is enabled by applying V_{ID} to the $\overline{RESET}$ pin. In this state any block can be programmed or erased. The device returns to the previous condition after V_{ID} is removed from the $\overline{RESET}$ pin. That is, previously protected blocks are protected again.

BLOCK UNPROTECTION

The TC58F400/401 has a block unprotection feature which disables the block protection for a protected block. All blocks should be protected before block unprotection (refer to Block Protection Mode). Block unprotection is enabled either through hardware (1) or by a software command (2). All blocks are unprotected using either method.

(1) Block unprotection is enabled when: A9 = $\overline{OE}$ = V_{ID} (the maximum input voltage), $\overline{CE}$ = V_{IL}, A1 = A6 = V_{IH}, and A0 = V_{IL}. All blocks are unprotected while $\overline{WE}$ is Low. Block unprotection is verified by reading out the data 00H (in ×8 mode), or 0000H (in ×16 mode) from the unprotected block when A9 = V_{ID}, $\overline{CE}$ and $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, A1 = V_{IH}, and A0 = A6 = V_{IL}. The address of the unprotected block is held in A12 to A17 (refer to Timing Diagram for Block Unprotection (Hardware) and Block Unprotection Algorithm (Hardware)).

(2) All blocks can also be unprotected using software commands (refer to Command Definitions). Block unprotection is verified by a subsequent Verify Block Protect command which terminates the Block Unprotect operation. The output data from an unprotected block is 00H (in ×8 mode) and 0000H (in ×16 mode) when A1 = V_{IH} and A0 = A6 = V_{IL}. The address of the unprotected block is held in A12 to A17 (refer to Timing Diagram for Software Block Unprotect Operation and Block Unprotection Algorithm (Software)).

STANDBY MODE

The TC58F400/401 has a low-power Standby mode which uses less than 100 μA at CMOS voltage levels ($\overline{RESET}$ = $\overline{CE}$ = V_{DD} ±0.2 V, or $\overline{RESET}$ = V_{SS} ±0.2 V) or 1 mA at the TTL level ($\overline{RESET}$ = $\overline{CE}$ = V_{IH}, or $\overline{RESET}$ = V_{IL}). The outputs are in High-Impedance state. The $\overline{CE}$ signal is ignored during a Program or Erase operation until the operation has been completed.

AUTO PROGRAM, AUTO ERASE OPERATION

$\overline{\text{DATA}}$ POLLING/STATUS READ

- DQ7: $\overline{\text{DATA}}$ Polling

The device status can be determined by the Data Polling function during an Auto Program or Auto Erase operation. In an Auto Program operation, the $\overline{\text{DATA}}$ Polling mode begins from the rising edge of $\overline{\text{WE}}$ in the fourth cycle. DQ7 outputs inverted data during the programming operation and outputs real data after programming has finished. In an Auto Erase operation, data polling begins from the rising edge of $\overline{\text{WE}}$ in the sixth cycle. DQ7 outputs 0 during the Erase operation and 1 when the Erase operation has finished. The polling data is asynchronous with the $\overline{\text{OE}}$ signal.

- DQ6: Toggle Bit

The device status can also be determined by the toggling of DQ6 during an Auto Program or Auto Erase operation. DQ6 alternately outputs a 0 or a 1 for each read attempt ($\overline{\text{OE}}$ toggling) while the device is busy. When the internal operation has been completed, toggling stops and valid data can be read by subsequent reading. The Toggle mode begins from the rising edge of $\overline{\text{WE}}$ in the fourth cycle for auto programming and in the sixth cycle for an Auto Erase.

DQ6 toggles for 2 μs when an attempt is made to execute the Auto Program operation on a protected block. DQ6 toggles for 100 μs when an attempt is made to execute the Auto Erase operation on a protected block. DQ6 toggles on either the $\overline{\text{CE}}$ or $\overline{\text{OE}}$ clock signal.

- DQ5: Internal Time-out

DQ5 outputs a 1 when the internal timer has timed out during a Program or Erase operation. This indicates that the operation has not been completed within the allotted time.

- DQ3: Block Erase Timer

The Block Erase operation starts 80 μs (Block Erase Hold Time) after the rising edge of $\overline{\text{WE}}$ in the last command cycle. The $\overline{\text{DATA}}$ polling (on DQ7) and toggling bit (DQ6) begin immediately after the Block Erase command (30H). DQ3 outputs a 0 during the Block Erase Hold Time and a 1 when the Erase operation starts. Additional Block Erase commands can only be accepted during this Block Erase Hold Time. Each Block Erase command received within this hold time resets the timer, allowing additional blocks to be marked for erasing. DQ3 outputs a 1 if the Program or Erase operation fails.

- RDY/$\overline{BSY}$: (READY/$\overline{BUSY}$)

  The TC58F400/401 has a RDY/$\overline{BSY}$ signal to indicate the device status to the host processor. A 0 (Busy) indicates that an Auto Program or Auto Erase operation is in progress. A 1 (Ready) indicates that the operation has finished and that the device can accept a new command. During an Auto Block Erase operation, commands other than Erase Suspend are ignored. The RDY/$\overline{BSY}$ signal outputs a 1 during an Erase Suspend operation. The output buffer for the RDY/$\overline{BSY}$ pin is an open drain type circuit, allowing a wired-OR connection. A pull-up resistor needs be inserted between V_{DD} and the RDY/$\overline{BSY}$ pin.

  The RDY/$\overline{BSY}$ signal outputs a 0 after the rising edge of $\overline{WE}$ in the fourth cycle of an Auto Program operation and the sixth cycle of an Auto Erase operation. The RDY/$\overline{BSY}$ signal is invalid when $\overline{RESET} = V_{IL}$.

- $\overline{RESET}$: (Hardware Reset)

  The device is reset by the $\overline{RESET}$ signal. The Reset operation is initiated by holding $\overline{RESET} = V_{IL}$ for 500 ns. The Reset operation completes 20 μs after $\overline{RESET}$ goes Low. From this point on, while $\overline{RESET}$ remains Low the device is in Standby mode. If $\overline{RESET}$ goes High, the device enters Read mode.

  The device is in Standby mode and the output is High-Impedance when $\overline{RESET} = GND \pm 0.2\,V$ (Deep-Power-down mode: approximately 20 μA). The device resets to Read mode 500 ns (max) after the $\overline{RESET}$ signal goes from V_{IL} to V_{IH}. The Read operation or new command inputs must allow for this recovery time in order for operation to proceed smoothly.

  The Reset function aborts the Auto Program and Auto Erase operations. In this case, the operations are not correctly completed.

RESET MODE

The Reset mode is useful for resetting any operation and setting the device to Read mode. The Reset mode is enabled by executing the Reset command sequence (refer to Command Definitions). The device is set to Read mode after 50 ns of recovery time.

- $\overline{BYTE}$/WORD mode control

  The $\overline{BYTE}$ pin is used to set the DQ bit organization. The device is set to ×8 mode when $\overline{BYTE} = V_{IL}$ and to ×16 mode when $\overline{BYTE} = V_{IH}$. The DQ15/A-1 pin is used for the LSB address. DQ8 to DQ14 are High-Impedance in Byte mode.

AUTO PROGRAM OPERATION

The Auto Program operation is executed using the following sequence:

1) Auto Program setup cycle

   The Auto Program mode is setup on the rising edge of $\overline{WE}$ in the third command cycle.

2) Address / Data latch cycle

   The address is latched on the falling edge of $\overline{WE}$ and the data is latched on the rising edge of $\overline{WE}$ in the fourth cycle. The Auto Program operation starts on the rising edge of $\overline{WE}$ in the fourth cycle.

3) Auto Program, Program Verify cycle

   The Program and Verify operations are carried out automatically. The address and data are latched during the operation.

4) Status Read cycle during Auto Program

   The Auto Program operation completes successfully if DQ7 (Data Polling) outputs the same value as the input data. The latched address is cancelled after the program address and data are input; therefore, the address needs to be input for $\overline{DATA}$ polling (see Timing Diagram for Program Operation and Timing Diagram for Data Polling During Auto Algorithm Operation). When program operations start, DQ3 and DQ5 output 0 and the DQ6 bit toggles each time $\overline{OE}$ goes Low (refer to Hardware Status Flags). DQ7 outputs the same data as the input data and DQ6 stops toggling when the program operation has completed correctly. The device returns to Read mode after an Auto Program operation.

   If the program operation fails, DQ7 outputs the inverse of the input data, DQ6 keeps toggling, and DQ3 and DQ5 output 1. The device retains this status and does not return to Read mode. The Reset command must be input to reset the device. The block which includes the address which could not be programmed must be managed by the host processor.

   Commands are ignored during the Program operation. The operation is aborted and the device is reset and returns to Read mode when $\overline{RESET} = V_{IL}$. The programmed data is invalid when the operation is aborted. V_{DD} must be held higher than V_{DDLKO}; otherwise, the device is reset.

   The programming of memory cells from 1 to 0 is allowed. A cell must be erased to turn it from a 0 to a 1. The program operation fails if an attempt is made to program a 1 into a 0 cell. If an attempt is made to program a protected block, DQ6 stops toggling 2 μs after the last command cycle and the device returns to Read mode.

AUTO CHIP ERASE OPERATION

The Auto Erase operation is executed using the following sequence:

1) Auto Chip Erase setup cycle

It takes six command cycles to setup Auto Chip Erase mode. The Auto Chip Erase operation starts in the sixth cycle.

2) Auto Pre-Program, Chip Erase, Erase Verify cycle

All memory cells are pre-programmed to 0 before the device carries out the Chip Erase operation. Erase Verify operations are automatically executed after Chip Erase.

3) Status Read cycle during Auto Chip Erase

DQ7 outputs a 1 when the Erase operation has completed successfully. The address must be set to an unprotected block for correct $\overline{DATA}$ polling. During the Erase operation, DQ3 outputs a 1, DQ5 and DQ7 output 0 and the DQ6 bit toggles each time $\overline{OE}$ goes Low (see Hardware Status Flags). DQ7 outputs a 1 and DQ6 stops toggling when the Erase operation has completed correctly. The device returns to Read mode after an Auto Chip Erase operation.

If the Chip Erase operation fails, DQ7 outputs a 0, the DQ6 bit keeps toggling, and DQ3 and DQ5 output a 1. The device retains this status and does not return to Read mode. A Reset command or a hardware reset ($\overline{RESET} = V_{IL}$) must be input to reset the device. The failed block cannot be identified. Therefore, the device must either be rejected and replaced, or the failed block must be identified as a bad block using the Auto Block Erase operation. Bad blocks must be managed by the host processor.

Commands are ignored during a Chip Erase operation. The operation is aborted and the device is reset and returns to Read mode when $\overline{RESET} = V_{IL}$. The memory cell data is invalid when the operation is aborted. V_{DD} must be held higher than V_{DDLKO}; otherwise, the device is reset. The Chip Erase operation must be re-executed after the device has been reset.

If the device has protected blocks, these blocks are protected from erasing and only unprotected blocks are erased. If all blocks are protected, the DQ6 bit stops toggling 100 μs after the rising edge of $\overline{WE}$ in the sixth command cycle, and the device returns to Read mode.

AUTO BLOCK ERASE OPERATION

The Auto Block Erase operation is executed using the following sequence:

1) Auto Block Erase setup cycle

   It takes six command cycles to setup Auto Block Erase mode.

2) Block address / Command latch cycle

   The block address and the Block Erase command (30H) are latched respectively on the falling and rising edges of $\overline{WE}$ in the sixth command cycle (see Timing Diagram for Block Erase Operation). The Block Erase operation starts 80 μs (Block Erase Hold Time) after the rising edge of $\overline{WE}$ in the last command cycle.

3) Auto Pre-Program, Block Erase, Erase Verify cycle

   All memory cells in the selected block are pre-programmed to 0 before the device automatically carries out the Block Erase and Erase Verify operations.

4) Status Read cycle during Auto Block Erase

   DQ7 outputs a 1 when the Erase operation has completed successfully. For correct $\overline{DATA}$ polling, the address must be set to the address of the block which is being erased. During the Erase operation DQ3 outputs a 1, DQ5 and DQ7 output 0 and DQ6 toggles each time $\overline{OE}$ goes Low (see Hardware Status Flags). DQ7 outputs a 1 and DQ6 stops toggling when the Erase operation has completed correctly. The device returns to Read mode after an Auto Block Erase operation.

   If the Block Erase operation fails, DQ7 outputs a 0, DQ6 keeps toggling, and DQ3 and DQ5 output a 1. The device retains this status and does not return to Read mode. A Reset command or a hardware reset ($\overline{RESET} = V_{IL}$) must be used to reset the device. The failed block must be managed as a bad block by the host processor. Other than Erase Suspend, commands are ignored during a Block Erase operation. The operation is aborted and the device is reset and returns to Read mode when $\overline{RESET} = V_{IL}$. The memory cell data is invalid when the operation is aborted. V_{DD} must be held above V_{DDLKO}; otherwise, the device is reset. The Block Erase operation must be re-executed when the device has been reset.

   If the selected block is protected, the DQ6 bit stops toggling 100 μs after the rising edge of $\overline{WE}$ in the last command cycle, and the device returns to Read mode.

AUTO MULTI BLOCK ERASE OPERATION

The Auto Multi Block operation is executed using the following sequence:

1) Auto Multi Block Erase setup cycle

   It take six command cycles to setup Auto Multi Block Erase mode.

2) Block address / Command latch cycle

   The block address and the Block Erase command (30H) are latched respectively on the falling and rising edge of $\overline{WE}$ in the sixth command cycle (see Timing diagram for Block Erase operation). The Multi Block Erase operation starts 80 μs (Block Erase Hold Time) after the rising edge of $\overline{WE}$ in the last command cycle. Additional block addresses and Multi Block Erase commands must be input during the Erase Hold Time; however, the Block Erase Hold Time restarts after each block address and a Block Erase command is input. If no writes occur for 80 μs, erasing of the selected blocks begins. The block addresses can be input in any order.

3) Auto Pre-Program, Block Erase, Erase Verify cycle

   All memory cells in the selected block are pre-programmed to 0 before the device automatically carries out the Multi Block Erase and Erase Verify operations.

4) Status Read cycle during Auto Multi Block Erase

   DQ7 outputs a 1 when the Erase operation has completed successfully. For correct $\overline{DATA}$ polling, the address must be set to the address of the block which is being erased. During the Erase operation DQ3 outputs a 1, DQ5 and DQ7 output 0 and DQ6 toggles each time $\overline{OE}$ goes Low (see Hardware Status Flags). DQ7 outputs a 1 and DQ6 stops toggling when the Erase operation has completed correctly. The device returns to Read mode after an Auto Block Erase operation.

   If the Block Erase operation fails, DQ7 outputs a 0, DQ6 keeps toggling, and DQ3 and DQ5 output a 1. The device retains this status and does not return to Read mode. A Reset command or a hardware reset ($\overline{RESET} = V_{IL}$) must be used to reset the device. The failed block cannot be identified. Therefore, the device must either be rejected and replaced, or the failed block must be identified as a bad block using the Auto Block Erase operation. Bad blocks must be managed by the host processor.

   Commands (except for Erase Suspend and Reset) are ignored during a Multi Block Erase operation. The operation is aborted and the device is reset and returns to Read mode after a Reset command or when $\overline{RESET} = V_{IL}$. The memory cell data is invalid when the operation is aborted. V_{DD} must be held higher than V_{DDLKO}; otherwise, the device is reset. The Block Erase operation must be re-executed when the device has been reset.

   If a protected block is included in the list of clocks to be erased by the Multi Block Erase, the protected block is not erased. Only the unprotected blocks are erased. If all the selected blocks are protected, the DQ6 bit stops toggling 100 μs after the rising edge of $\overline{WE}$ in the sixth command cycle, and then the device returns to Read mode.

DATA PROTECTION

The TC58F400/401 utilizes a JEDEC standard command sequence which protects data against accidental alteration due to noise (refer to Command Definitions).

V_{DD} LOCK-OUT VOLTAGE

The device is reset when V_{DD} is less than V_{DDLKO} (which is typically 3.7 V) to protect memory cell data against V_{DD} noise, and during power-up and Power-down. All commands are ignored when $V_{DD} < V_{DDLKO}$.

GLITCH PULSES

Glitches must be suppressed (to less than 5 ns) in order for operation to proceed smoothly.

POWER-ON

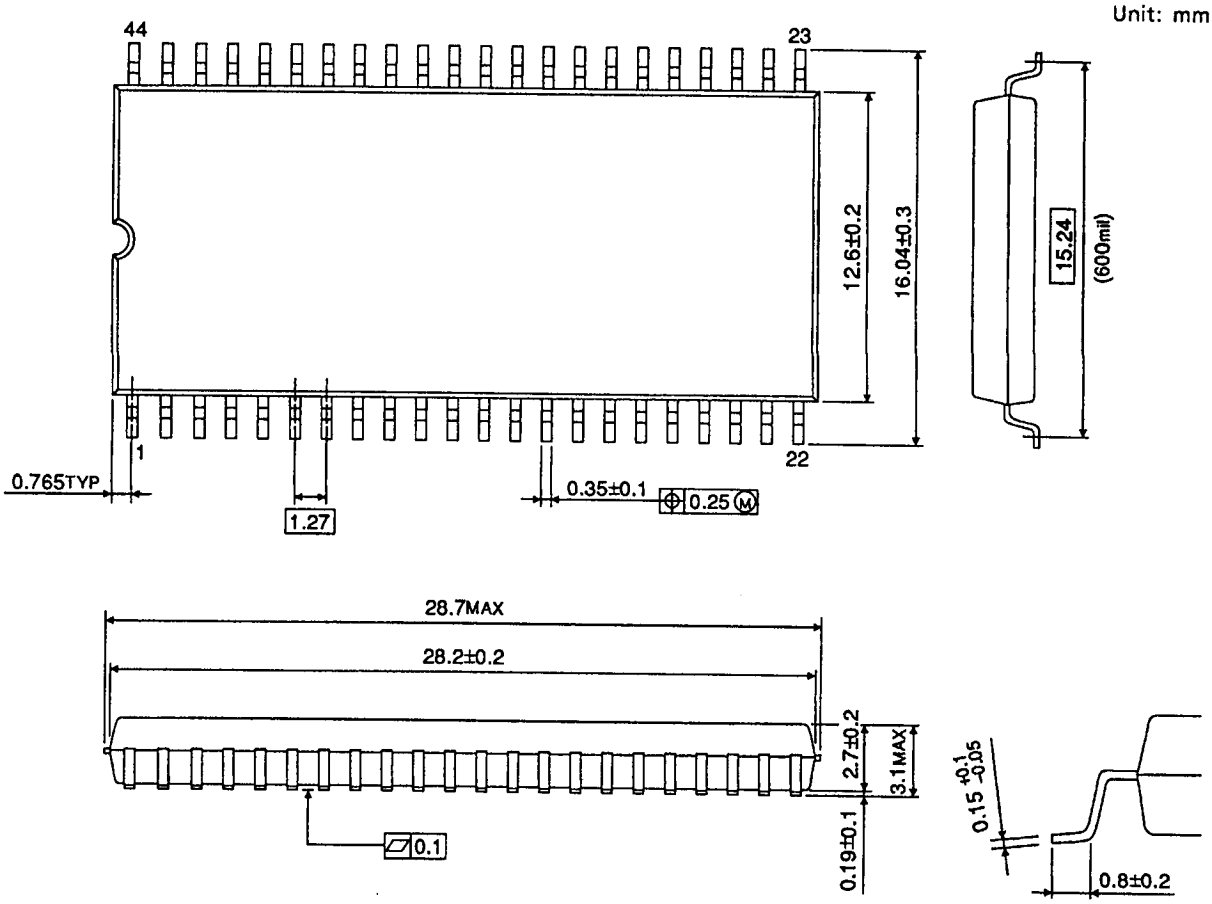
A command is not recognized on the rising edge of $\overline{WE}$ if V_{DD} rises from 0 V to the operating voltage while $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$. In this case the device is reset and enters Read mode.

PACKAGE DIMENSIONS

- Plastic SOP

  SOP44-P-600-1.27

Unit: mm



PACKAGE DIMENSIONS

- Plastic TSOP

TSOP I 48-P-1220-0.50

Unit: mm