INTEGRATED CIRCUIT

TOSHIBA

TECHNICAL DATA

TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT

TC58A040 F

SILICON GATE CMOS

4 MBIT (4 M × 1 BITS) CMOS AUDIO NAND E^{2}PROM

TENTATIVE DATA

DESCRIPTION

The TC58A040 is a 5-volt 4 Mbit NAND Electrically Erasable and Programmable Read Only Memory (NAND EEPROM) organized as 256 bits × 128 pages × 128 blocks.

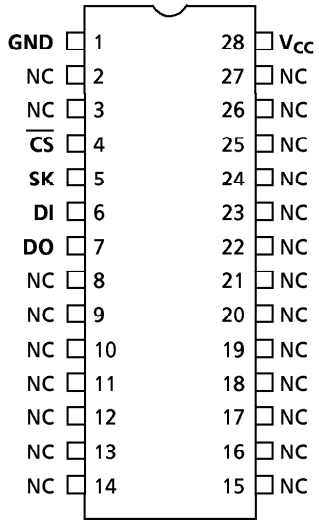
The device has a 256-bit static register which allows the program and read data to be transferred between the register and the memory cell array in 256-bit increments. The Erase operation is implemented in a single block unit (4 kbytes).

The TC58A040 is suitable for digital recording systems such as digital answering machines and personal digital recorders.

FEATURES

- Organization
  - Memory cell array 4 M × 1
  - Page Buffer 256 bits
  - Page size 256 bits
  - Block size 4 kbytes
- Mode
  - Read, Auto Program
  - Auto Block Erase, Status Read
- Mode control
  - Serial input/output
  - Command control
- Power supply
  - V_{CC} = 5 V ± 10%
- Access time
  - Cell array-Register 25 μs
  - Serial Read Cycle 250 ns
- Operating current
  - Read (500 ns cycle) 5 mA typ
  - Write 15 mA typ
  - Erase 10 mA typ
  - Standby 50 μA
- Package
  - TC58A040F: SOP28-P-450
    (Weight: 0.81 g typ)

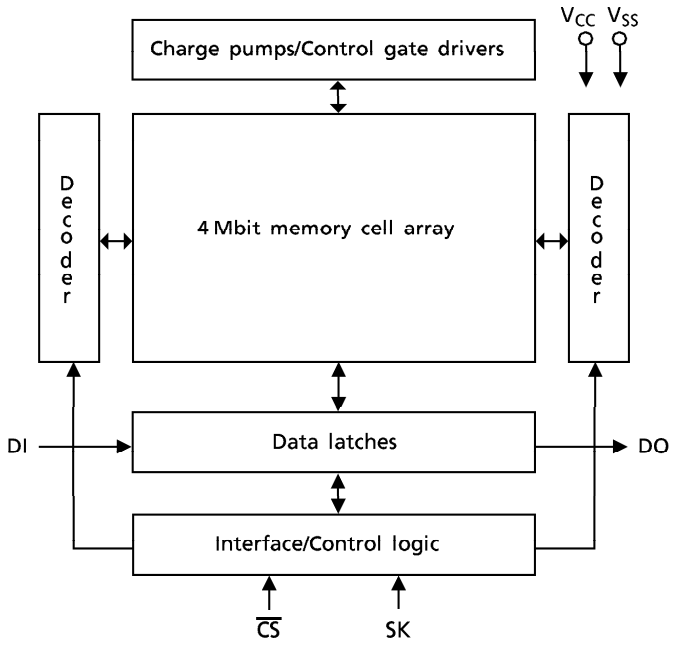
PIN ASSIGNMENT (TOP VIEW)



PIN NAMES

DO	Serial Data Output
DI	Serial Data Input
SK	Serial Clock
$\overline{CS}$	Chip Select
NC	No Connection
V_{CC}/V_{SS}	Power Supply

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{CC}	Power Supply	− 0.6 to 7.0	V
V_{IN}	Input Voltage	− 0.6 to 7.0	V
$V_{I/O}$	Input/Output Voltage	− 0.6 V to Vcc + 0.5 V (≦ 7 V)	V
P_D	Power Dissipation	0.5	W
T_{SOLDER}	Soldering Temperature (10 s)	260	°C
T_{STG}	Storage Temperature	− 55 to 150	°C
T_{OPR}	Operating Temperature	0 to 70	°C

CAPACITANCE *(Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
C_{IN}	Input	V_{IN} = 0 V	−	5	10	pF
C_{OUT}	Output	V_{OUT} = 0 V	−	5	10	pF

* This parameter is periodically sampled and is not tested for every component.

VALID BLOCKS

(1) The number of valid blocks in the range Block 0 to Block 126 (2) is:

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
N_{VP1}	Number of Valid blocks	117	TBD	127 (2)	Block

Note 1: The TC58A040 occasionally contains unusable blocks. Refer to Application Note (8) toward the end of this document.

Note 2: Block 127 is guaranteed to be good.

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{CC}	Power Supply	4.5	5.0	5.5	V
V_{IH}	High Level Input Voltage	2.2	–	V_{CC} + 0.5	V
V_{IL}	Low Level Input Voltage	– 0.3*	–	0.8	V

* – 2 V (pulse width ≦ 20 ns)

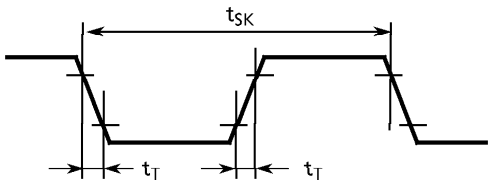
DC CHARACTERISTICS (Ta = 0° to 70°C, V_{CC} = 5 V ± 10%)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	–	–	± 10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0.4 V to V_{CC}	–	–	± 10	μA
I_{CCO1}	Operating Current (Read Cycle)	t_{cycle} = 250 ns	–	5	20	mA
I_{CCO2}	Operating Current (Read Cycle)	t_{cycle} = 1 μs	–	–	10	mA
I_{CCO3}	Operating Current (Program)	–	–	15	60	mA
I_{CCO4}	Operating Current (Erase)	–	–	10	40	mA
I_{CCS1}	Standby Current	$\overline{CE}$ = VIH	–	–	500	μA
I_{CCS2}	Standby Current	$\overline{CE}$ = V_{CC} – 0.2 V	–	–	50	μA
V_{OH}	High Level Output Voltage	I_{OH} = – 400 μA	2.4	–	–	V
V_{OL}	Low Level Output Voltage	I_{OL} = 2.1 mA	–	–	0.4	V

AC CHARACTERISTICS AND OPERATING CONDITIONS (Ta = 0° to 70°C, V_{CC} = 5 V ± 10%)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
t_{SK}	Serial Clock Cycle Time		250 *	–	ns
t_{SKH}	SK High Time		120	–	ns
t_{SKL}	SK Low Time		120	–	ns
t_{CS}	$\overline{CS}$ High Time		250	–	ns
t_{CSS}	$\overline{CS}$ Set-Up Time	Relative to SK Rising Edge	100	–	ns
t_{DIS}	DI Set-Up Time	Relative to SK Rising Edge	50	–	ns
t_{CSH1}	$\overline{CS}$ Hold Time	t_{CSH1}: Relative to DO Rising Edge	0	–	ns
t_{CSH2}	$\overline{CS}$ Hold Time	t_{CSH2}: Relative to SK Falling Edge	20	–	ns
t_{DIH}	DI Hold Time	Relative to SK Rising Edge	20	–	ns
t_{DF}	$\overline{CS}$ to DO in High Z		–	100	ns
t_{DH}	DO Hold Time	Relative to SK Falling Edge	0	–	ns
t_{PD}	Output Delay	Relative to SK Falling Edge	–	100	ns
t_{SADD}	Set Address Time		–	200	μs
t_R	Page Read Transfer Time		–	25	μs
t_{SKB}	SK to DO (Busy)	Relative to SK Falling Edge	–	200	ns

* t_T (transition time) = 5 ns



PROGRAMMING AND ERASING CHARACTERISTICS (Ta = 0° to 70°C, V_{CC} = 5 V ± 10%)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
t_{PROG}	Programming Time	–	300 to 1000	2000	μs
t_{BERASE}	Block Erasing Time	–	7	100	ms
$N_{W/E}$	Number of Write/Erase Cycles	–	–	10^5	Cycles
N_{PP} *	Number of Programming Cycles on Same Master Page	–	–	50	Cycles

*: Refer to the Partial Page Write operation.

PIN DESCRIPTIONS

Serial Data Input: DI

The DI pin is used for inputting in commands and data. Commands and data are latched on the rising edge of SK.

Serial Data Output: DO

The DO pin is used for outputting status and data. Data is available t_{PD} after the falling edge of SK. DO indicates the internal state except during data output. A low level indicates that the device is busy. A high level indicates that the device is ready.

Chip Select: $\overline{CS}$

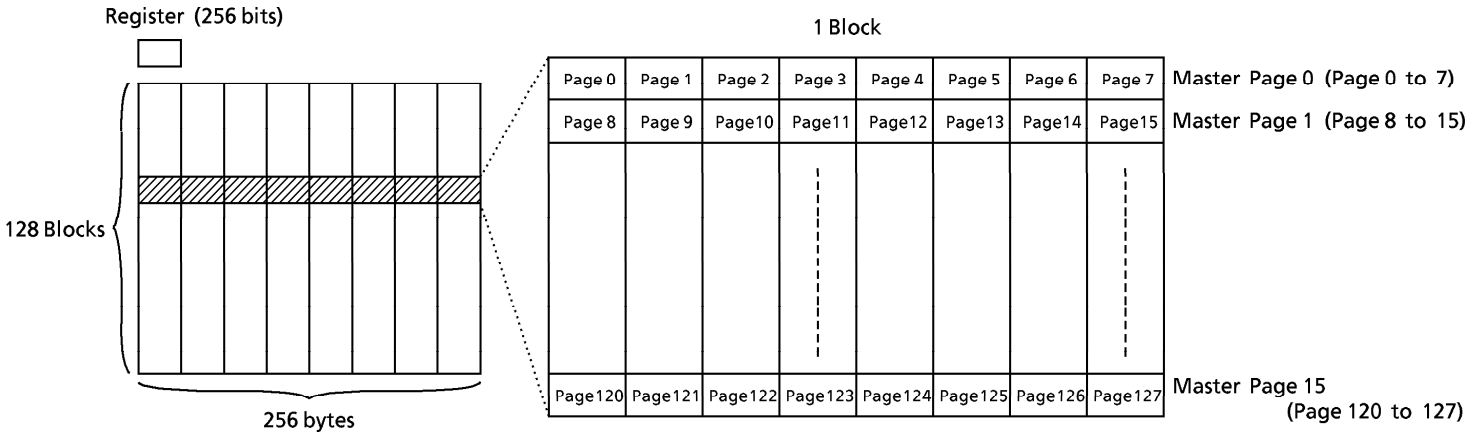
This signal enables the device. When this signal is high, the device ignores SK. This signal can be tied to ground when there is only one Audio-NAND device. The $\overline{CS}$ pin may be pulled high to reset the device.

Serial Clock: SK

This signal controls serial data input and output. Commands and data are latched on the rising edge of SK. Data is output on the falling edge of SK.

ORGANIZATION

The TC58A040F is a 4 Mbit device organized as 128 blocks of 16 master pages. A master page is further segmented into 8 pages as shown in the following figure. The Write and Read operations are executed on a page basis and Erase is executed on a block basis.



1 page = 256 bits

1 master page = 8 pages = 256 bytes

1 block = 16 master pages = 128 pages = 4096 bytes

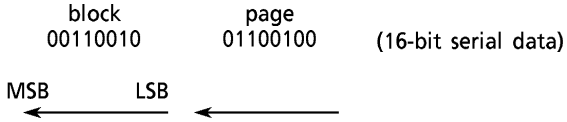
A page is the unit of reading and programming.
A block is the unit of erasure.
A master page is divided into 8 pages. These 8 pages are controlled by a common word line.

ADDRESS ASSIGNMENT

The address is acquired through the DI pin using 16 consecutive clock cycles. The first 8 bits are the block address. The last 8 bits are the page address.

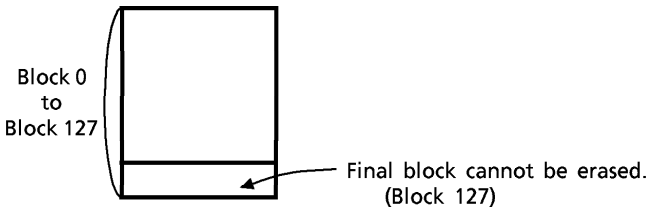
	DECIMAL	BINARY
Block address	0 to 126	00000000 to 01111110
Page address	0 to 127	00000000 to 01111111

example: Page 100 in block 50



WRITE-ONCE BLOCK

The TC58A040 has 128 blocks (blocks 0 to 127). The final block (block 127) has been set aside as a read-only block. Once data is written, this block cannot be erased. This block needs a special command for reading and writing. Block 127 may be used for storing system configuration information that cannot be lost.



COMMAND TABLE

There are 12 commands in the TC58A040 command set. All operations are controlled by these commands, shown in the following table.

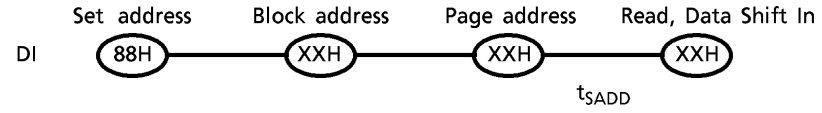
INSTRUCTION	START BIT	OPCODE	RESERVED	HEX COMMAND
Get Status	1	0000	000	80H
Set Address	1	0001	000	88H
Increment	1	0010	000	90H
Read	1	0011	000	98H
Write	1	0100	000	A0H
Erase	1	0101	000	A8H
Data Shift In	1	0110	000	B0H
Data Shift Out	1	0111	000	B8H
Write Enable	1	1100	000	E0H
Write Disable	1	1101	000	E8H
Write Last Block	1	1110	000	F0H
Read Last Block	1	1010	000	D0H

COMMANDS

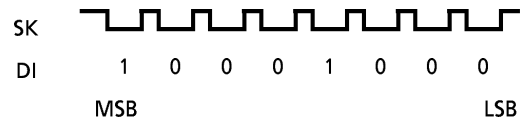
Set Address

The Set Address command defines which block and page of the memory an operation will operate on. The Set Address command is followed by two bytes, the first indicating the block number and the second indicating the page number. The Set Address command is usually followed by a Read or a Data Shift In command. Between the page address byte and the next command there is a delay of t_{SADD}.

The address that is selected remains the active address until a new Set Address or Increment command is given.



Example: If inputting the 88H command, the MSB must be input first.



Increment

The Increment command automatically increments the page address.
When the last page in a block is selected, if the Increment command is input, the address is set to 00H (Page 0) in the next block.
However, if the last page in the last block (Block 126) is selected, the Increment command will set the address to 00H (page 0) in the same block (Block 126).

Read

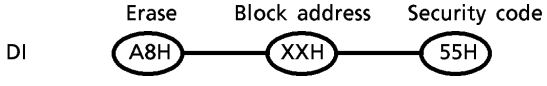
The Read command transfers data from the selected page of the memory array into the on-chip buffer (256-bit shift register). The Read command is usually followed by a Data Shift Out command. There is a delay of t_R between the Read command and the Data Shift Out command as the data is transferred from the memory array to the on-chip buffer.

Write

The Write command programs data from the on-chip buffer into the selected page of the memory array. A security code (55H) follows the Write command to ensure against accidental writes. Get Status may be used to ensure that the operation was successful. The Write command will be ignored if Write Disable has been set.

Erase

The Erase command erases a selected block. The Erase command is followed by the block address. A security code (55H) follows the block address to ensure against accidental erasure. The Get Status command may be used to verify that the operation was successful. The Erase command will be ignored if Write Disable has been set.



Get Status

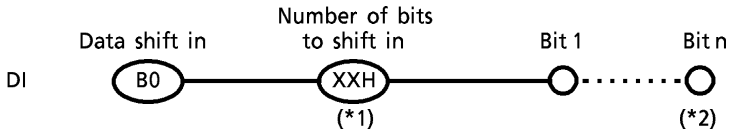
The Get Status command is used to output the status of the TC58A040. The eight status bits are defined as follows.

BIT	STATUS	OUTPUT
0 (LSB)	Ready/Busy	Ready: "1" Busy: "0"
1	Pass/Fail	Pass: "1" Fail: "0"
2	Write Enable/Write Disable	Write Enable: "1" Write Disable: "0"
3	Not Used	Unknown "1" or "0"
4	Not Used	Unknown "1" or "0"
5	Not Used	Unknown "1" or "0"
6	Not Used	Unknown "1" or "0"
7 (MSB)	Not Used	Unknown "1" or "0"

The status is output LSB first.

Data Shift In

The Data Shift In command is used to shift data into the on-chip buffer. The number of bits sent into the buffer is determined by an 8-bit argument following the command. The Data Shift In command is usually used prior to the Write command.



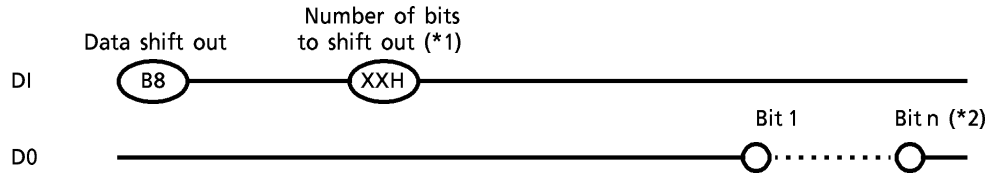
The value of (*1) is 1 less than the actual number of bits to be shifted in (*2).

Example:

Number of bits (*2)	n = 256	n = 128	n = 1
Number of bits argument (*1)	FFH = 11111111	7FH = 01111111	00H = 00000000

Data Shift Out

The data Shift Out command is used to shift data out of the on-chip buffer. The number of bits sent out of the buffer is determined by an 8-bit argument following the command. The Data Shift Out command is usually used after a Read command.



The value of (*1) is 1 less than the actual number of bits to be shifted out (*2).

Example :

Number of bits (*2)	n = 256	n = 128	n = 1
Number of bits argument (*1)	FFH = 11111111	7FH = 01111111	00H = 00000000

Write Disable

The Write Disable command is used to prevent inadvertent writing or erasure. Once this command has been executed, no subsequent Write or Erase commands will be accepted. The Status Read operation (Get Status command) can be used to determine whether the device is in the Write Enable or Disable state.

Write Enable

The Write Enable command is used to cancel Write Disable mode.

Read Last Block

The Read Last Block command is used to read the contents of the final block (Block 127). The Set Address command and 2 address bytes are required to set the page address. The block address is automatically set to 127, so the first address byte is ignored.

Write Last Block

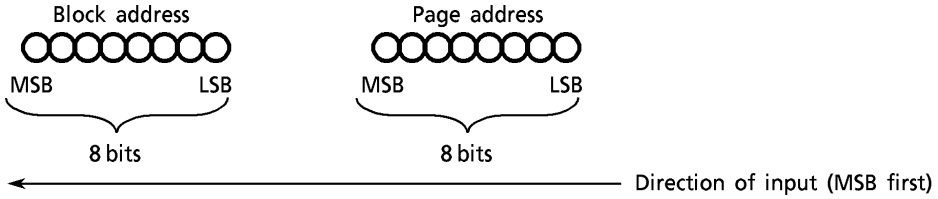
The Write Last Block command is used to program into the selected page in the final block (Block 127). Once data is written into the last block, it cannot be erased. A security code (55H) follows the Write Last Block command to ensure against accidental writes.

DEVICE OPERATION

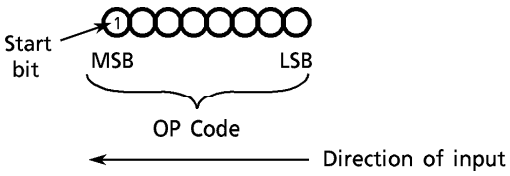
Input/Output operation

The TC58A040 has separate input and output pins. Address, command and input data are input as serial data through DI. Status data and output data are output as serial data through DO. Input and output operations are as follows.

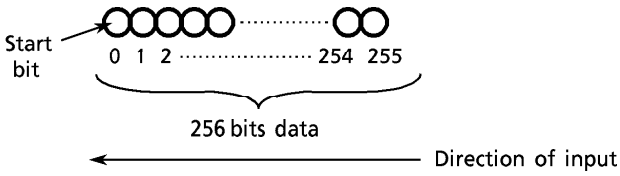
(1) Address input



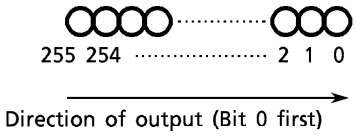
(2) Command input



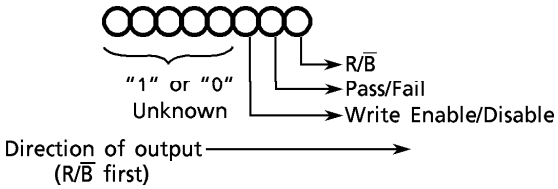
(3) Data input



(4) Data output



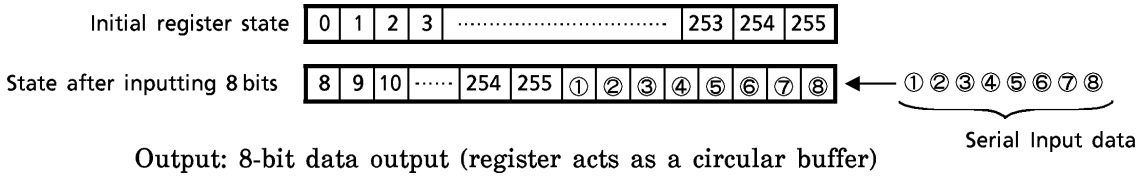
(5) Status data output



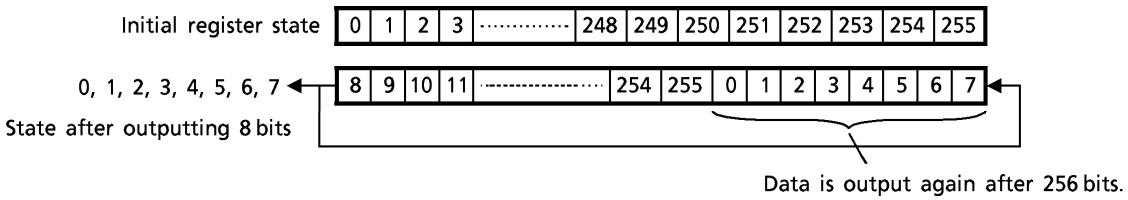
Register operation

The TC58A040 has a 256-bit shift register on the chip. This register is used to transfer data to and from the memory cell array. The register operation is as follows:

Input: 8-bit data input (new data shifts out oldest data)



Output: 8-bit data output (register acts as a circular buffer)



Read Operation

The Read operation transfers data to the register from the memory cell array and outputs data synchronized to SK. This operation is shown in Figure 1.

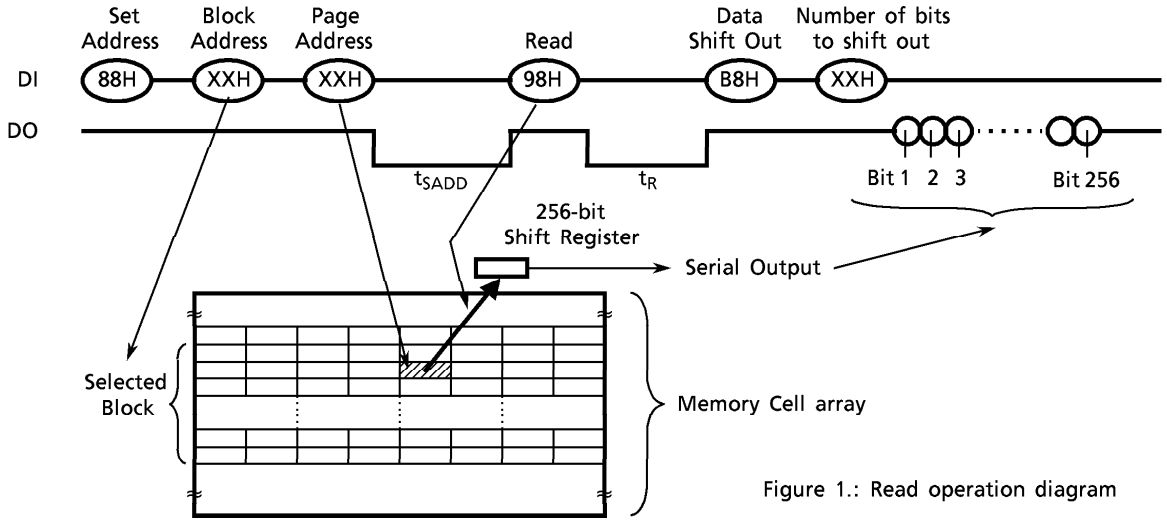
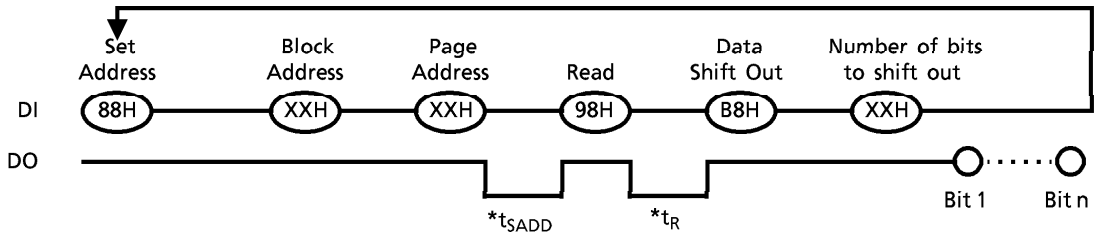


Figure 1.: Read operation diagram

The read operation is executed page by page. When reading from two or more consecutive pages, two methods are possible:

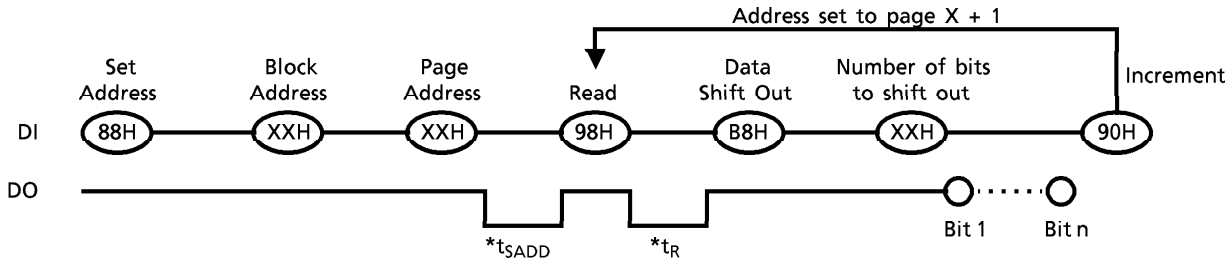
· Read Mode (1)

The set address command is input for every page read cycle.



· Read Mode (2)

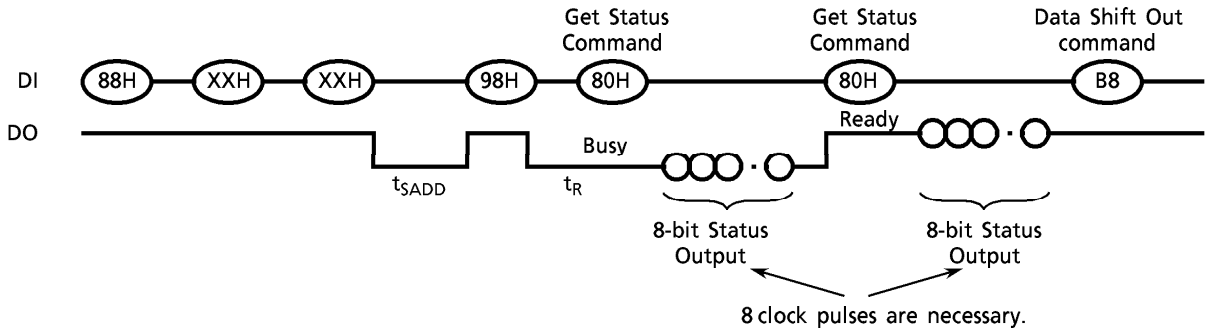
The Increment command is used instead of applying the Set Address command.



* D0 becomes low and is held low during the Busy state.
The device state (Busy or Ready) can be output by executing the Status Read operation.

Status Read Operation

This operation outputs the device's internal state by using the Get Status command.



Write Operation

The Write operation inputs data into the on-chip data register, and transfers the data from the register into the selected page in the memory array. This operation is shown in Figure 2.

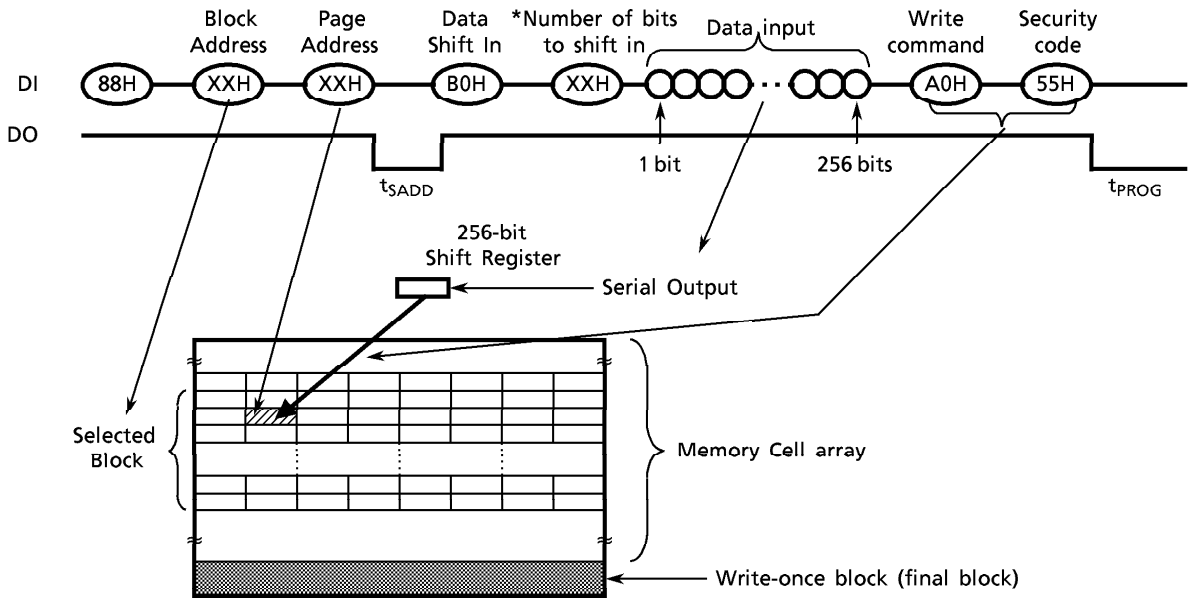
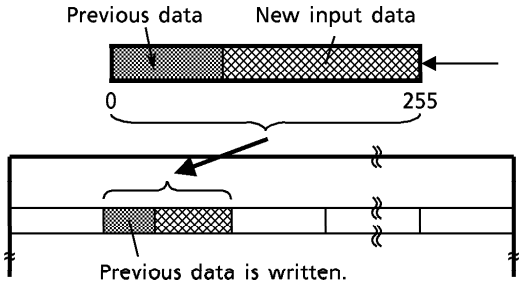


Figure 2. Write operation diagram

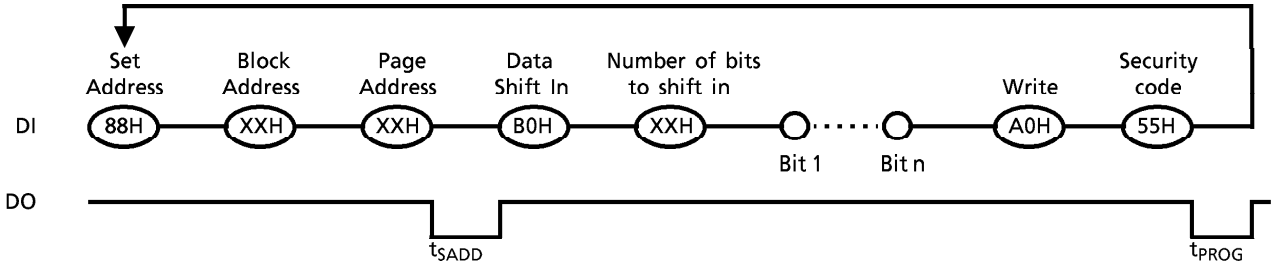
* Number of bits to shift in: 256 (#FFH) should be input.
If the number of bits to shift in is less than 256 (#FFH), previous data will be written into the memory array.



The Write operation is executed page by page. When writing two or more consecutive pages, two methods are possible:

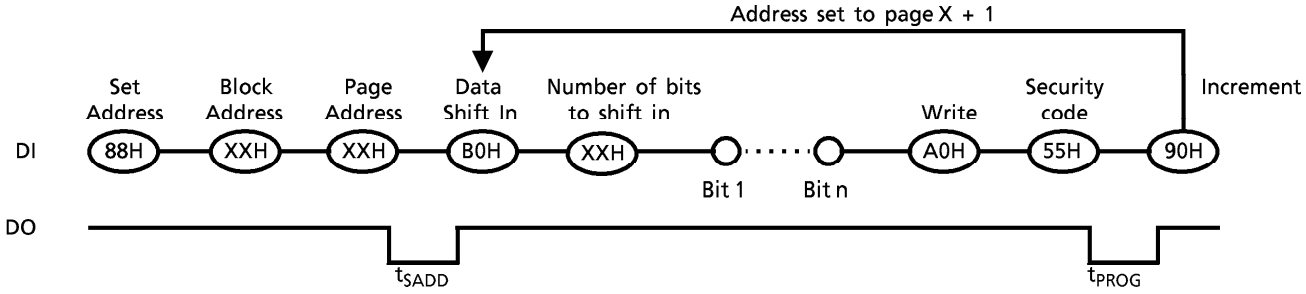
· Write Mode (1)

The Set Address command is input for every Page Write operation.



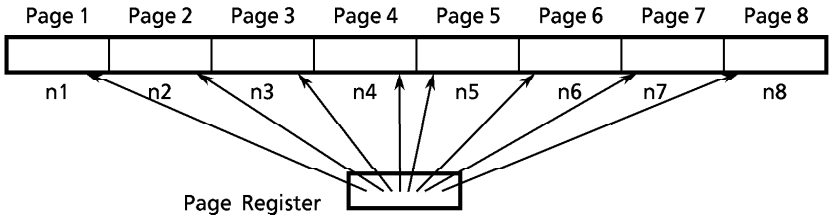
· Write Mode (2)

The Increment command is used instead of applying the Set Address command.



· Partial Page Write operation

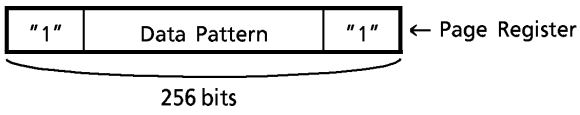
The TC58A040 allows a master page to be divided into a maximum of 50 segments with each page segment written individually as follows:



Npp = n1 + n2 + n3 + n4 + n5 + n6 + n7 + n8 = 50
* n1 to n8: Number of partial programs in a page
* Npp : Number of partial programs in a master page

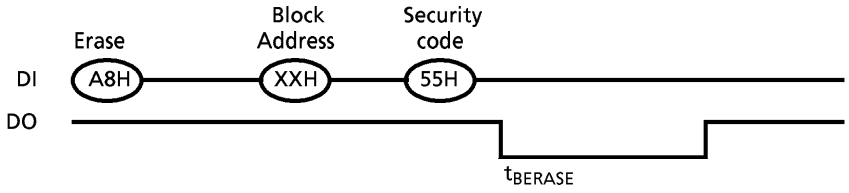
The input data for unprogrammed or previously programmed page segments must be "1".

Example:



Erase Operation

The Erase operation is executed block by block. The Erase operation sequence is shown below.

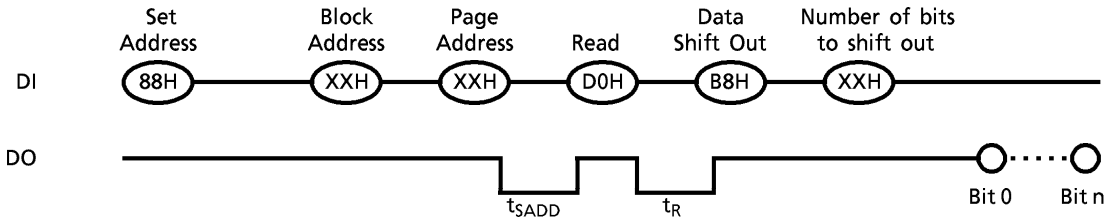


Read and Write operation for the final block (write-once block)

The final block (Block 127) has been set aside as a read-only block. Hence, the final block needs special commands for the Read and Write operations.

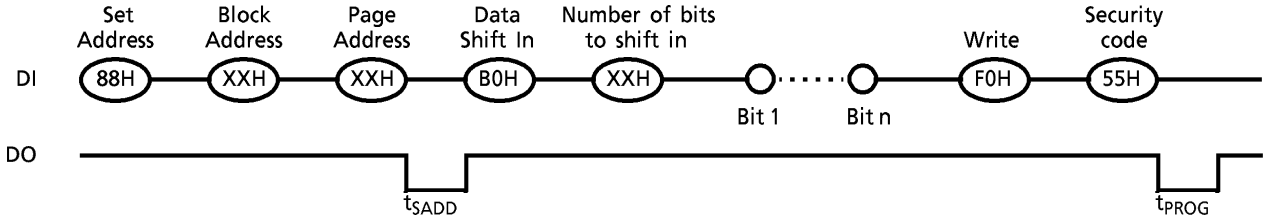
Read Last Block

The block address is ignored.



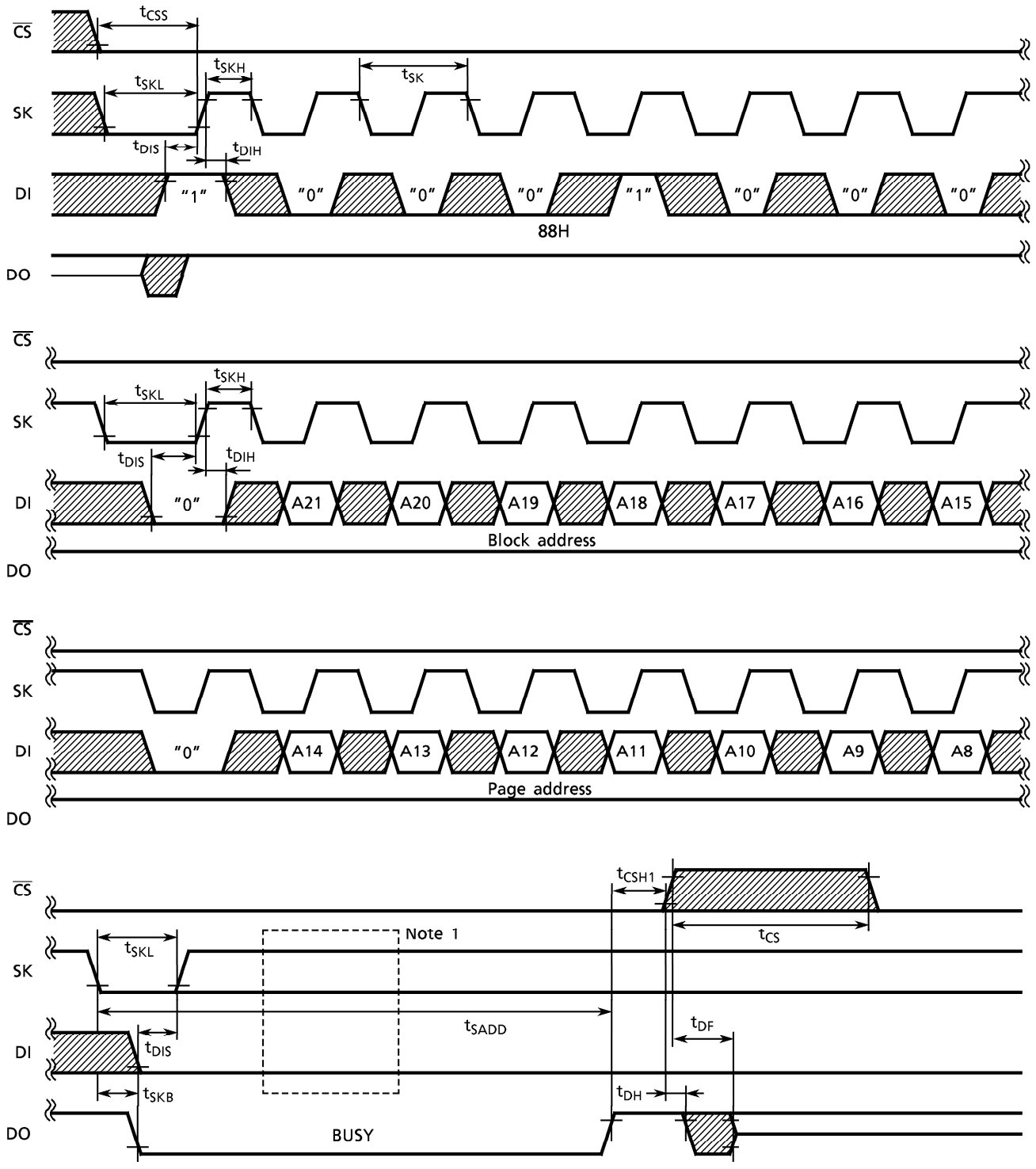
Write Last Block

The block address is ignored.



TIMING DIAGRAMS

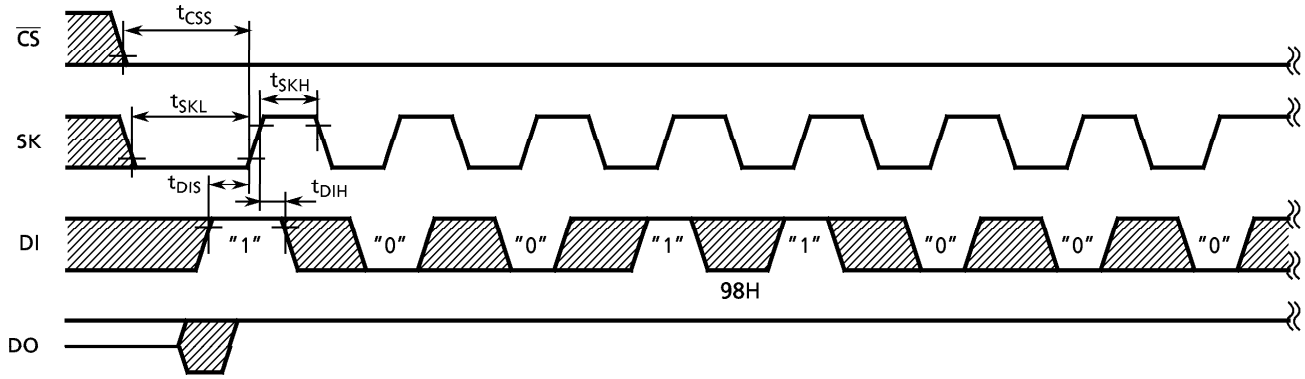
Set Address

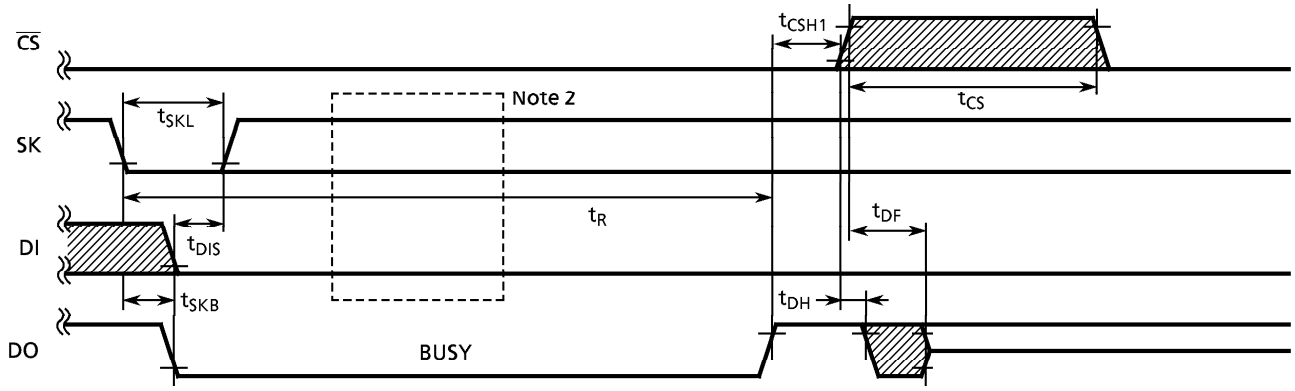


* Note 1: Refer to Application Note (7).

Note: The above 4 timing diagrams are contiguous.

Read

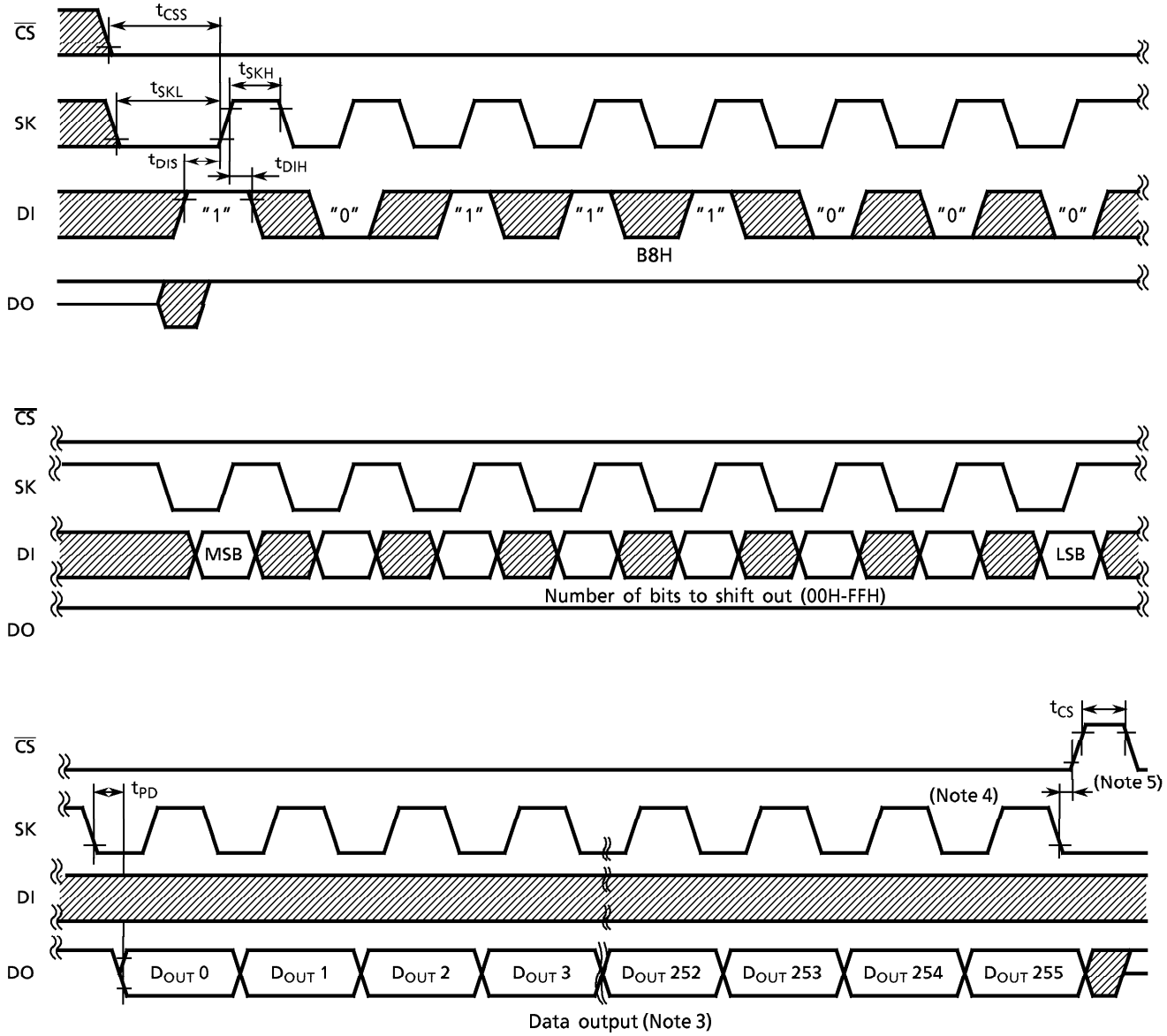




* Note 2: Refer to Application Note (7).

Note: The above 2 timing diagrams are contiguous.

Data Shift Out



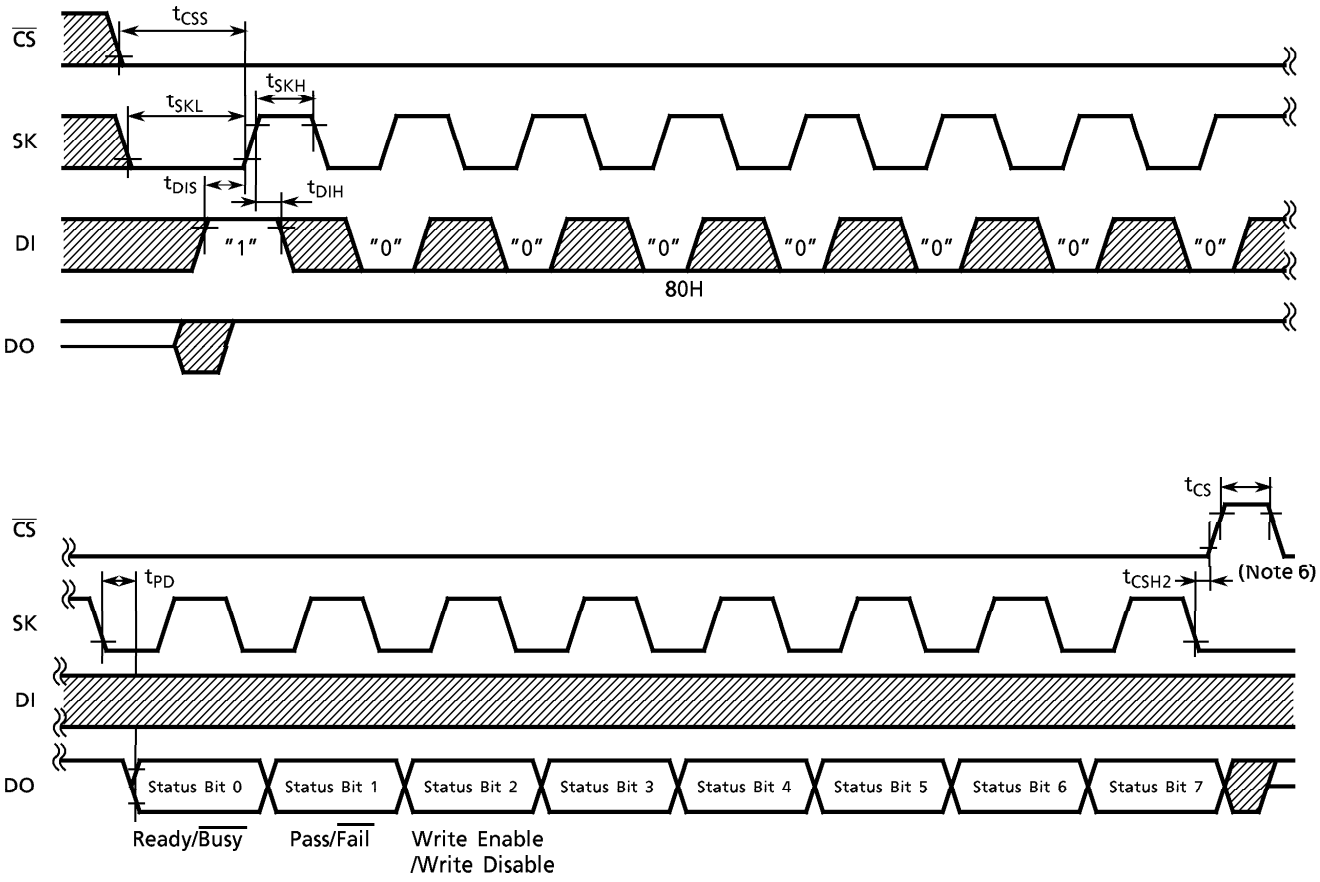
Note 3: FFH input as the number of bits to shift out.

Note 4: Refer to Applicaton Note (6).

Note 5: Refer to Applicaton Note (9).

Note: The above 3 timing diagrams are contiguous.

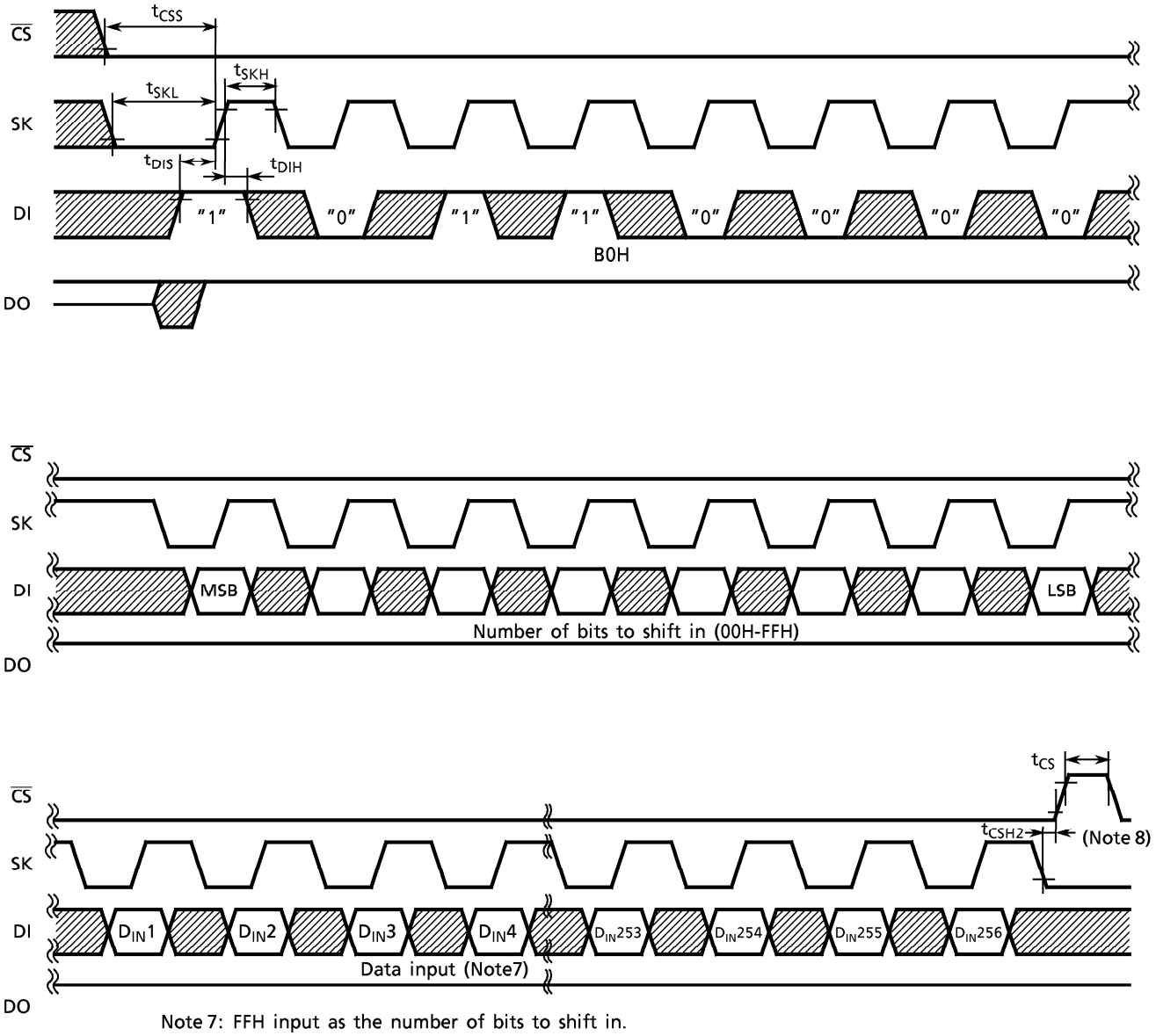
Status Read



Note 6: Refer to Applicaton Note (9).

Note: The above 2 timing diagrams are contiguous.

Data Shift In

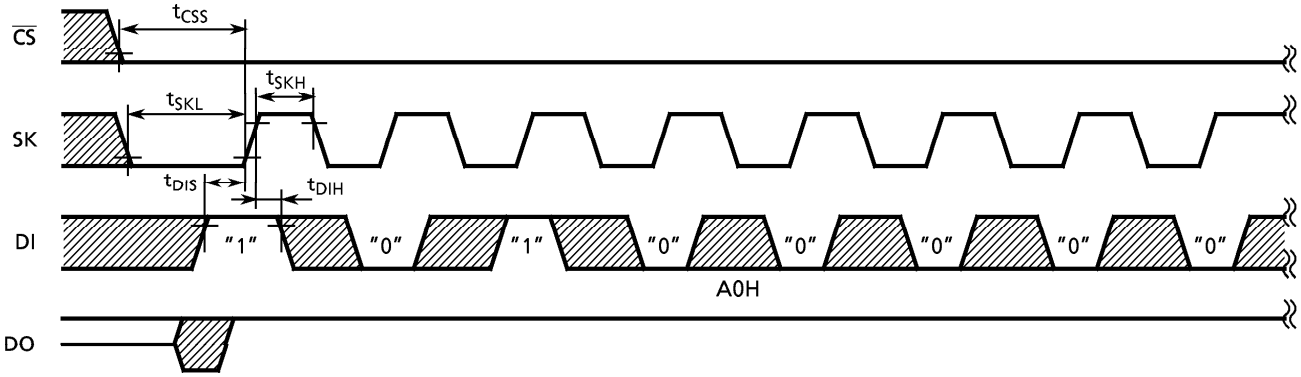


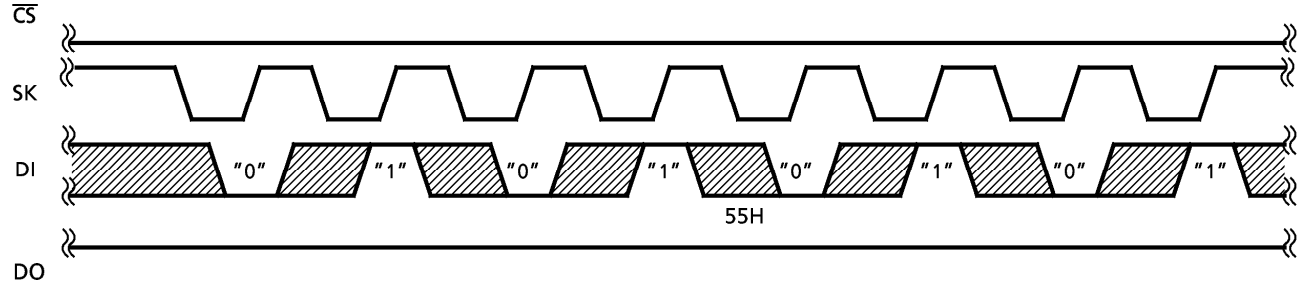
Note 7: FFH input as the number of bits to shift in.

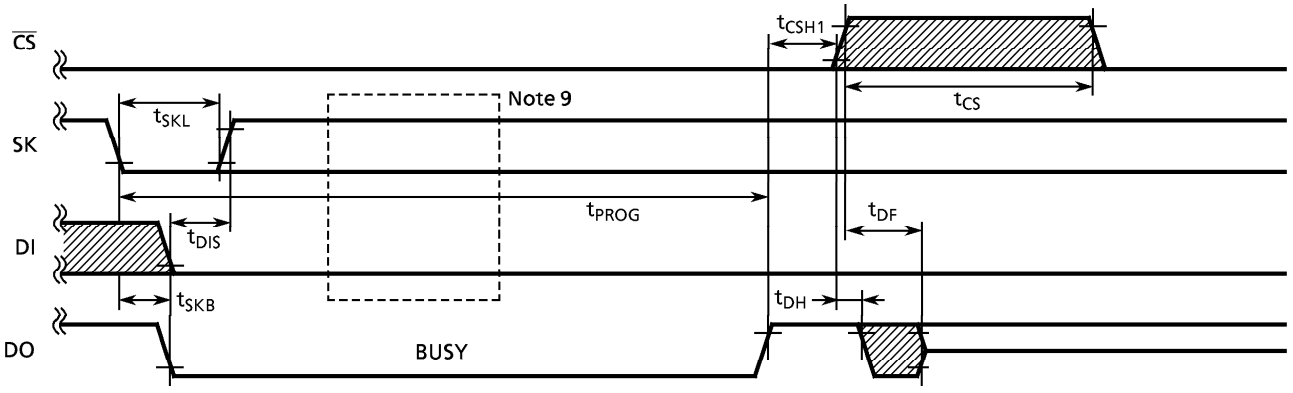
Note 8: Refer to Applicaton Note (9).

Note: The above 3 timing diagrams are contiguous.

Write



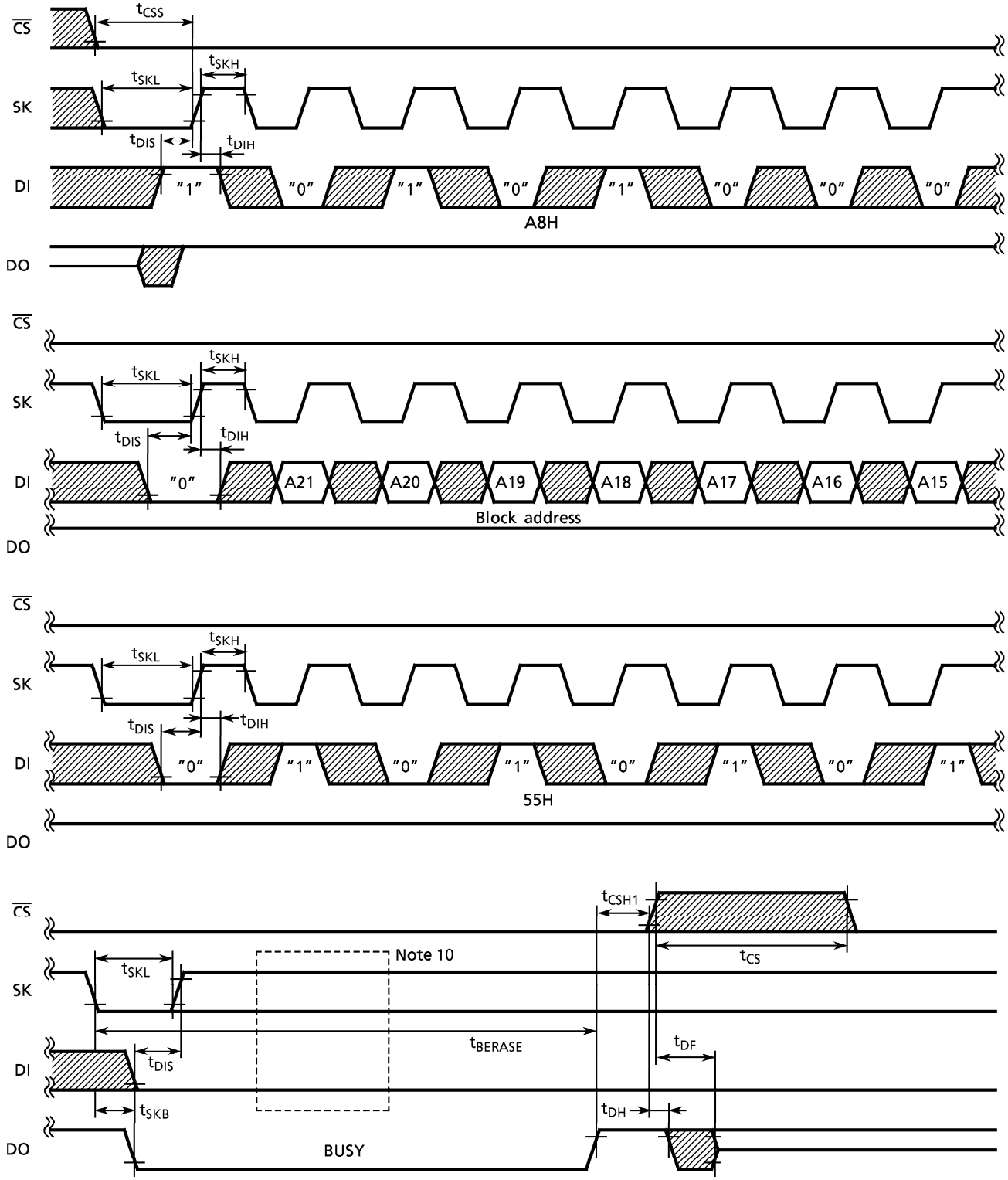




* Note 9: Refer to Applicaton Note (7).

Note: The above 3 timing diagrams are contiguous.

Erase



* Note 10: Refer to Applicaton Note (7).

Note: The above 4 timing diagrams are contiguous.

APPLICATION NOTES AND COMMENTS

(1) Prohibition of unspecified commands

The 12 operation commands are listed in the command table. Commands other than these specified commands are prohibited. Stored data may be corrupted if an unspecified command is entered during the command cycle.

(2) Interruption by $\overline{CS}$ going high

During the period when the TC58A040 is reading a page from the array (t_R), writing a page to the array (t_{PROG}), or erasing a block (t_{BERASE}) or setting address (t_{SADD}), the operation will complete regardless of the state of $\overline{CS}$. When the $\overline{CS}$ pin go high during busy, the DO pin is in high impedance.

(3) Device reset

The TC58A040 is reset whenever $\overline{CS}$ changes from low to high. The command register will be cleared at this point. The data register will continue to hold whatever data is in the register. To clear the data register, 32 bytes of "00H" data must be input. $\overline{CS}$ does not affect operations as described in Application Note (2) above.

(4) Write disable at power-up

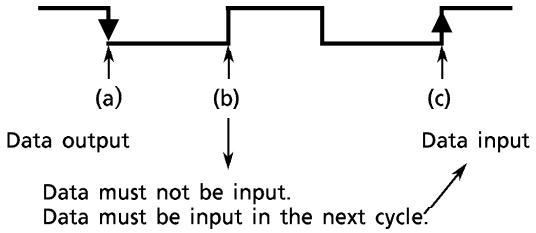
On power-up, the TC58A040 is set to Write Disable mode. This prevents any spurious writes to the device. To enable write operations, the Write Enable (E0H) command must be given.

(5) Prohibition of extra clocks

If an unexpected clock pulse is induced on the SK terminal by noise, the device may malfunction. Also, the device has no reset command. Therefore, noise must be controlled.

(6) Prohibition of data output and data input in the same cycle

Input and output operations in one cycle is prohibited. The following diagram shows an example.



(7) Busy state signal

When the device is in the Busy state (when the TC58A040 reads a page from the array (t_R), writes a page to the array (t_{PROG}), erases a block (t_{BERASE}), or decodes an address (t_{SADD})), the DO pin outputs a low level (Busy status). During this period operations, other than Status Read, are prohibited. If SK is clocked during this period, other than during a Status Read operation, the DI pin must be kept low. If SK is held high or low, the DI pin = "don't care".

(8) Identification of bad blocks

The TC58A040 may contain unusable blocks. Bad blocks must be identified by user software during initial operation. The figure below describes how to identify bad blocks.

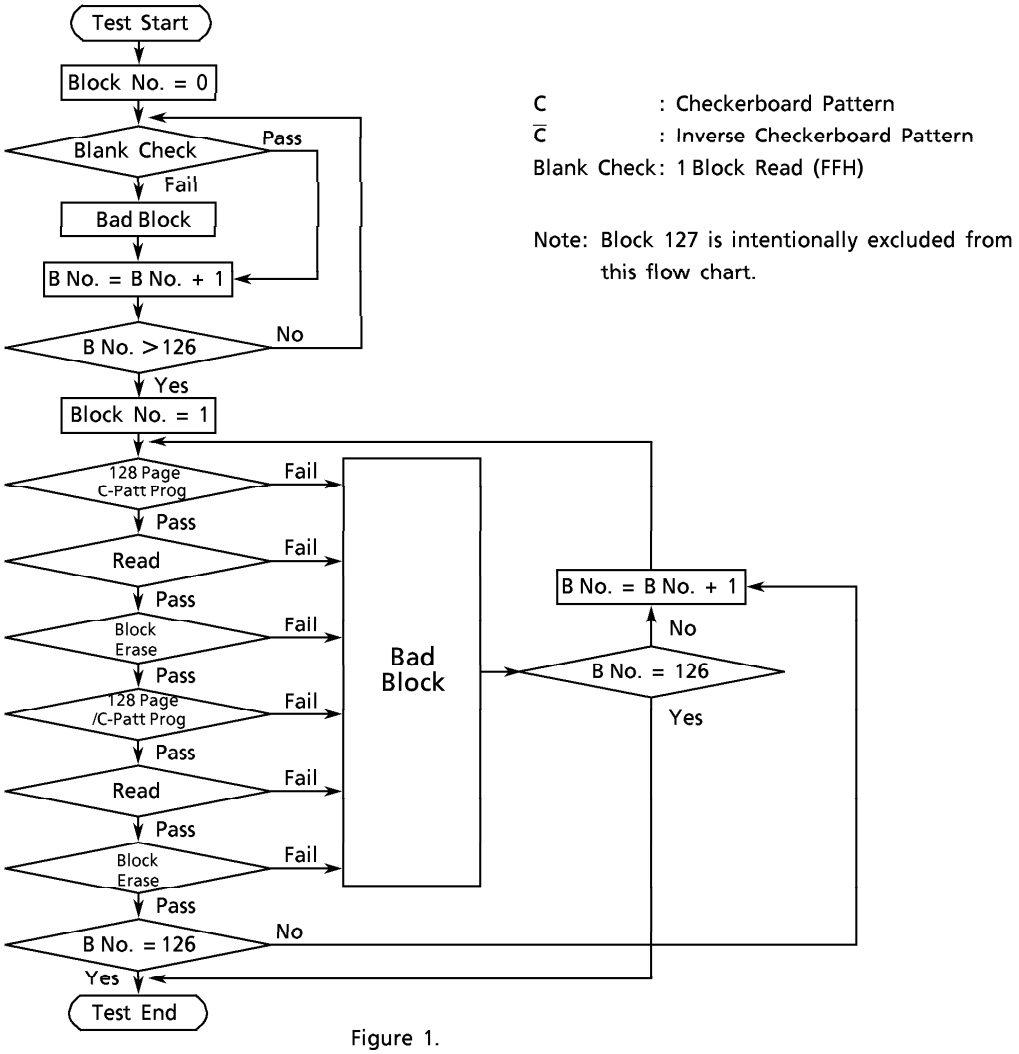
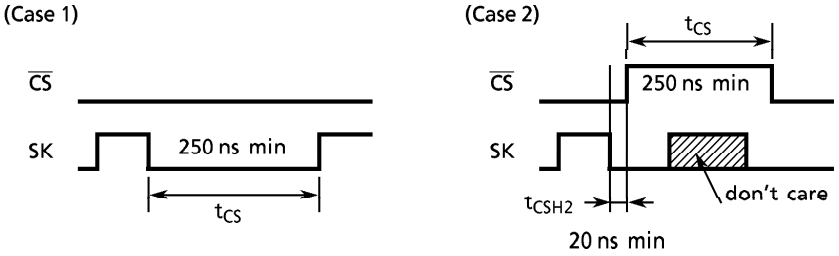


Figure 1.

(9) End-of-operation signal

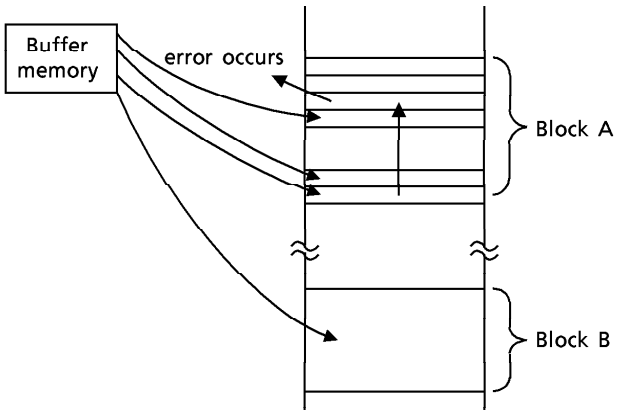
When a Data Shift Out, Data Shift In, or Status Read operation finishes, the $\overline{CS}$ pin must go high or SK must stay low for at least 250 ns. This must occur before subsequent commands are input, such as Increment, Write Enable, or Write Disable.



(10) Error in Program or Erase operation (failure of at Status Read)

The device may fail during a Program or Erase operation due, for example, to the Write/Erase cycle limits being exceeded. The following system architecture will ensure high system reliability if a failure occurs:

Program



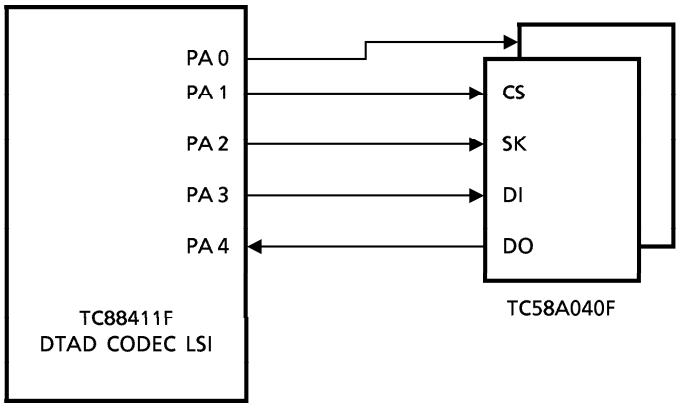
If an error occurs in Block A, try to reprogram the data into another block, Block B, by loading from an external buffer. Then, prevent further system accesses to Block A (by creating a "bad block" table or some other appropriate scheme).

Erase

When the error occurs after an Erase operation, prevent future accesses to this bad block (again by creating a table within the system or some other appropriate scheme).

SYSTEM CONCEPTS

TC58A040 is a 4 Mbit NAND E²PROM designed to provide the most cost effective solution for digital audio recording applications. For digital audio storage, the TC58A040 has been matched with DTAD CODEC LSI TC88411F. Applications that can benefit from this combination include digital answering machines and personal digital recorders. Customers can quickly bring to market systems capable of recording up to 15 minutes of audio on a single 4 Mbit device. Multiple TC58A040s can be used to extend the recording time.



DATA TRANSFER RATE

The data transfer rate of the TC58A040 is as follows:

	DATA TRANSFER RATE		TOTAL TIME	
	PAGE	BLOCK	PAGE	BLOCK
Read	0.85 Mbits/s	2.60 Mbits/s	301 μs	12.6 ms
Write (t_{PROG}: 400 μs)	377.6 kbits/s	538.3 kbits/s	678 μs	60.9 ms
Erase (t_{ERASE}: 7.0 ms)	–	–	–	7.0 ms

DEVICE PHYSICS

Program Operation

Figure 2 shows the NAND memory cell level details of the programming mechanism. The Program operation is used to write "0" data into an erased memory cell ("1" data cell) using a tunneling mechanism. An example Program operation to program "0" data into TR1 and "1" data into TR2 is as follows:

(1) A high level is applied to Select line 1 and a low level is applied to Select line 2 so that the device is connected to the Bit line and disconnected from the ground line.
(2) Vpp (to 20 V) is applied to the selected word line and an inhibit voltage of VPI (≈ 10 V) is applied to the unselected word lines.
(3) 0 volts is applied to the bit line tied to cell transistor TR1 and the inhibit voltage VDP1 (≈ 10 V) is applied to the bit line tied to TR2.
(4) Vpp is applied between the control gate and the channel in TR1, as shown in Figure 2, which causes electrons to be injected from the channel to the floating gate by a tunneling.
(5) The injected electrons are captured in the floating gate (surrounded by an oxide layer) and will remain, even after power is cut off, until they are removed by an Erase operation.
(6) Although 20 volts is applied to the control gate of TR2, the voltage difference between the control gate and the channel is only 10 V because the voltage of the channel is 10 V. Therefore, tunneling does not take place (i.e. the electron is not injected into the floating gate.)
(7) Tunneling does not take place in the unselected pages because of the 10 V (VPI) applied to the unselected word lines which makes the voltage difference between the control gate and channel only 10 volts.
Thus, the floating gate of the "0" cell is charged to "Minus" and that of the "1" cell is charged to "Plus".

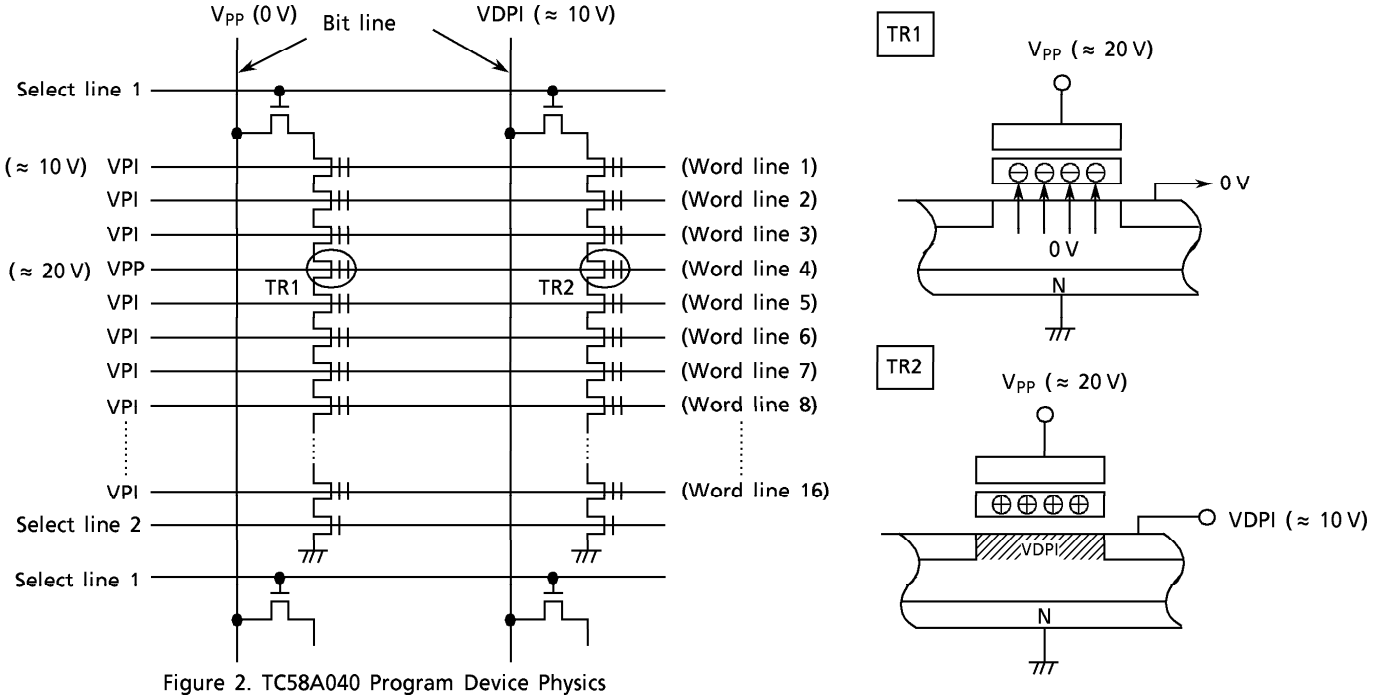


Figure 2. TC58A040 Program Device Physics

Erase Operation

Figure 3 shows the NAND memory cell level details of the Erase mechanism. The Erase operation is used to turn the "0" (programmed) cells back to "1" in a block. The captured electrons are pulled out from the floating gate to the substrate by a tunneling.
Zero volts is applied to the control gate and Vpp (to 20 V) is applied to the substrate so that a 20-volt potential is created and the electrons in the floating gate are pulled out by the tunneling.

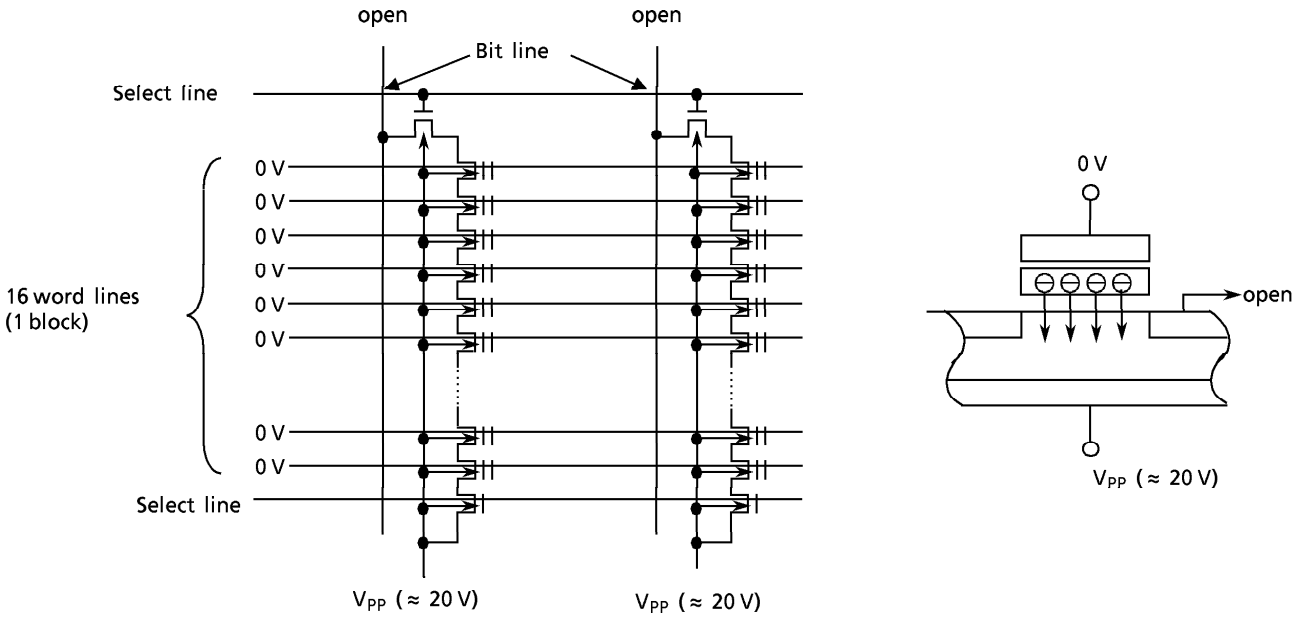


Figure 3. TC58A040 Erase Device Physics

Read operation

After programing the state of the memory cell is either "0" (minus charge on the floating gate) or "1" (plus charge on the floating gate). Each state is indicated by a "threshold voltage (Vth)" which is a characterization parameter of the MOS transistor as shown in Figure 4. The threshold voltage of a transistor with data "0" is distributed in the "plus" region while a transistor with data "1" is distributed in the "minus" region. The distribution band depends on transistor fluctuations.

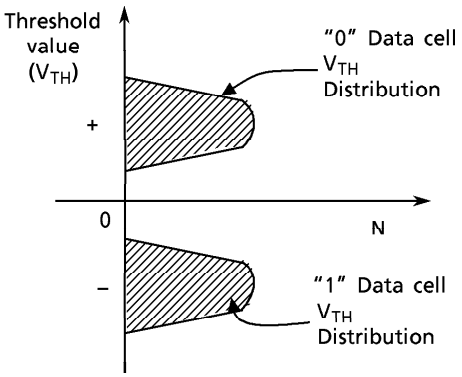


Figure 4. V_{TH} Distribution for "0" and "1" data cells

Figure 5 shows memory cell level details of the Read operation.

(1) A high voltage is applied to Select lines 1 and 2 in the block which includes the selected page, so that the 16 NAND memory cells are connected to the Bit line and ground.

(2) Zero volts is applied to the control gates of the selected page and a high level voltage is applied to the control gates of the unselected pages.

(3) In Figure 5, transistor TR2 with data "1" turns on, transistor TR1 with data "0" turns off, and all other unselected transistors turn on.

(4) The precharged bit line tied to TR2 is discharged through TR2 as cell current flows to ground, while the precharged bit line tied to TR1 remains high level because current does not flow. The sense amplifiers tied to the bit lines thus sense the voltage levels as "1" and "0" respectively.

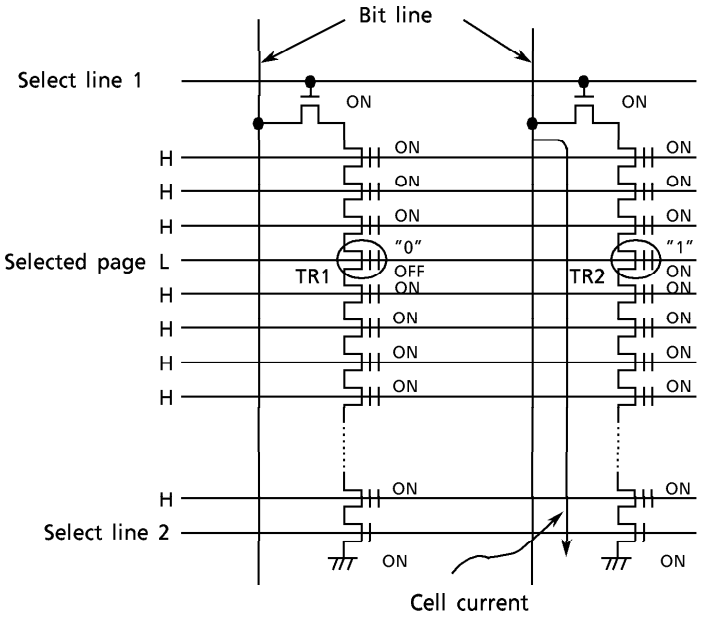


Figure 5. TC58A040 Read Device Physics

PACKAGE DIMENSIONS

● Plastic SOP

SOP28-P-450

UNITS: mm