TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

8 M (1 M × 8) BIT CMOS FLASH MEMORY

DESCRIPTION

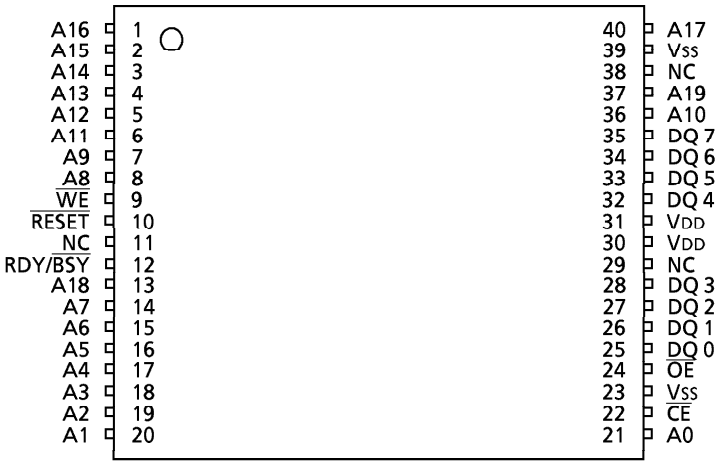
The TC58FVT008/B008 is a 8,388,608 - bits, 3.0 Volt - only Electrically Erasable and Programmable Flash memory organized as 1,048,576 words × 8 bits. The TC58FVT008/B008 features commands for read, program and erase operations to allow easy interfacing to microprocessors. The commands are based on the JEDEC standard. The program and erase operations are automatically executed in the chip. The device has chip, block and multi - block erase capability.

The TC58FVT008/B008 is available in a 40 - pin TSOP package to suit a variety of design applications.

FEATURES

- Power Supply
  V_{DD} = 2.7 V to 3.6 V
- Organization
  1 M × 8 bits
- Modes
  Auto Program
  Auto Chip Erase
  Auto Block Erase
  Auto Multiple Block Erase
  Erase Suspend / Resume
  Block Protection
  Data Polling / Toggle Bit
- Block Erase Architecture
  1 × 16 K byte / 2 × 8 K byte / 1 × 32 K byte / 15 × 64 K byte
- Boot Block Architecture
  TC58FVT008FT ····· Top Boot Block
  TC58FVB008FT ····· Bottom Boot Block
- Mode Control
  Compatible with JEDEC - standard command
- Erase / Program Cycles
  10^5 Cycles Typ.
- Access Time
  85 ns (V_{DD} = 3.0 V to 3.6 V)
  100 ns / 120 ns (V_{DD} = 2.7 V to 3.0 V)
- Power Dissipation
  250 μA (Standby TTL level)
  10 μA (Standby CMOS level)
  30 mA (Read Operating)
  40 mA (Program / Erase Operating)
- Package
  TC58FVT008FT/B008FT : TSOP I 40 - P - 1020 - 0.50
  (Weight : 0.45 g Typ.)

PIN ASSIGNMENT (TOP VIEW)



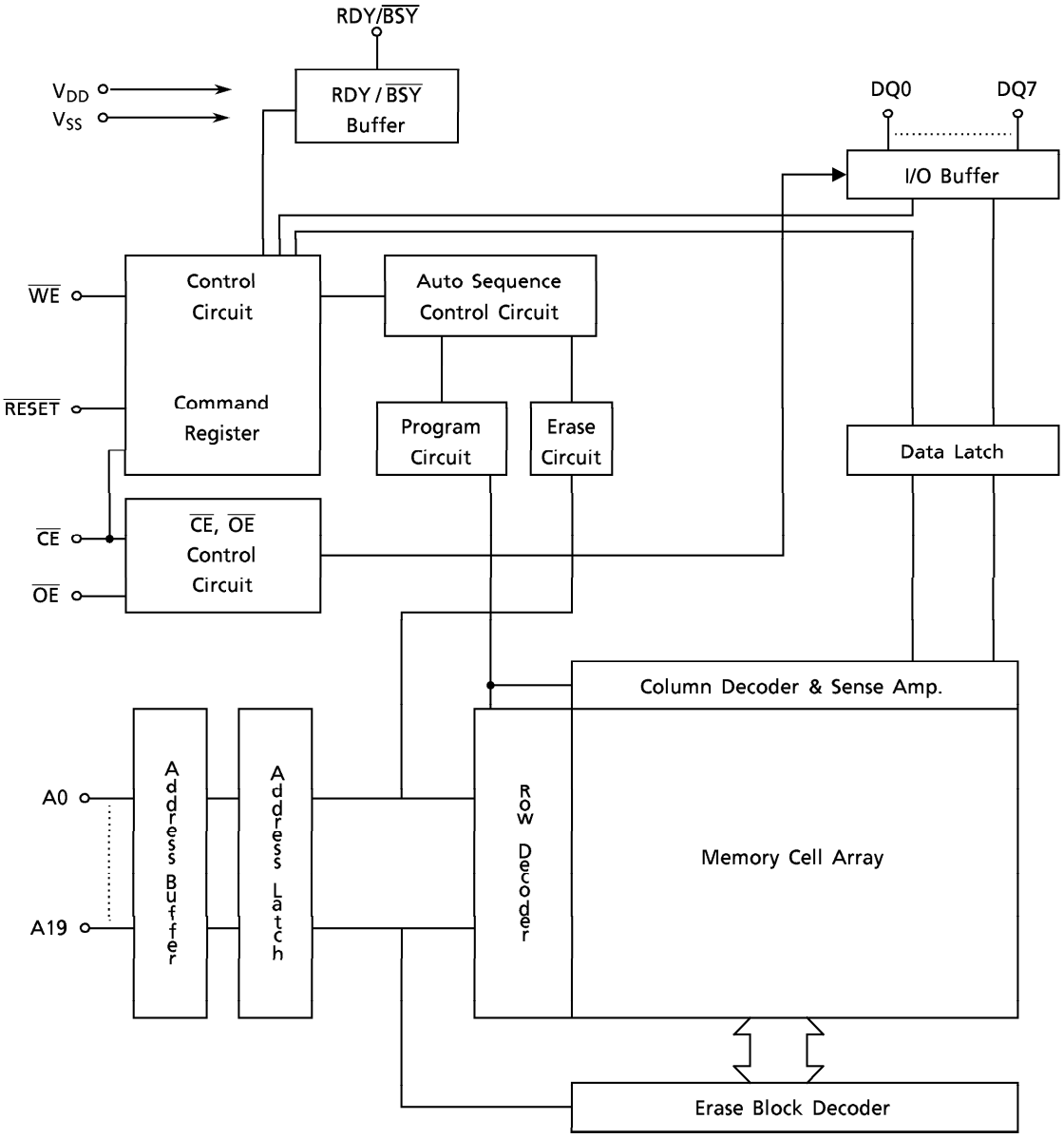
TC58FVT008FT / B008FT (TSOP Type - I)

PIN NAMES

A0 to A19	Address Input
DQ0 to DQ7	Data Input / Output
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
RDY/$\overline{BSY}$	Ready / Busy Output
$\overline{RESET}$	Hardware Reset Input
NC	No Connection
V_{DD}	Power Supply
V_{SS}	Ground

961001EBA1

BLOCK DIAGRAM



MODE SELECTION

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A9	A6	A1	A0	$\overline{RESET}$	DQ0 to DQ7
Read	L	L	H	A9	A6	A1	A0	H	Dout
ID Read (Manufacturer Code)	L	L	H	V_{ID}	L	L	L	H	Code
ID Read (Device Code)	L	L	H	V_{ID}	L	L	H	H	Code
Standby	H	*	*	*	*	*	*	H	High - Z
Output Disable	*	H	H	*	*	*	*	*	High - Z
Write	L	H	L	A9	A6	A1	A0	H	Din
Block Protect	L	V_{ID}	L	V_{ID}	L	H	L	H	*
Verify Block Protect	L	L	H	V_{ID}	L	H	L	H	Code
Temporary Block Unprotect	*	*	*	*	*	*	*	V_{ID}	*
Hardware Reset / Standby	*	*	*	*	*	*	*	L	High - Z

Notes : * : V_{IH} or V_{IL}

ID CODE TABLE

TYPE		A19 to A13	A6	A1	A0	CODE (HEX)
Manufacturer Code		*	V_{IL}	V_{IL}	V_{IL}	98h
Device Code	TC58FVT008	*	V_{IL}	V_{IL}	V_{IH}	3Eh
	TC58FVB008	*	V_{IL}	V_{IL}	V_{IH}	3Dh
Verfy Block Protect		BA 1)	V_{IL}	V_{IH}	V_{IL}	Data 2)

Notes : * : V_{IH} or V_{IL}
1) BA : Block Address
2) 01h – Protected Block
00h – Unprotected Block

COMMAND SEQUENCE

COMMAND SEQUENCE	BUS WRITE CYCLES REQ'D	FIRST BUS WRITE CYCLE		SECOND BUS WRITE CYCLE		THIRD BUS WRITE CYCLE		FOURTH BUS READ/WRITE CYCLE		FIFTH BUS WRITE CYCLE		SIXTH BUS WRITE CYCLE	
		Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read / Reset	1	XXXXh	F0h										
Read / Reset	3	5555h	AAh	2AAAh	55h	5555h	F0h	RA [1]	RD [2]				
ID Read / Verify Block Protect	3	5555h	AAh	2AAAh	55h	5555h	90h	IA [3]	ID [4]				
Auto Program	4	5555h	AAh	2AAAh	55h	5555h	A0h	PA [5]	PD [6]				
Auto Chip Erase	6	5555h	AAh	2AAAh	55h	5555h	80h	5555h	AAh	2AAAh	55h	5555h	10h
Auto Block Erase	6	5555h	AAh	2AAAh	55h	5555h	80h	5555h	AAh	2AAAh	55h	BA [7]	30h
Block Protect	6	5555h	AAh	2AAAh	55h	5555h	9Ah	5555h	AAh	2AAAh	55h	5555h	9Ah
Block Erase Suspend		Addr : V_{IH} or V_{IL}, Data : B0h											
Block Erase Resume		Addr : V_{IH} or V_{IL}, Data : 30h											

Notes :
The system should generate the following address patterns ;
5555h or 2AAAh to addresses A14 to A0.

1) RA : Read Adress
2) RD : Read Data
3) IA : ID Adderss (A6, A1, A0)
00h = Manuafcturer Code
01h = Device Code
02h = Verify Block Protect (A19 to A13 = Block Address)
4) ID : ID Data
98h – Manuafcturer Code
3Eh – Device Code (TC58FVT008)
3Dh – Device Code (TC58FVB008)
01h – Protected Block
00h – Unproteted Block
5) PA : Program Address
6) PD : Program Data
7) BA : Block Address

HARDWARE STATUS FLAGS

STATUS		DQ7	DQ6	DQ5	DQ3	RDY/$\overline{BSY}$
In Progress	Auto Programming	$\overline{DQ7}$	Toggle	0	0	0
	Auto Erase (Erase Hold Time)	0	Toggle	0	0	0
	Auto Erase	0	Toggle	0	1	0
Exeeceded Time Limits	Auto Programming	$\overline{DQ7}$	Toggle	1	1	0
	Auto Erase	0	Toggle	1	1	0

Notes : 1. DQ outputs a cell data and RDY/$\overline{BSY}$ outputs '1' when the operation has completed.
2. DQ0, DQ1, DQ2 are reserved for future use.
3. DQ0 to DQ2, DQ4 : Output '0'.

BLOCK ERASE ADDRESS TABLES

TC58FVT008 (Top Boot Block)

BLOCK#	A19	A18	A17	A16	A15	A14	A13	ADDRESS RANGE	SIZE
BA0	L	L	L	L	*	*	*	00000h - 0FFFFh	64 K byte
BA1	L	L	L	H	*	*	*	10000h - 1FFFFh	64 K byte
BA2	L	L	H	L	*	*	*	20000h - 2FFFFh	64 K byte
BA3	L	L	H	H	*	*	*	30000h - 3FFFFh	64 K byte
BA4	L	H	L	L	*	*	*	40000h - 4FFFFh	64 K byte
BA5	L	H	L	H	*	*	*	50000h - 5FFFFh	64 K byte
BA6	L	H	H	L	*	*	*	60000h - 6FFFFh	64 K byte
BA7	L	H	H	H	*	*	*	70000h - 7FFFFh	64 K byte
BA8	H	L	L	L	*	*	*	80000h - 8FFFFh	64 K byte
BA9	H	L	L	H	*	*	*	90000h - 9FFFFh	64 K byte
BA10	H	L	H	L	*	*	*	A0000h - AFFFFh	64 K byte
BA11	H	L	H	H	*	*	*	B0000h - BFFFFh	64 K byte
BA12	H	H	L	L	*	*	*	C0000h - CFFFFh	64 K byte
BA13	H	H	L	H	*	*	*	D0000h - DFFFFh	64 K byte
BA14	H	H	H	L	*	*	*	E0000h - EFFFFh	64 K byte
BA15	H	H	H	H	L	*	*	F0000h - F7FFFh	32 K byte
BA16	H	H	H	H	H	L	L	F8000h - F9FFFh	8 K byte
BA17	H	H	H	H	H	L	H	FA000h - FBFFFh	8 K byte
BA18	H	H	H	H	H	H	*	FC000h - FFFFFh	16 K byte

TC58FVB008 (Bottom Boot Block)

BLOCK#	A19	A18	A17	A16	A15	A14	A13	ADDRESS RANGE	SIZE
BA0	L	L	L	L	L	L	*	00000h - 03FFFh	16 K byte
BA1	L	L	L	L	L	H	L	04000h - 05FFFh	8 K byte
BA2	L	L	L	L	L	H	H	06000h - 07FFFh	8 K byte
BA3	L	L	L	L	H	*	*	08000h - 0FFFFh	32 K byte
BA4	L	L	L	H	*	*	*	10000h - 1FFFFh	64 K byte
BA5	L	L	H	L	*	*	*	20000h - 2FFFFh	64 K byte
BA6	L	L	H	H	*	*	*	30000h - 3FFFFh	64 K byte
BA7	L	H	L	L	*	*	*	40000h - 4FFFFh	64 K byte
BA8	L	H	L	H	*	*	*	50000h - 5FFFFh	64 K byte
BA9	L	H	H	L	*	*	*	60000h - 6FFFFh	64 K byte
BA10	L	H	H	H	*	*	*	70000h - 7FFFFh	64 K byte
BA11	H	L	L	L	*	*	*	80000h - 8FFFFh	64 K byte
BA12	H	L	L	H	*	*	*	90000h - 9FFFFh	64 K byte
BA13	H	L	H	L	*	*	*	A0000h - AFFFFh	64 K byte
BA14	H	L	H	H	*	*	*	B0000h - BFFFFh	64 K byte
BA15	H	H	L	L	*	*	*	C0000h - CFFFFh	64 K byte
BA16	H	H	L	H	*	*	*	D0000h - DFFFFh	64 K byte
BA17	H	H	H	L	*	*	*	E0000h - EFFFFh	64 K byte
BA18	H	H	H	H	*	*	*	F0000h - FFFFFh	64K byte

* : V_{IH} or V_{IL}

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RANGE	UNIT
V_{DD}	V_{DD} Supply Voltage	− 0.6 to 4.6	V
V_{IN}	Input Voltage	− 0.6 to V_{DD} + 0.5 (≦ 4.6)	V
V_{DQ}	Input / Output Voltage	− 0.6 to V_{DD} + 0.5 (≦ 4.6)	V
P_D	Power Dissipation	0.6	W
T_{SOLDER}	Soldering Temperature (10 s)	260	°C
T_{STG}	Strage Temperature	− 55 to 150	°C
T_{OPR}	Operating Temperature	− 40 to 85	°C
N_{EW}	Erase / Program Cycling Capability	100,000	Cycle
V_{IDH}	Input High Voltage 1)	13.0	V
I_{OSHORT}	Output Short Circuit Current 2)	100	mA

1) V_{IDH} supply over 10 second is not recommended. The device might be damaged.
2) Output shorted for no more than one second.
No more than one output shorted at a time.

CAPPACITANCE (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	CONDITION	TYP	MAX	UNIT
C_{IN}	Input Pin Capacitance	V_{IN} = 0 V	4	8	pF
C_{OUT}	Output Pin Capacitance	V_{OUT} = 0 V	10	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0 V	8	10	pF

This parameter is periodically sampled and is not 100% tested.

DC and OPERATING CHARACTERISTICS (Ta = − 40 to 85°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{DD}	V_{DD} Supply Voltage	2.7	3.6	V
V_{IH}	Input High Level Voltage	2.0	V_{DD} + 0.5	
V_{IL}	Input Low Level Voltage	− 0.3 1)	0.8	
V_{ID}	Voltage for ID Read and Block Protect 2)	11.4	12.6	

1) − 2 V (Pulse width of 20 ns Max.)
2) V_{IDH} supply over 10 second is not recommended. The device might be damaged.

DC CHARACTERISTICS (Ta = −40 to 85°C, V_{DD} = 2.7 to 3.6 V)

SYMBOL	PARAMETER	CONDITION	MIN.	MAX.	UNIT
I_{LI}	Input Leakage Current	0 V ≦ V_{IN} ≦ V_{DD}	–	±1	μA
I_{LO}	Output Leakage Current	0 V ≦ V_{OUT} ≦ V_{DD}	–	±1	
$V_{OH}1$	Output High Voltage (TTL)	I_{OH} = −0.4 mA	2.4	–	V
$V_{OH}2$	Output High Voltage (CMOS)	I_{OH} = −0.1 mA	V_{DD} - 0.4	–	
		I_{OH} = −2.5 mA	0.85 × V_{DD}	–	
V_{OL}	Output Low Voltage	I_{OL} = 4.0 mA	–	0.4	
$I_{DDO}1$	V_{DD} Average Read Current	V_{IN} = V_{IH} / V_{IL}, I_{OUT} = 0 mA t_{CYCLE} = t_{RC} (Min)	–	30	mA
$I_{DDO}2$	V_{DD} Average Program Current	V_{IN} = V_{IH} / V_{IL}, I_{OUT} = 0 mA	–	40	
$I_{DDO}3$	V_{DD} Average Erase Current	V_{IN} = V_{IH} / V_{IL}, I_{OUT} = 0 mA	–	40	
$I_{DDS}1$	V_{DD} Standby Current (TTL)	$\overline{CE}$ = $\overline{RESET}$ = V_{IH} or $\overline{RESET}$ = V_{IL}	–	250	μA
$I_{DDS}2$	V_{DD} Standby Current (CMOS)	$\overline{CE}$ = $\overline{RESET}$ = V_{DD} ± 0.2 V or $\overline{RESET}$ = V_{SS} ± 0.2 V	–	10	
I_{ID}	High Voltage Input Current	11.4 V ≦ V_{ID} ≦ 12.6 1)	–	200	
V_{LKO}	Low V_{DD} Lock-out Voltage	–	–	2.5	V

1) Less than 10 seconds

AC TEST CONDITIONS

PARAMETER	CONDITION
Input Pulse Level	2.4 V / 0.4 V
Input Pulse Rise and Fall Time (10% to 90%)	5 ns
Timing Measurement Reference Level (Input)	1.5 V / 1.5 V
Timing Measurement Reference Level (Output)	1.5 V / 1.5 V
Output Load	C_L (100 pF) + 1 TTL Gate

AC CHARACTERISTICS

SYMBOL	PARAMETER	–85		–10		–12		UNIT
		Ta = 0 to 70 °C		Ta = –40 to 85 °C				
		V_{DD} = 3.0 to 3.6V		V_{DD} = 2.7 to 3.6 V				
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Read Cycle Time	85	–	100	–	120	–	ns
t_{ACC}	Address Access Time	–	85	–	100	–	120	ns
t_{CE}	$\overline{CE}$ Access Time	–	85	–	100	–	120	ns
t_{OE}	$\overline{OE}$ Access Time	–	35	–	40	–	50	ns
t_{CEE}	$\overline{CE}$ to Output Low Z	0	–	0	–	0	–	ns
t_{OEE}	$\overline{OE}$ to Output Low Z	0	–	0	–	0	–	ns
t_{OEH}	$\overline{OE}$ Hold Time (Read)	0	–	0	–	0	–	ns
t_{OH}	Output Data Hold Time	0	–	0	–	0	–	ns
t_{DF1}	$\overline{CE}$ to Output High Z	–	30	–	30	–	30	ns
t_{DF2}	$\overline{OE}$ to Output High Z	–	30	–	30	–	30	ns
t_{CMD}	Command Write Cycle Time	85	–	100	–	120	–	ns
t_{AS}	Address Setup Time	0	–	0	–	0	–	ns
t_{AH}	Address Hold Time	45	–	50	–	50	–	ns
t_{DS}	Data Setup Time	45	–	50	–	60	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	ns
t_{WELH}	$\overline{WE}$ Low Level Hold Time *	45	–	50	–	50	–	ns
t_{WEHH}	$\overline{WE}$ High Level Hold Time *	20	–	20	–	20	–	ns
t_{CES}	$\overline{CE}$ Setup Time to $\overline{WE}$ Active *	0	–	0	–	0	–	ns
t_{CEH}	$\overline{CE}$ Hold Time from $\overline{WE}$ High Level *	0	–	0	–	0	–	ns
t_{OES}	$\overline{OE}$ Setup to $\overline{WE}$ Active	0	–	0	–	0	–	ns
t_{OEHP}	$\overline{OE}$ Hold Time (Toggle / Data Polling)	10	–	10	–	10	–	ns
t_{OEHT}	$\overline{OE}$ High Level Hold Time (Toggle)	20	–	20	–	20	–	ns
t_{PPW}	Auto Program Time	16 **	–	16 **	–	16 **	–	μs
t_{PCEW}	Auto Chip Erase Time	15 **	–	15 **	–	15 **	–	s
t_{PBEW}	Auto Block Erase Time	1.5 **	–	1.5 **	–	1.5 **	–	s
t_{VDS}	V_{DD} Setup Time	500	–	500	–	500	–	μs
t_{BUSY}	Program / Erase Valid to RDY / $\overline{BSY}$ Delay	35	–	40	–	50	–	ns
t_{RP}	$\overline{RESET}$ Low Level Hold Time	500	–	500	–	500	–	ns
t_{READY}	$\overline{RESET}$ Low Level to Read Mode	–	20	–	20	–	20	μs
t_{RB}	RDY / $\overline{BSY}$ Recovery Time	0	–	0	–	0	–	ns
t_{RH}	$\overline{RESET}$ Recovery Time	500	–	500	–	500	–	ns
t_{VPT}	V_{ID} Transition Time	4	–	4	–	4	–	μs
t_{VPS}	V_{ID} Setup Time	4	–	4	–	4	–	μs
t_{VPH}	$\overline{OE}$ Hold Time (Block Protect)	8	–	8	–	8	–	μs
t_{PPLH}	$\overline{WE}$ Low Level Hold Time (Block Protect)	100	–	100	–	100	–	μs
t_{PAS}	Protect Address Setup Time	0	–	0	–	0	–	ns
t_{PAH}	Protect Address Hold Time	0	–	0	–	0	–	ns
t_{CESP}	$\overline{CE}$ Setup Time (Block Protect)	4	–	4	–	4	–	μs
t_{CEHP}	$\overline{CE}$ Hold Time (Block Protect)	8	–	8	–	8	–	μs

* : $\overline{WE}$ Control ** : Typ.

OPERATING MODE

Read Mode

When the device is set to the Read Mode, it acts as an asynchronous ROM with an access time of 85 / 100 / 120 ns. The device is set to the Read Mode after power - on or Auto - Program / Erase completed. Either software or hardware reset needs to be input to return to the Read Mode when Auto - Program / Erase operation fails.

Standby Mode

The TC58FVT008/B008 has a low power Standby Mode controlled by either $\overline{CE}$ or $\overline{RESET}$ pin. The Standby current is less than 10 μA at CMOS voltage levels ($\overline{CE}$ = $\overline{RESET}$ = $V_{DD} \pm 0.2$ V or $\overline{RESET}$ = $V_{SS} \pm 0.2$ V) or 250 μA at TTL levels ($\overline{CE}$ = $\overline{RESET}$ = V_{IH} or $\overline{RESET}$ = V_{IL}). The $\overline{RESET}$ controls not only the power but all command mode such as Auto - Program / Erase, ID - Read, etc., beside the $\overline{CE}$ controls the power. The I/O pins are in high impedance at Standby Mode.

Command Write

The TC58FVT008/B008 utilizes the JEDEC command control standrized for single power supply E^{2}PROM. The Command is executed by inputting address and data into the command register. The Command is entered by $\overline{WE}$ control write ($\overline{WE}$ pulse at $\overline{CE}$ = V_{IL} and $\overline{OE}$ = V_{IH}) or $\overline{CE}$ control write ($\overline{CE}$ pulse at $\overline{WE}$ = V_{IL} and $\overline{OE}$ = V_{IH}). The Address is latched at falling edge of either $\overline{WE}$ or $\overline{CE}$. The Data is latched at rising edge of either $\overline{WE}$ or $\overline{CE}$.

The Command is reset by inputting the Reset Command and then the device goes into the Read Mode. When the undefined command is input, the Command Register is reset and the device goes into the Read Mode.

RESET (Software Reset)

The device does not go into the read mode automatically when the command mode such as Auto-Program / Erase and ID - Read Operations are not correctly executed (for example; Program fail, Erase fail). The Reset or Read Command is needed for returning to the Read Mode. The Reset and Read Command are also needed for resetting the Command Register.

RESET (Hardware Reset)

The hardware reset is used for aborting the auto mode operation such as Auto-Program/Erase and for resetting the Operation Mode. The device goes into the Read Mode at 20 μs after inputting 500 ns low level pulse to $\overline{RESET}$ pin. The data might be corrupted when the device is reset during the auto mode operation.

The device goes into the Read Mode at $\overline{RESET}$ = V_{IH} or the Standby Mode at $\overline{RESET}$ = V_{IL} after the hardware reset. The I/O pins are in high impedance state at $\overline{RESET}$ = V_{IL}. The Read Operation and the Command Input are allowed after the device goes into the Read Mode.

ID - Read Mode

The ID Read Mode is utilized to identify the device type. The ID Read Mode is set by either the command mode by inputting "90h" command or the EPROM mode by applying V_{ID} to the A9 pin.

The data at address A0 / A1 / A6 = V_{IL} is the manufacturer code (98h) while the data at address A0 = V_{IH}, A1 / A6 = V_{IL} is the device code (TC58FVT008 = 3Eh / TC58FVB008 = 3Dh). The access time of an ID read is the same as normal read operation.

Auto Program Mode

The TC58FVT008/B008 can be programmed by byte unit. The Auto Program Mode is set by entering the Program Command. The program address is latched at the falling edge of the $\overline{WE}$ signal and the data is latched at the rising edge in the fourth bus cycle. The auto programming starts at the rising edge of the $\overline{WE}$ signal in the forth bus cycle. The Program and Program Verify is automatically excuted by he chip. The device status in programming is determined by the hardware sequence flag.

The programming to the protected block is ignored. The device goes to the read mode 3 μs after rising edge of the $\overline{WE}$ signal in the fouth bus cycle when the auto program is addressed to the protected block.

The device allows the programming of "0" data into "1" memory cells. The programming of "1" data into "0" cell will fail. Erasure is necessary to turn "0" cell to "1" cell.

If the Auto Program Operation fails, the device keeps the programming state and does not return to the Read Mode. This device status is determined by the hardware sequence flag. Either Reset Command or hardware reset is necessary to turn the device into the Read Mode when fail.

Auto Chip Erase Mode

The Auto Chip Erase mode is set by entering the Chip Erase Command. The Auto Chip Erase operation starts at the rising edge of the $\overline{WE}$ in the sixth bus cycle. All memory cells are automatically preprogrammed to "0", erased and verified for erasure by the chip. This device status is determined by the hardware sequence flag.

The command input is ignored during an Auto Chip Erase. The hardware reset enables to interrupt the Auto Chip Erase Operation. The Auto Chip Erase Operation is not correctly completed when interrupted, therefore, the re - erase operation is necessary to erase.

The erasing to the protected block is ignored. If all blocks are protected, the Auto Erase Operation is not excuted and the device turns to the Read Mode 100 μs after rising edge of the $\overline{WE}$ signal in the sixth bus cycle.

If the Auto Chip Erase Operation fails, the device keeps the erasing state and does not return to the Read Mode. This device status is determined by the hardware sequence flag. Either reset command or hardware reset is necessary to turn the device into the Read Mode when fail.

Auto Block / Multi Block Erase Mode

The Auto Block / Multi Block Erase Mode are set by entering the Block Erase Command. The Block Address is latched at the falling edge of the $\overline{WE}$ signal in the sixth bus cycle. The block erase starts at the hold time from the rising edge of the $\overline{WE}$ signal. All memory cells in the selected block are automatically preprogrammed to "0", erased and verified for erasure by the chip. The Multi Block Erase Operation enables to erase the multiple blocks. Additional block addresses and the Multi Block Erase Command must be input during the erase hold time of 50 μs after each rising edge of the $\overline{WE}$ signal. The device status is determined by the hardware sequence flag.

Commands (except erase suspend) are ignored during the Block/Multi Block Erase Operation. The operation is aborted by the hardware reset. The Auto Erase Operation is not correctly completed when aborted, therefore, the re - erase operation is necessary to erase.

The erasing to the protected block is ignored. If all blocks of selected block are protected, the Auto Erase Operation is not excuted and the device turns to the Read Mode 100 μs after rising edge of the $\overline{WE}$ signal in the last bus cycle.

If the Auto Erase Operation fails, the device keeps the erasing state and does not return to the Read Mode. This device status is determined by the hardware sequence flag. Either reset command or hardware reset is necessary to turn the device into the Read Mode when fail.

Erase Suspend / Resume Mode

The Erase Suspend mode is used to read a data from the block not selected for erasure. The Erase Suspend command is allowed during block erase operation or block erase hold time; it is ignored for other operation modes. The Block Erase Operation is also suspended if the suspend command is input during the Block Erase Hold Time. The device is reset if any other commands than suspend are input. The suspended device allows only read or Resume Command.

The device goes to the suspend mode 15 μs after the Erase Suspend Command is input and the device goes to a Pseudo Read Mode. The data can be read out from an unselected block but the data is invalid if the address is set to a selected block for erasure. The device status can be determined by the hardware sequence flag. DQ6 (Toggle bit) stops toggling and RDY/$\overline{BSY}$ outputs "1" once the device is set the Pseudo Read Mode. The host processor must track the current device mode since there is no identification whether the device is in Pseudo or Normal Read Mode. The Pseudo Read Status is held when the Suspend Command is input during Suspend.

The device restarts the Block Erase Operation after receiving a Resume Command. The device returns to the status of which a suspend command is input. DQ6 outputs the toggle signal and RDY/$\overline{BSY}$ outputs "0".

Block Protect

The TC58FVT008/B008 has a block Protection feature to prevent program and erasure for protected block. Block protection is enabled by either hardware protection (1) or software command mode (2). The initial device is shipped unprotected.

(1) A block protected when ; A9 = $\overline{OE}$ = V_{ID}, $\overline{CE}$ = V_{IL}, A0 / A6 = V_{IL}, A1 = V_{IH} and the block address set using A13 to A19. The Block Protect Data is programmed during the t_{PPLH} of $\overline{WE}$ signal.

(2) A block can also be protected by using software command. The block protection is excuted by inputting the $\overline{WE}$ pulse of t_{PPLH} at $\overline{CE}$ = V_{IL}, A13 to A19 = Block Address after command input in the sixth bus cycle. Block protection is verified by the Verify Block Protect.

Temporary Block Protect

The TC58FVT008/B008 has a Temporary Block Unprotect feature which disables block protection for all protected blocks. The unprotection is enabled by applying V_{ID} to the $\overline{RESET}$ pin. The device can be programmed or erased for any block under this condition. The device returns to the previous condition after V_{ID} removed from the $\overline{RESET}$ pin. That is, previously protected blocks are protected again.

Verify Block Protect

The Verify Block Protect is used to verify either block protected or unprotected. Verify Block Protect is enabled either through hardware (1) or software command (2). The data outputs '01h' when protected and "00h" when unprotected.

(1) A Verify Block Protection is enabled when ; A9 = V_{ID}, A0 / A6 = V_{IL}, A1 = V_{IH}, A13 to A19 = Block Address.

(2) A Verify Block Protection can also be enabled by using software command.

HARDWARE SEQUENCE FLAG

The TC58FVT008/B008 has a Hardware Sequence flag to determine the device status during auto operation. The output data is read out with the same timing as Read Mode at $\overline{CE}$ = $\overline{OE}$ = V_{IL}. RDY/$\overline{BSY}$ outputs either high or low level.

The device turns to the Read Mode automatically after auto operation has finished successfully. The device status is read out by hardware sequence flag and the operation result is verified by comparing a read-out data to an original data.

DQ7 ($\overline{DATA}$ Polling)

The device status can be determined by the data polling function during auto program or auto erase operation. $\overline{DATA}$ Polling begins from the rising edge of $\overline{WE}$ in the last bus cycle. In auto program operation, the DQ7 outputs an inverted data during the programming operation and outputs a true data after programming has finished. In auto erase operation, the DQ7 outputs "0" during the erasing operation and outputs "1" when the erase operation has finished. DQ7 outputs the same result as a data during auto operation if the operation has failed.

The latched address is reset after an operation has finished. The polling data is asynchronous with the $\overline{OE}$ signal.

DQ6 (Toggle Bit)

The device status can be determined by the Toggle Bit function during Auto Program or Auto Erase Operation. Toggle Bit begins from the rising edge of $\overline{WE}$ in the last bus cycle in Program operation and begins at Erase Hold Time after the rising edge of $\overline{WE}$ in the last bus cycle. DQ6 outputs an alternating "0" and "1" for each attempt ($\overline{OE}$ access) at $\overline{CE}$ = V_{IL} while the device is busy. When the internal operation is completed, toggling stops and valid memory cell data can be read on subsequent read. DQ6 outputs a toggling data if the operation has failed.

DQ6 toggles for around 3 μs when the Auto Program Operation is addressed to the protected block and then stops toggling. DQ6 toggles for around 100 μs when the Auto Erase Operation is addressed to the protected block and then stops toggling. After toggling stops, the device turns into the Read Mode.

DQ5 (Internal Time Out)

DQ5 outputs "1" when the Internal Timer has timed out during Program or Erase Operation. This indicates that the Operation has not completed within the allotted time.

The programming of "1" data into "0" cell will fail (See Auto Program Mode). DQ5 outputs "1" in this case. Either hardware reset or software reset command is necessary to turn the device into the Read Mode.

DQ3 (Block Erase Timer)

The Block Erase operation starts 50 μs (Erase Hold Time) after the rising edge of $\overline{WE}$ in the last command cycle. DQ3 outputs "0" during the Block Erase Hold Time and "1" when the Erase Operation starts. Additional Block Erase Command can only be accepted during this Block Erase Hold Time. Each Block Erase Command given within this Hold Time resets the timer so that additional blocks can be marked for erasure. DQ3 outputs "1" if the device fails in Program or Erase Operation.

RDY/$\overline{BSY}$ (READY/$\overline{BUSY}$)

TC58FVT008/B008 has a RDY/$\overline{BSY}$ signal to indicate the device status to the host processor. A "0" (busy state) indicates that Auto Program or Auto Erase Operation is in progress. A "1" (ready state) indicates that the operation has finished and the device can accept a new command. RDY/$\overline{BSY}$ outputs "0" when the operation has failed.

RDY/$\overline{BSY}$ outputs "0" data after the rising edge of $\overline{WE}$ in the last command cycle in Program Operation or in the Erase Hold Time after the last command cycle in Erase Operation.

During Auto Block Erase Operation, commands other than Erase Suspend will be ignored. RDY/$\overline{BSY}$ outputs "1" during Erase Suspend. The output buffer of the RDY/$\overline{BSY}$ pin is an open drain type circuit enabling a wired - or connection. A pullup resistor needs to be tied between V_{DD} and the RDY/$\overline{BSY}$ pin.

DATA PROTECTION

The TC58FVT008/B008 utilizes a JEDEC standard command sequence which protects data against inadvertent operation due to noise.

Vcc Lock Out Voltage

The device is reset when V_{DD} is less than V_{LKO} to protect memory cell data against V_{DD} noise or during power up and down. The Auto Program or Erase Operation stops when V_{DD} goes down below V_{LKO}. The Erase Suspend is reset and the Erase Operation stops when the device is in Suspend mode. The Operation will not be correctly finished when interrupted by V_{DD} Lock Out.

$\overline{WE}$ Glitch Pulse

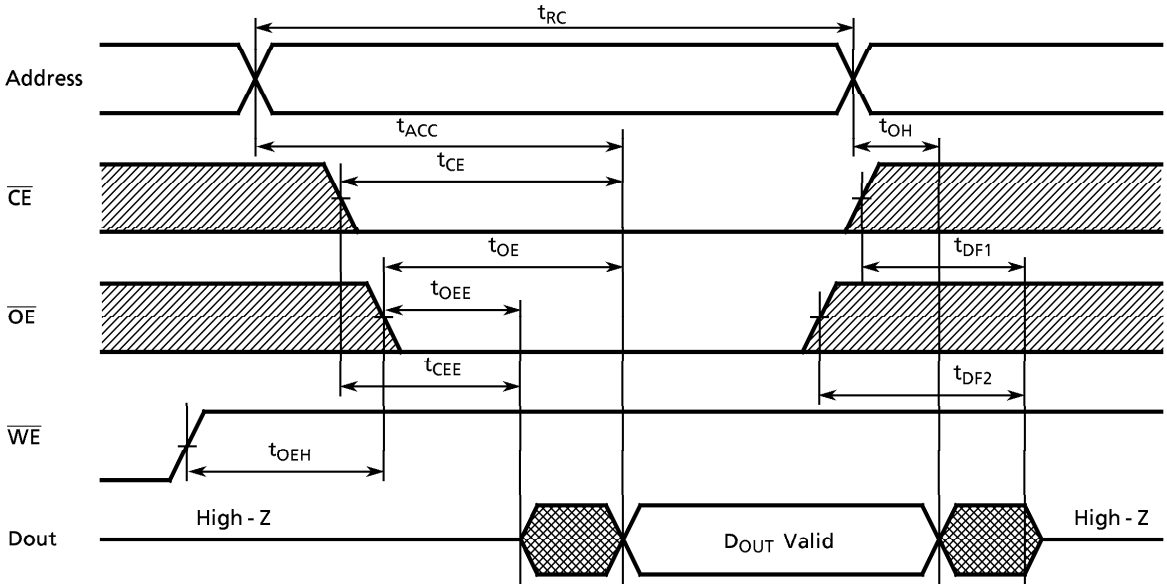
Glitches must be suppressed (less than 5 ns) for proper operation.

Protection for Power On

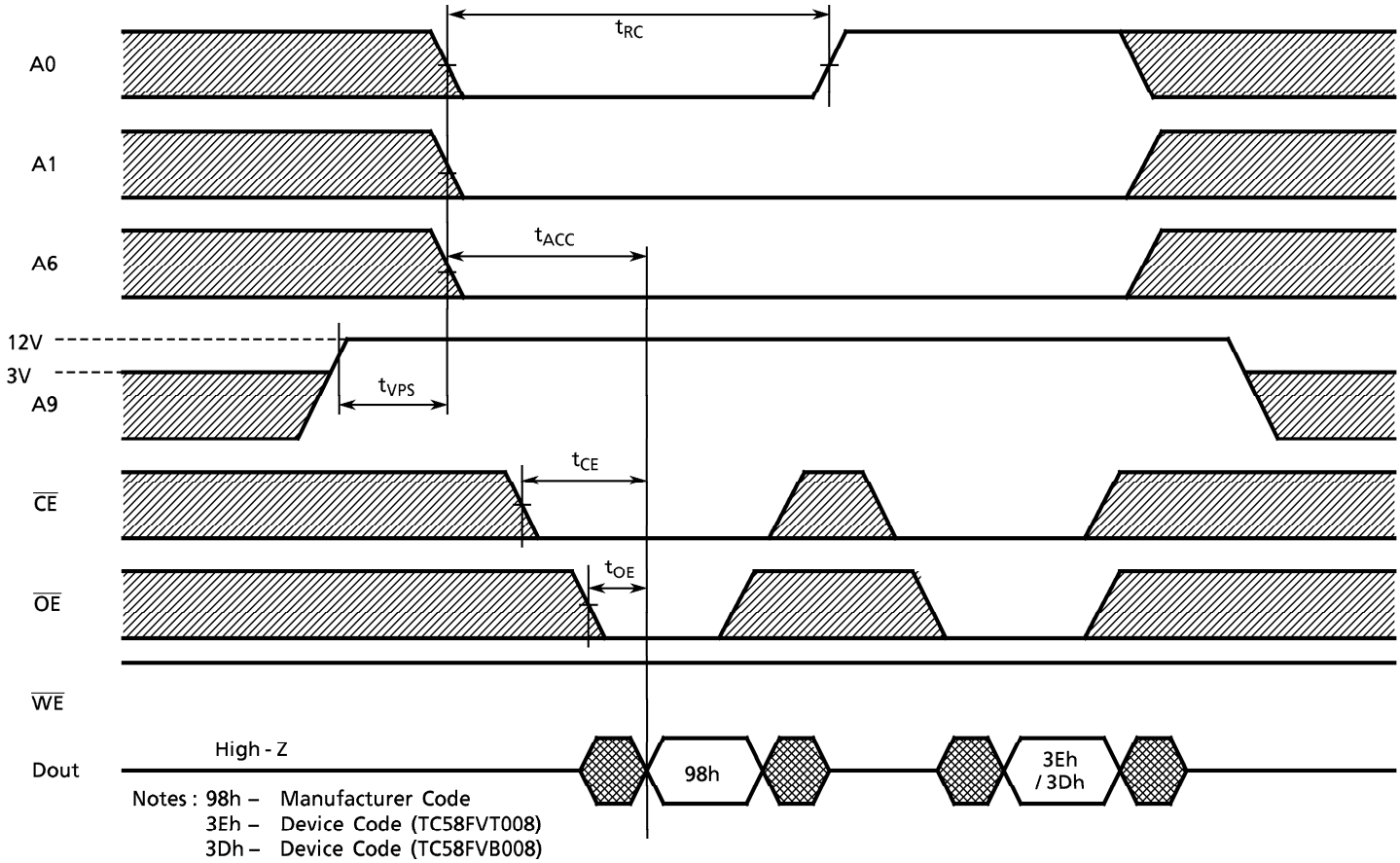
The device is reset and goes into the Read Mode after power on. A command is not accepted at the rising edge of $\overline{WE}$ if V_{DD} rises from 0 V to the operating voltage under the condition of $\overline{CE} = \overline{WE} = V_{IL}$, $\overline{OE} = V_{IH}$.

TIMING DIAGRAM

Read / ID Read Operation

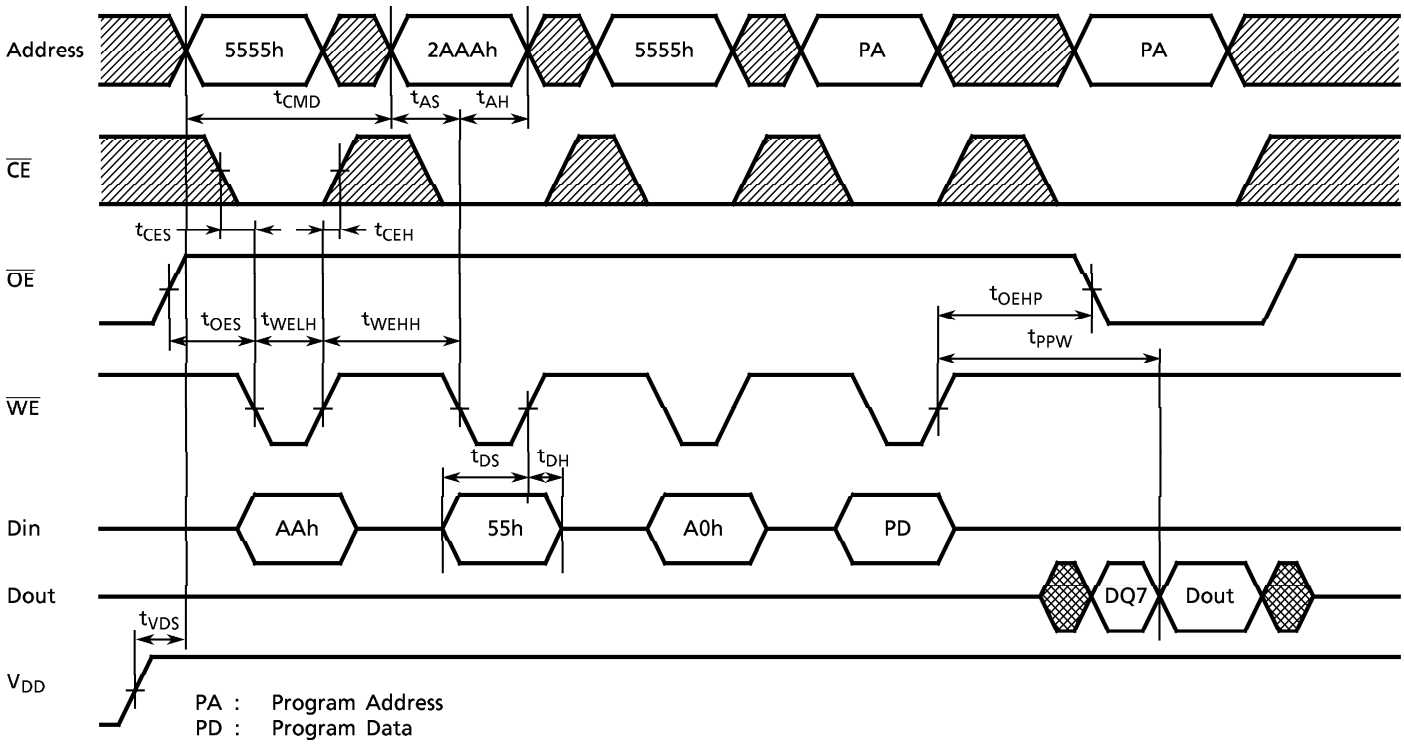


ID Read Operation (Hardware)



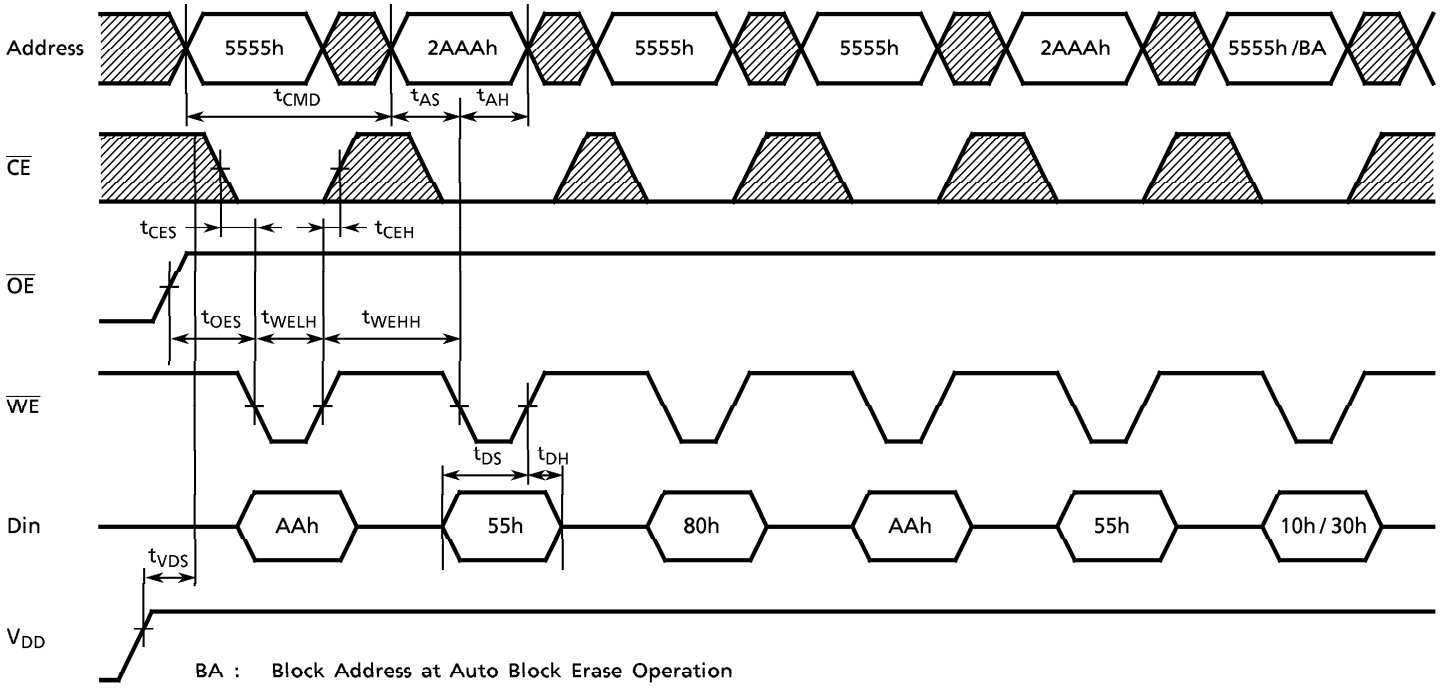
Notes : 98h – Manufacturer Code
3Eh – Device Code (TC58FVT008)
3Dh – Device Code (TC58FVB008)

Auto Program Operation ($\overline{WE}$ Contorl)



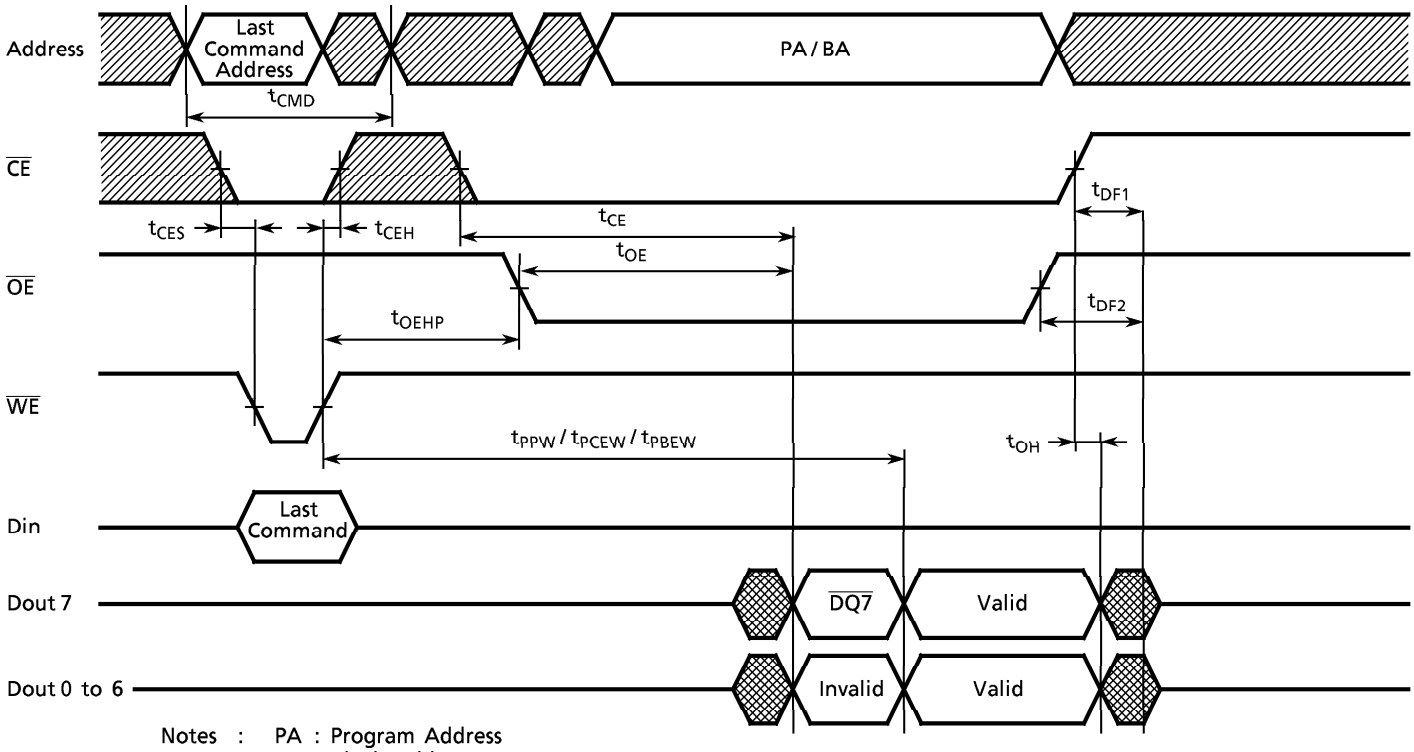
PA : Program Address
PD : Program Data

Auto Chip Erase / Auto Block Erase Operation ($\overline{WE}$ Control)



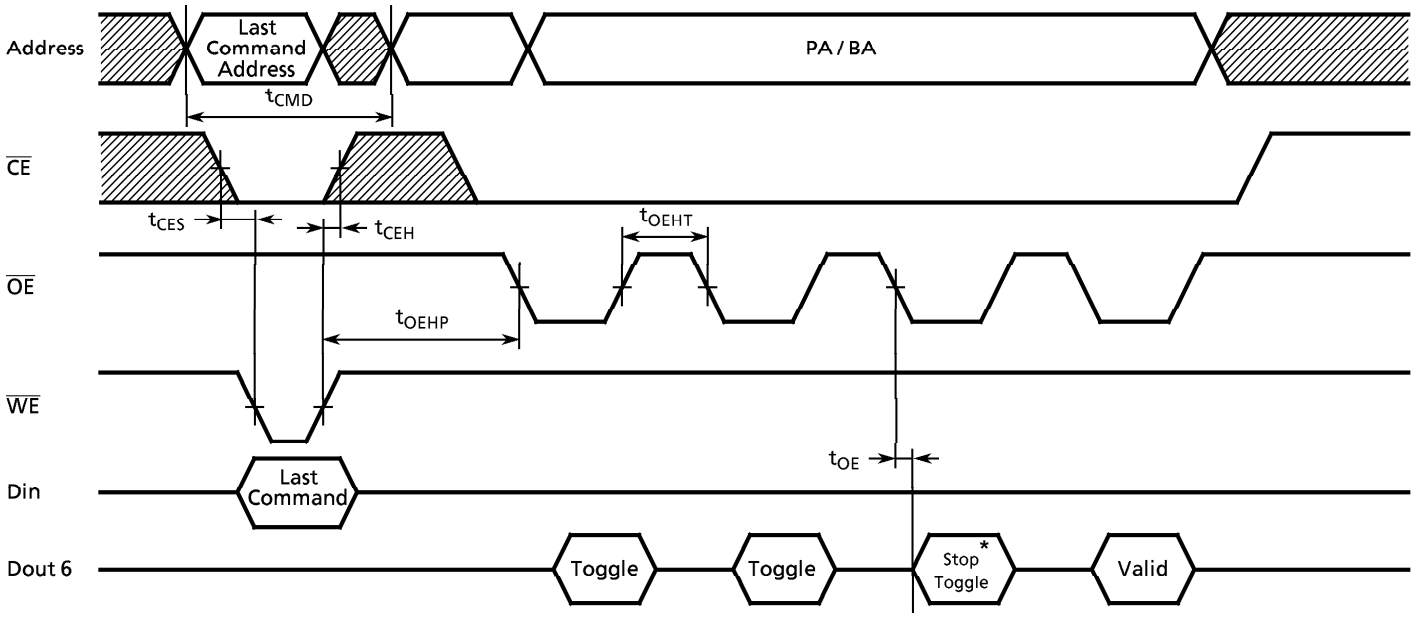
BA : Block Address at Auto Block Erase Operation

$\overline{\text{DATA}}$ Polling during Program / Erase Opeation



Notes : PA : Program Address
BA : Block Address

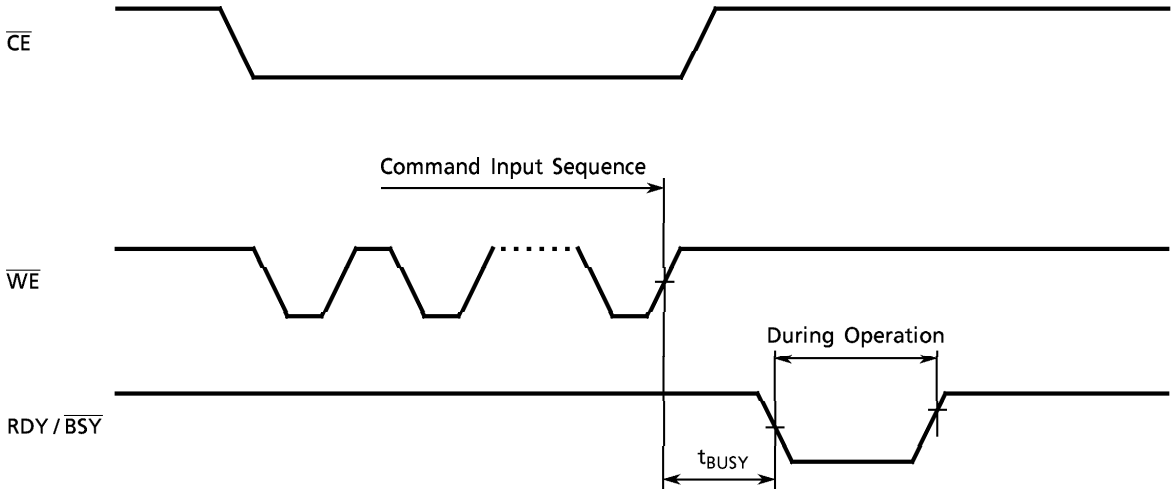
Toggle Bit during Program / Erase Operation



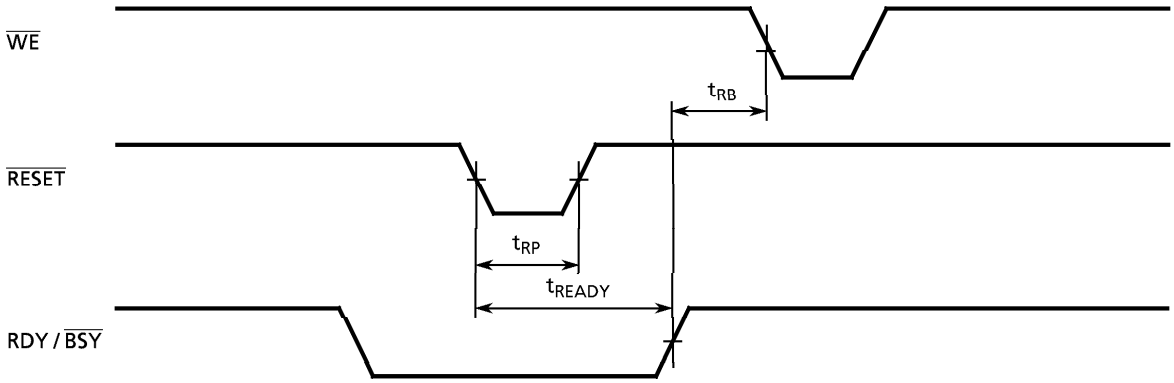
* Dout 6 stops toggling when the last command has completed.

Notes : PA : Program Address
BA : Block Address

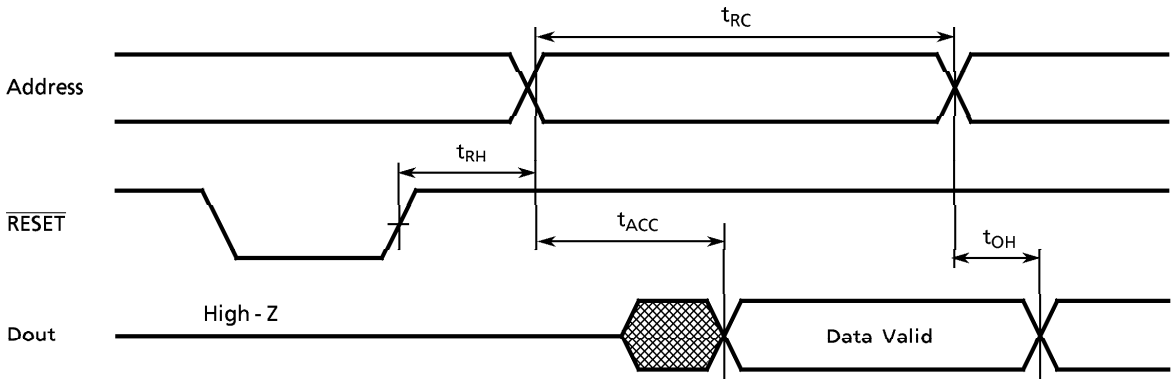
RDY / $\overline{BSY}$ during Auto Program / Erase Operation



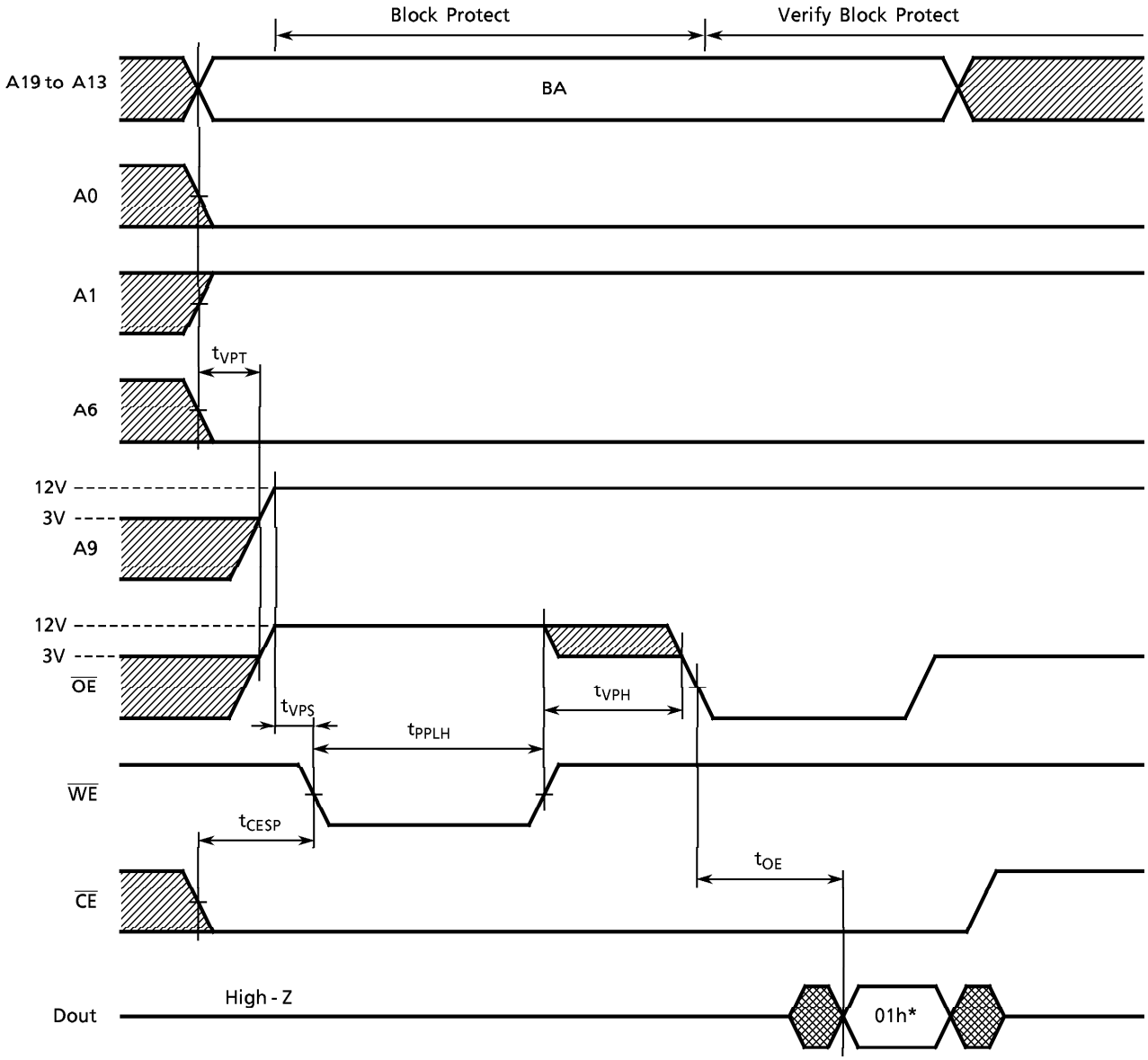
Hardware Reset Operation



Read after $\overline{RESET}$



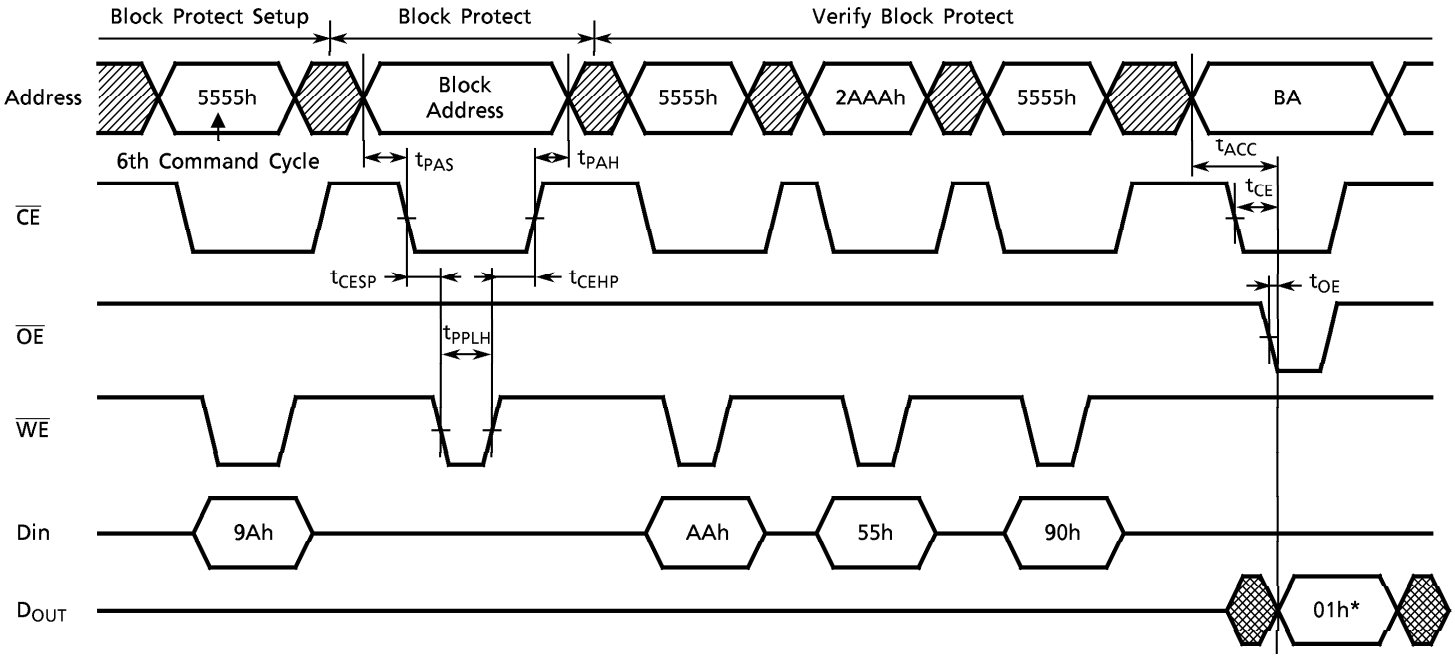
Block Protect Operation (Hardware)



BA : Block Address

* : 01h indicates that block is protected.

Block Protect (Software)

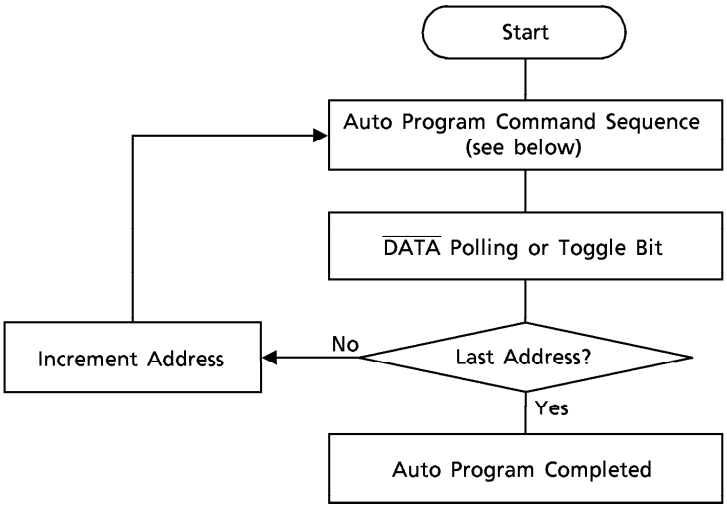


BA : Block Address

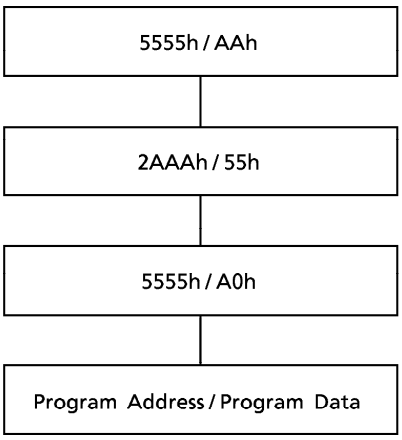
* : 01h indicates that block is protected.

FLOW CHART

Auto Program

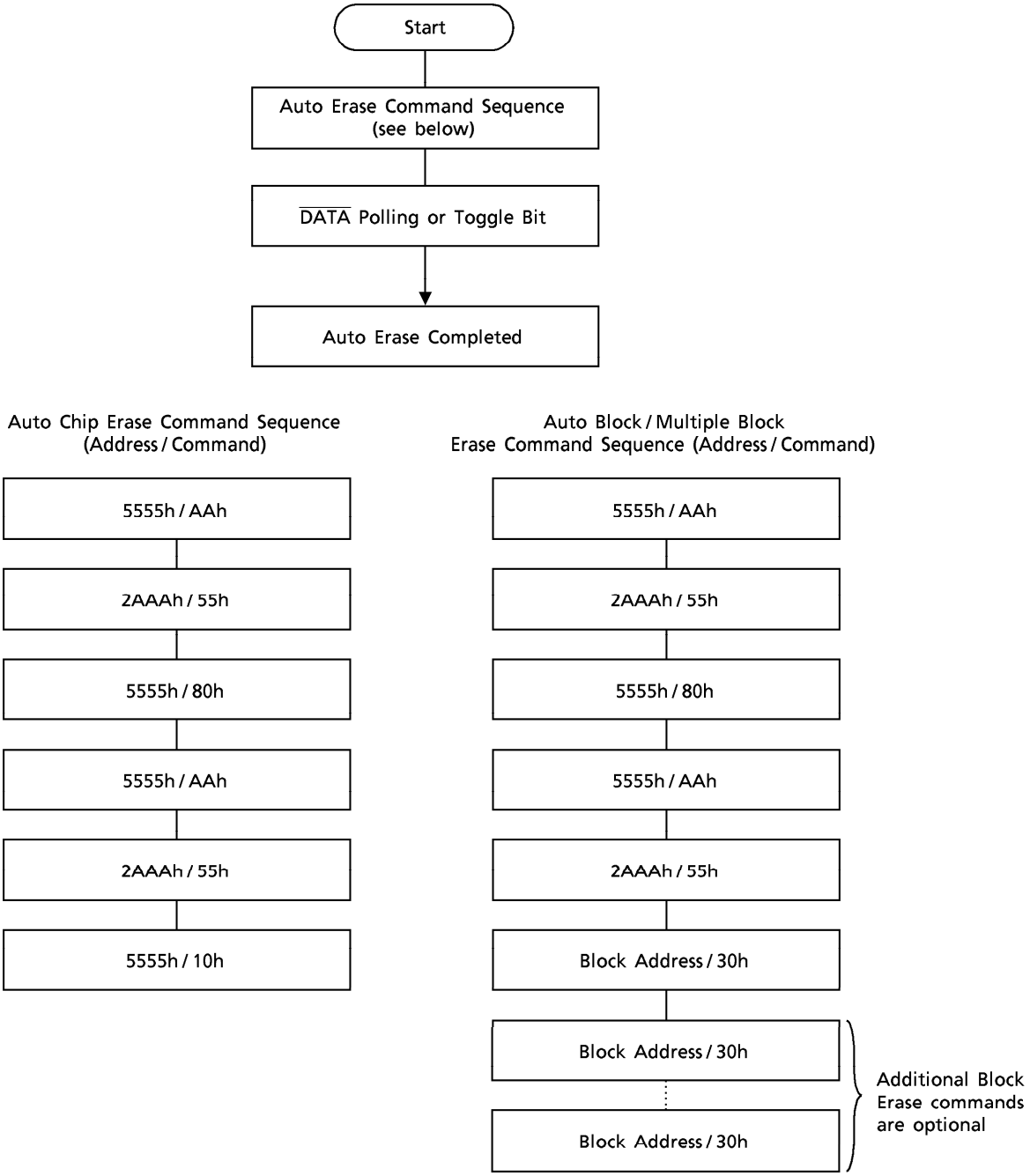


Auto Program Command Sequence (Address / Command)



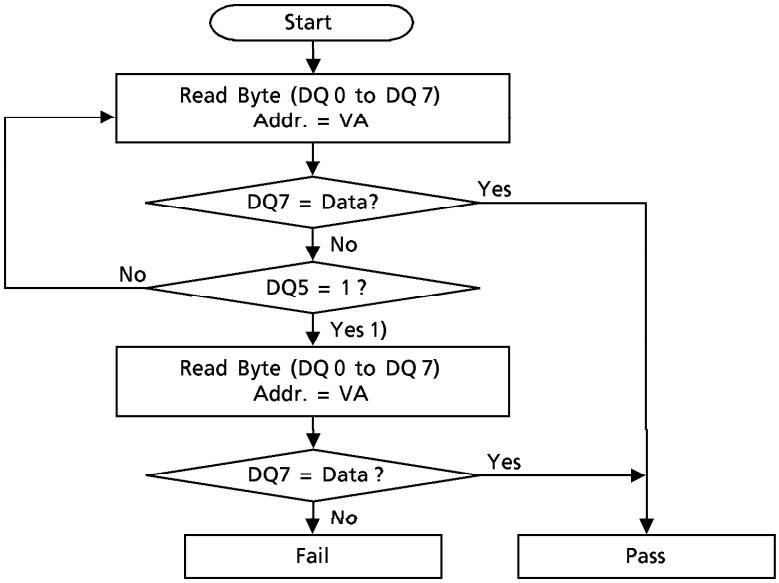
Note : Word mode command sequence is shown.

Auto Erase



Note : Word mode command sequence is shown.

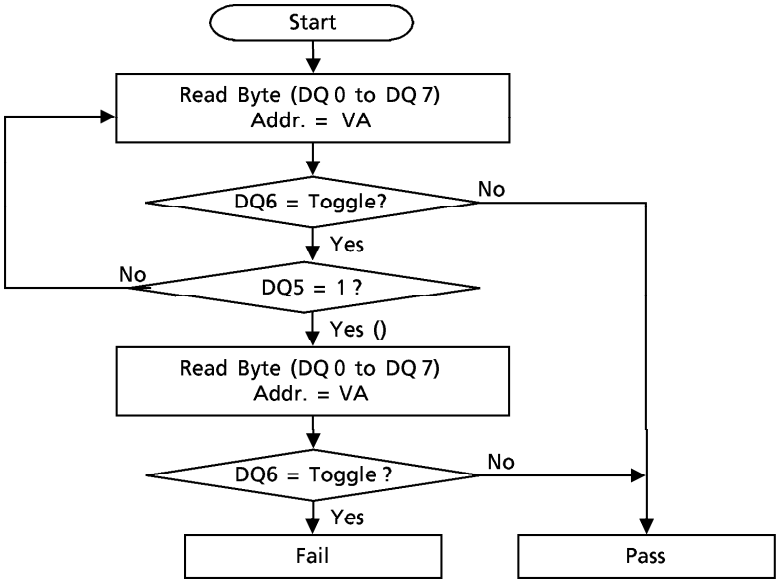
DQ 7 $\overline{\text{DATA}}$ Polling



VA : Byte address for programming.
Any of the addresses within the block being erased during a block erase operation.
Don't care during chip erase.

Note : 1) DQ7 must be rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5.

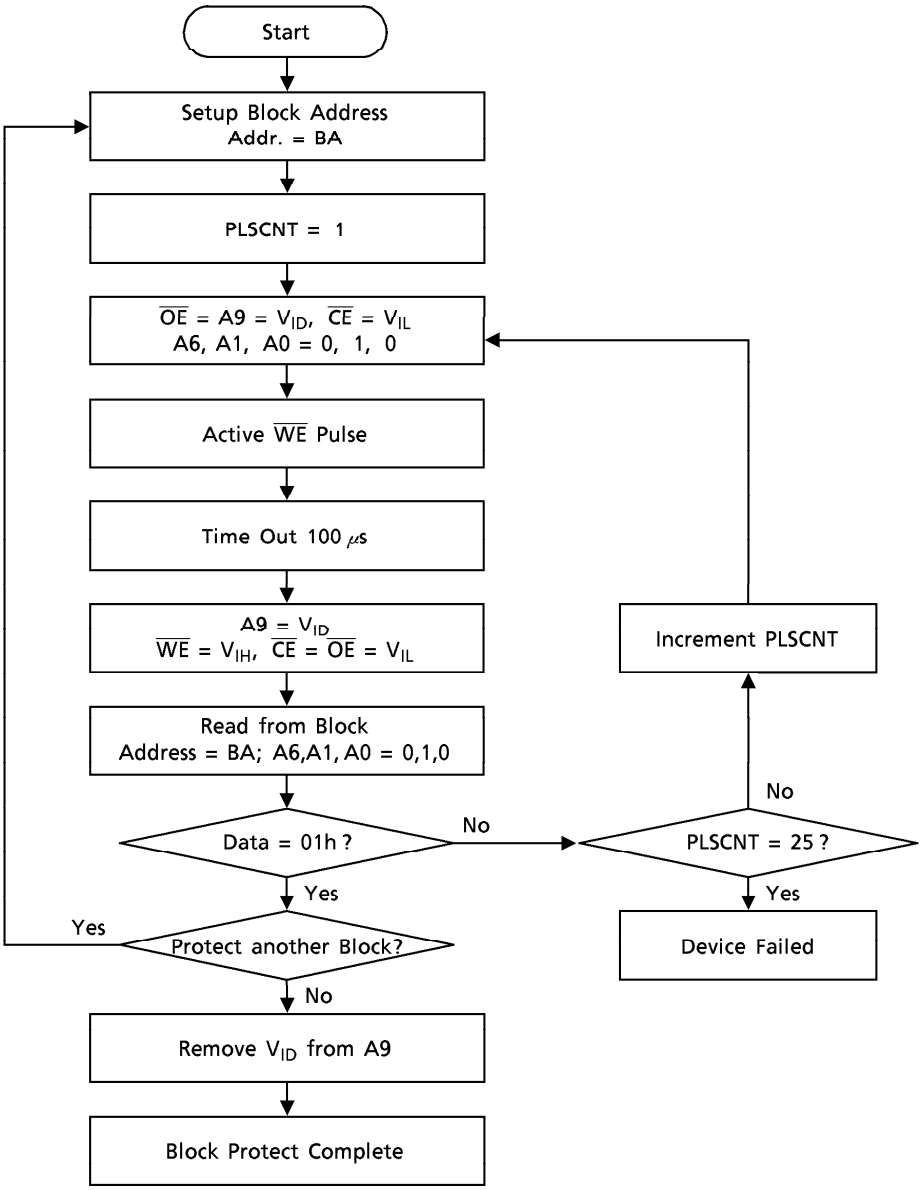
DQ 6 Toggle Bit



VA : Byte address for programming.
Any of the addresses within the block being erased during a block erase operation.
Don't care during chip erase.
Any address not within the block in the process of an Erase Suspend operation.

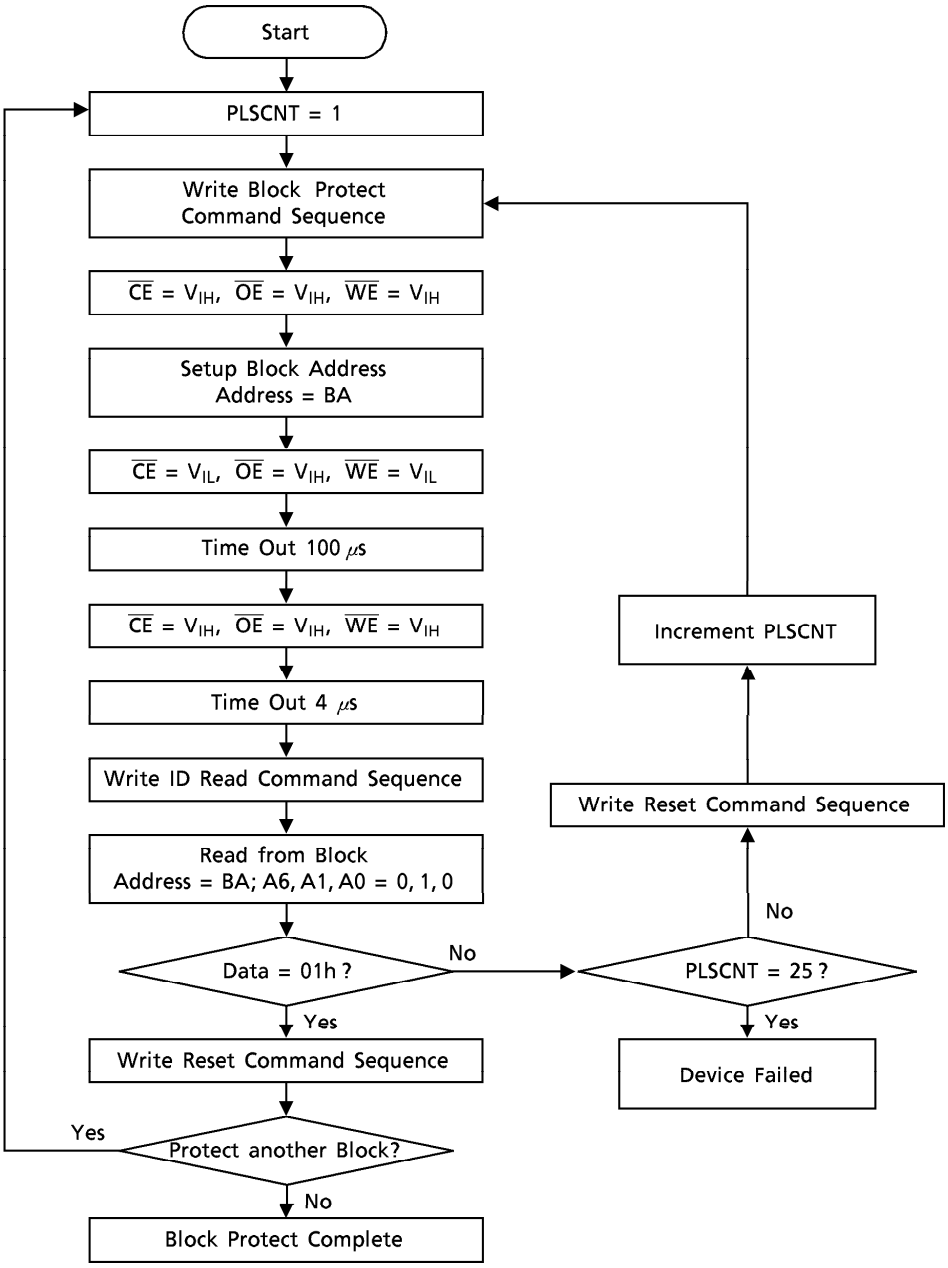
Note : 1) DQ 6 must be rechecked even if DQ 5 = "1" because DQ 6 may stop toggling at the same time that DQ 5 changes to "1".

Block Protect (Hardware)



BA : Block Address

Block Protect (Software)



BA : Block Address

PACKAGE DIMENSIONS

- Plastic TSOP

  TSOP I 40 – P – 1020 – 0.50

単位 : mm