TTIA0110G 10 Gbits/s Transimpedance Amplifier

Features

- 10 GHz bandwidth
- 1 kΩ transimpedance (single-ended)
- Complementary 50 Ω outputs can be ac or dc coupled
- Equivalent input noise current 1.5 μArms
- Group delay ±15 ps
- dc output offset control
- Single –5.2 V power supply
- Power dissipation 0.8 W
- Die size: 1.600 mm x 1.225 mm
- Low pulse-width distortion
- Maximum input current 1.25 mA average

Applications

- SONET/SDH OC-192/STM-64 receivers
- SONET/SDH OC-192/STM-64 test equipment
- Digital video transmission

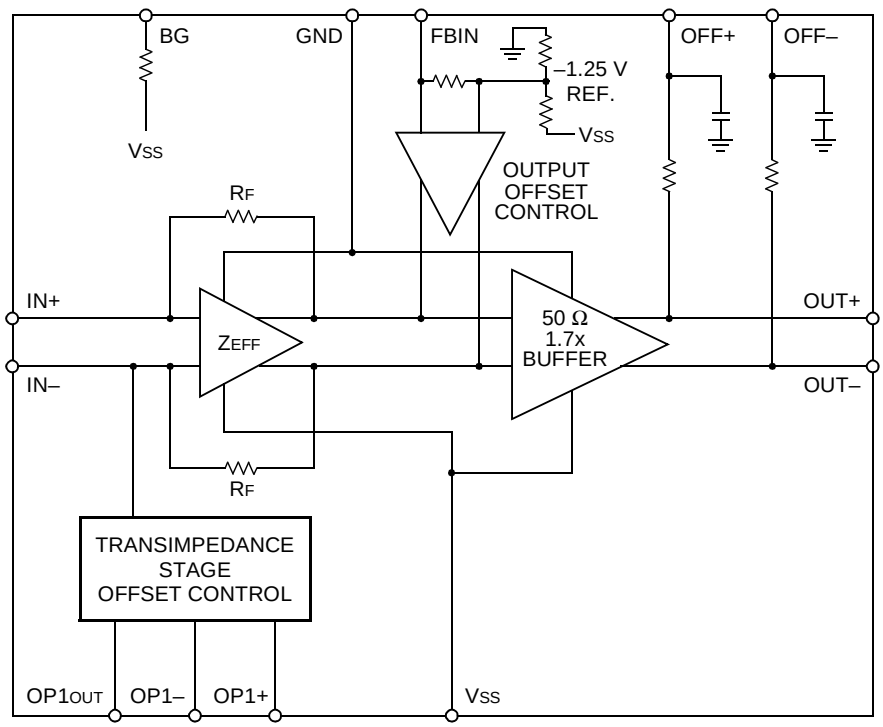

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Figure 1. Functional Block Diagram

Functional Description

The Agere Systems Inc. TTIA0110G is a high-speed, wide dynamic range transimpedance amplifier. A typical application is a low-noise, high-speed lightwave receiver when combined with an APD or PIN photodetector. The targeted transmission system is OC-192/STM-64.

The amplifier consists of a differential transimpedance stage followed by an output buffer which provides complementary 50 Ω outputs. A wide dynamic range of linear operation is achieved by combining a low-noise input stage with an output buffer capable of providing a single-ended output swing of 800 mVp-p. Large output swings provide linear operation up to 360 µA average input current. The offset between the two outputs is user adjustable and is controlled by the dc voltage at the FBIN pin.

The TTIA0110G contains two offset control circuits. The transimpedance stage offset control removes the average current from the input. This causes the average voltage of the differential outputs of the transimpedance stage to be equal. A second offset control immediately following the transimpedance stage is available to the user. A single pin, FBIN, allows the user to apply a voltage to produce an offset between the two outputs of the TIA. FBIN nominally operates at around –1.25 V, has an input impedance of 10 kΩ, and has an inverting gain of 2 to the positive data output, OUT+, when the outputs are dc-coupled to 50 Ω loads. When the outputs are ac-coupled, there is an inverting gain of 4 from FBIN to OUT+. Differential gains are twice these values. Two 10 kΩ resistors are provided on the die to sense the average voltage of the two data outputs. One resistor is connected between OFF+ and OUT+, and the other is connected between OFF– and OUT–. An external op amp can be used to close the loop between the sensing points, OFF+ and OFF–, and FBIN (see Figure 5 and Figure 6).

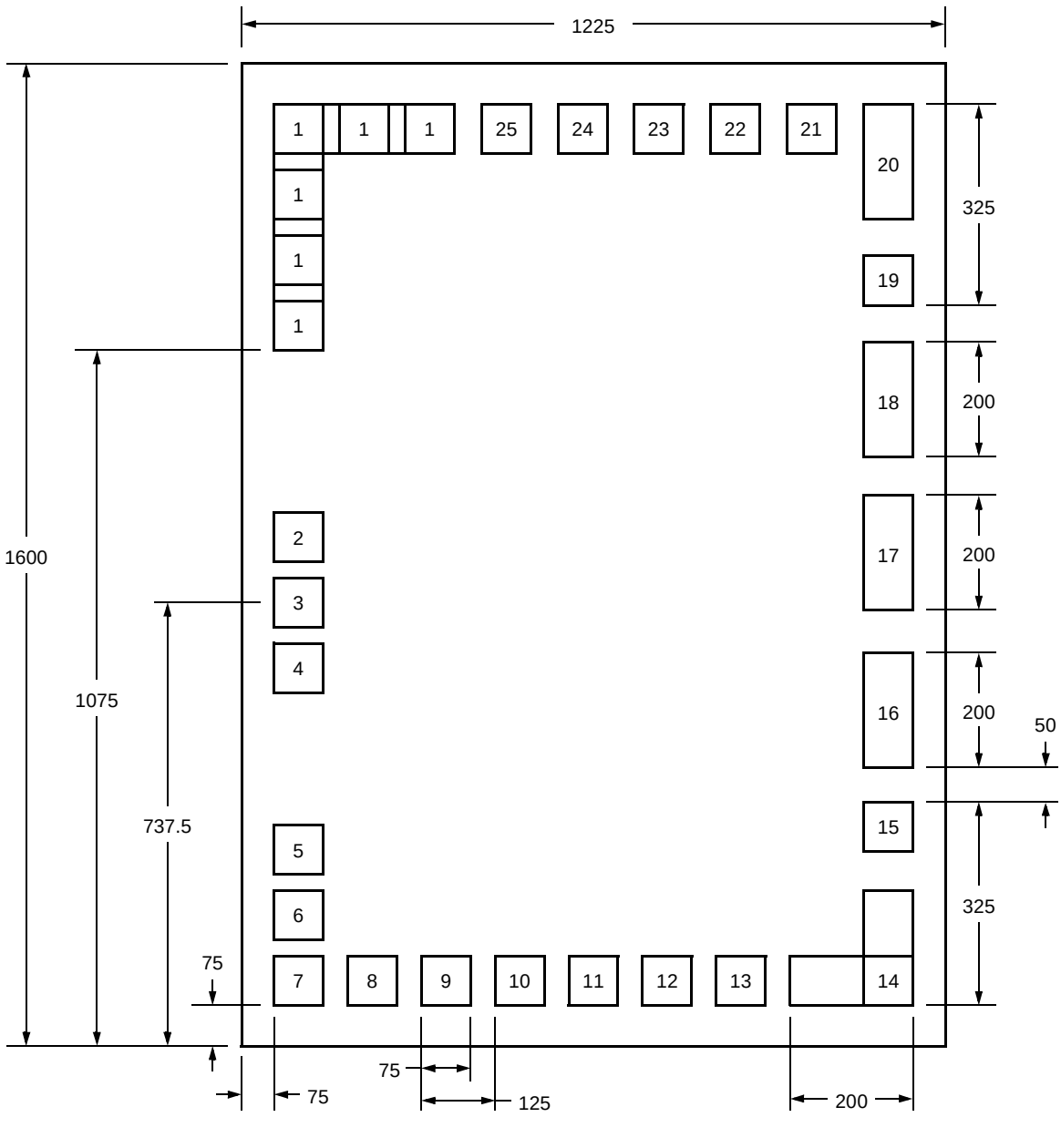
Amplifier operation is from a single –5.2 V power supply. The TTIA0110G is available in die form.

Pin Information

Table 1. Pad Descriptions

Pad	Symbol	Name/Function
1	IN+	**Complementary Input.** This node must be ac-bypassed to ground.
2, 4, 15, 17, 19	GND	**Ground.** Pads are connected to the back side of the die through substrate vias. The back side of the die must be electrically connected to ground.
3	IN–	**Amplifier Input.** Connect to detector anode, current should enter this node.
5, 6, 7, 8, 12, 13, 25	DNC	**Do Not Connect.** Internal test point or reserved future use.
9	$OP1_{OUT}$	**Transimpedance Stage Offset Control Output.**
10	OP1–	**Transimpedance Stage Offset Control Inverting Input.**
11	OP1+	**Transimpedance Stage Offset Control Noninverting Input.**
14, 20	V_{SS}	**Supply Voltage.** –5.2 V_{dc} nominal.
16	OUT–	**Inverted Data Output.** Produces low-level output for current entering IN–.
18	OUT+	**Noninverted Data Output.** Produces high-level output for current entering IN–.
21	OFF–	**Offset –.** Senses average voltage of OUT– pin.
22	OFF+	**Offset +.** Senses average voltage of OUT+ pin.
23	FBIN	**Feedback In.** Apply external voltage to produce offset between OUT– and OUT+.
24	BG	**Band Gap Reference.** Connection for external –2.5 Vdc voltage reference (typical use is an Si band gap).

Pin Information (continued)



Note: All dimensions are in microns.

Figure 2. Die Pad Configuration

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 2. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Max	Unit
Supply Voltage (reference to ground)	V_{SS}	—	–5.75	V
Input Voltage	V_{IN}	GND	Vss	V
Power Dissipation	P_D	—	0.85	W
Storage Temperature Range	T_{stg}	–40	125	°C
Operating Temperature Range	T_A	0	100	°C

1. Long term reliability is not guaranteed in a non-hermetic environment.

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Agere employs a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used in the defined model. No industry-wide standard has been adopted for the CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and, therefore, can be used for comparison purposes.

Table 3. Handling Precautions

Device	Voltage
TTIA0110G	TBD

Die Attachment

The TTIA0110G die must be used in a hermetic environment. The die should be attached with conductive epoxy. If solder is required, an 80 Au/20 Sn solder preform can be used. Using a solder preform eliminates the need for flux. Preforms typically melt at 280 °C, but should be soaked at 305 °C for five to eight seconds. Once the preform melts, a die scrub motion should be used to ensure a good contact. Do not use a vacuum tool to pick-up the die. This may result in damage to air bridges on the die surface. Use a collet for die pick-up to avoid air bridge damage. The TTIA0110G die is 4 mils thick.

Recommended Operating Conditions

Table 4. Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage	V_{SS}	–4.75	–5.5	V
Operating Temperature	T_A	0	70	°C

Electrical Characteristics

T_A = 25 °C, V_{SS} = –5.2 V, and R_{LOAD} = 50 Ω, dc coupled. Bit rate = 9,953.28 Mbits/s NRZ and data pattern = 2^{31} – 1 PRBS, unless otherwise indicated. Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluations. Typical values are for information purposes only and are not part of the testing requirements.

Table 5. Electrical Characteristics

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
Z_{EFF}	Small Signal Transimpedance	Single Ended	—	1	—	kΩ
—	Equivalent Input Noise Current	f = 8 GHz	—	1.5	—	µArms
—	Input Current for Linear Operation	—	—	360	—	μA_{AVG}
$V_{\pm OUT}$	Output Voltage	Single Ended	—	800	—	mVp-p
f_{3dB}	Small Signal Bandwidth	—	—	10	—	GHz
—	Group Delay	50 MHz to 7 GHz	—	±15	—	ps
S_{22}	Output Return Loss	Over f_{3dB} Bandwidth	—	12	—	dB
I_{SS}	Power Supply Current	Vss = –5.2 V	—	155	—	mA

1. C_{DET} = 0.2 pF, L_{DET} = 1.0 nH, R_{DET} = 10 Ω.

Application Information

The ground pads on the die are connected to the back side of the die through substrate vias. The back side of the die is metallized with gold and must be electrically connected to ground. It is not necessary to wire bond to the ground pads of the die.

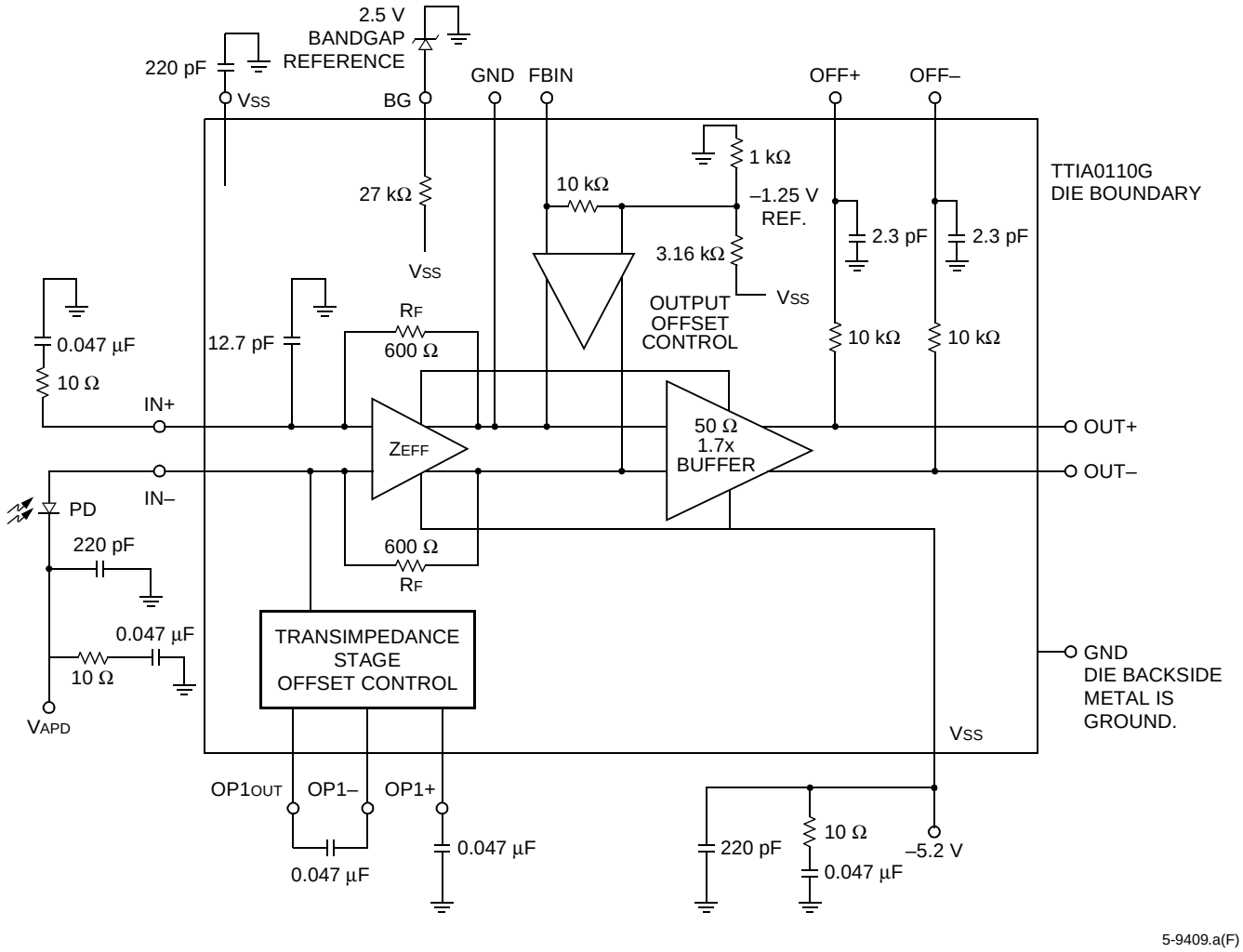


Figure 3. Application Diagram

Applications Information (continued)

Typical Application Circuits

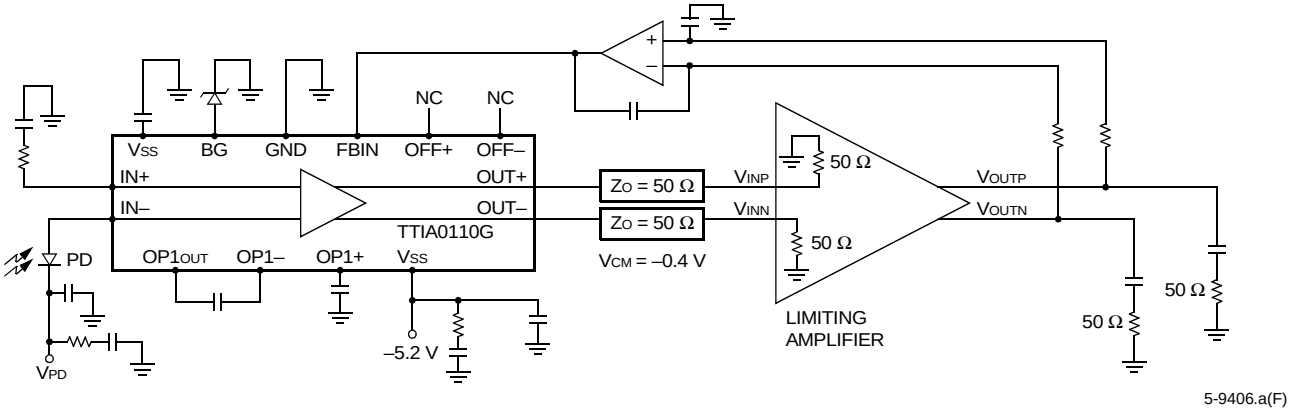


Figure 4. dc-Coupled to Limiting Amplifier

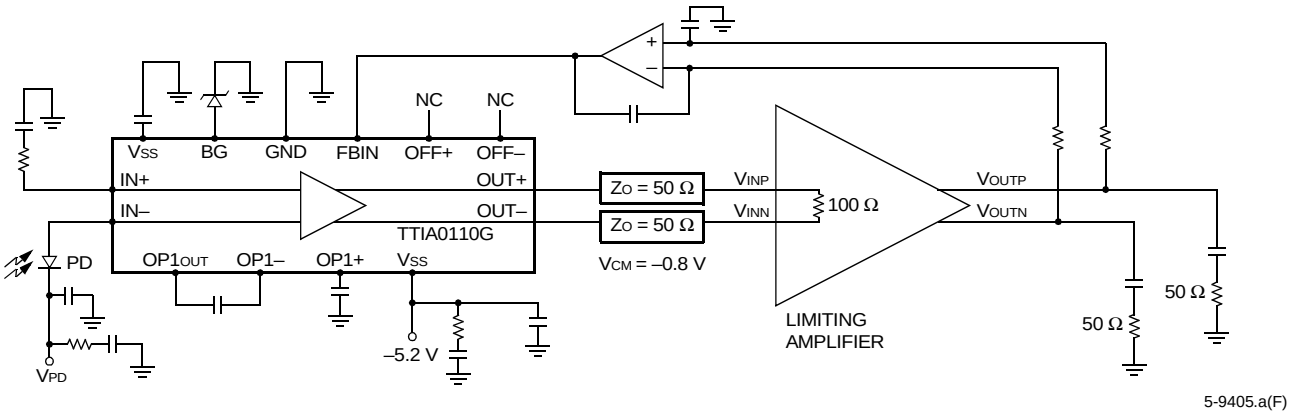


Figure 5. dc-Coupled to Limiting Amplifier

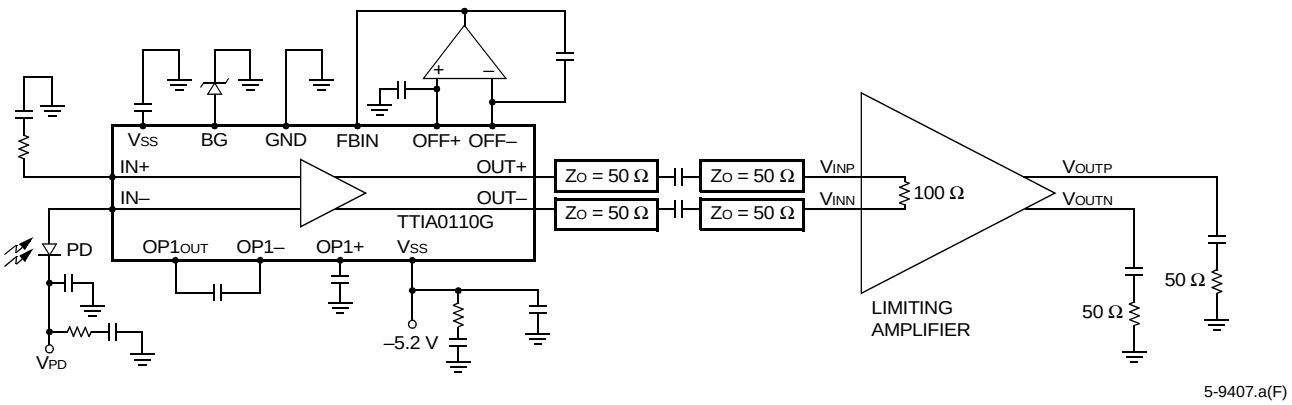


Figure 6. ac-Coupled to Limiting Amplifier

Chip Visual Inspection Criteria

The chips will be visually free of the following defects, at 100x:

- Scratches in the metallization (including air-bridges) that leave less than 50% of the original width undisturbed and distort the outline of the metal feature.
- Voids or missing metallization that leave less than 50% of the original width undisturbed.
- Extra metals that bridge adjacent same layer metal feature. This includes bond pads damaged from probing.
- Crack or chip out that extends into the active area of the device.
- Damaged air-bridges that have been distorted or torn off.
- Particles on the surface of the chip that are large enough to bridge between bond pads.
- Stains larger than the size of a bond pad.
- Lifted or blistered metallization.
- Missing nitride that occurs over or under an active feature.
- Defects to bond pad area:
  - Stains larger than 25% of bond pads.
  - Extra nitride on the bond pad that reduces the open area by more than 25%.
  - Probe damage that removes more than 25% of the bond pad.
  - Probe damage that causes cracks in the surrounding nitride of substrate.

Ordering Information

Device Code	Package	Comcode
TTIA0110G51	Die	108559071

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