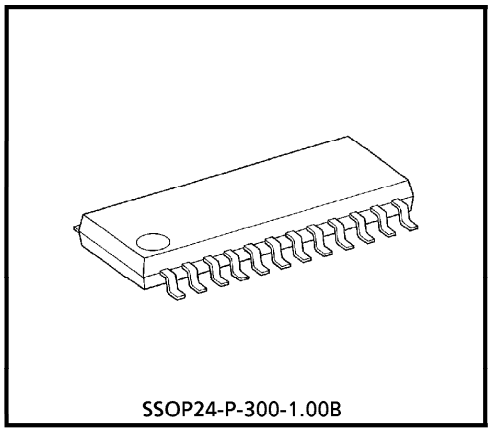
TENTATIVE

TOSHIBA INTELLIGENT POWER DEVICE
SILICON MONOLITHIC POWER MOS INTEGRATED CIRCUIT

TPD7202F

POWER MOSFET GATE DRIVER FOR H BRIDGE

TPD7202F is a power MOSFET Gate driver for H-bridge circuit using charge pump system. Because this IC contains a charge pump circuit for high-side drive, it allows you to configure H-bridge circuit.



SSOP24-P-300-1.00B

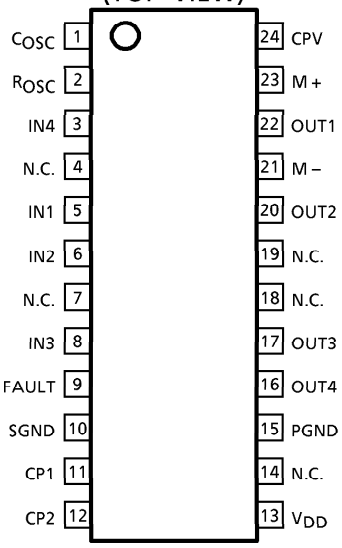
Weight : 0.29 g (typ.)

FEATURES

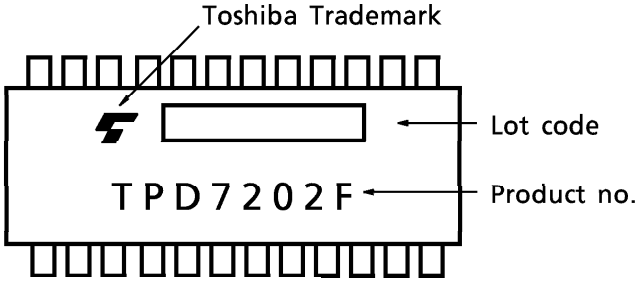
- Power MOSFET Gate Driver for H-bridge circuit
- Built-in power MOSFET protection and diagnosis functions: Overvoltage and low-voltage protection
- Built-in a charge pump circuit.
- Package : SSOP-24 (300 mil) with embossed-tape packing

PIN ASSIGNMENT

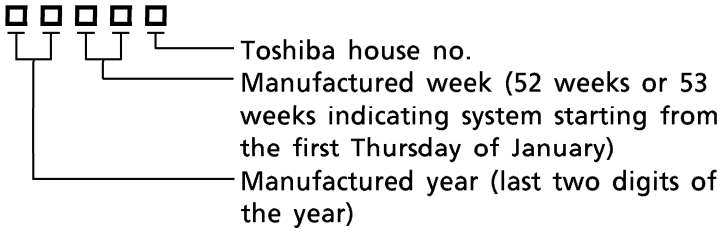
(TOP VIEW)



MARKING



Lot code naming system



Because this product uses MOS structure, must take special care with electrostatic when handling.

980910EBA2

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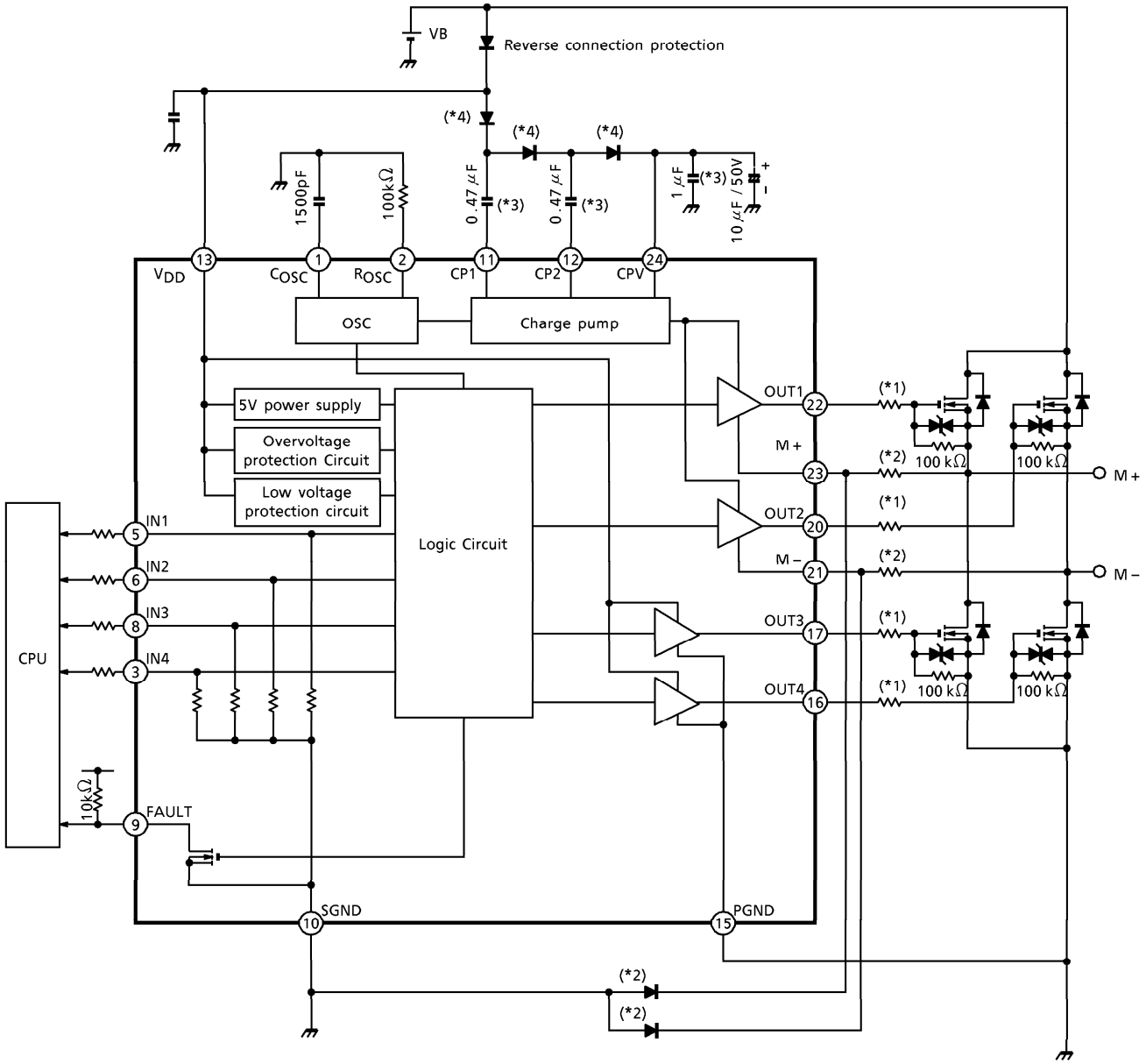
BLOCK DIAGRAM / APPLICATION CIRCUIT



(*1) : Optimum conditions depend on switching loss, EMI, etc. of external MOSFET.
(*2) : SBD VF = 0.5 V max (Recommended : CRS03)
This is needed when the M+ or M − pin is biased to the negative side by more than 0.5 V.
(*3) : This is a laminated ceramic capacitor.
(*4) : High-speed diode trr = 100 ns max (Recommended : CRH01)

(Note) : When selecting external parts, please read "Method for selecting external parts" described later.

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PIN DESCRIPTION

PIN No.	SYMBOL	PIN DESCRIPTION
1	C_{OSC}	This pin sets the oscillation frequency for charge pump drive. Connect a 1500 pF (recommended) capacitor.
2	R_{OSC}	This pin sets the oscillation frequency for charge pump drive. Connect a 100 kΩ (recommended) resistor.
3	IN4	Input pin: it controls the power MOS connected to OUT4 (low side of M−). Built-in pull-down resistor (100 kΩ typ.).
4	N.C.	—
5	IN1	Input pin: it controls the power MOS connected to OUT1 (high side of M+). Built-in pull-down resistor (100 kΩ typ.)
6	IN2	Input pin: it controls the power MOS connected to OUT2 (high side of M−). Built-in pull-down resistor (100 kΩ typ.)
7	N.C.	—
8	IN3	Input pin: it controls the power MOS connected to OUT3 (low side of M+). Built-in pull-down resistor (100 kΩ typ.)
9	FAULT	Diagnosis output pin: when low-voltage 6 V (typ.) or overvoltage 22 V (typ.) is detected, output "H". Circuit configuration is N-ch open drain.
10	SGND	Signal block GND pin
11	CP1	Capacitor pin for charge pump. Connect a 0.47 μF (recommended) laminated ceramic capacitor.
12	CP2	Capacitor pin for charge pump. Connect a 0.47 μF (recommended) laminated ceramic capacitor.
13	V_{DD}	Power supply pin: when low voltage (6 V typ.) or overvoltage (22 V typ.) is detected, all outputs are shut down.
14	N.C.	—
15	PGND	Power block GND pin
16	OUT4	Drives the power MOSFET connected to the low side of M−.
17	OUT3	Drives the power MOSFET connected to the low side of M+.
18	N.C.	—
19	N.C.	—
20	OUT2	Drives the power MOSFET connected to the high side of M−.
21	M−	Output pin
22	OUT1	Drives the power MOSFET connected to the high side of M+.
23	M+	Output pin
24	CPV	Final stage capacitor for the charge pump. Connect 1 μF (recommended) laminated ceramic capacitor and 10 μF (recommended) aluminum electrolytic capacitor in parallel.

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TRUTH TABLE

INPUT				OUTPUT				REMARKS
IN1	IN2	IN3	IN4	OUT1	OUT2	OUT3	OUT4	
L	L	L	L	L	L	L	L	Stop mode
H	L	L	H	H	L	L	H	Forward mode
L	H	H	L	L	H	H	L	Reverse mode
L	L	H	H	L	L	H	H	Brake mode
H	L	H	L	L	L	L	L	High side / Low side arm shorting mode (*)
L	H	L	H	L	L	L	L	High side / Low side arm shorting mode (*)

(*) : High side / Low side arm shorting mode is disabled by the internal logic. (FAULT is kept low.)
When undervoltage (6 V typ.) or overvoltage (22 V typ.) is detected, all outputs are pulled low regardless of input signals. At this time, FAULT output goes high (open-drain, high-impedance).

MAXIMUM RATING (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT	REMARKS
Power Supply Voltage	V_{DD}	−0.5~30	V	
Output Current	I_{SOURCE}	1	A	Pulse width ≦ 10 μs
	I_{SINK}	1		
Input Voltage	V_{IN}	−0.5~7.0	V	
FAULT Pin Voltage	V_{FAULT}	30	V	
M+, M− Pin Negative Voltage	M+ (−) M− (−)	−0.5	V	Negative voltage that can be applied to M+ and M− pins (Reference to SGND pin)
PGND Pin Negative Voltage	PGND (−)	−0.5	V	Negative voltage that can be applied to PGND pin (Reference to SGND pin)
Fault Pin Current	I_{FAULT}	5	mA	
Power Dissipation	P_D	0.8	W	
		1.5 (Note)		
Operating Temperature	T_{opr}	−40~125	°C	
Storage Temperature	T_{stg}	−40~150	°C	

THERMAL RESISTANCE

CHARACTERISTIC	SYMBOL	RATING	UNIT
Junction to Ambient Thermal Resistance	$R_{th\ (j\text{-}a)}$	156.3	°C / W
		83.4 (Note)	

(Note) : When a device mounted on 60 mm × 60 mm × 1.6 t glass epoxy PCB.

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ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta = −40~125°C)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	CONDITION	MIN.	TYP.	MAX.	UNIT	REMARKS
Operating Supply Voltage		V_{DD}	—	—	7	13.5	18	V	
Supply Current		I_{DD} (1)	1	V_{DD} = 13.5 V	—	—	10	mA	Oscillation circuit stops
		I_{DD} (2)	2	V_{DD} = 13.5 V, V_{IN1}~V_{IN4} = 0 V	—	—	100		When oscillation circuit is operating f = 20 kHz, mean current
Input Voltage		V_{IH}	2	V_{DD} = 7~18 V, I_O = 0 A	3.5	—	—	V	IN1-IN4 high-level input voltage
		V_{IL}			—	—	1.5		IIN1-IN4 low-level input voltage
Input Current		I_{IH}	2	V_{DD} = 7~18 V, V_{IN} = 5 V, I_O = 0 A	—	—	1	mA	IN1-IN4 input current
		I_{IL}		V_{DD} = 7~18 V, VIN = 0 V, I_O = 0 A	− 10	—	10	μA	
Output Voltage	High side	V_{OH}	2	V_{DD} = 13.5 V, V_{IN} = 5 V, I_O = 0 A	V_{CPV} − 2	—	V_{CPV}	V	OUT1 pin voltage (reference to M + pin) OUT2 pin voltage (reference to M − pin) V_{CPV} denotes CPV pin voltage
		V_{OL}		V_{DD} = 13.5 V, V_{IN} = 0 V, I_O = 0 A	—	—	0.1		
	Low side	V_{OH}		V_{DD} = 13.5 V V_{IN} = 5 V,, I_O = 0 A	11.5	—	13.5		OUT3 pin voltage (reference to PGND pin) OUT4 pin voltage (reference to PGND pin)
		V_{OL}		V_{DD} = 13.5 V, V_{IN} = 0 V, I_O = 0 A	—	—	0.1		
Charge Pump Voltage		V_{CPV}	2	V_{DD} = 13.5 V	23.5	—	34	V	CPV pin voltage (reference to SGND pin)
Active Clamp Voltage	High side	V_{CLAMP}	—	V_{IN} = 5 V, I_O = 10 mA	14	—	20	V	Clamp voltage between OUT1 and M + pins Clamp voltage between OUT2 and M − pins
	Low side			V_{IN} = 5 V, I_O = 10 mA	—	18	—		OUT3 and OUT4 pins clamp voltage (reference to PGND pin)

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CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	CONDITION	MIN.	TYP.	MAX.	UNIT	REMARKS
Output Resistance		R_{SOURCE}	2	V_{DD} = 13.5 V, V_{IN} = 5 V, I_O = 0.5 A	—	7	10	Ω	OUT1-OUT4 output resistance pulse width ≦ 10 μs
		R_{SINK}		V_{DD} = 13.5 V, V_{IN} = 0 V, I_O = −0.5 A	—	4.5	10		
Low-Voltage Protection	Detection	V_{SD} (L)	3	—	5.5	6	6.5	V	Lowvoltage detection voltage and hysteresis (V_{DD} voltage detected)
	Hysteresis	ΔV_{SD} (L)			—	0.5	—		
Over-Voltage Protection	Detection	V_{SD} (H)	3	—	20	22	24	V	Overvoltage detection voltage and hysteresis (V_{DD} voltage detected)
	Hysteresis	ΔV_{SD} (H)			—	2	—		
Swithcing Time	Turn-on delay time	t_{d} (ON)	4	V_{DD} = 7~18 V, C_{OUT} = 0.047 μF, R_G = 47 Ω	—	—	4	μs	OUT1-OUT4 switching time
	Turn-on time	t_{ON}			—	—	6		
	Turn-off delay time	t_{d} (OFF)			—	—	4		
	Turn-off time	t_{OFF}			—	—	6		
Oscillating Frequency		f_{OSC}	2	V_{DD} = 7~18 V, R_{OSC} = 100 kΩ, C_{OSC} = 1500 pF	—	20	—	kHz	f_{OSC} calculation formula $f_{OSC} = 3 / \{C_{OSC} (R_{OSC} + 2\ k)\}$ (Hz)
FAULT Pin Voltage		V_{FAULT}	2	I_{FAULT} = 1 mA	—	—	0.8	V	FAULT pin low-level voltage (open-drain)
FAULT Delay Time		t_{ON}	3	R_{FAULT} = 5.1 kΩ V_{FAULT} = 5 V (External power supply)	—	1	—	μs	Time from low voltage / overvoltage detection or restoration to FAULT output inversion
		t_{OFF}			—	1	—		

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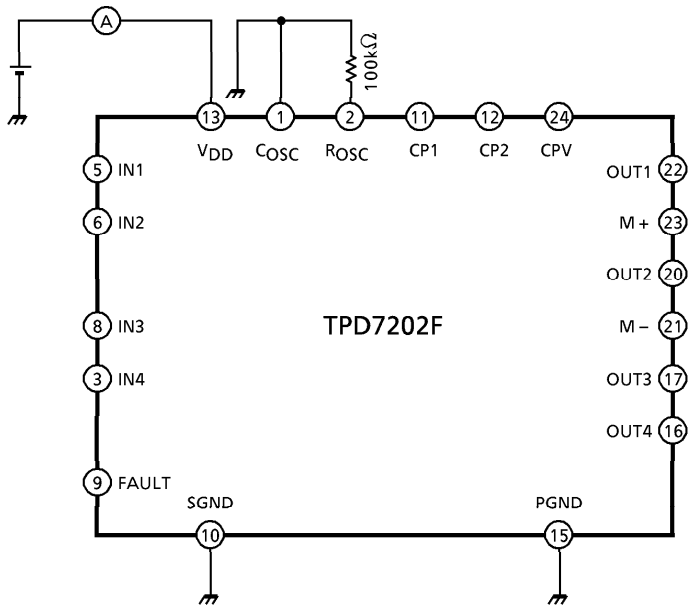
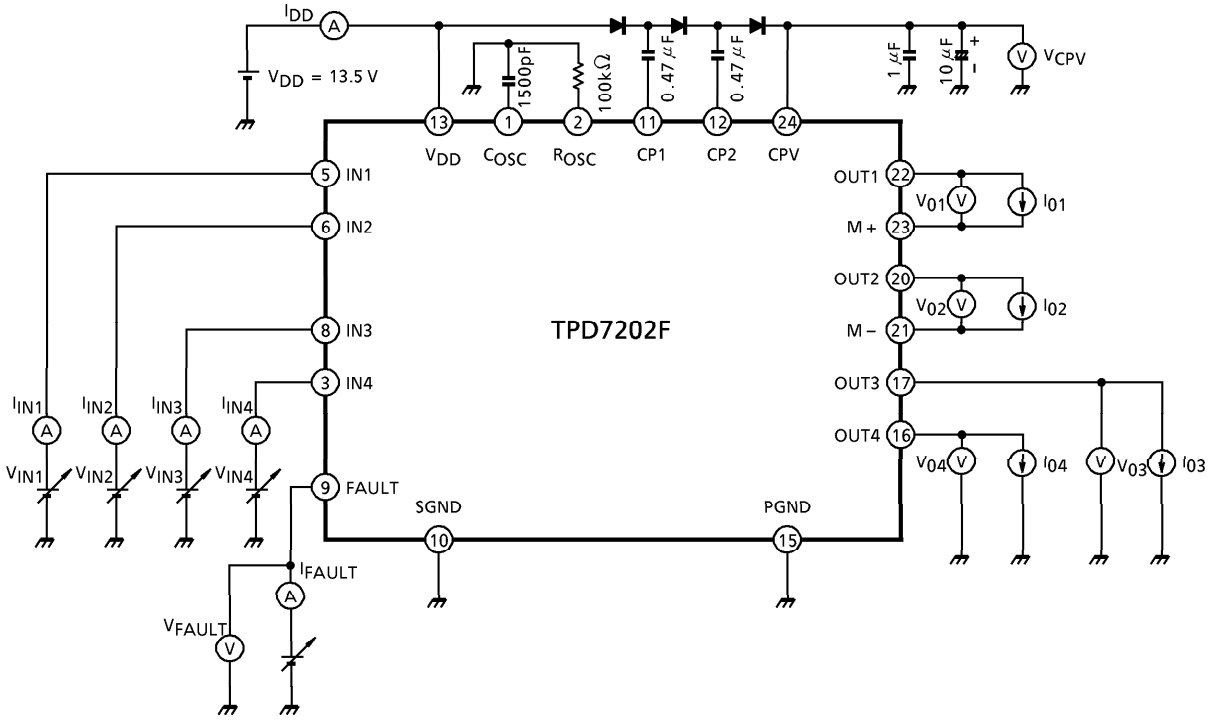
TESTING CIRCUIT 1 I_{DD} (1)



TESTING CIRCUIT 2 I_{DD} (2), V_{IH}, V_{IL}, I_{IH}, I_{IL}, V_{OH}, V_{OL}, V_{CPV}, V_{FAULT}



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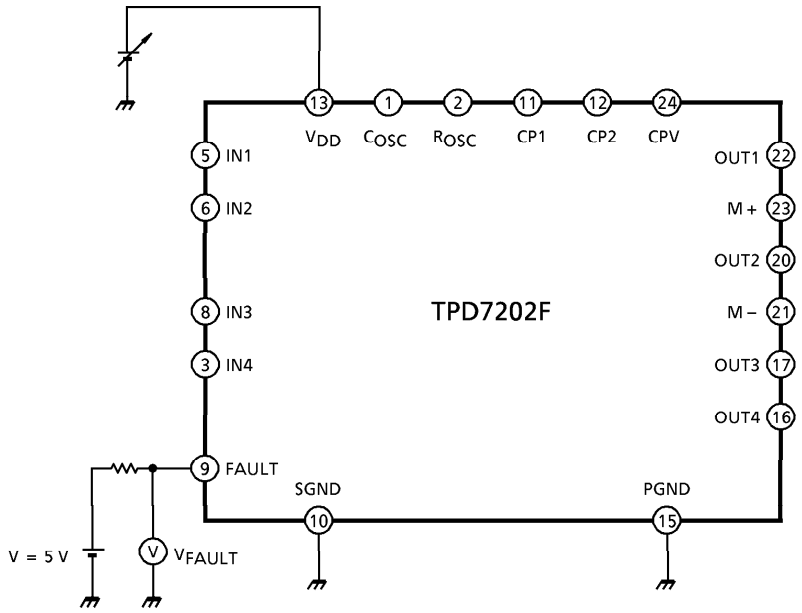
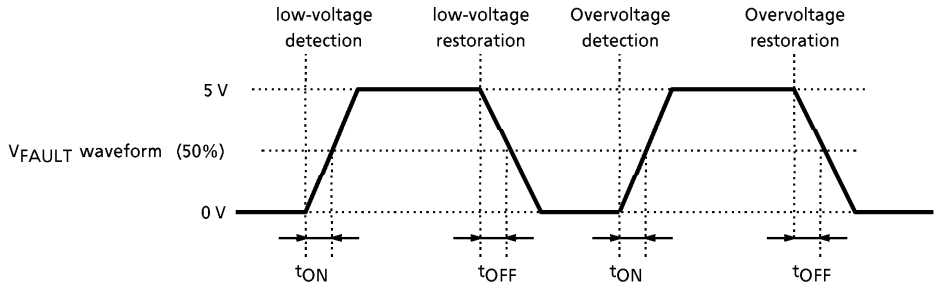
TESTING CIRCUIT 3 $V_{SD\,(L)}$, $\Delta V_{SD\,(L)}$, $V_{SD\,(H)}$, $\Delta V_{SD\,(H)}$, FAULT delay time t_{ON}, t_{OFF}





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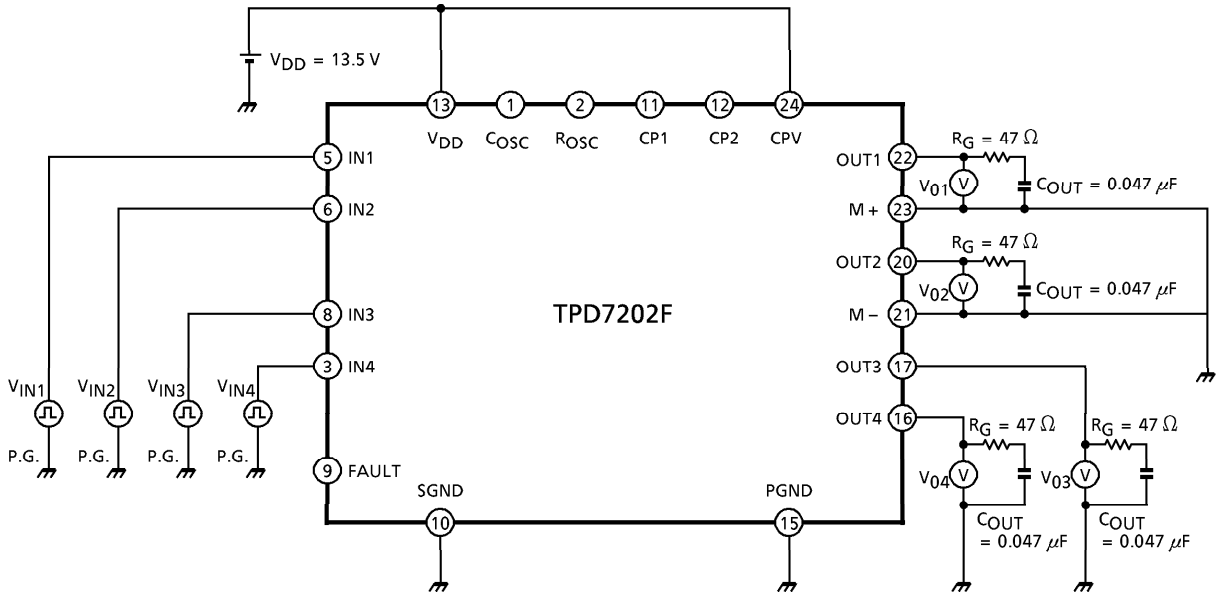
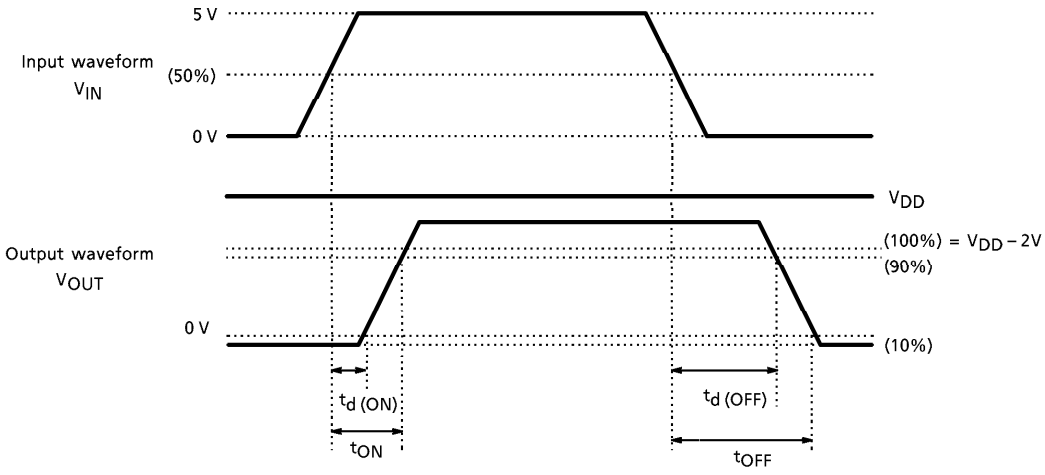
TESTING CIRCUIT 4 $t_{d\,(ON)}$, t_{ON}, $t_{d\,(OFF)}$, t_{OFF}





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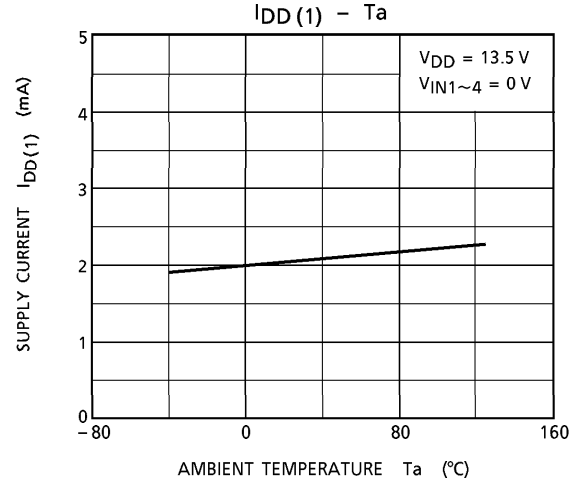
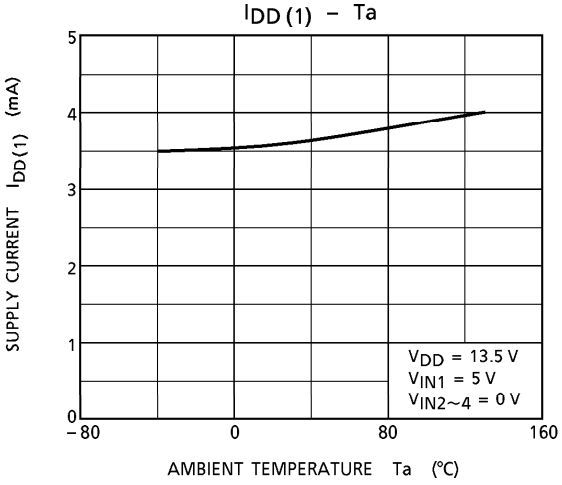
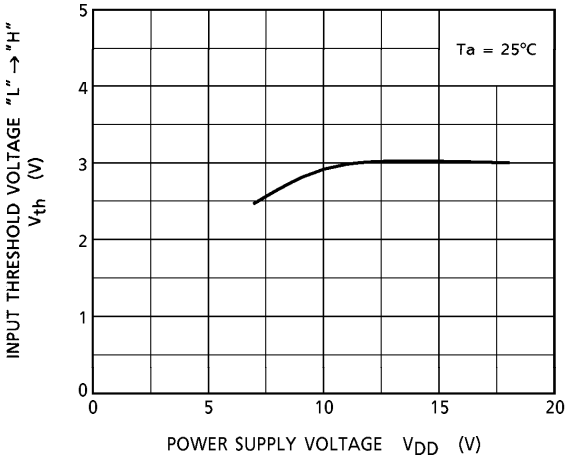
I_{DD} (1) – Ta



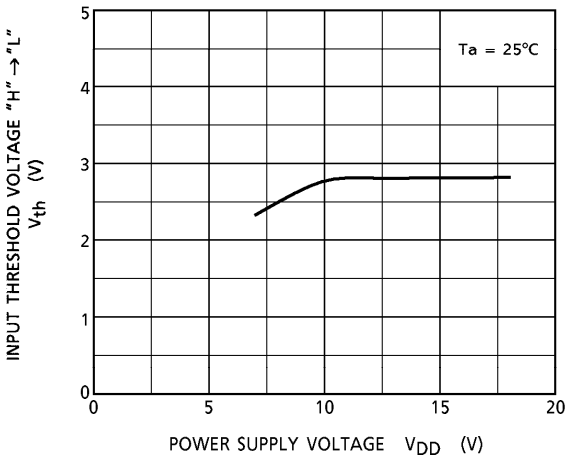
I_{DD} (1) – Ta



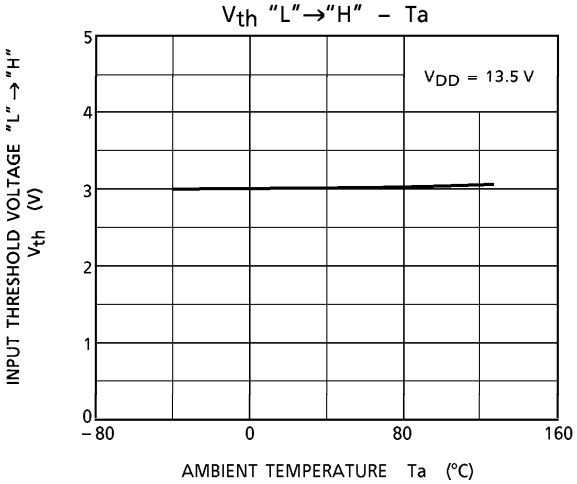
V_{th} "L"→"H" – V_{DD}



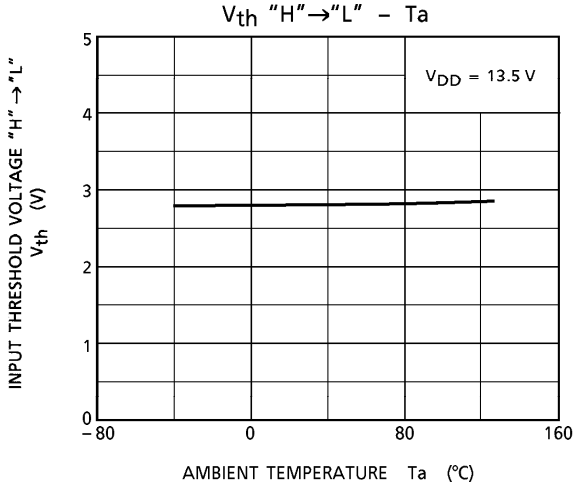
V_{th} "H"→"L" – V_{DD}



V_{th} "L"→"H" – Ta



V_{th} "H"→"L" – Ta



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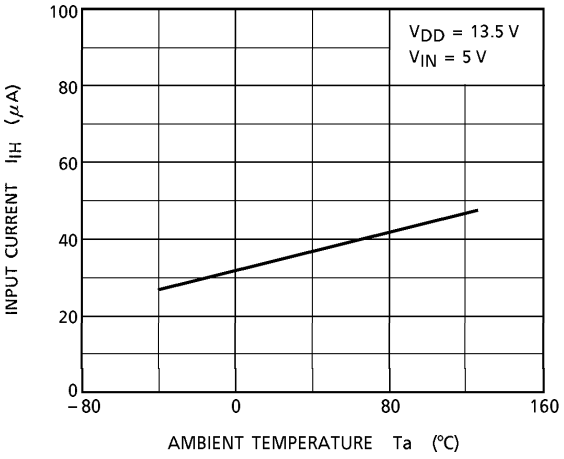
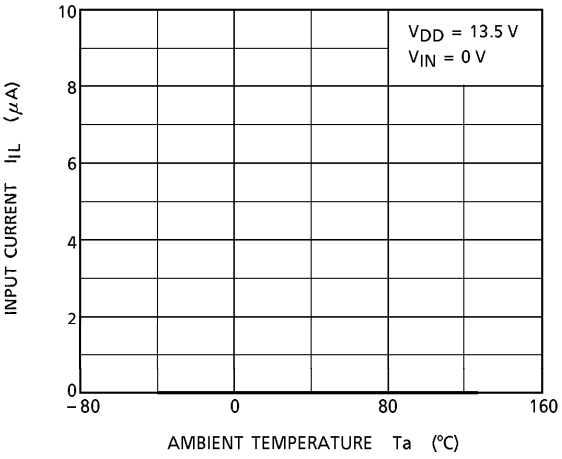
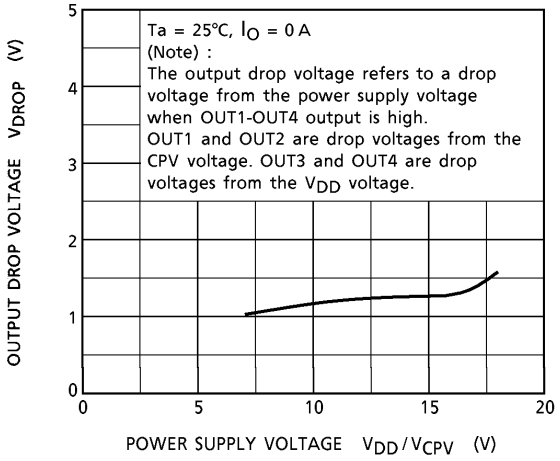
I_{IH} – Ta



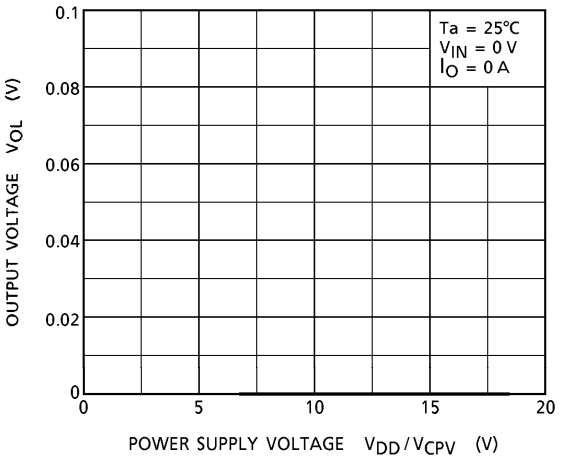
I_{IL} – Ta



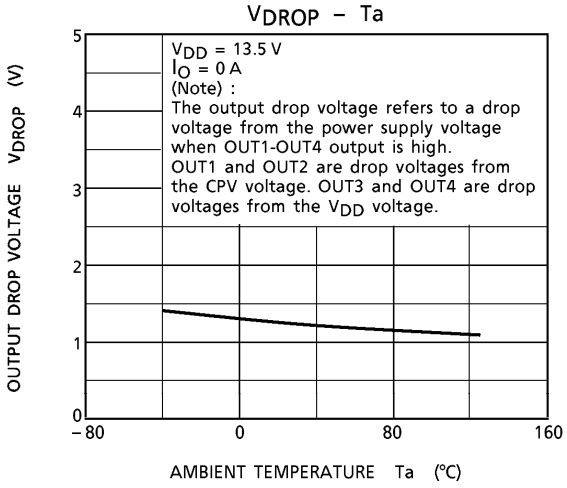
V_{DROP} – POWER SUPPLY VOLTAGE



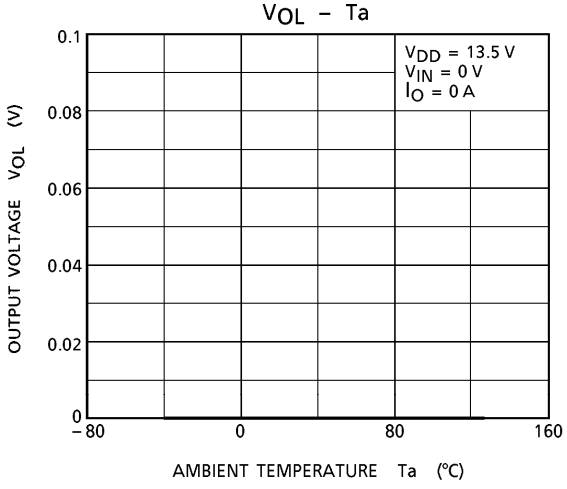
V_{OL} – POWER SUPPLY VOLTAGE



V_{DROP} – Ta



V_{OL} – Ta



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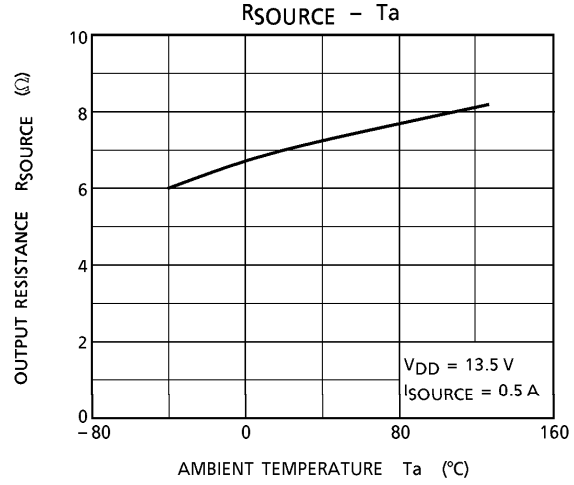
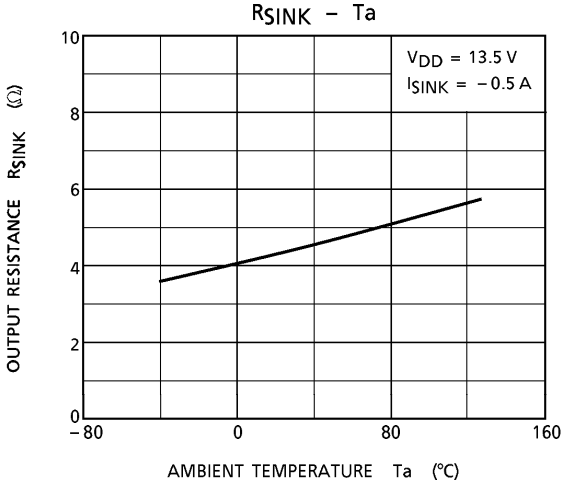
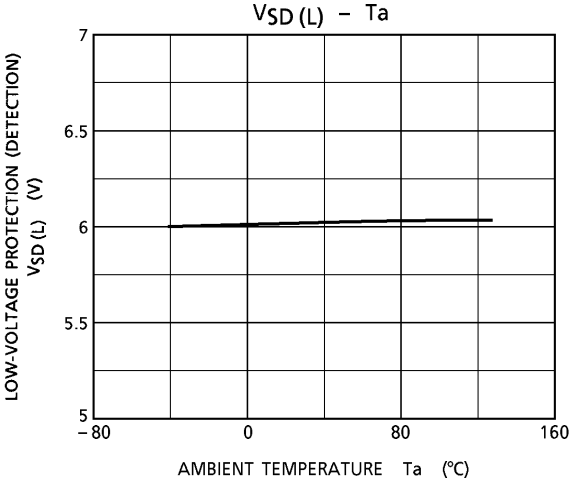
R_{SOURCE} – Ta



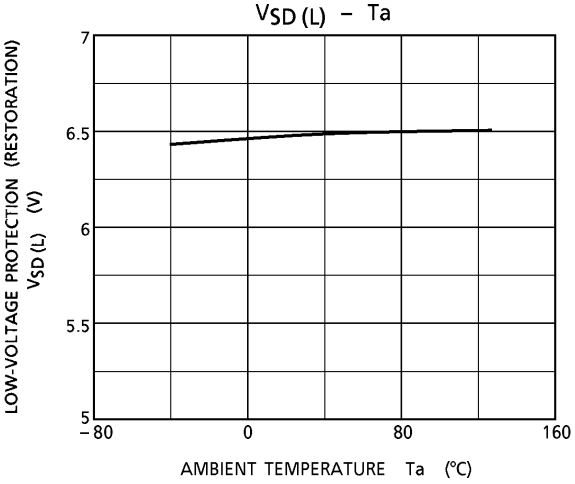
R_{SINK} – Ta



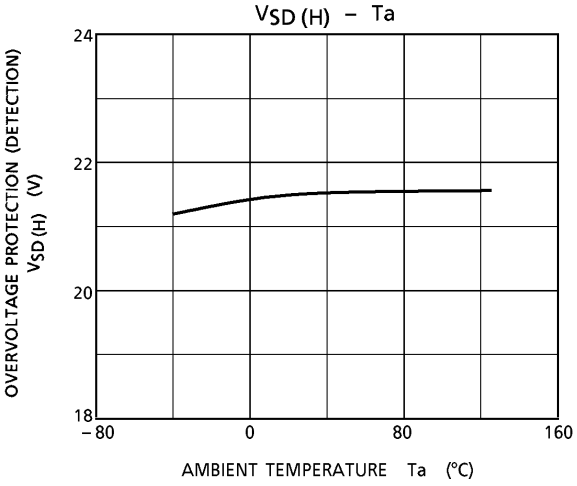
$V_{SD\,(L)}$ – Ta



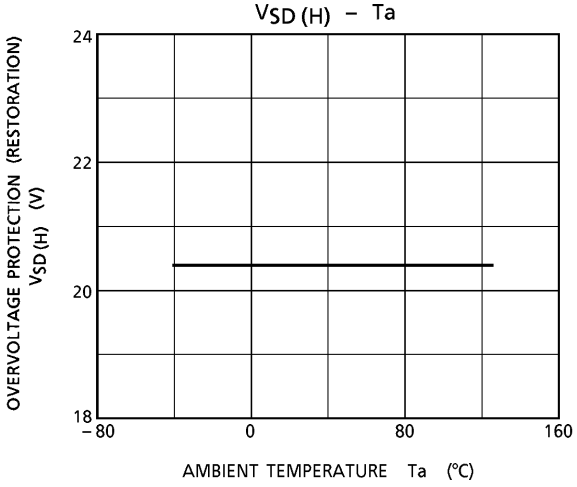
$V_{SD\,(L)}$ – Ta



$V_{SD\,(H)}$ – Ta



$V_{SD\,(H)}$ – Ta



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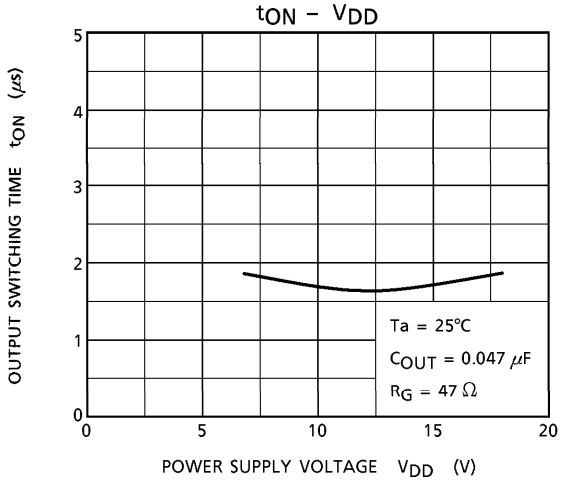
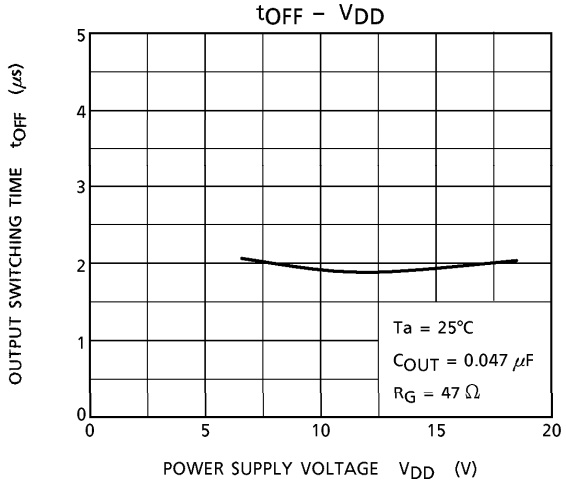
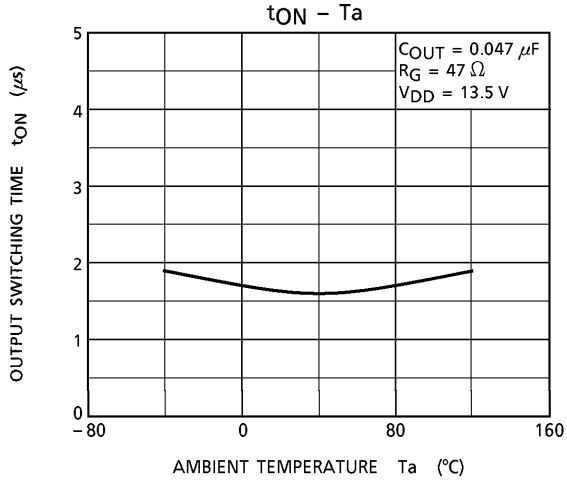
OUTPUT SWITCHING TIME (OUT1~OUT4)
t_{ON} – V_{DD}



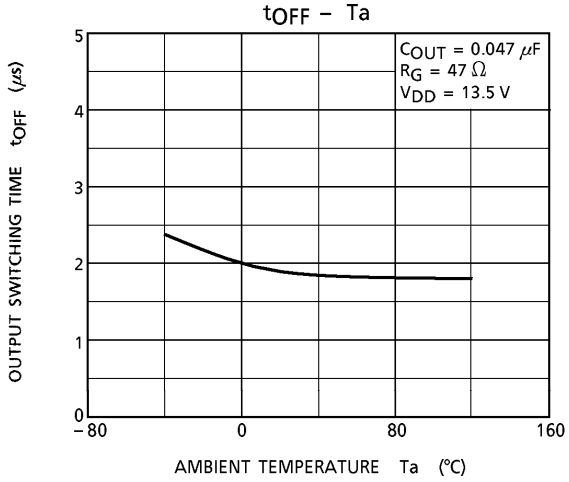
OUTPUT SWITCHING TIME (OUT1~OUT4)
t_{OFF} – V_{DD}



OUTPUT SWITCHING TIME (OUT1~OUT4)
t_{ON} – Ta



OUTPUT SWITCHING TIME (OUT1~OUT4)
t_{OFF} – Ta



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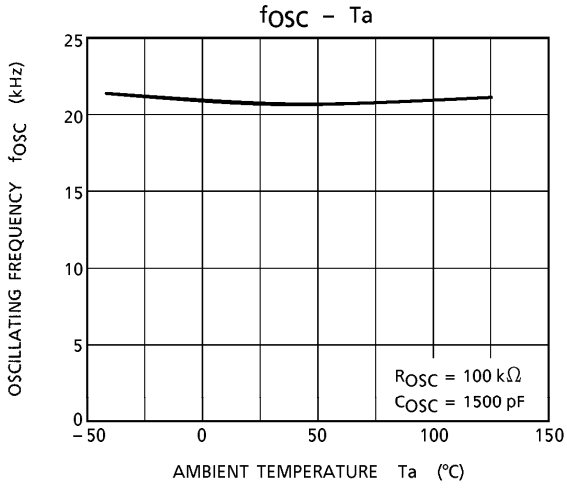
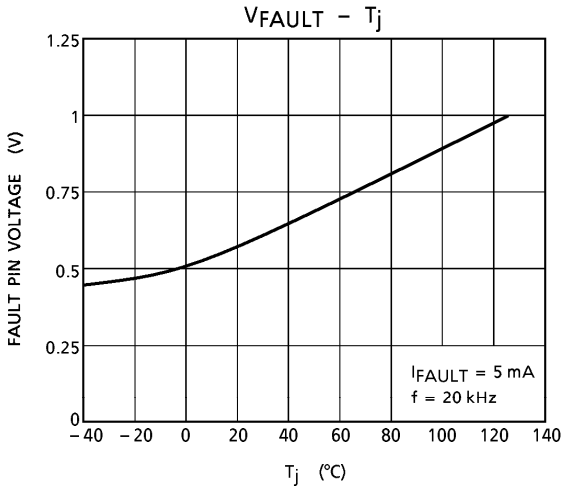
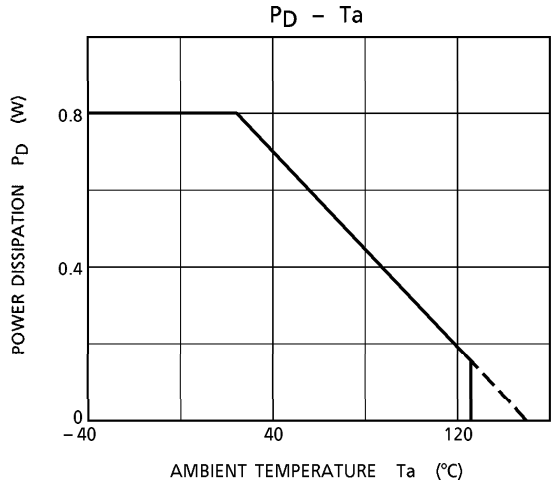

fOSC – Ta
OSCILLATING FREQUENCY fOSC (kHz)
25
20
15
10
5
0
– 50
0
50
100
150
ROSC = 100 kΩ
COSC = 1500 pF
AMBIENT TEMPERATURE Ta (°C)


VFAULT – Tj
FAULT PIN VOLTAGE (V)
1.25
1
0.75
0.5
0.25
0
– 40
– 20
0
20
40
60
80
100
120
140
IFAULT = 5 mA
f = 20 kHz
Tj (°C)


PD – Ta
POWER DISSIPATION PD (W)
0.8
0.4
0
– 40
40
120
AMBIENT TEMPERATURE Ta (°C)

TENTATIVE

Method for selecting external parts

PIN No.	PIN NAME	TYPE	RECOMMENDED VALUE / RECOMMENDED PRODUCT	DESCRIPTION
1	C_{OSC}	Capacitor	1500 pF (ceramic)	Sets charge pump's oscillation frequency.
2	ROSC	Resistor	100 kΩ	Sets charge pump's oscillation frequency.
11 12	CP1 CP2	Capacitor	0.47 μF (laminated ceramic)	Capacitor for the charge pump. Greater this capacitance larger the charging current to the capacitor, so there is a greater loss in the IC.
24	CPV	Capacitor	1 μF (laminated ceramic) and 10 μF (aluminum electrolytic) connected in parallel	Greater this capacitance, larger the charge pump (CPV pin)'s current supply capacity, so there is a greater loss in the IC. Therefore, be careful not to exceed the allowable loss.
11 12 24	CP1 CP2 CPV	High-speed diode	t_{rr} = 100 ns (max.) CRH01 (t_{rr} = 35 ns max.) recommended	Diode for the charge pump. An electric charge equal to the diode's Q_{rr} component goes out of the capacitor's charged electricity. Therefore, use a high-speed diode.
22 20 17 16	OUT1 OUT2 OUT3 OUT4	Resistor	—	Gate resistor for external power MOSFET. Choose the optimum value by considering the switching loss and EMI of the power MOSFET.
10 21 23	SGND M + M –	SBD	V_F = 0.5 V (max.) CRS03 (V_F = 0.45 V max. @0.7 A) recommended	This is needed when the M + or M – pin is biased to the negative side by more than 0.5 V from the SGND voltage. Because this IC operates relative to SGND, a parasitic diode exists toward each pin. When the M + or M – pin is biased to the negative side by more than 0.5 V from SGND, the parasitic diode conducts, causing the IC to operate erratically or generate abnormal heat.
21 23	M + M –	Resistor	—	This is needed when the M + or M – pin is biased to the negative side by more than 0.5 V from the SGND voltage. This is used to limit current for external SBD.

TENTATIVE

USAGE PRECAUTIONS

(Note 1) : About taking the charge pump voltage to external devices

Current can be taken out of the charge pump's final stage (CPV pin) to external devices without causing any problem. In this case, because the charge pump voltage drops, increase the capacitance of the capacitor connected to the CPV pin. However, this may cause the charging current to the capacitor and, hence, loss in the IC to increase. So be careful not to exceed the allowable loss.

(Note 2) : About heat sink design

Because this IC contains a charge pump function, loss in it affects external capacitor capacitance and diode characteristics. It is recommended that the junction temperature, T_j, be judged from the on-voltage of the FAULT pin (open-drain). When V_{DD} is within the range of operating power supply voltages, the FAULT pin outputs a low. For details about on-voltage characteristics, see T_j-V_{FAULT} characteristic curves.

(Note 3) : About dead time setting

For arm-shorting input logic, all outputs (OUT1-OUT4) are pulled low. When operating in forward or reverse mode, consider the OUT1-OUT4 switching time and the switching time (including temperature characteristic) of the external power MOSFET as you set the dead time. The dead time required for only the IC, not including the external power MOSFET, is 4 μs (within all operating power supply voltages and all operating temperatures).

(Note 4) : Shorting between outputs, Shortcircuit of outputs and V_{DD} pin or shortcircuit of outputs GND pin may cause the IC to break down. Therefore, pay careful attention to the design of output lines and V_{DD} and GND lines.

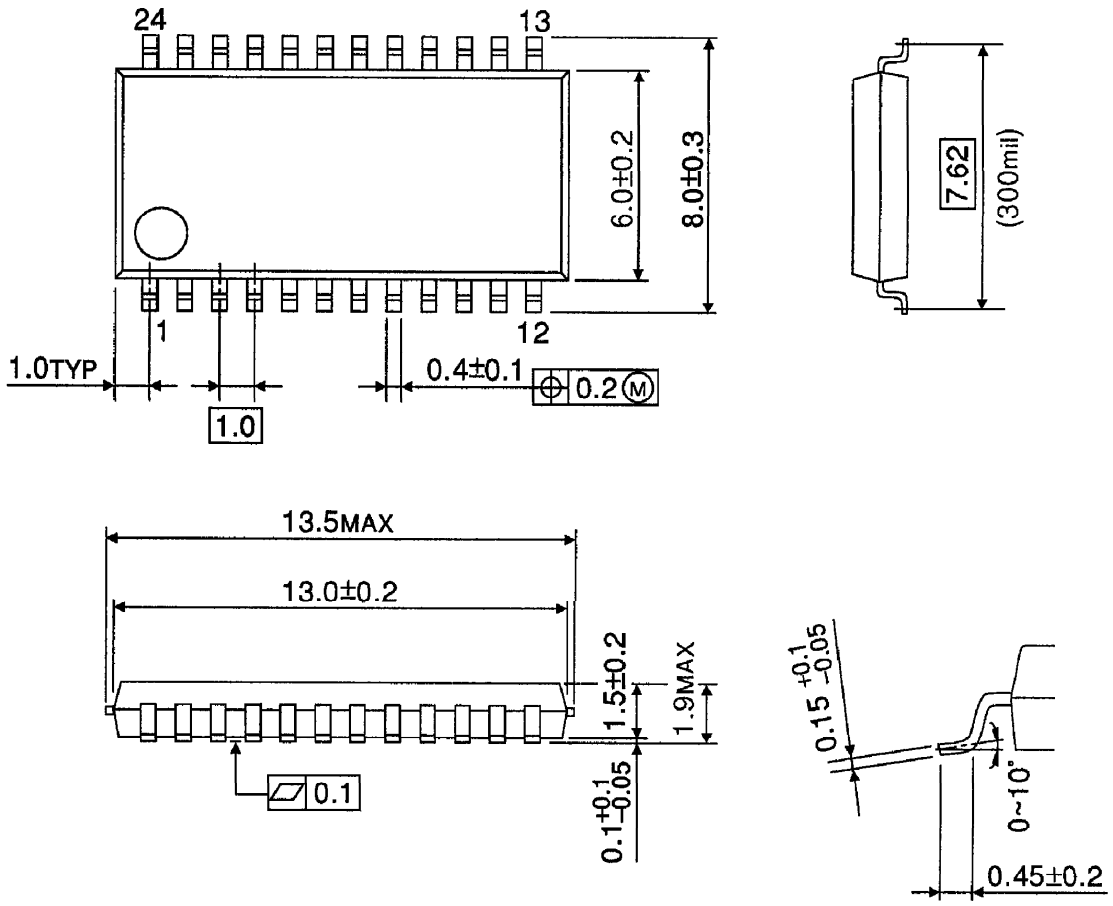
(Note 5) : Precautions on dry packing

After unpacking dry or moistureproof packing, please make sure the device is mounted in place within 48 hours at temperature and humidity of 30°C and 60% RH or less. Because the device is emboss-taped and cannot be processed by baking, always be sure to use it within said allowable time after unpacking.
Tape packing quantity: 500 devices / reel (EL) or 2000 devices / reel (EL1)

TENTATIVE

PACKAGE DIMENSIONS

SSOP24-P-300-1.00B Unit : mm



Weight : 0.29 g (typ.)