

TENTATIVE

TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

## 16-MBIT (2M × 8 BITS) CMOS FLASH MEMORY

## DESCRIPTION

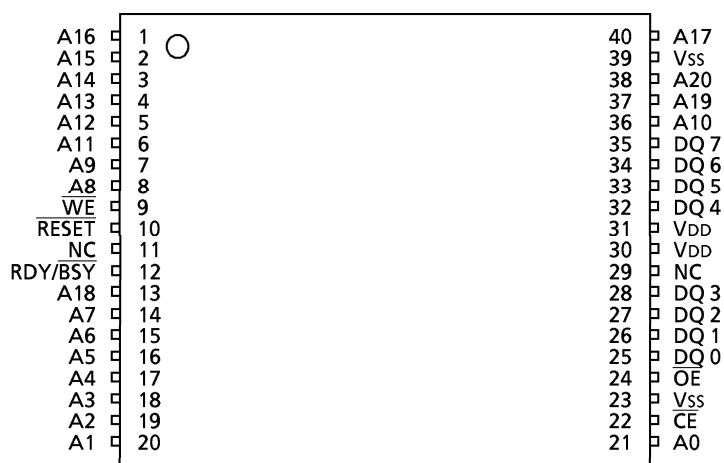
The TC58FVT016/B016 is a 16,777,216-bit, 3.0-V read-only electrically erasable and programmable flash memory organized as 2,097,152 words × 8 bits. The TC58FVT016/B016 features commands for Read, Program and Erase operations to allow easy interfacing with microprocessors. The commands are based on the JEDEC standard. The Program and Erase operations are automatically executed in the chip. The device has Chip, Block and Multi-Block Erase capability.

The TC58FVT016/B016 is available in either a 40-pin TSOP package to suit a variety of design applications.

## FEATURES

- Power Supply  
V<sub>DD</sub> = 2.7 V to 3.6 V
- Organization  
2M × 8 bits
- Modes  
Auto Program, Auto Chip Erase  
Auto Block Erase, Auto Multiple Block Erase  
Erase Suspend/Resume, Block Protection  
Data Polling/Toggle Bit
- Block Erase Architecture  
1 × 16 Kbytes / 2 × 8 Kbytes /  
1 × 32 Kbytes / 31 × 64 Kbytes
- Boot Block Architecture  
TC58FVT016FT ----- Top Boot Block  
TC58FVB016FT ----- Bottom Boot Block
- Mode Control  
Compatible with JEDEC standard commands
- Erase/Program Cycles  
10<sup>5</sup> Cycles typ.
- Access Time  
85 ns (V<sub>DD</sub> = 3.0 V to 3.6 V)  
100 ns / 120 ns (V<sub>DD</sub> = 2.7 V to 3.6 V)
- Power Dissipation  
250 μA (Standby TTL level)  
5 μA (Standby CMOS level)  
30 mA (Read operation)  
40 mA (Program/Erase Operations)
- Package  
TC58FVT016FT/B016FT : TSOP I 40 - P - 1020 - 0.50  
(Weight: 0.43 g typ.)

## PIN ASSIGNMENT (TOP VIEW)



TC58FVT016FT / B016FT (TSOP)

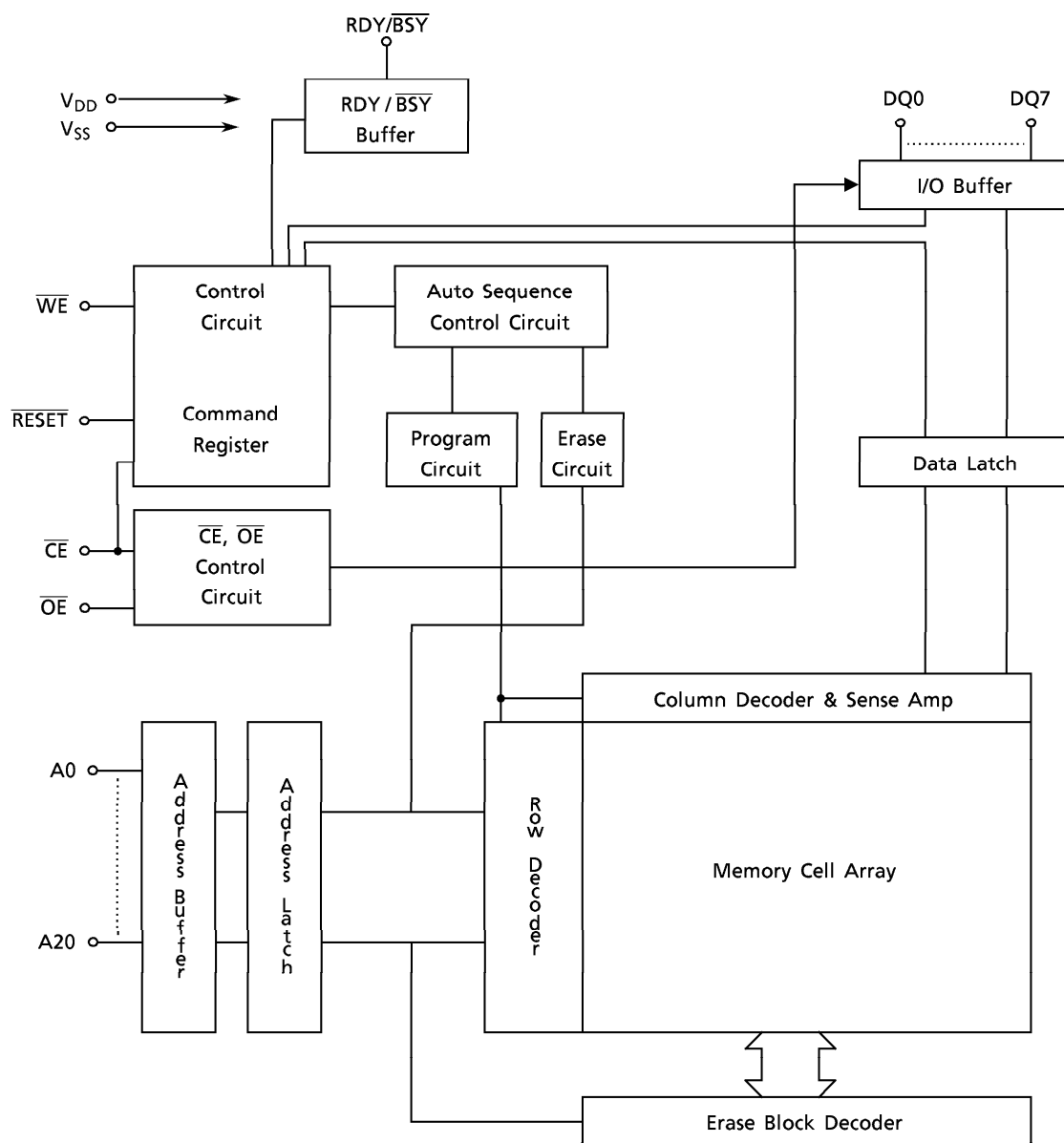
## PIN NAMES

A0 to A20	Address Input
DQ0 to DQ7	Data Input / Output
CE	Chip Enable Input
OE	Output Enable Input
WE	Write Enable Input
RDY/BSY	Ready / Busy Output
RESET	Hardware Reset Input
NC	No Connection
V <sub>DD</sub>	Power Supply
V <sub>SS</sub>	Ground

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BLOCK DIAGRAM



**MODE SELECTION**

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A9	A6	A1	A0	$\overline{RESET}$	DQ0 to DQ7
Read	L	L	H	A9	A6	A1	A0	H	Dout
ID Read (Manufacturer Code)	L	L	H	V <sub>ID</sub>	L	L	L	H	Code
ID Read (Device Code)	L	L	H	V <sub>ID</sub>	L	L	H	H	Code
Standby	H	*	*	*	*	*	*	H	High-Z
Output Disable	*	H	H	*	*	*	*	*	High-Z
Write	L	H	L	A9	A6	A1	A0	H	Din
Block Protect	L	V <sub>ID</sub>	L	V <sub>ID</sub>	L	H	L	H	*
Verify Block Protect	L	L	H	V <sub>ID</sub>	L	H	L	H	Code
Temporary Block Unprotect	*	*	*	*	*	*	*	V <sub>ID</sub>	*
Hardware Reset/Standby	*	*	*	*	*	*	*	L	High-Z

Notes: \* : V<sub>IH</sub> or V<sub>IL</sub>

**ID CODE TABLE**

CODE TYPE		A20 to A13	A6	A1	A0	CODE (HEX)
Manufacturer Code		*	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IL</sub>	98H
Device Code	TC58FVT016	*	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	46H
	TC58FVB016	*	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	C8H
Verify Block Protect		BA <sup>1)</sup>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	Data <sup>2)</sup>

Notes: \* : V<sub>IH</sub> or V<sub>IL</sub>

1) BA: Block Address

2) 01H – Protected Block

00H – Unprotected Block

**COMMAND DEFINITIONS**

COMMAND SEQUENCE	BUS WRITE CYCLES REQ'D	FIRST BUS WRITE CYCLE		SECOND BUS WRITE CYCLE		THIRD BUS WRITE CYCLE		FOURTH BUS READ/WRITE CYCLE		FIFTH BUS WRITE CYCLE		SIXTH BUS WRITE CYCLE	
		Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read/Reset	1	XXXXh	F0H										
Read/Reset	3	555H	AAH	2AAH	55H	555H	F0H	RA <sup>1)</sup>	RD <sup>2)</sup>				
ID Read/Verify Block Protect	3	555H	AAH	2AAH	55H	555H	90H	IA <sup>3)</sup>	ID <sup>4)</sup>				
Auto Program	4	555H	AAH	2AAH	55H	555H	A0H	PA <sup>5)</sup>	PD <sup>6)</sup>				
Auto Chip Erase	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	10H
Auto Block Erase	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	BA <sup>7)</sup>	30H
Block Protect	6	555H	AAH	2AAH	55H	555H	9AH	555H	AAH	2AAH	55H	555H	9AH
Block Erase Suspend		Addr : V <sub>IH</sub> or V <sub>IL</sub> , Data : B0H											
Block Erase Resume		Addr : V <sub>IH</sub> or V <sub>IL</sub> , Data : 30H											

Notes: The system should generate the following address patterns:

1) RA : Read Address

2) RD : Read Data

3) IA : ID Address (A6, A1, A0)

00H = Manufacturer Code

01H = Device Code

02H = Verify Block Protect (A20 to A13 = Block Address)

4) ID : ID Data

98H – Manufacturer Code

46H – Device Code (TC58FVT016)

C8H – Device Code (TC58FVB016)

01H – Protected Block

00H – Unprotected Block

5) PA : Program Address

6) PD : Program Data

7) BA : Block Address

**HARDWARE STATUS FLAGS**

STATUS		DQ7	DQ6	DQ5	DQ3	RDY/ $\overline{\text{BSY}}$
In Progress	Auto Programming	$\overline{\text{DQ7}}$	Toggle	0	0	0
	Auto Erase (Erase Hold Time)	0	Toggle	0	0	0
	Auto Erase	0	Toggle	0	1	0
Time Limits Exceeded	Auto Programming	$\overline{\text{DQ7}}$	Toggle	1	1	0
	Auto Erase	0	Toggle	1	1	0

Notes: 1. DQ outputs cell data and RDY/ $\overline{\text{BSY}}$  outputs 1 when the operation has completed.

2. DQ0, DQ1 and DQ2 pins are reserved for future use.

3. DQ0 to DQ2 and DQ4 : Output 0.

**BLOCK ERASE ADDRESS TABLES**

TC58FVT016 (Top Boot Block)

BLOCK #	A20	A19	A18	A17	A16	A15	A14	A13	ADDRESS RANGE	SIZE
BA0	L	L	L	L	L	*	*	*	000000H - 00FFFFH	64 K bytes
BA1	L	L	L	L	H	*	*	*	010000H - 01FFFFH	64 K bytes
BA2	L	L	L	H	L	*	*	*	020000H - 02FFFFH	64 K bytes
BA3	L	L	L	H	H	*	*	*	030000H - 03FFFFH	64 K bytes
BA4	L	L	H	L	L	*	*	*	040000H - 04FFFFH	64 K bytes
BA5	L	L	H	L	H	*	*	*	050000H - 05FFFFH	64 K bytes
BA6	L	L	H	H	L	*	*	*	060000H - 06FFFFH	64 K bytes
BA7	L	L	H	H	H	*	*	*	070000H - 07FFFFH	64 K bytes
BA8	L	H	L	L	L	*	*	*	080000H - 08FFFFH	64 K bytes
BA9	L	H	L	L	H	*	*	*	090000H - 09FFFFH	64 K bytes
BA10	L	H	L	H	L	*	*	*	0A0000H - 0AFFFFH	64 K bytes
BA11	L	H	L	H	H	*	*	*	0B0000H - 0BFFFFH	64 K bytes
BA12	L	H	H	L	L	*	*	*	0C0000H - 0CFFFFH	64 K bytes
BA13	L	H	H	L	H	*	*	*	0D0000H - 0DFFFFH	64 K bytes
BA14	L	H	H	H	L	*	*	*	0E0000H - 0EFFFFH	64 K bytes
BA15	L	H	H	H	H	*	*	*	0F0000H - 0FFFFFH	64 K bytes
BA16	H	L	L	L	L	*	*	*	100000H - 10FFFFH	64 K bytes
BA17	H	L	L	L	H	*	*	*	110000H - 11FFFFH	64 K bytes
BA18	H	L	L	H	L	*	*	*	120000H - 12FFFFH	64 K bytes
BA19	H	L	L	H	H	*	*	*	130000H - 13FFFFH	64 K bytes
BA20	H	L	H	L	L	*	*	*	140000H - 14FFFFH	64 K bytes
BA21	H	L	H	L	H	*	*	*	150000H - 15FFFFH	64 K bytes
BA22	H	L	H	H	L	*	*	*	160000H - 16FFFFH	64 K bytes
BA23	H	L	H	H	H	*	*	*	170000H - 17FFFFH	64 K bytes
BA24	H	H	L	L	L	*	*	*	180000H - 18FFFFH	64 K bytes
BA25	H	H	L	L	H	*	*	*	190000H - 19FFFFH	64 K bytes
BA26	H	H	L	H	L	*	*	*	1A0000H - 1AFFFFH	64 K bytes
BA27	H	H	L	H	H	*	*	*	1B0000H - 1BFFFFH	64 K bytes
BA28	H	H	H	L	L	*	*	*	1C0000H - 1CFFFFH	64 K bytes
BA29	H	H	H	L	H	*	*	*	1D0000H - 1DFFFFH	64 K bytes
BA30	H	H	H	H	L	*	*	*	1E0000H - 1EFFFFH	64 K bytes
BA31	H	H	H	H	H	L	*	*	1F0000H - 1F7FFFFH	32 K bytes
BA32	H	H	H	H	H	H	L	L	1F8000H - 1F9FFFFH	8 K bytes
BA33	H	H	H	H	H	H	L	H	1FA000H - 1FBFFFFH	8 K bytes
BA34	H	H	H	H	H	H	H	*	1FC000H - 1FFFFFFH	16 K bytes

TC58FVB016 (Bottom Boot Block)

BLOCK #	A20	A19	A18	A17	A16	A15	A14	A13	ADDRESS RANGE	SIZE
BA0	L	L	L	L	L	L	L	*	000000H - 003FFFH	16 K bytes
BA1	L	L	L	L	L	L	H	L	004000H - 005FFFH	8 K bytes
BA2	L	L	L	L	L	L	H	H	006000H - 007FFFH	8 K bytes
BA3	L	L	L	L	L	H	*	*	008000H - 00FFFFH	32 K bytes
BA4	L	L	L	L	H	*	*	*	010000H - 01FFFFH	64 K bytes
BA5	L	L	L	H	L	*	*	*	020000H - 02FFFFH	64 K bytes
BA6	L	L	L	H	H	*	*	*	030000H - 03FFFFH	64 K bytes
BA7	L	L	H	L	L	*	*	*	040000H - 04FFFFH	64 K bytes
BA8	L	L	H	L	H	*	*	*	050000H - 05FFFFH	64 K bytes
BA9	L	L	H	H	L	*	*	*	060000H - 06FFFFH	64 K bytes
BA10	L	L	H	H	H	*	*	*	070000H - 07FFFFH	64 K bytes
BA11	L	H	L	L	L	*	*	*	080000H - 08FFFFH	64 K bytes
BA12	L	H	L	L	H	*	*	*	090000H - 09FFFFH	64 K bytes
BA13	L	H	L	H	L	*	*	*	0A0000H - 0AFFFFH	64 K bytes
BA14	L	H	L	H	H	*	*	*	0B0000H - 0BFFFFH	64 K bytes
BA15	L	H	H	L	L	*	*	*	0C0000H - 0CFFFFH	64 K bytes
BA16	L	H	H	L	H	*	*	*	0D0000H - 0DFFFFH	64 K bytes
BA17	L	H	H	H	L	*	*	*	0E0000H - 0EFFFFH	64 K bytes
BA18	L	H	H	H	H	*	*	*	0F0000H - 0FFFFFH	64 K bytes
BA19	H	L	L	L	L	*	*	*	100000H - 10FFFFH	64 K bytes
BA20	H	L	L	L	H	*	*	*	110000H - 11FFFFH	64 K bytes
BA21	H	L	L	H	L	*	*	*	120000H - 12FFFFH	64 K bytes
BA22	H	L	L	H	H	*	*	*	130000H - 13FFFFH	64 K bytes
BA23	H	L	H	L	L	*	*	*	140000H - 14FFFFH	64 K bytes
BA24	H	L	H	L	H	*	*	*	150000H - 15FFFFH	64 K bytes
BA25	H	L	H	H	L	*	*	*	160000H - 16FFFFH	64 K bytes
BA26	H	L	H	H	H	*	*	*	170000H - 17FFFFH	64 K bytes
BA27	H	H	L	L	L	*	*	*	180000H - 18FFFFH	64 K bytes
BA28	H	H	L	L	H	*	*	*	190000H - 19FFFFH	64 K bytes
BA29	H	H	L	H	L	*	*	*	1A0000H - 1AFFFFH	64 K bytes
BA30	H	H	L	H	H	*	*	*	1B0000H - 1BFFFFH	64 K bytes
BA31	H	H	H	L	L	*	*	*	1C0000H - 1CFFFFH	64 K bytes
BA32	H	H	H	L	H	*	*	*	1D0000H - 1DFFFFH	64 K bytes
BA33	H	H	H	H	L	*	*	*	1E0000H - 1EFFFFH	64 K bytes
BA34	H	H	H	H	H	*	*	*	1F0000H - 1FFFFFH	64 K bytes

**ABSOLUTE MAXIMUM RATINGS**

SYMBOL	PARAMETER	RANGE	UNIT
$V_{DD}$	$V_{DD}$ Supply Voltage	-0.6 to 4.6	V
$V_{IN}$	Input Voltage	-0.6 to $V_{DD} + 0.5$ ( $\leq 4.6$ )	V
$V_{DQ}$	Input / Output Voltage	-0.6 to $V_{DD} + 0.5$ ( $\leq 4.6$ )	V
$P_D$	Power Dissipation	0.6	W
$T_{SOLDER}$	Soldering Temperature (10 s)	260	°C
$T_{STG}$	Storage Temperature	-55 to 150	°C
$T_{OPR}$	Operating Temperature	-40 to 85	°C
$N_{EW}$	Erase / Program Cycling Capability	100,000	Cycles
$V_{IDH}$	Maximum Input Voltage <sup>1)</sup>	13.0	V
$I_{SHORT}$	Output Short Circuit Current <sup>2)</sup>	100	mA

1)  $V_{IDH}$  supply for more than 10 seconds is not recommended. The device could be damaged.

2) Outputs should be shorted for no more than one second.  
No more than one output should be shorted at a time.

**CAPACITANCE** ( $T_a = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ )

SYMBOL	PARAMETER	CONDITION	TYP.	MAX	UNIT
$C_{IN}$	Input Pin Capacitance	$V_{IN} = 0\text{ V}$	4	8	pF
$C_{OUT}$	Output Pin Capacitance	$V_{OUT} = 0\text{ V}$	10	12	pF
$C_{IN2}$	Control Pin Capacitance	$V_{IN} = 0\text{ V}$	8	10	pF

This parameter is periodically sampled and is not tested for every device.

**RECOMMENDED DC OPERATING CONDITIONS** ( $T_a = -40$  to  $85^\circ\text{C}$ )

SYMBOL	PARAMETER	MIN	MAX	UNIT
$V_{DD}$	$V_{DD}$ Supply Voltage	2.7	3.6	V
$V_{IH}$	Input High Level Voltage	$0.7V_{DD}$	$V_{DD} + 0.5$	
$V_{IL}$	Input Low Level Voltage	-0.3 <sup>1)</sup>	0.8	
$V_{ID}$	Voltage for ID Read and Block Protect <sup>2)</sup>	11.4	12.6	

1) -2 V (pulse width of 20 ns Max)

2)  $V_{IDH}$  supply for more than 10 seconds is not recommended. The device could be damaged.

DC CHARACTERISTICS ( $T_a = -40$  to  $85^\circ\text{C}$ ,  $V_{DD} = 2.7$  to  $3.6\text{ V}$ )

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
$I_{LI}$	Input Leakage Current	$0\text{ V} \leq V_{IN} \leq V_{DD}$	–	$\pm 1$	$\mu\text{A}$
$I_{LO}$	Output Leakage Current	$0\text{ V} \leq V_{OUT} \leq V_{DD}$	–	$\pm 1$	
$V_{OH1}$	Output High Voltage (TTL)	$I_{OH} = -0.4\text{ mA}$	2.4	–	V
$V_{OH2}$	Output High Voltage (CMOS)	$I_{OH} = -0.1\text{ mA}$	$V_{DD} - 0.4$	–	
		$I_{OH} = -2.5\text{ mA}$	$0.85 \times V_{DD}$	–	
$V_{OL}$	Output Low Voltage	$I_{OL} = 4.0\text{ mA}$	–	0.4	
$I_{DDO1}$	$V_{DD}$ Average Read Current	$V_{IN} = V_{IH} / V_{IL}$ , $I_{OUT} = 0\text{ mA}$ CYCLE = $t_{RC}$ (min)	–	30	mA
$I_{DDO2}$	$V_{DD}$ Average Program Current	$V_{IN} = V_{IH} / V_{IL}$ , $I_{OUT} = 0\text{ mA}$	–	40	
$I_{DDO3}$	$V_{DD}$ Average Erase Current	$V_{IN} = V_{IH} / V_{IL}$ , $I_{OUT} = 0\text{ mA}$	–	40	
$I_{DDS1}$	$V_{DD}$ Standby Current (TTL)	$\overline{CE} = \overline{RESET} = V_{IH}$ or $\overline{RESET} = V_{IL}$	–	250	$\mu\text{A}$
$I_{DDS2}$	$V_{DD}$ Standby Current (CMOS)	$\overline{CE} = \overline{RESET} = V_{DD} \pm 0.2\text{ V}$ or $\overline{RESET} = V_{SS} \pm 0.2\text{ V}$	–	5	
$I_{ID}$	High Voltage Input Current	$11.4\text{ V} \leq V_{ID} \leq 12.6$ 1)	–	200	
$V_{LKO}$	Low $V_{DD}$ Lock-out Voltage	–	–	2.5	V

1) Less than 10 seconds

AC TEST CONDITIONS

PARAMETER	CONDITION
Input Pulse Level	2.4 V / 0.4 V
Input Pulse Rise and Fall Time (10% to 90%)	5 ns
Timing Measurement Reference Level (Input)	1.5 V / 1.5 V
Timing Measurement Reference Level (Output)	1.5 V / 1.5 V
Output Load	$C_L$ (100 pF) + 1 TTL Gate



**AC CHARACTERISTICS AND OPERATING CONDITIONS**

SYMBOL	PARAMETER	-85		-10		-12		UNIT
		Ta = −40 to 85 °C						
		V <sub>DD</sub> = 3.0 to 3.6 V		V <sub>DD</sub> = 2.7 to 3.6 V				
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>RC</sub>	Read Cycle Time	85	–	100	–	120	–	ns
t <sub>ACC</sub>	Address Access Time	–	85	–	100	–	120	ns
t <sub>CE</sub>	$\overline{\text{CE}}$ Access Time	–	85	–	100	–	120	ns
t <sub>OE</sub>	$\overline{\text{OE}}$ Access Time	–	35	–	40	–	50	ns
t <sub>CEE</sub>	$\overline{\text{CE}}$ to Output Low-Z	0	–	0	–	0	–	ns
t <sub>OEE</sub>	$\overline{\text{OE}}$ to Output Low-Z	0	–	0	–	0	–	ns
t <sub>OEH</sub>	$\overline{\text{OE}}$ Hold Time (Read)	0	–	0	–	0	–	ns
t <sub>OH</sub>	Output Data Hold Time	0	–	0	–	0	–	ns
t <sub>DF1</sub>	$\overline{\text{CE}}$ to Output High-Z	–	30	–	30	–	30	ns
t <sub>DF2</sub>	$\overline{\text{OE}}$ to Output High-Z	–	30	–	30	–	30	ns
t <sub>CMD</sub>	Command Write Cycle Time	85	–	100	–	120	–	ns
t <sub>AS</sub>	Address Setup Time	0	–	0	–	0	–	ns
t <sub>AH</sub>	Address Hold Time	45	–	50	–	50	–	ns
t <sub>DS</sub>	Data Setup Time	45	–	50	–	60	–	ns
t <sub>DH</sub>	Data Hold Time	0	–	0	–	0	–	ns
t <sub>WELH</sub>	$\overline{\text{WE}}$ Low Level Hold Time ( $\overline{\text{WE}}$ Control)	45	–	50	–	50	–	ns
t <sub>WEHH</sub>	$\overline{\text{WE}}$ High Level Hold Time ( $\overline{\text{WE}}$ Control)	20	–	20	–	20	–	ns
t <sub>CES</sub>	$\overline{\text{CE}}$ Setup Time to $\overline{\text{WE}}$ Active ( $\overline{\text{WE}}$ Control)	0	–	0	–	0	–	ns
t <sub>CEH</sub>	$\overline{\text{CE}}$ Hold Time from $\overline{\text{WE}}$ High Level ( $\overline{\text{WE}}$ Control)	0	–	0	–	0	–	ns
t <sub>CELH</sub>	$\overline{\text{CE}}$ Low Level Hold Time ( $\overline{\text{CE}}$ Control)	45	–	50	–	50	–	ns
t <sub>CEHH</sub>	$\overline{\text{CE}}$ High Level Hold Time ( $\overline{\text{CE}}$ Control)	20	–	20	–	20	–	ns
t <sub>WES</sub>	$\overline{\text{WE}}$ Setup Time to $\overline{\text{CE}}$ Active ( $\overline{\text{CE}}$ Control)	0	–	0	–	0	–	ns
t <sub>WEH</sub>	$\overline{\text{WE}}$ Hold Time from High Level ( $\overline{\text{CE}}$ Control)	0	–	0	–	0	–	ns
t <sub>OES</sub>	$\overline{\text{OE}}$ Setup to $\overline{\text{WE}}$ Active	0	–	0	–	0	–	ns
t <sub>OEHP</sub>	$\overline{\text{OE}}$ Hold Time (Toggle / Data Polling)	10	–	10	–	10	–	ns
t <sub>OEHT</sub>	$\overline{\text{OE}}$ High Level Hold Time (Toggle)	20	–	20	–	20	–	ns
t <sub>PPW</sub>	Auto Program Time	16 *	3600	16 *	3600	16 *	3600	μs
t <sub>PCEW</sub>	Auto Chip Erase Time	50 *	–	50 *	–	50 *	–	s
t <sub>PBEW</sub>	Auto Block Erase Time	1.5 *	15	1.5 *	15	1.5 *	15	s
t <sub>VDS</sub>	V <sub>DD</sub> Setup Time	500	–	500	–	500	–	μs
t <sub>BUSY</sub>	Program / Erase Valid to RDY / $\overline{\text{BSY}}$ Delay	35	–	40	–	50	–	ns
t <sub>RP</sub>	$\overline{\text{RESET}}$ Low Level Hold Time	500	–	500	–	500	–	ns
t <sub>READY</sub>	$\overline{\text{RESET}}$ Low Level to Read Mode	–	20	–	20	–	20	μs
t <sub>RB</sub>	RDY / $\overline{\text{BSY}}$ Recovery Time	0	–	0	–	0	–	ns
t <sub>RH</sub>	$\overline{\text{RESET}}$ Recovery Time	500	–	500	–	500	–	ns
t <sub>VPT</sub>	V <sub>ID</sub> Transition Time	4	–	4	–	4	–	μs
t <sub>VPS</sub>	V <sub>ID</sub> Setup Time	4	–	4	–	4	–	μs
t <sub>VPH</sub>	$\overline{\text{OE}}$ Hold Time (Block Protect)	8	–	8	–	8	–	μs
t <sub>PPLH</sub>	$\overline{\text{WE}}$ Low Level Hold Time (Block Protect)	100	–	100	–	100	–	μs
t <sub>PAS</sub>	Protect Address Setup Time	0	–	0	–	0	–	ns
t <sub>PAH</sub>	Protect Address Hold Time	0	–	0	–	0	–	ns
t <sub>CESP</sub>	$\overline{\text{CE}}$ Setup Time (Block Protect)	4	–	4	–	4	–	μs
t <sub>CEHP</sub>	$\overline{\text{CE}}$ Hold Time (Block Protect)	8	–	8	–	8	–	μs
t <sub>SUS</sub>	Suspend Command to Suspend Mode	–	15	–	15	–	15	μs
t <sub>RES</sub>	Resume Command to Erase Mode	–	1	–	1	–	1	μs

\* : Typ.

## OPERATING MODES

### READ MODE

When the device is set to Read mode, it acts as an asynchronous ROM with an access time of 85/100/120 ns. The device is set to Read mode at power-on or when an Auto - Program / Erase operation completes. A software or hardware reset is necessary to return the device to Read mode when an Auto Program / Erase operation fails.

### STANDBY MODE

There are two methods of entering Standby mode: the first involves using both  $\overline{CE}$  and  $\overline{RESET}$  and the second using only  $\overline{RESET}$ .

The first method involves using  $\overline{CE}$  and  $\overline{RESET}$  for mode control. If  $V_{DD} \pm 0.2$  V (CMOS level) is applied to  $\overline{CE}$  and  $\overline{RESET}$  when the device is operating in Read mode, the current is reduced below 5  $\mu$ A. Similarly, if  $V_{IH}$  (TTL level) is applied to  $\overline{CE}$  and  $\overline{RESET}$ , the current is reduced below 250  $\mu$ A. When using  $\overline{CE}$  for control, make sure that the device is operating in Read mode; otherwise, it is not possible to enter Standby mode.

The second method involves using only  $\overline{RESET}$  for mode control. If  $V_{SS} \pm 0.2$  V (CMOS level) is applied to  $\overline{RESET}$  when the device is operating in Read mode, the current is reduced below 5  $\mu$ A. Similarly, if  $V_{IL}$  (TTL level) is applied to  $\overline{RESET}$ , the current is reduced below 250  $\mu$ A. The difference the control method using  $\overline{CE}$  described above, is that if  $V_{IL}$  is applied to  $\overline{RESET}$  when the device is operating in any mode other than Read mode, it enters Standby mode after stopping the operating which is currently being executed. This is a hardware reset and is described later.

In standby mode, DQ is put in high-impedance state.

### COMMAND WRITE

The TC58FVT016/B016 utilizes the JEDEC command control standard for a single power supply E<sup>2</sup>PROM. A command is executed by inputting an address and data into the Command register. The command is entered by a  $\overline{WE}$  Control Write ( $\overline{WE}$  pulse with  $\overline{CE} = V_{IL}$  and  $\overline{OE} = V_{IH}$ ) or a  $\overline{CE}$  Control Write ( $\overline{CE}$  pulse with  $\overline{WE} = V_{IL}$  and  $\overline{OE} = V_{IH}$ ). The address is latched on the falling edge of either  $\overline{WE}$  or  $\overline{CE}$ . The data is latched on the rising edge of either  $\overline{WE}$  or  $\overline{CE}$ . DQ0 to 7 are valid for data input.

A command is when the Reset command is input. The device then enters Read Mode. When an undefined command is input, the Command register is reset and the device enters Read mode.

### RESET (Software Reset)

The device does not enter Read mode automatically when a command such as Auto Program / Erase or ID Read is not correctly executed (for example, if Program or Erase fails). The Reset or Read Command is necessary to return the device to Read mode. The Reset and Read commands must also be used to reset the Command register.

### RESET (Hardware Reset)

A hardware reset is used for aborting Auto mode operations such as Auto Program/Erase and for resetting the operation mode. The device enters Read mode 20  $\mu$ s after a 500-ns Low level input pulse to the  $\overline{RESET}$  pin. Data may be corrupted if the device is reset during an Auto mode operation.

After a hardware reset the device enters Read mode when  $\overline{\text{RESET}} = V_{\text{IH}}$  and Standby mode when  $\overline{\text{RESET}} = V_{\text{IL}}$ . The DQ pins are High-Impedance when  $\overline{\text{RESET}} = V_{\text{IL}}$ . The Read operation sequence and input of any command are allowed after the device enters Read mode.

### ID READ MODE

The ID Read mode is used to establish the device type. The ID Read mode is set either from the Command mode by inputting a 90H command or from the EPROM mode by applying  $V_{\text{ID}}$  to the A9 pin.

When A0, A1 and A6 =  $V_{\text{IL}}$ , the data that is read is the manufacturer code (98H). When A0 =  $V_{\text{IH}}$  and A1 and A6 =  $V_{\text{IL}}$ , the data that is read is the device code (TC58FVT016 : 46H / TC58FVB016 : C8H). The access time for an ID Read is the same as that of a normal Read operation.

### AUTO PROGRAM MODE

The TC58FVT016/B016 can be programmed in byte units. The Auto Program mode is set using the Program command. The program address is latched on the falling edge of the  $\overline{\text{WE}}$  signal and data is latched on the rising edge of the fourth bus cycle. Auto programming starts on the rising edge of the  $\overline{\text{WE}}$  signal in the fourth bus cycle. The Program and Program Verify commands are automatically executed by the chip. The device status during programming is determined from the Hardware Sequence flag.

Programming of a protected block is ignored. The device enters Read mode 3  $\mu\text{s}$  after the rising edge of the  $\overline{\text{WE}}$  signal in the fourth bus cycle.

The device allows the programming of memory cells from 1 to 0. The programming of Memory cells from 0 to 1 will fail. A cell must be erased to turn it from 0 to 1.

If an Auto Program operation fails, the device remains in programming state and does not automatically return to Read mode. The device status can be determined from the setting of the Hardware Sequence flag. Either a Reset command or a hardware reset is necessary to return the device to Read mode after a failure.

If a programming operation fails, please do not try to use the block which contains the address to which data could not be programmed.

### Auto Chip Erase Mode

The Auto Chip Erase mode is set using the Chip Erase command. The Auto Chip Erase operation starts on the rising edge of  $\overline{\text{WE}}$  in the sixth bus cycle. All memory cells are automatically preprogrammed to 0, erased and verified as erased by the chip. The device status is determined from the Hardware Sequence flag.

Command inputs are ignored during an Auto Chip Erase. The hardware reset allows interruption of an Auto Chip Erase operation. The Auto Chip Erase operation does not complete correctly when interrupted. Hence a further Erase operation is necessary.

An attempt to erase a protected block is ignored. If all blocks are protected, the Auto Erase operation will not be executed and the device will enter Read mode 100  $\mu\text{s}$  after the rising edge of the  $\overline{\text{WE}}$  signal in the sixth bus cycle.

If an Auto Chip Erase operation fails, the device remains in, erasing state and does not return to Read mode. The device status is determined from the Hardware Sequence flag. Either a Reset command or a hardware reset is necessary to return the device to Read mode after a failure.

### Auto Block / Multi Block Erase Mode

The Auto Block and Multi Block Erase modes are set using the Block Erase command. The block address is latched on the falling edge of the  $\overline{WE}$  signal in the sixth bus cycle. The Block Erase starts as soon as the hold time has elapsed after the rising edge of the  $\overline{WE}$  signal. All memory cells in the selected block are automatically programmed to 0, erased and verified as erased by the chip. The Multi Block Erase operation allows erasing of multiple blocks. Any additional block addresses or Multi Block Erase commands must be input within the Erase Hold Time - that is, within 50  $\mu s$  of any  $\overline{WE}$  signal rising edge. The device status can be determined from the setting of the Hardware Sequence flag.

Commands (except Erase Suspend) are ignored during a Block/Multi Block Erase operation. The operation can be aborted by a hardware reset. The Auto Erase operation does not complete correctly when aborted, therefore, a further Erase operation is necessary.

An attempt to erase a protected block is ignored. If all the selected blocks are protected, the Auto Erase operation is not executed and the device returns to Read mode 100  $\mu s$  after the rising edge of the  $\overline{WE}$  signal in the last bus cycle.

If an Auto Erase operation fails, the device remains in erasing state and does not return to Read mode. The device status is determined from the Hardware Sequence flag. Either a Reset command or a hardware reset is necessary to return the device to Read mode after a failure.

### Erase Suspend / Resume Mode

The Erase Suspend mode is used to read data from a block not selected for erasing. The Erase Suspend command is allowed during a Block Erase operation or during the Block Erase Hold Time; it is ignored in other operation modes. A Block Erase operation is also suspended if the Suspend command is input during the Block Erase Hold Time. The device is reset if any command other than Suspend is input. The suspended device recognizes only Read and Resume commands.

The device enters Suspend mode 15  $\mu s$  after the Erase Suspend command is input. The device then enters a pseudo-Read Mode. Data can be read out from an unselected block but is invalid if the address is set to a block selected for erasing. The device status can be determined from the Hardware Sequence flag. DQ6 (the toggle bit) stops toggling and RDY/ $\overline{BSY}$  outputs 1 once the device is set to pseudo-Read mode. The host processor must track the current device mode since there is no way of telling whether the device is in pseudo-or ordinary Read mode. The device remains in pseudo-Read mode even if a Suspend command is input.

The device restarts the Block Erase operation after receiving a Resume command. The device returns to the status in which the Suspend command was input. The DQ6 output toggles and RDY/ $\overline{BSY}$  outputs a 0.

### **BLOCK PROTECT**

The TC58FVT016/B016 has a block protection feature to prevent programming and erasing of protected blocks. Block protection is enabled by either hardware protection (1) or a software command mode (2). The initial device is shipped with all blocks unprotected.

- (1) A block is protected when:  $A9 = \overline{OE} = V_{ID}$ ,  $\overline{CE} = V_{IL}$ ,  $A0 / A6 = V_{IL}$ ,  $A1 = V_{IH}$ ; the block address is set using A13 to A20. The block protect data is programmed within  $t_{PPLH}$  of the  $\overline{WE}$  signal going Low.
- (2) A block can also be protected using a software command. Block protection is executed by setting the  $\overline{WE}$  signal to Low for  $t_{PPLH}$  while  $\overline{CE} = V_{IL}$ . After the command input in the sixth bus cycle A13 to A20 = the block address. Block protection can be verified using the Verify Block Protect command.

### **TEMPORARY BLOCK UNPROTECTION**

The TC58FVT016/B016 has a temporary block unprotection feature which disables block protection for all protected blocks. Unprotection is enabled by applying  $V_{ID}$  to the  $\overline{RESET}$  pin. In this state any block can be programmed or erased. The device returns to the previous condition after  $V_{ID}$  is removed from the  $\overline{RESET}$  pin. That is, previously protected blocks are protected again.

### **VERIFY BLOCK PROTECT**

The Verify Block Protect command is used to check whether a block is protected or unprotected. Verify Block Protect is enabled either through hardware (1) or by a software command (2). In Word mode 01H is output when the block is protected and 00H is output when it is unprotected. .

- (1) Verify Block Protection is enabled when:  $A9 = V_{ID}$ , A0 and A6 =  $V_{IL}$  and A1 =  $V_{IH}$ .  
A13 to A20 = the block address.
- (2) Verify Block Protection can also be enabled using a software command.

### HARDWARE SEQUENCE FLAG

The TC58FVT016/B016 has a Hardware Sequence flag which allows the device status to be determined during Auto operation. The output data is read out with the same timing as Read mode at  $\overline{CE} = \overline{OE} = V_{IL}$ . RDY/BSY outputs either High or Low.

The device re-enters the Read mode automatically after Auto operation has completed successfully. The device status is read out from the Hardware Sequence flag and the operation result is verified by comparing the read-out data to the original data.

### DQ7 ( $\overline{DATA}$ Polling)

The device status can be determined using the data polling function during an Auto Program or Auto Erase operation.  $\overline{DATA}$  polling begins on the rising edge of  $\overline{WE}$  in the last bus cycle. In an Auto Program operation, DQ7 outputs inverted data during the programming operation and outputs real data after programming has finished. In an Auto Erase operation, DQ7 outputs 0 during the Erase operation and outputs 1 when the Erase operation has finished. If an Auto Program or Auto Erase operation fails, DQ7 simply outputs the data.

The latched address is reset after an operation has finished. The polling data is asynchronous with the  $\overline{OE}$  signal.

### DQ6 (Toggle Bit)

The device status can be determined by the Toggle Bit function during an Auto Program or Auto Erase operation. The Toggle bit begins toggling on the rising edge of  $\overline{WE}$  in the last bus cycle. DQ6 alternately outputs a 0 or a 1 for each attempt ( $\overline{OE}$  access) while  $\overline{CE} = V_{IL}$  while the device is busy. When the internal operation has been completed, toggling stops and valid memory cell data can be read by subsequent reading. If the operation failed, the DQ6 output toggles.

DQ6 toggles for around 3  $\mu s$  when an attempt is made to execute an Auto Program operation on a protected block. It then stops toggling. DQ6 toggles for around 100  $\mu s$  when an attempt is made to execute an Auto Erase operation on a protected block. It then stops toggling. After toggling stops the device returns to Read mode.

### DQ5 (Internal Time-out)

DQ5 outputs a 1 when the Internal Timer has timed out during a Program or Erase operation. This indicates that the operation has not completed within the allotted time.

An attempt to program 1 into a cell containing 0 will fail (see Auto Program mode). DQ5 outputs 1 in this case. Either a hardware reset or a software Reset command is required to put the device into Read mode.

### DQ3 (Block Erase Timer)

The Block Erase operation starts 50  $\mu$ s (Erase Hold Time) after the rising edge of  $\overline{WE}$  in the last command cycle. DQ3 outputs a 0 during the Block Erase Hold Time and a 1 when the Erase operation starts. Additional Block Erase commands can only be accepted during this Block Erase Hold Time. Each Block Erase command received within this hold time resets the timer, allowing additional blocks to be marked for erasing. DQ3 outputs a 1 if the Program or Erase operation fails.

### RDY/ $\overline{BSY}$ (READY/ $\overline{BUSY}$ )

TC58FVT016/B016 has a RDY/ $\overline{BSY}$  signal to indicate the device status to the host processor. A 0 (Busy state) indicates that an Auto Program or Auto Erase operation is in progress. A 1 (Ready state) indicates that the operation has finished and that the device can accept a new command. The RDY/ $\overline{BSY}$  signal outputs a 0 when an operation has failed.

The RDY/ $\overline{BSY}$  signal outputs a 0 after the rising edge of  $\overline{WE}$  in the last command cycle.

During an Auto Block Erase operation, commands other than Erase Suspend are ignored. The RDY/ $\overline{BSY}$  signal outputs a 1 during an Erase Suspend operation. The output buffer for the RDY/ $\overline{BSY}$  pin is an open drain type circuit, allowing a wired-OR connection. A pull-up resistor needs to be inserted between  $V_{DD}$  and the RDY/ $\overline{BSY}$  pin.

## DATA PROTECTION

The TC58FVT016/B016 utilizes a JEDEC standard command sequence which protects data against accidental alteration due to noise.

### $V_{DD}$ Lock-out Voltage

The device is reset when  $V_{DD}$  is less than  $V_{LKO}$  to protect memory cell data against  $V_{DD}$  noise, and during power-up and power-down. An Auto Program or Erase operation stops when  $V_{DD}$  drops below  $V_{LKO}$ . An Erase Suspend operation is reset and an Erase operation stops if the device is in Suspend mode. An operation will not complete correctly if it is interrupted by  $V_{DD}$  Lock-out.

### $\overline{WE}$ Glitch Pulses

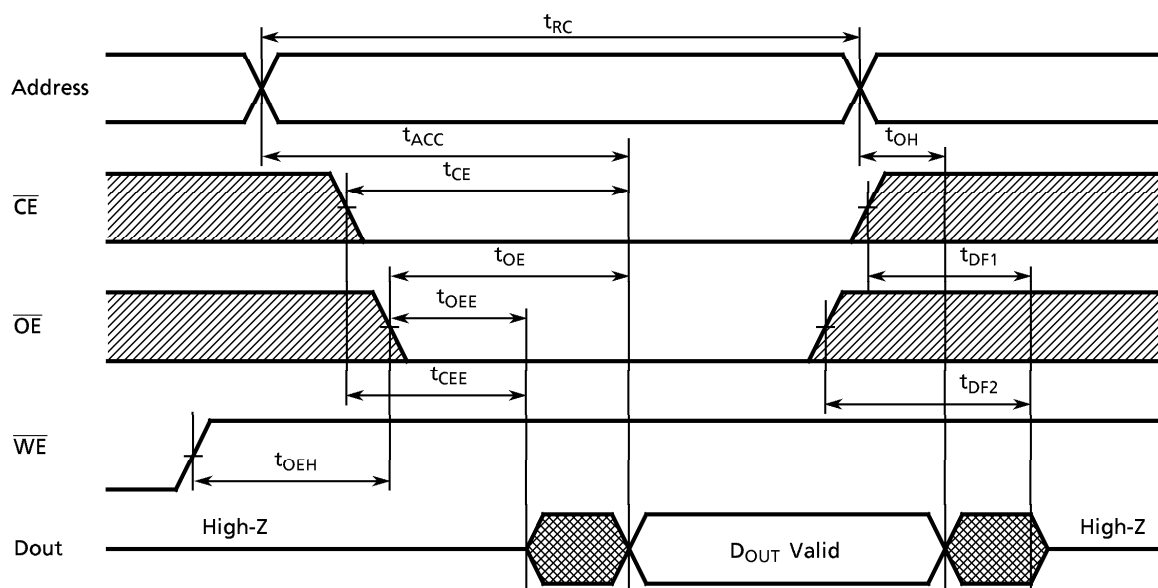
Glitches must be suppressed (to less than 5 ns) in order for operation to proceed smoothly.

### Protection at Power-on

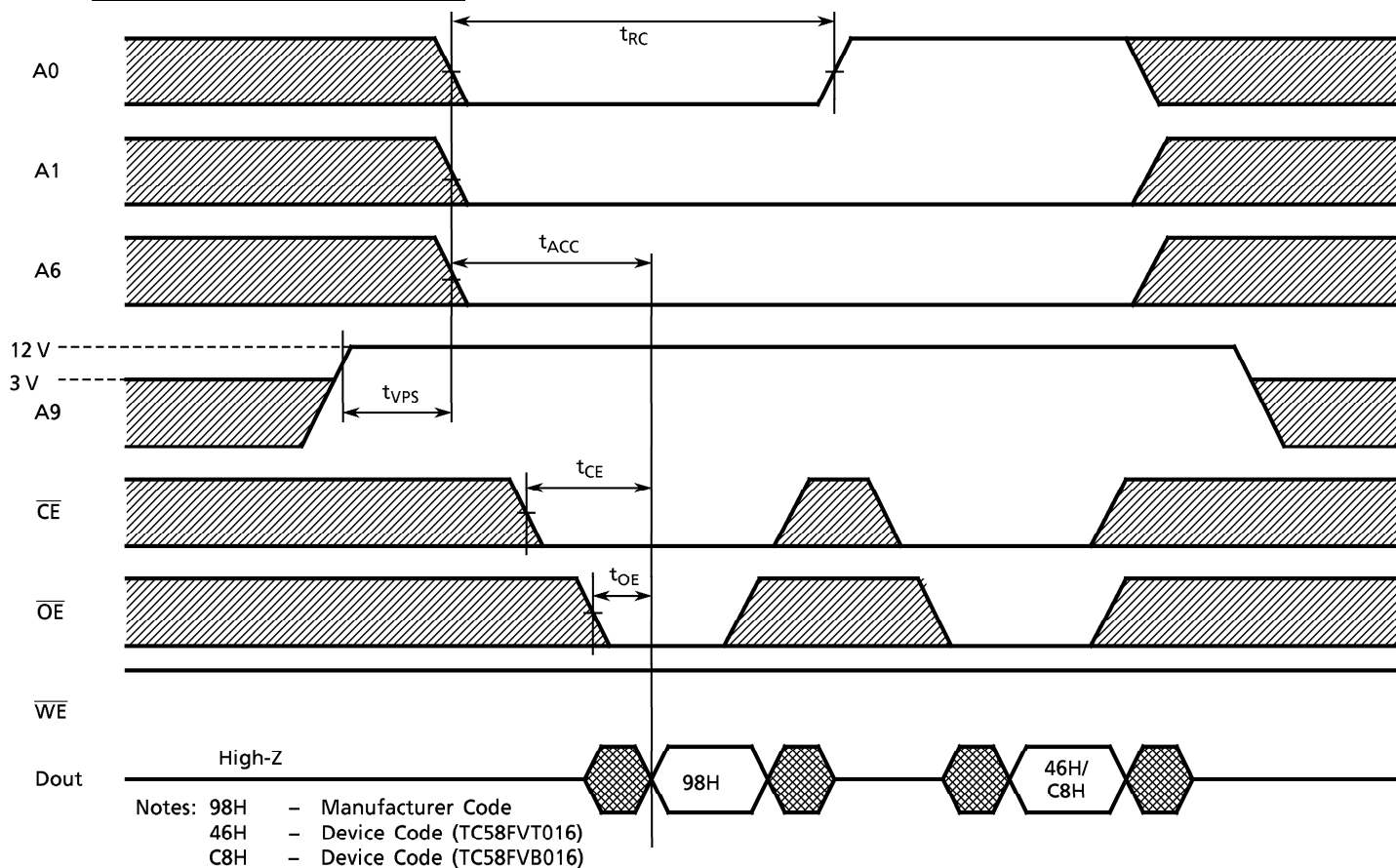
A command is not recognized on the rising edge of  $\overline{WE}$  if  $V_{DD}$  rises from 0 V to the operating voltage while  $\overline{WE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$  and  $\overline{OE} = V_{IH}$ . In this case the device is reset and enters Read mode.

## TIMING DIAGRAMS

### Read / ID Read Operation

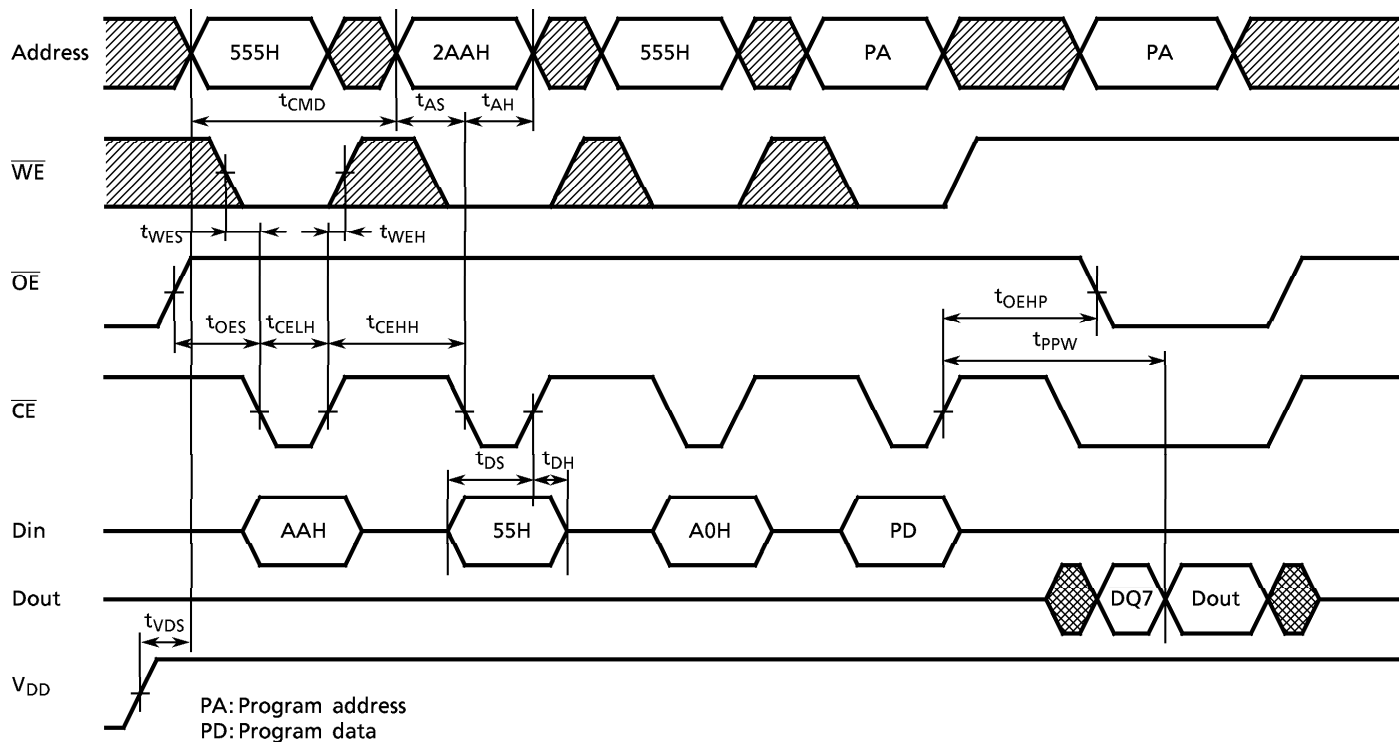


### ID Read Operation (Hardware)

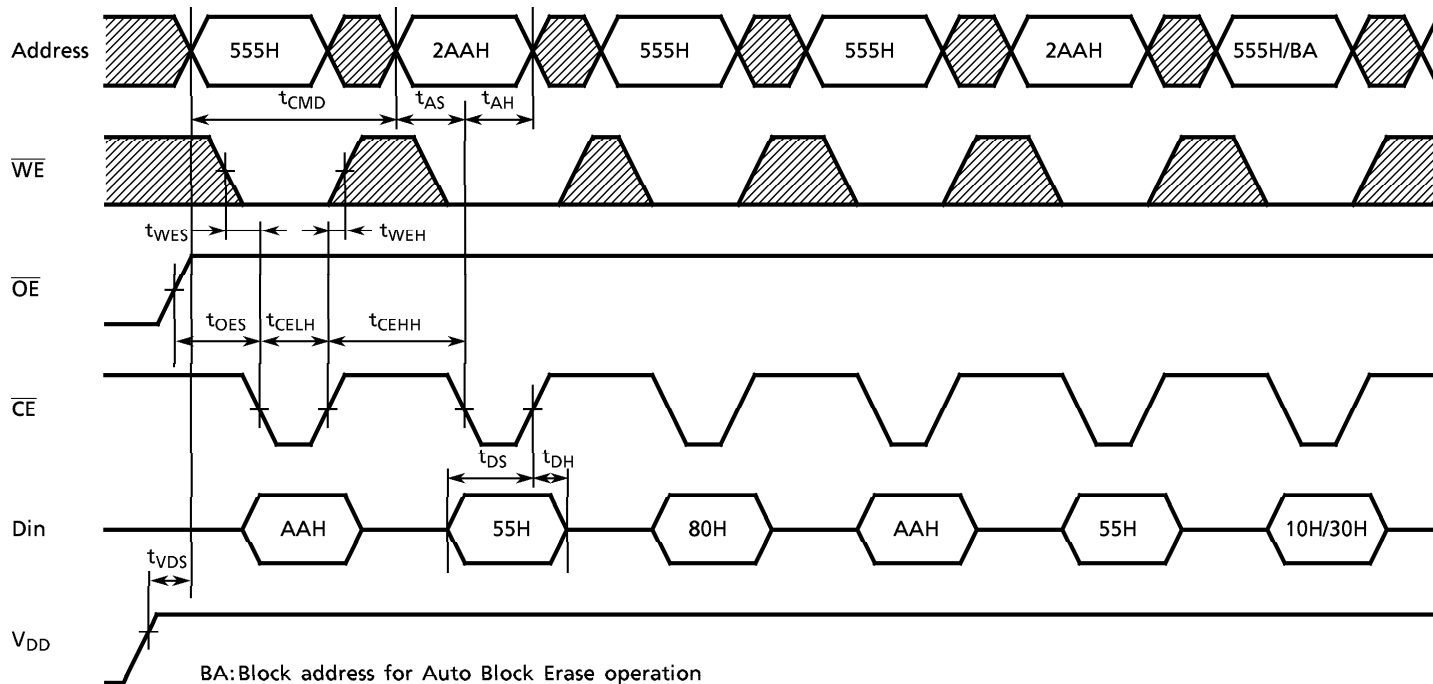




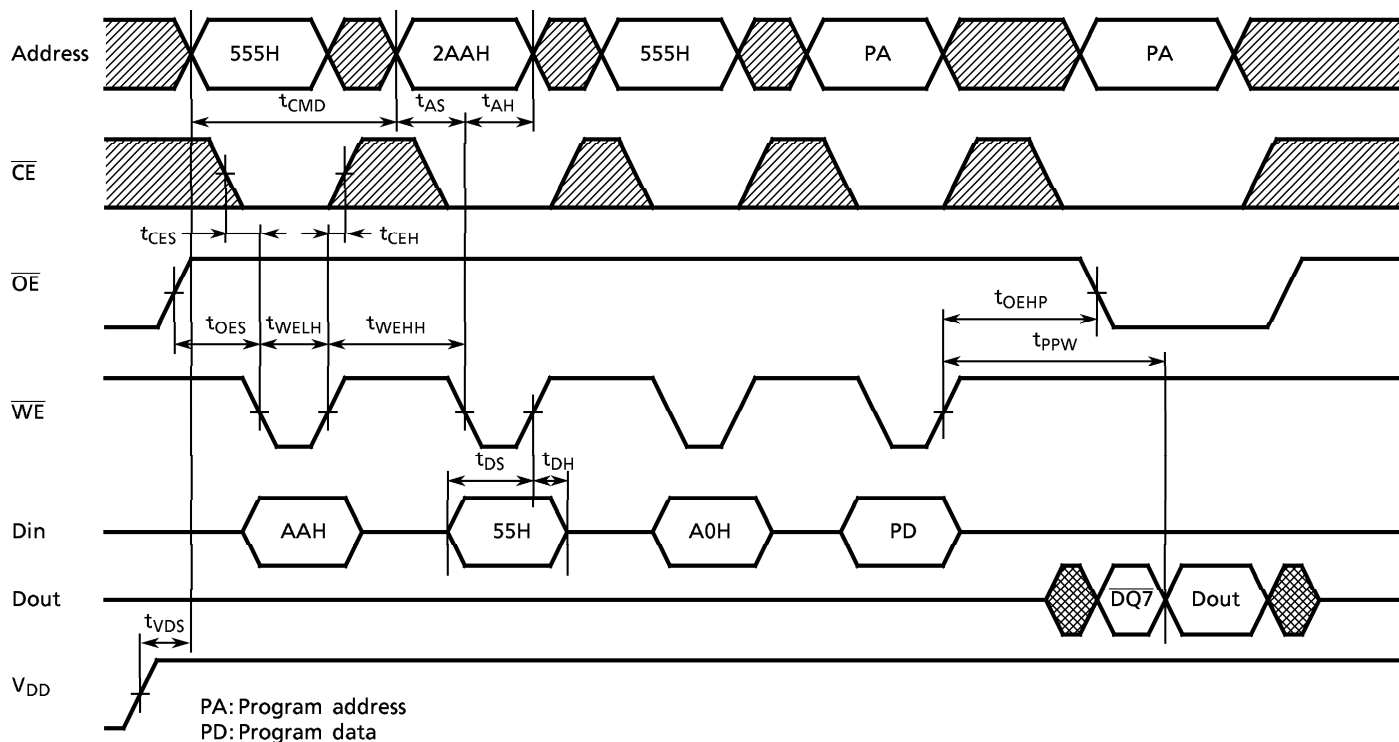
Auto Program Operation ( $\overline{CE}$  Control)



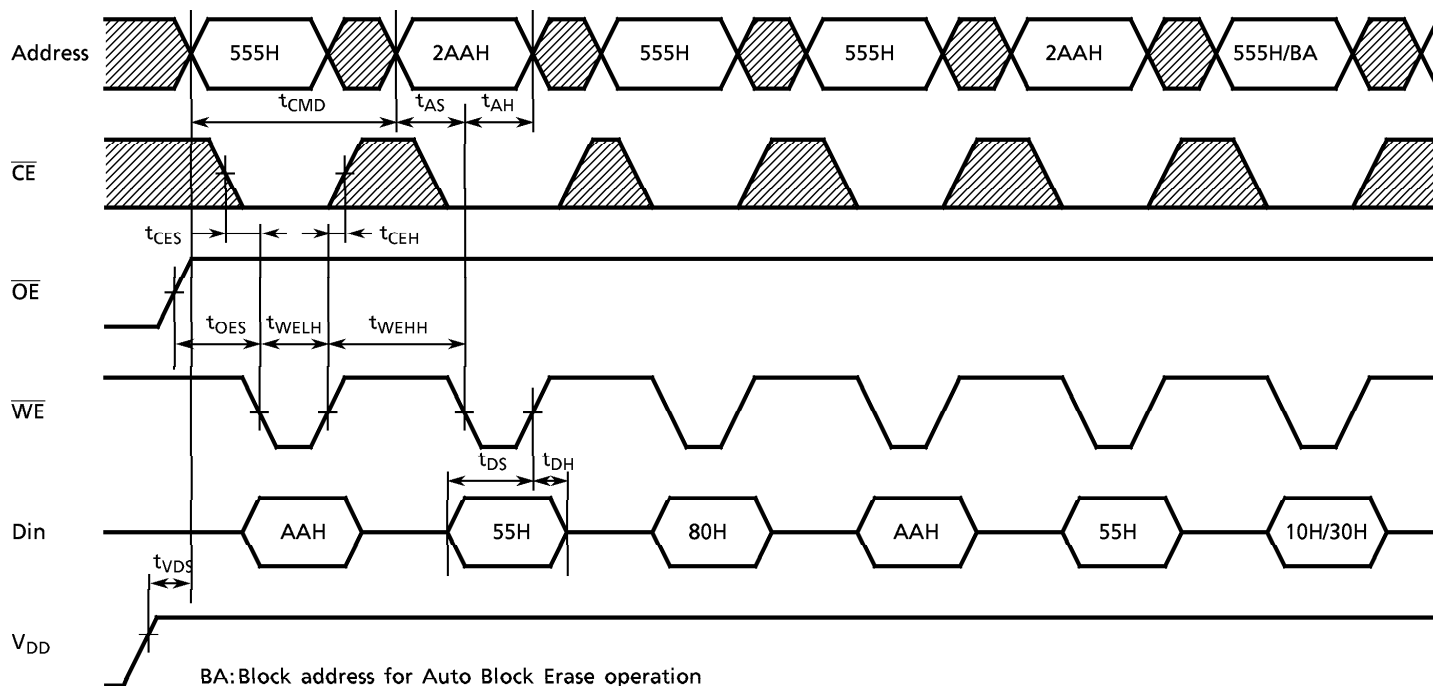
Auto Chip Erase / Auto Block Erase Operation ( $\overline{CE}$  Control)



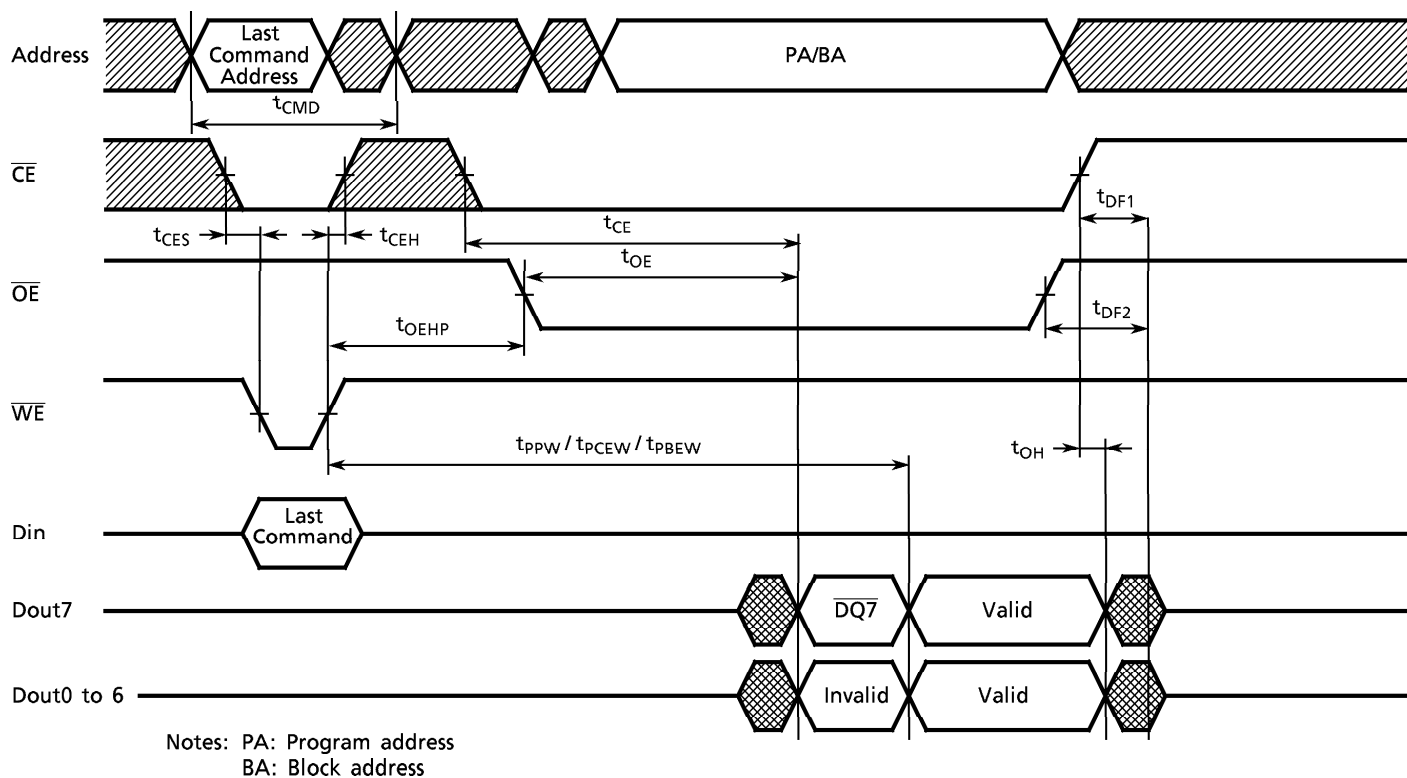
Auto Program Operation ( $\overline{WE}$  Control)



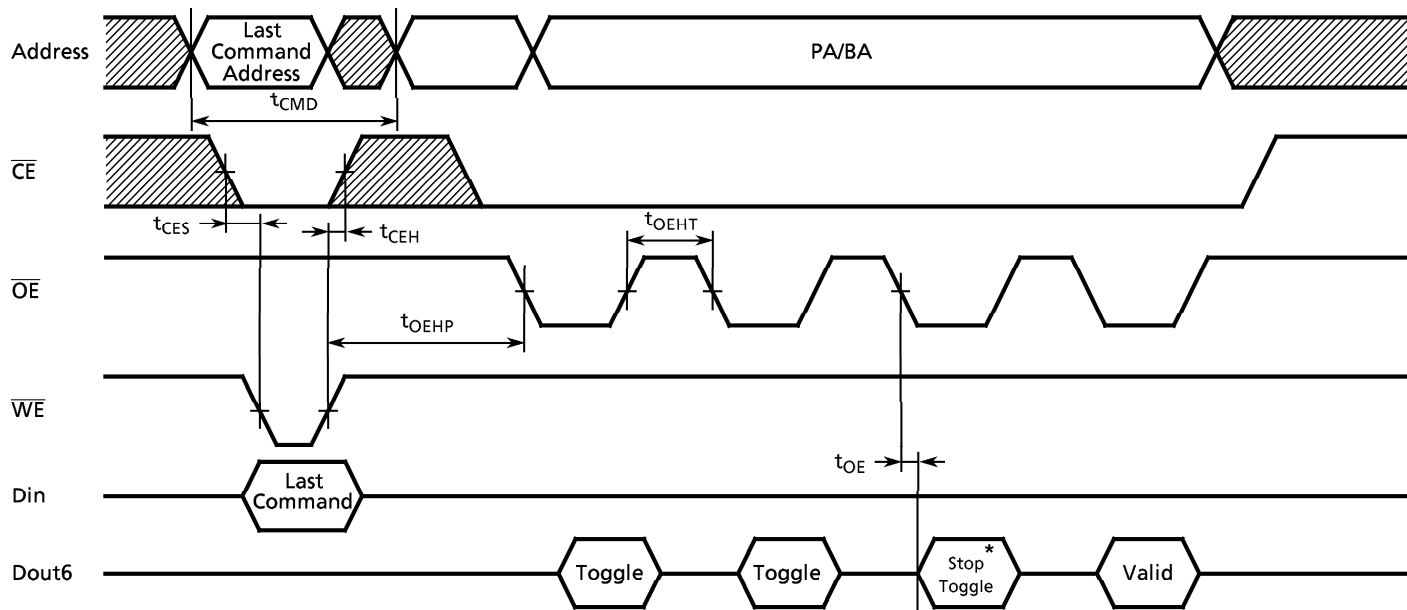
Auto Chip Erase / Auto Block Erase Operation ( $\overline{CE}$  Control)



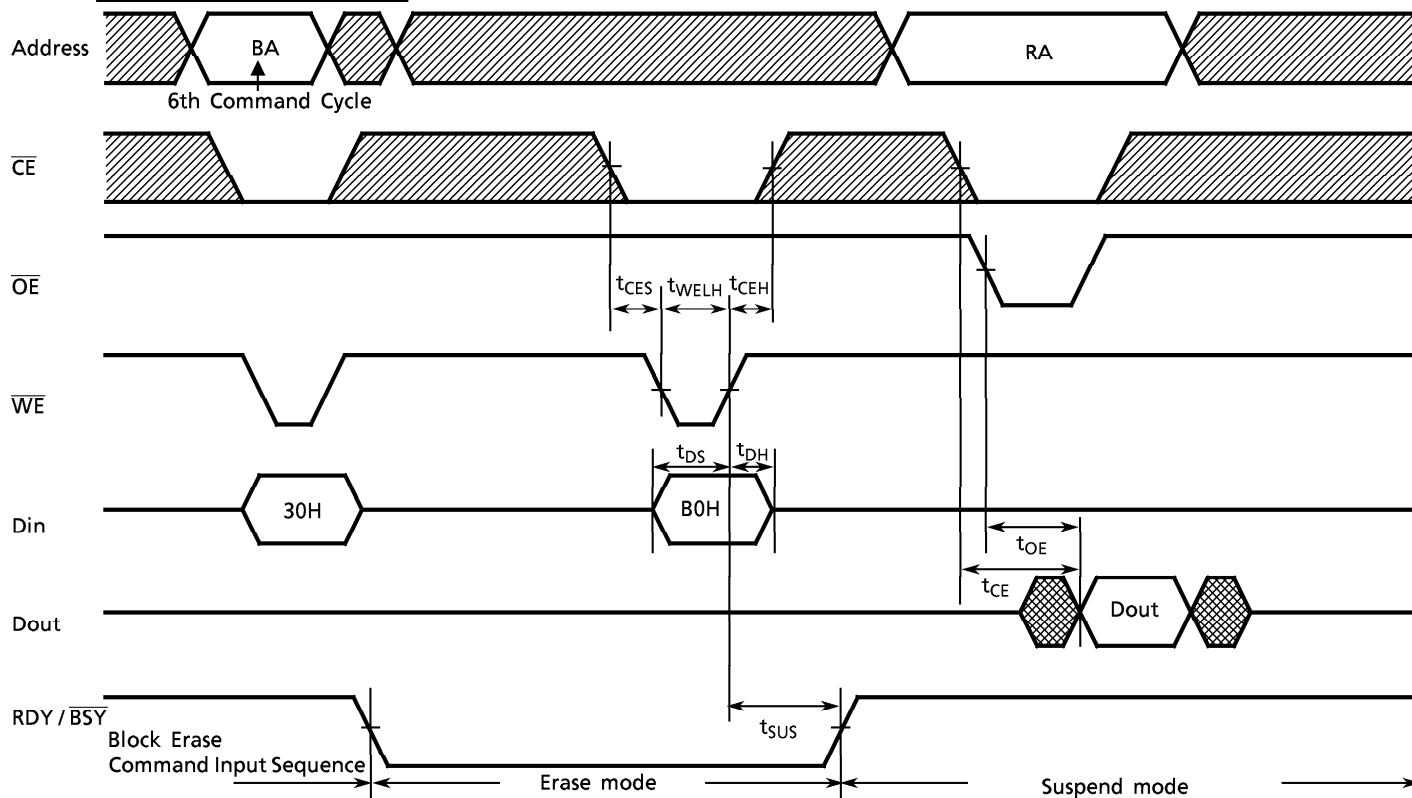
DATA Polling during Program/Erase Operation



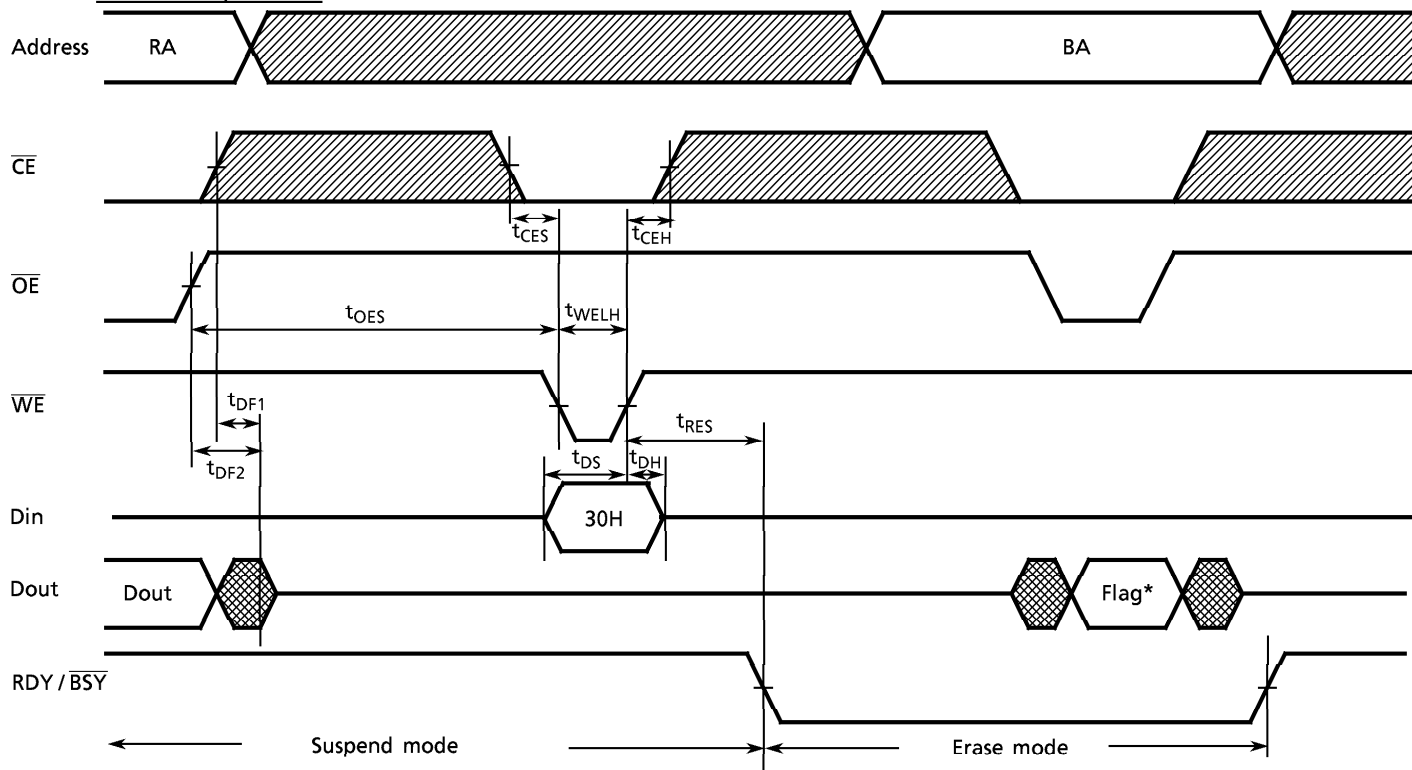
Toggle Bit during Program/Erase Operation



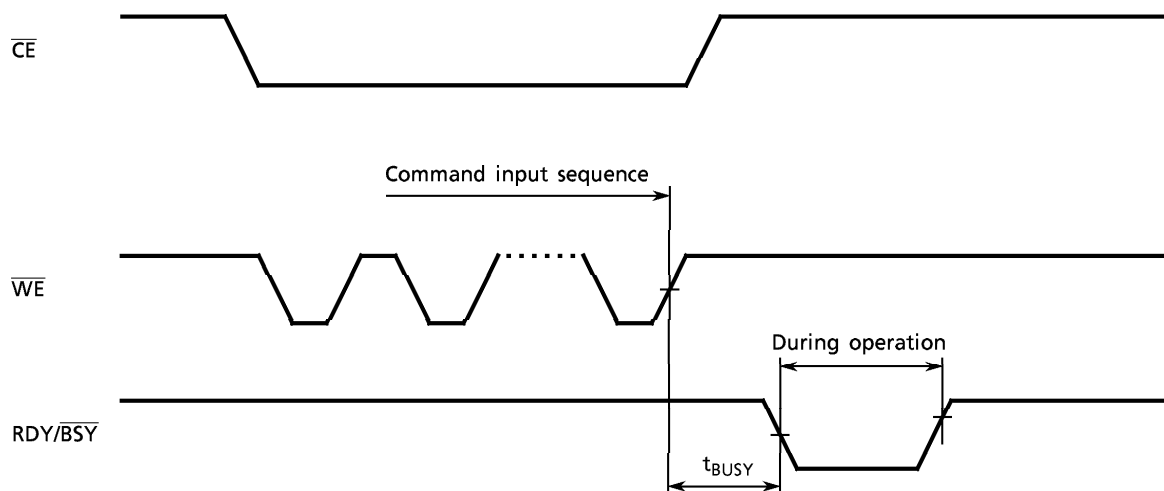
## Erase Suspend Operation



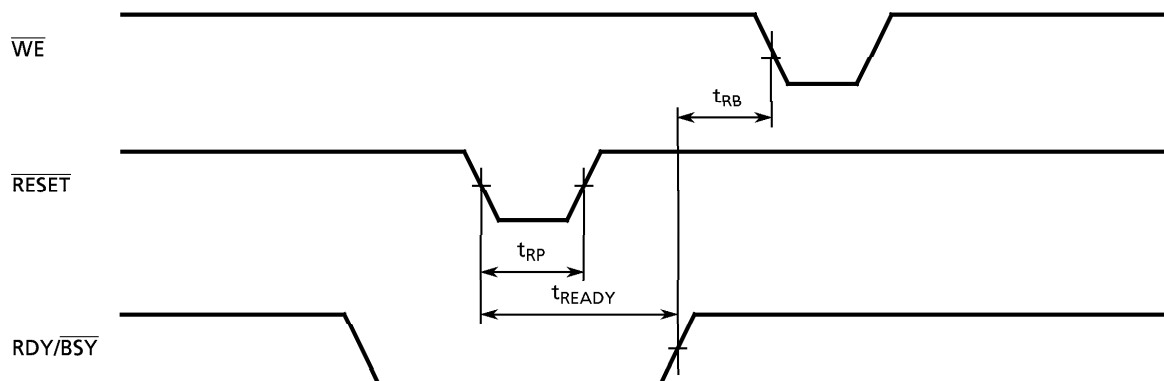
## Resume Operation



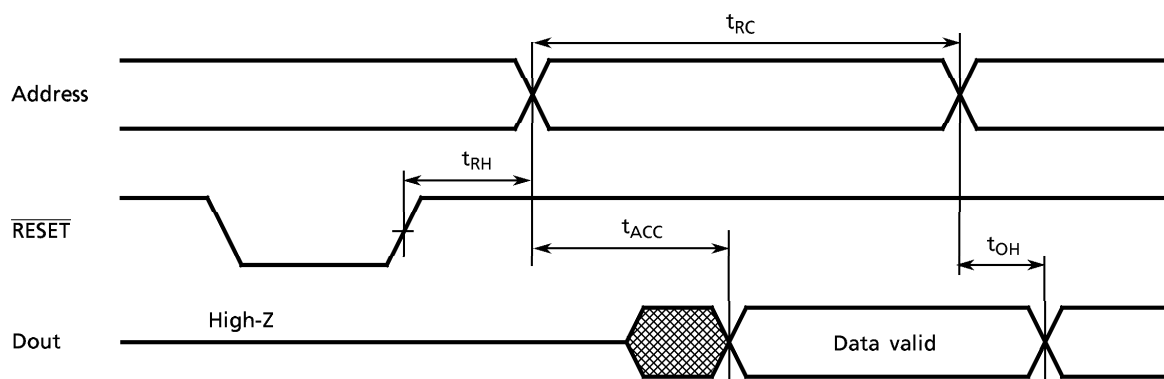
RDY/BSY during Auto Program/Erase Operation



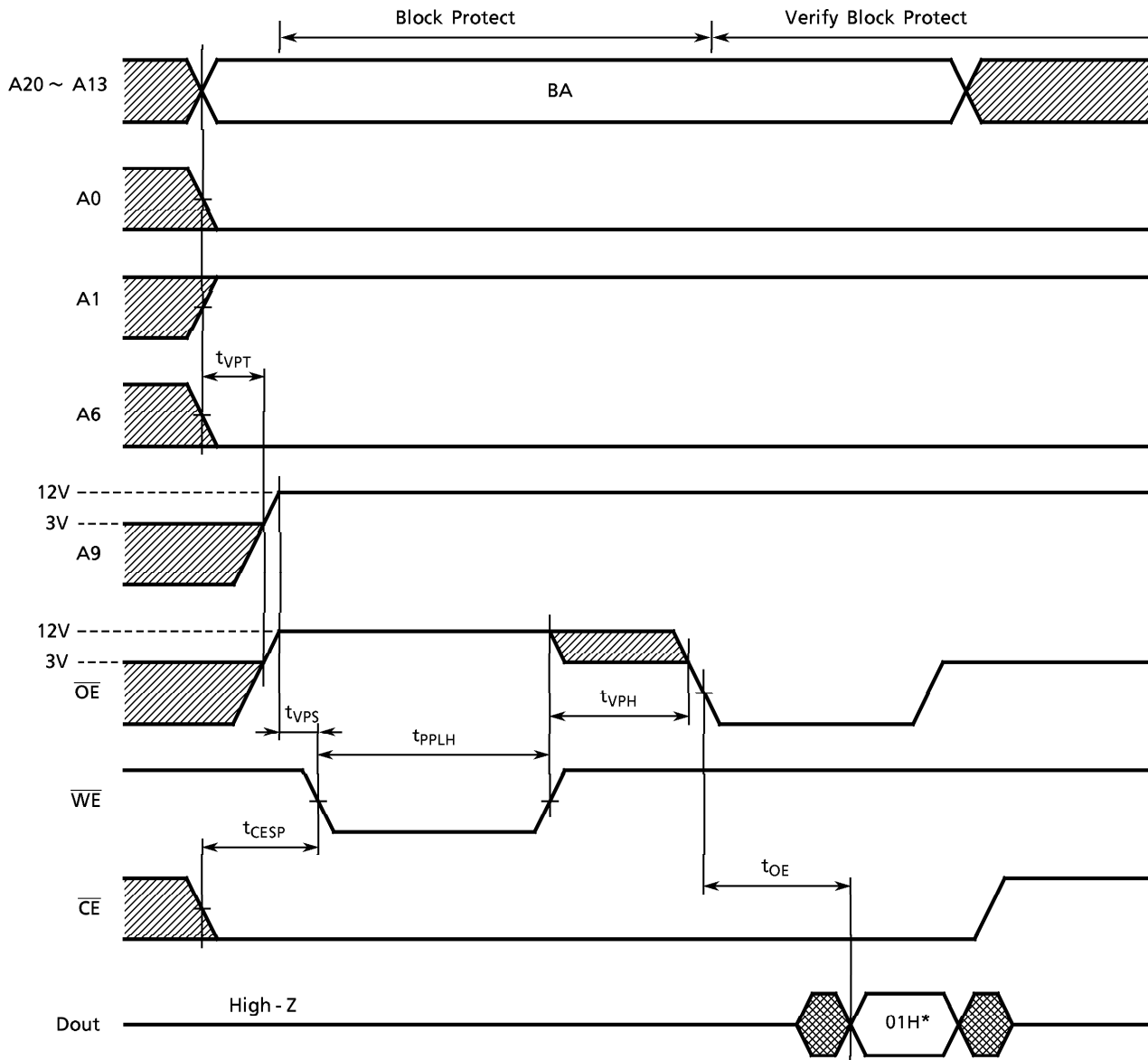
Hardware Reset Operation



Read after RESET



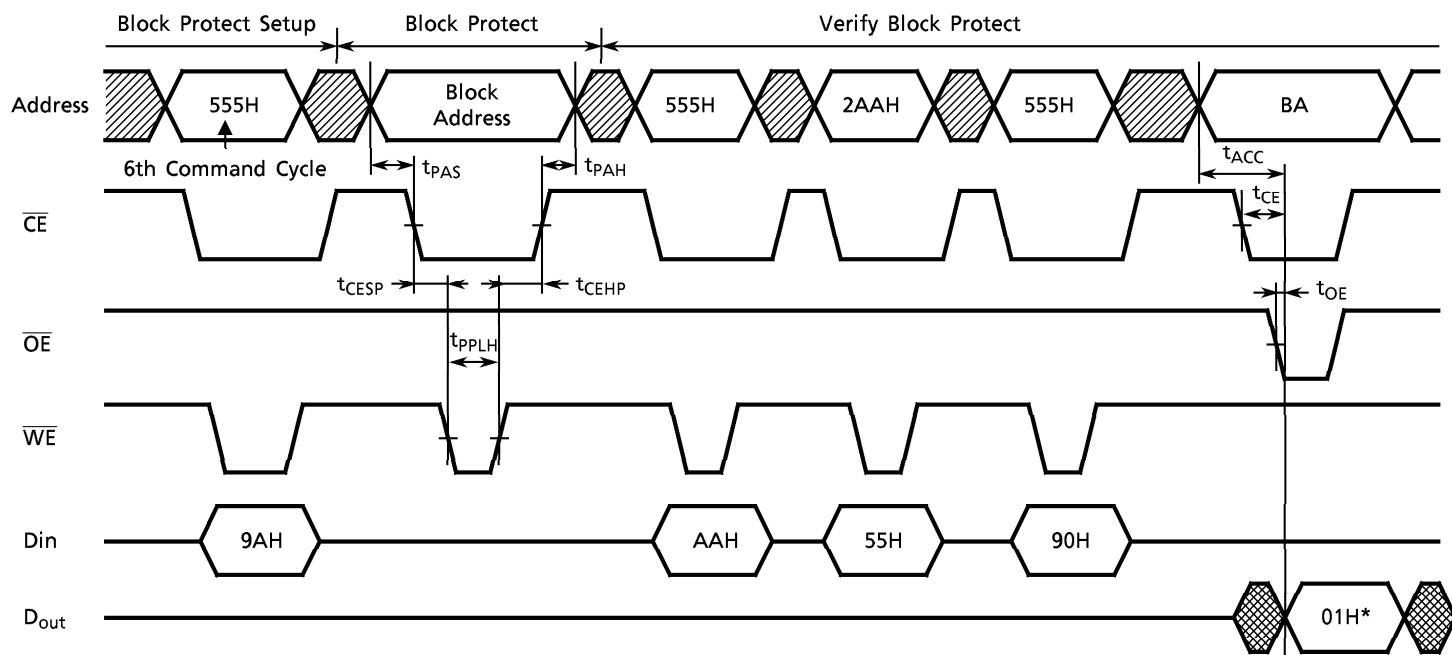
Block Protect Operation (Hardware)



BA : Block address

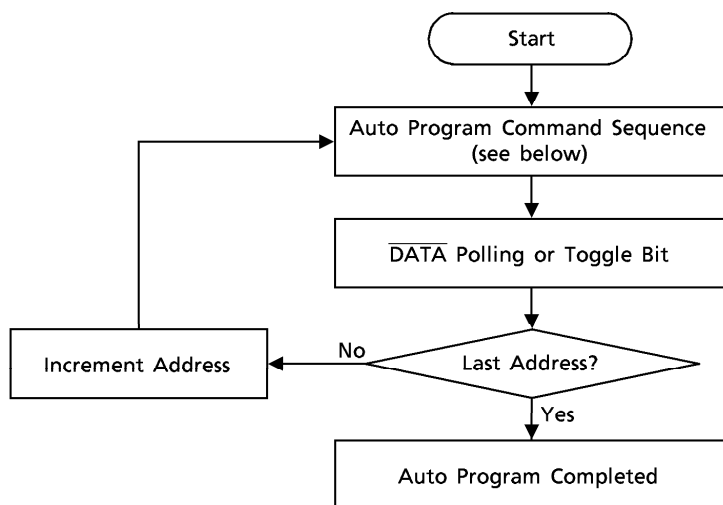
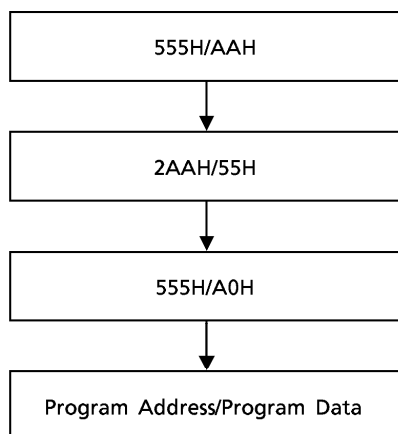
\* : 01H indicates that block protected.

Block Protect (Software)



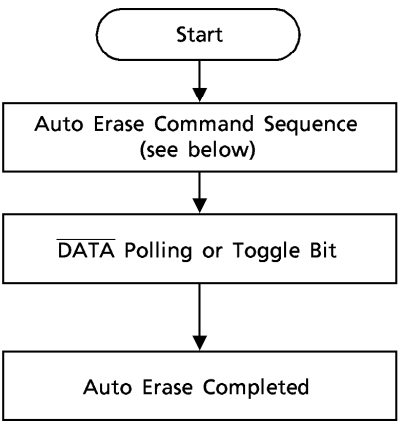
BA : Block address

\* : 0001H indicates that block is protected.

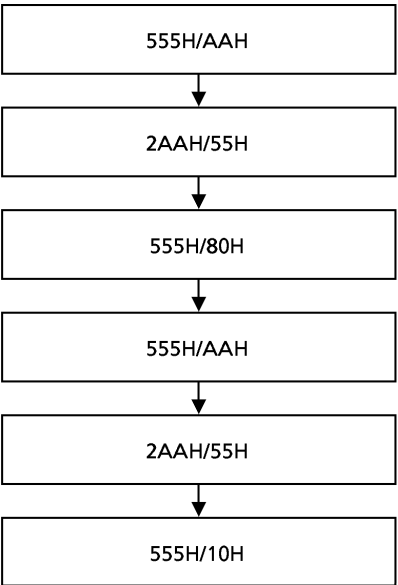
**FLOWCHARTS**
**Auto Program**

**Auto Program Command Sequence (Address/Command)**




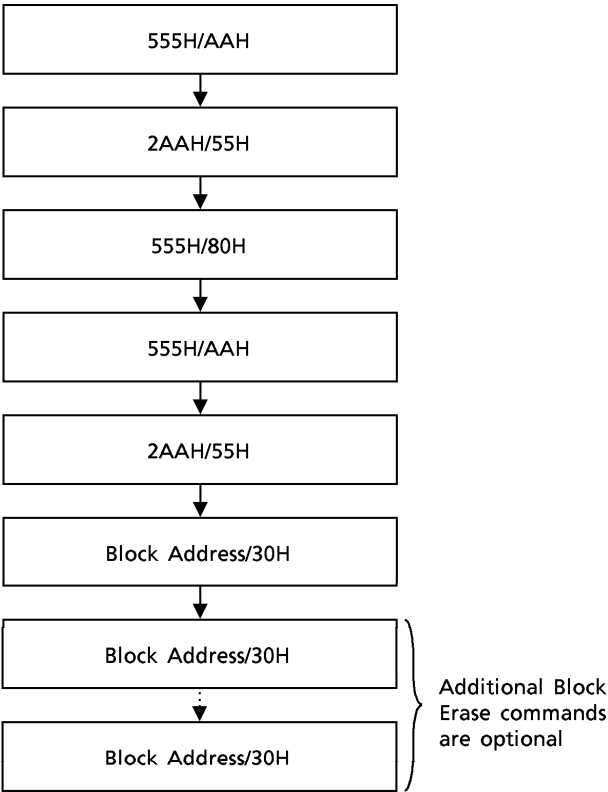
Auto Erase



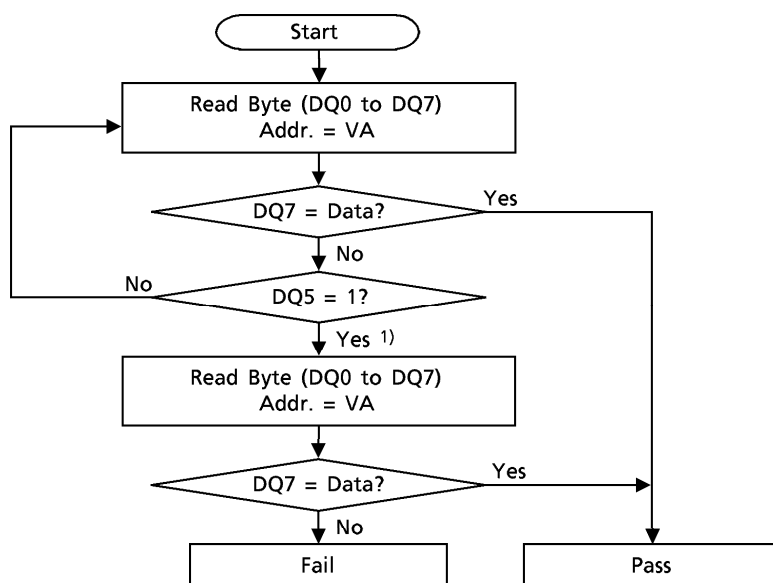
Auto Chip Erase Command Sequence  
(Address/Command)



Auto Block/Multiple Block  
Erase Command Sequence (Address/Command)



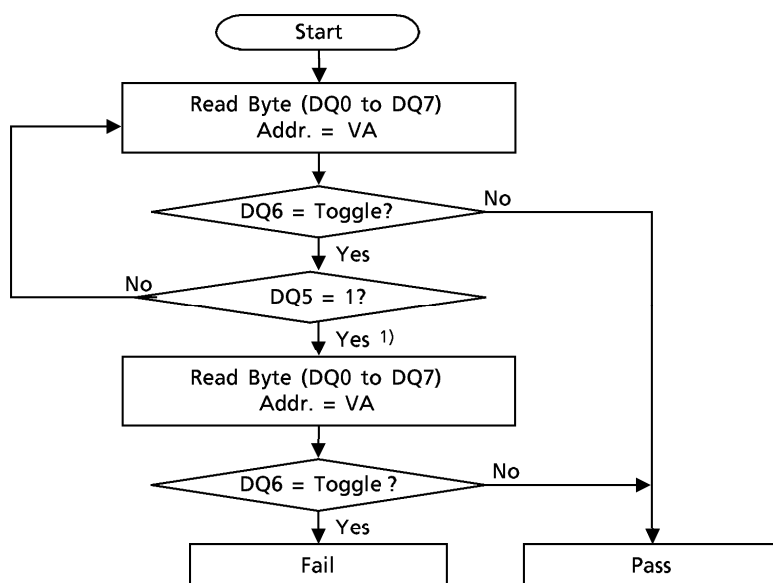
### DQ7 DATA Polling



VA: Byte address for programming.  
Any of the addresses within the block being erased during a Block Erase operation.  
Don't care during a Chip Erase operation

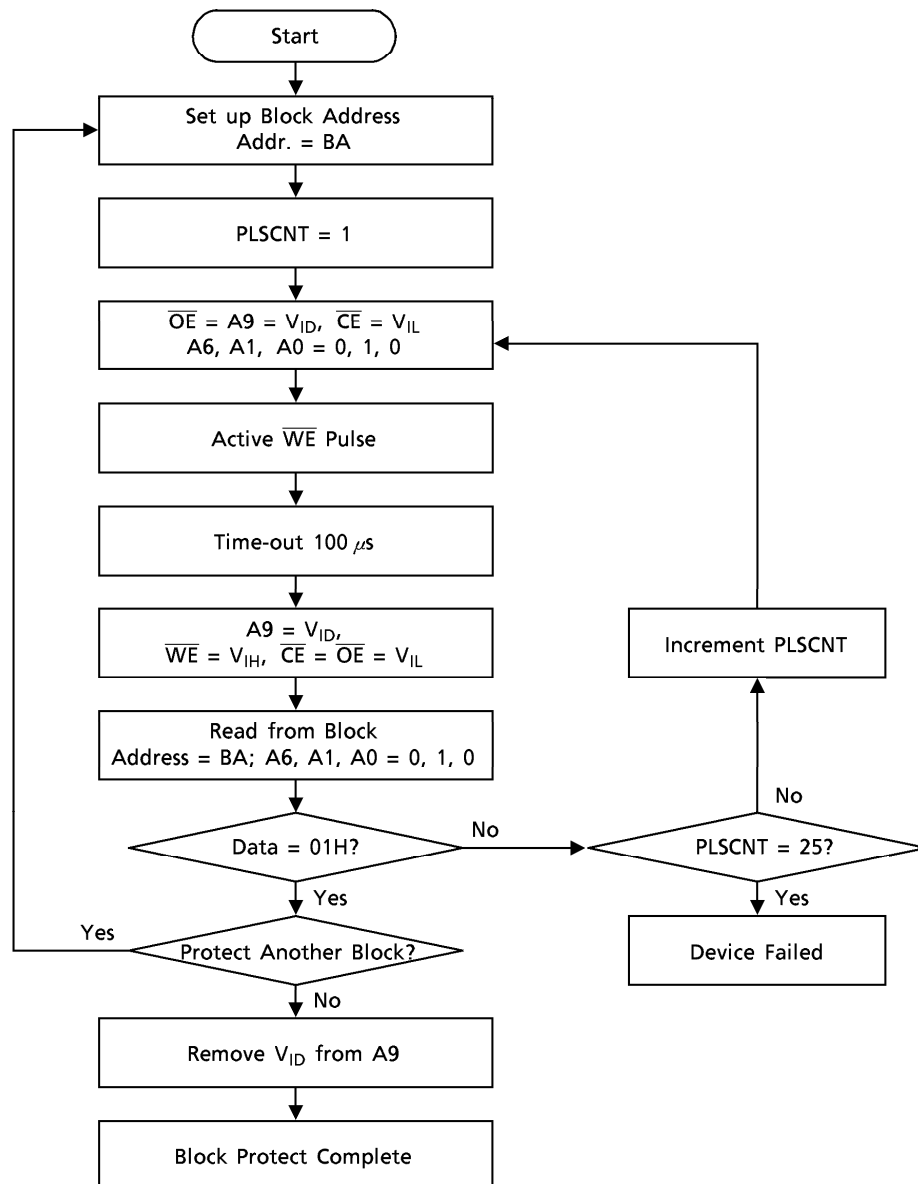
Note: 1) DQ7 must be rechecked even if DQ5 = 1 because DQ7 may change at the same time as DQ5.

### DQ6 Toggle Bit

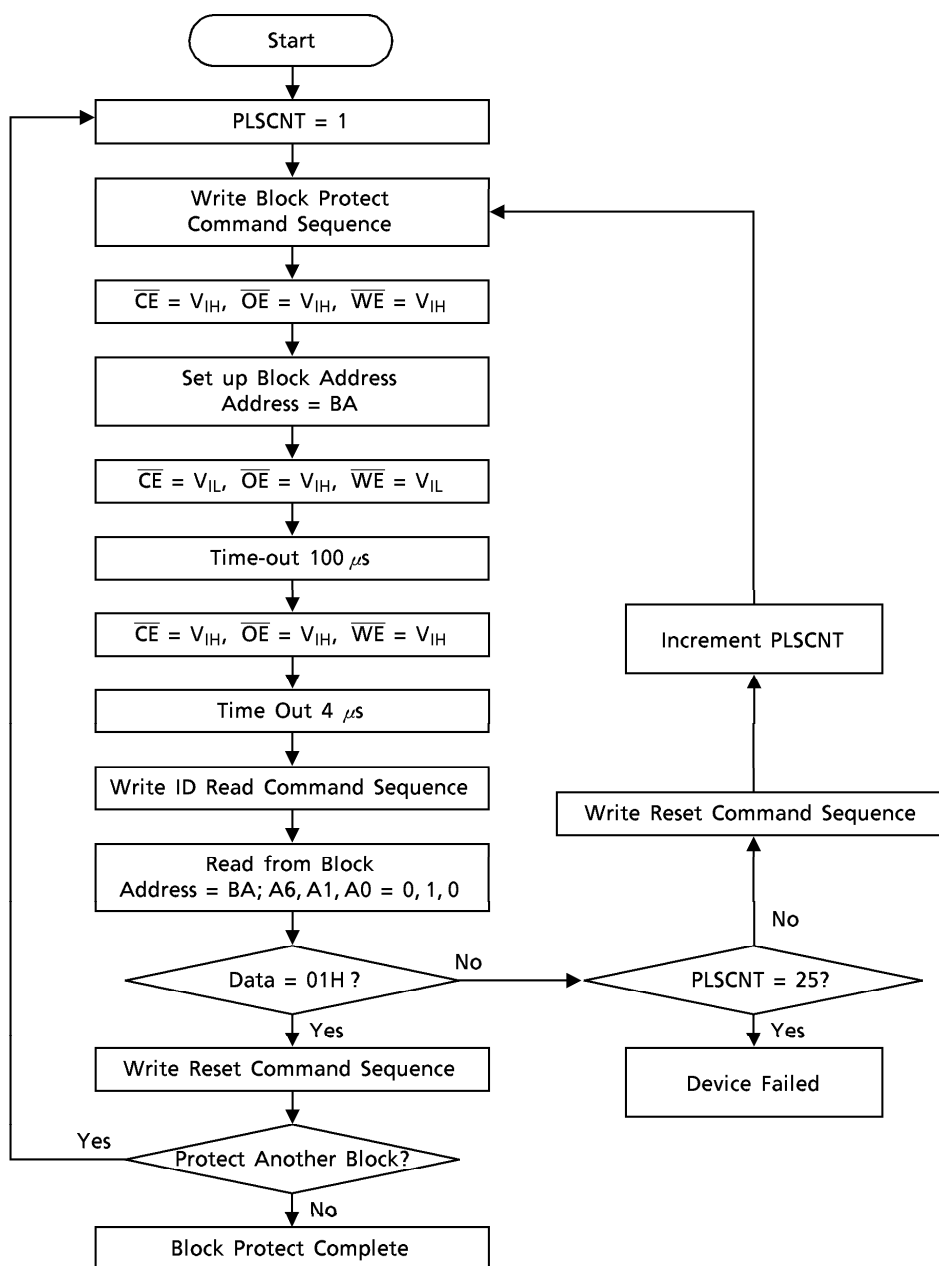


VA: Byte address for programming.  
Any of the addresses within the block being erased during a Block Erase operation.  
Don't care during a Chip Erase operation  
Any address not within the current block during an Erase Suspend operation

Note: 1) DQ6 must be rechecked even if DQ5 = 1 because DQ6 may stop toggling at the same time that DQ5 changes to 1.

Block Protect (Hardware)

BA: Block address

Block Protect (Software)

BA: Block Address

**PACKAGE DIMENSIONS**

- Plastic TSOP

TSOP I 40 – P – 1020 – 0.50

Unit: mm

