TOSHIBA CCD LINEAR IMAGE SENSOR CCD (Charge Coupled Device)

TCD2255D

The TCD2255D is a high sensitive and low dark current 2700 elements×3 line CCD color image sensor which includes CCD drive circuit, clamp circuit and sample & hold circuit.

The sensor is designed for scanner. The device contains a row of 2700 elements×3 line photodiodes which provide a 12 lines / mm (300DPI) across a A4 size paper. The device is operated by 5V pulse and 12V power supply.

FEATURES

Number of Image Sensing Elements

: 2700 elements×3 line

Image Sensing Element Size : 8μm by 8μm on 8μm centers
 Photo Sensing Region : High sensitive and low dark

current PN photodiode

• Distance Between Photodiode Array: 32μm (4 lines)

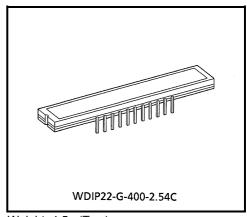
• Clock : 2 phase (5V)

Power Supply
 Internal Circuit
 Sample & Hold circuit, Clamp

circuit

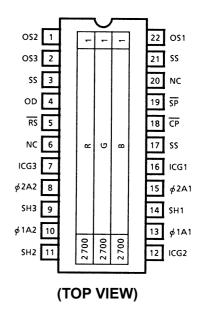
• Package : 22 pin CERDIP package

• Color Filter : Red, Green, Blue



Weight: 4.5g (Typ.)

PIN CONNECTION



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damage to property.

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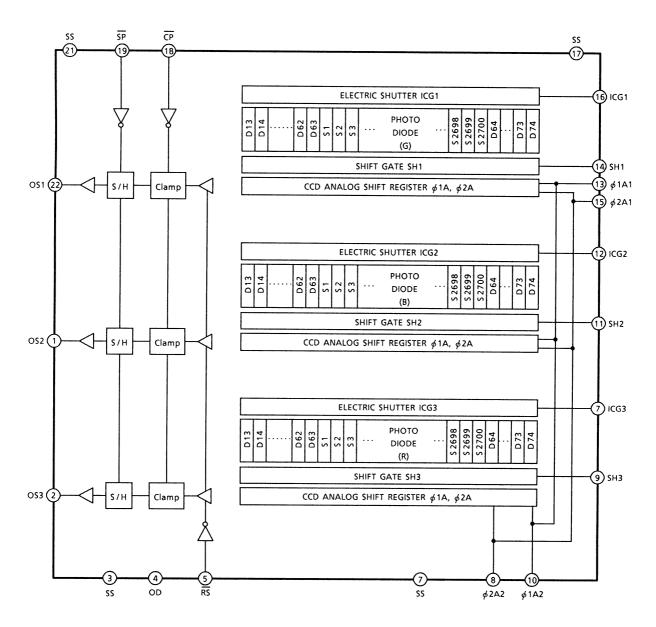


MAXIMUM RATINGS (Note 1)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Clock Pulse Voltage	$V_{\phi A}$		
Shift Pulse Voltage	V _{SH}		
Reset Pulse Voltage	V RS	-0.3~8.0	V
Clamp Pulse Voltage	V CP	0.5 0.0	V
Sample and Hold Pulse Voltage	V SP		
Electrical Shutter Voltage	VICG		
Power Supply Voltage	V _{OD}	-0.3~15	V
Operating Temperature	T _{opr}	0~60	°C
Storage Temperature	T _{stg}	-25~85	°C

Note 1: All voltage are with respect to SS terminals (Ground).

CIRCUIT DIAGRAM



TCD2255D



PIN NAMES

PIN No.	SYMBOL	NAME	PIN No.	SYMBOL	NAME
1	OS2	Signal Output 2 (Green)	22	OS1	Signal Output 1 (Blue)
2	OS3	Signal Output 3 (Red)	21	SS	Ground
3	SS	Ground	20	NC	Non Connection
4	OD	Power	19	SP	Sample and Hold Gate
5	RS	Reset Gate	18	СР	Clamp Gate
6	NC	Non Connection	17	SS	Ground
7	ICG3	Electric Shatter Gate 3	16	ICG1	Electric Shatter Gate 1
8	Ψ2A2	Clock 2 (Phase 2)	15	Ψ2A1	Clock 1 (Phase 2)
9	SH3	Shift Gate 3	14	SH1	Shift Gate 1
10	Ψ1A2	Clock 2 (Phase 1)	13	Ψ1Α1	Clock 1 (Phase 1)
11	SH2	Shift Gate 2	12	ICG2	Electric Shatter Gate 2

OPTICAL / ELECTRICAL CHARACTERISTICS

 $(Ta=25^{\circ}C,\,V_{OD}=12V,\,V_{\phi}=V_{RS}=V_{SH}=V_{CP}=5V\,\,(pulse),\,f_{\phi}=1.0MHz,\,f_{RS}=1.0MHz,\,LOAD\,\,RESISTANCE=100k\Omega,\,t_{INT}\,\,(INTEGRATION\,\,TIME)=10ms,\,LIGHT\,\,SOURCE=A\,\,LIGHT\,\,SOURCE+CM500S\,\,FILTER\,\,(t=1.0mm)\,\,)$

CHARACTERISTIC	SYMBOL	MIN	TYP.	MAX	UNIT	NOTE
	R_{R}	9.1	13.0	16.9		
Sensitivity	R _G	11.4	16.3	21.2	V / (lx·s)	(Note 2)
	R _B	4.0	5.7	7.4		
Photo Response Non Uniformity	PRNU (1)	_	10	20	%	(Note 3)
Filoto Response Non Officiality	PRNU (3)	_	2.5	10	mV	(Note 4)
Image Lag	IL	_	0.01	_	%	(Note 5)
Saturation Output Voltage	V _{SAT}	1.7	2.0	_	V	(Note 6)
Saturation Exposure	SE	_	0.12	_	lx⋅s	(Note 7)
Dark Signal Voltage	V_{DRK}	_	3	9	mV	(Note 8)
Dark Signal Non Uniformity	D _{SNU}	_	4	12	mV	(Note 8)
DC Power Dissipation	P_{D}	_	200	300	mW	
Total Transfer Efficiency	TTE	92	_	_	%	
Output Impedance	Z _o	_	0.4	1.0	kΩ	
DC Signal Output Voltage	Vos	3.0	5.0	7.0	V	(Note 9)
Random Noise	N _{Dσ}	_	0.7	_	mV	(Note 10)
Reset Noise	V _{RS}	_	1.5	_	٧	(Note 9)

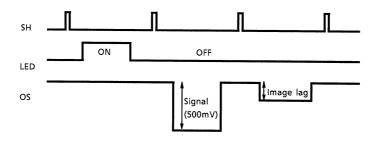
- Note 2: Sensitivity is defined for each color of signal outputs average when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature.
- Note 3: PRNU (1) is defined for each color on a single chip by the expressions below when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature.

PRNU (1) =
$$\frac{\Delta \chi}{\bar{\chi}}$$
 ×100 (%)

When $\bar{\chi}$ is average of total signal outputs and $\Delta\chi$ is the maximum deviation from $\bar{\chi}$. The amount of incident light is shown below.

Red =
$$\frac{1}{2}$$
 SE, Green = $\frac{1}{2}$ SE, Blue = $\frac{1}{4}$ SE

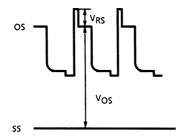
- Note 4: PRNU (3) is defined as maximum voltage with next pixel, where measured 5% of SE (Typ.).
- Note 5: Image Lag is defined as follows.



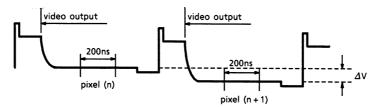
- Note 6: V_{SAT} is defined as minimum saturation output of all effective pixels.
- Note 7: Definition of SE: SE = $\frac{V_{SAT}}{R_{G}}$ (lx·s)
- Note 8: V_{DRK} is defined as average dark signal voltage of all effective pixels. DSNU is defined as different voltage between V_{DRK} and V_{MDK} when V_{MDK} is maximum dark signal voltage.



Note 9: DC signal Output Voltage Reset Noise is defined as follows, but Reset Noise is a fixed pattern noise.



Note 10: Random noise is defined as the standard deviation (sigma) of the output level difference between two adjacent effective pixels under no illumination (i.e. dark conditions) calculated by the following procedure.



Output wave form (Effective pixels under dark condition)

- 1) Two adjacent pixels (pixel n and n+1) in one reading are fixed as measurement points.
- 2) Each of the output level at video output periods averaged over 200ns period to get V (n) and V (n+1).
- 3) V (n+1) is subtracted from V (n) to get ΔV .

$$\Delta V = V(n)-V(n+1)$$

4) The standard deviation of ΔV is calculated after procedure 2) and 3) are repeated 30 times (30 readings).

$$\Delta V = \frac{1}{30} \sum_{i=1}^{30} \!\! \left| \Delta V i \right| \quad \sigma = \sqrt{\frac{1}{30} \sum_{i=1}^{30} \!\! \left| \!\! \left| \Delta V i \right| - \overline{\Delta V} \right|^2}$$

- 5) Procedure 2), 3) and 4) are repeated 10 times to get 10 sigma values.
- 6) 10 sigma values are averaged.

$$\overline{\sigma} = \frac{1}{10} \sum_{i=1}^{10} \sigma_i$$

7) $\bar{\sigma}$ ovalue calculated using the above procedure is observed $\sqrt{2}$ times larger than that measured relative to the ground level. So we specify the random noise as follows.

$$N_{d\sigma} = \frac{1}{\sqrt{2}} \bar{\sigma}$$



OPERATING CONDITION

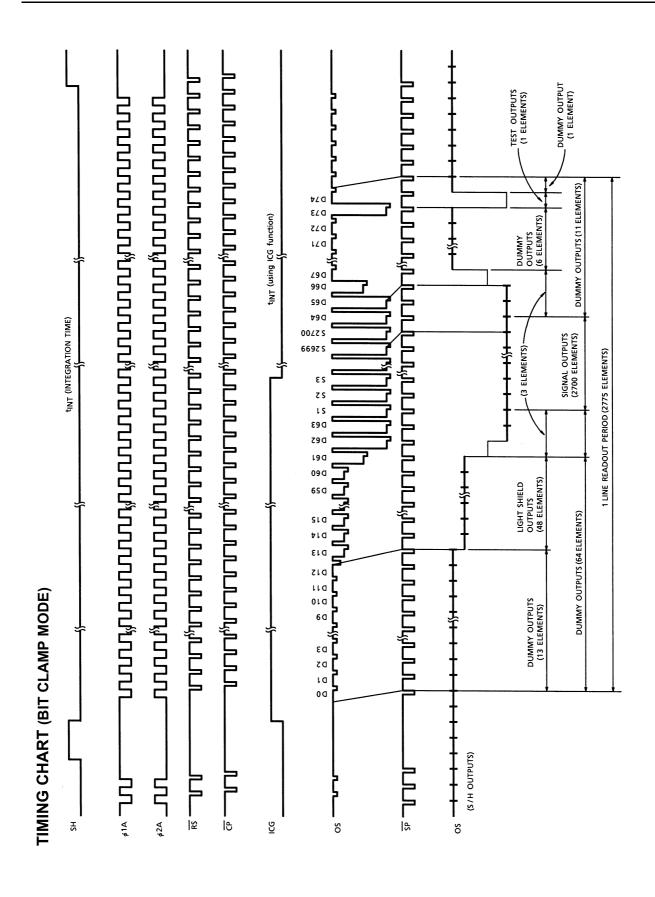
CHARACTERISTIC		SYMBOL	MIN	TYP.	MAX	UNIT	NOTE	
	"H" Level	٧/ ٨	4.7	5.0	5.5	V		
Clock Pulse Voltage	"L" Level	$V_{\phi}A$	0	0	0.05			
Shift Pulse Voltage	"H" Level	\/	V _φ A"H"-0.5	V _φ A"H"	V _φ A"H"	V	(Noto 11)	
Siliit Fuise Voltage	"L" Level	V _{SH}	0	0	0.3	V	(Note 11)	
Penet Bules Voltage	"H" Level	V _{RS}	\/	4.5	5.0	5.5	V	
Reset Pulse Voltage	"L" Level		0	0	0.3	V		
Sample and Hold Pulse	Sample and Hold Pulse "H" Level	V —	4.5	5.0	5.5	V	(Note 12)	
Voltage	"L" Level	V SP	0	0	0.3		(Note 12)	
Clamp Pulse Voltage	"H" Level	V —	4.5	5.0	5.5	V		
Clamp Fulse Voltage	"L" Level	V CP	0	0	0.3	V		
ICG Pulse Voltage	"H" Level	V _{ICG}	V _φ A"H"-0.5	V _φ Α"Η"	V _φ Α"Η"	V	(Note 11)	
	"L" Level	VICG	0	0	0.3	V	(NOTE 11)	
Power Supply Voltage		V _{OD}	11.4	12.0	13.0	V		

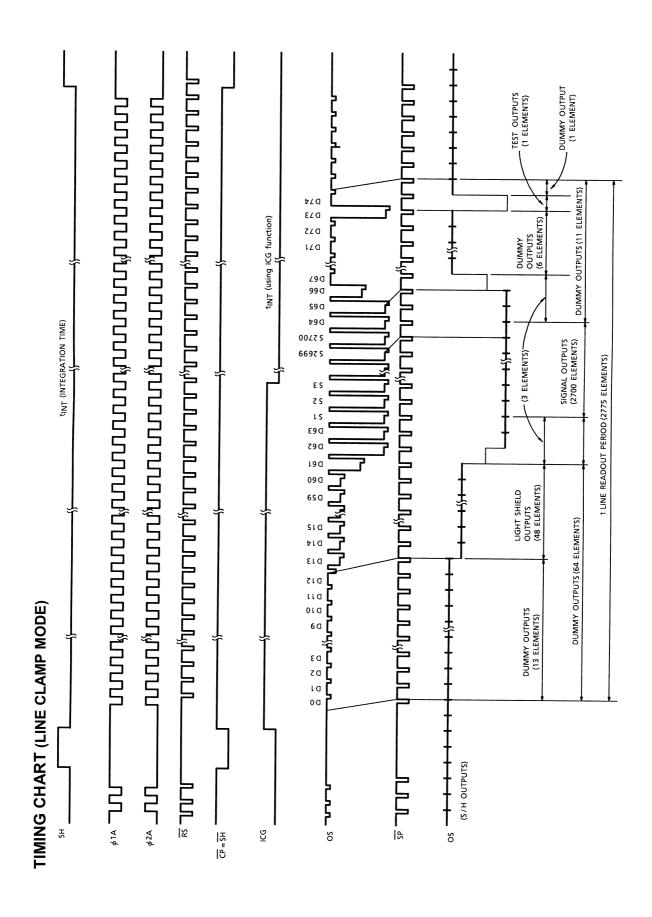
Note 11: $\,V_{\phi}A^{\text{\tiny "}}H^{\text{\tiny "}}$ means the high level voltage of $V_{\phi}A$ when SH pulse is high level.

Note 12: Supply "L" Level to \overline{SP} terminal when sample and hold circuitry is not used.

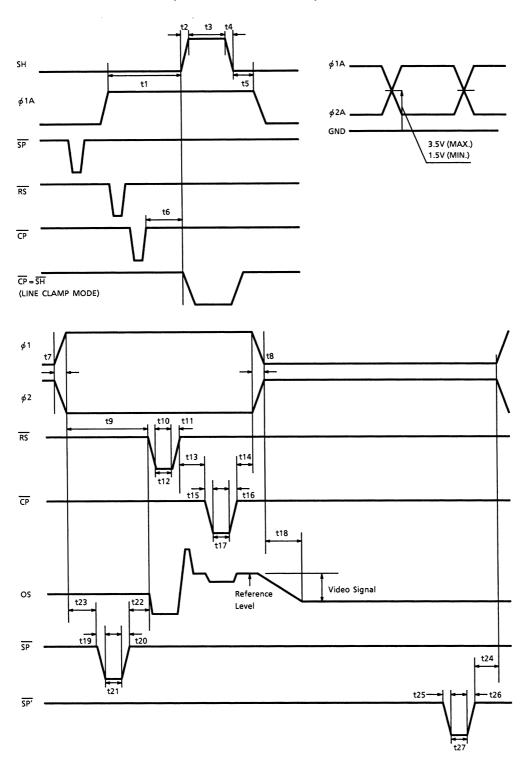
CLOCK CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	MIN	TYP.	MAX	UNIT
Clock Pulse Frequency	$f_{\phi}A$	_	1.0	5.0	MHz
Reset Pulse Frequency	f _{RS}	_	1.0	5.0	MHz
Clamp Pulse Frequency	f CP	_	1.0	5.0	MHz
Sample and Hold Pulse Frequency	f SP	_	1.0	5.0	MHz
Clock Capacitance	C _φ A	_	160	250	pF
Shift Gate Capacitance	C _{SH}	_	20	30	pF
Reset Gate Capacitance	CRS	_	20	30	pF
Sample and Hold Gate Capacitance	C SP	_	20	30	pF
Clamp Gate Capacitance	C CP	_	20	30	pF
ICG Gate Capacitance	C _{ICG}	_	20	30	pF



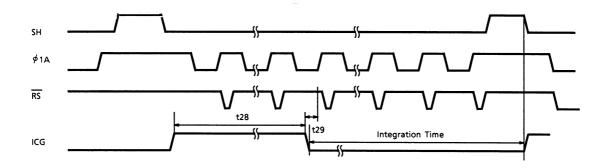


TIMING REQUIREMENTS (LINE CLAMP MODE)





TIMING REQUIREMENTS (Cont.)



CHARACTERISTIC	SYMBOL	MIN	TYP. (Note 13)	MAX	UNIT
Dulgo Timing of SH and (a.	t1	120	1000	_	
Pulse Timing of SH and φ ₁	t5	800	1000	_	ns
SH Pulse Rise Time, Fall Time	t2, t4	0	50	_	ns
SH Pulse Width	t3	3000	5000	_	ns
Pulse Timing of SH and $\overline{\text{CP}}$	t6	0	500	_	ns
φ ₁ , φ ₂ Pulse Rise Time, Fall Time	t7, t8	0	20	_	ns
Pulse Timing of φ ₁ and \overline{RS}	t9	0	20	_	ns
RS Pulse Rise Time, Fall Time	t10, t11	0	20	_	ns
RS Pulse Width	t12	55	100	_	ns
Pulse Timing of RS and CP	t13	10	30	_	ns
Pulse Timing of $\overline{\mbox{CP}}$ and ϕ_1	t14	0	20	_	ns
CP Pulse Rise Time, Fall Time	t15, t16	0	20	_	ns
CP Pulse Width	t17	50	100	_	ns
Video Data Delay Time (Note 14)	t18	70	100	_	ns
SP Pulse Rise Time, Fall Time	t19, t20, 25, t26	0	20	_	ns
SP Pulse Width	t21, t27	50	100	_	ns
Pulse Timing of RS and SP	t22	0	20	_	ns
Pulse Timing of ϕ_1 and \overline{SP}	t23, t24	0	20	_	ns
ICG Pulse Width	t18	5	_		μs
Pulse Timing of ICG and RS	t29	0	20	_	ns

Note 13: TYP. is the case of $f_{RS} = 1.0MHz$.

Note 14: Load Resistance is $100k\Omega$.



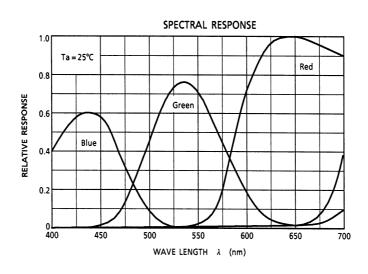
APPLICATION NOTE

	ON	OFF
Sample & Hold Function	SP Pulse	SP = Low
Electrical Shutter Function	ICG Pulse	ICG = Low

Clamp Mode Selection

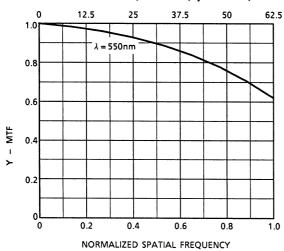
Bit Clamp	CP Pulse
Line Clamp	CP = SH

TYPICAL SPECTRAL REPONSE / MODURATION TRANFER FUNCTION



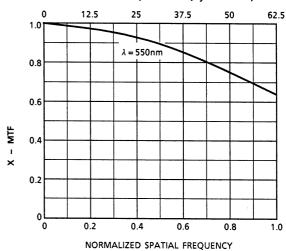
MODULATION TRANSFER FUNCTION OF Y-DIRECTION

SPATIAL FREQUENCY (Cycles/mm)

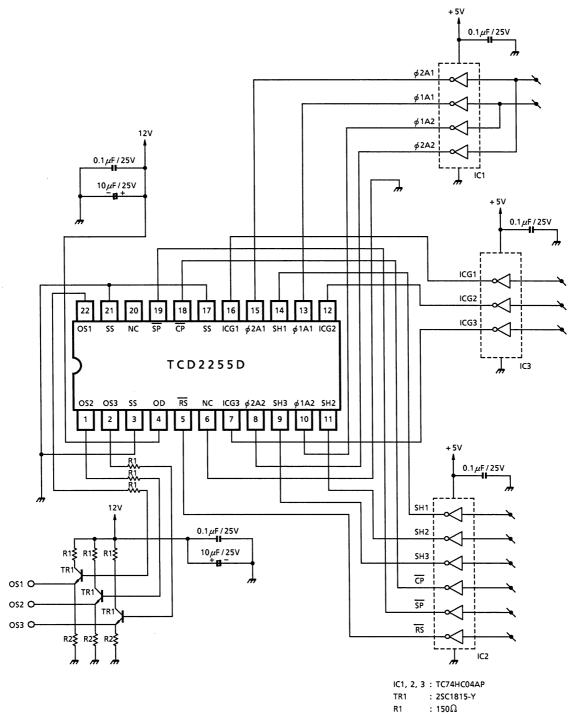


MODULATION TRANSFER FUNCTION OF X-DIRECTION

SPATIAL FREQUENCY (Cycles/mm)



TYPICAL DRIVE CIRCUIT



: 1500Ω R2

TOSHIBA TCD2255D

CAUTION

1. Window Glass

The dust and stain on the glass window of the package degrade optical performance of CCD sensor. Keep the glass window clean by saturating a cotton swab in alcohol and lightly wiping the surface, and allow the glass to dry, by blowing with filtered dry N2.

Care should be taken to avoid mechanical or thermal shock because the glass window is easily to damage.

2. Electrostatic Breakdown

Store in shorting clip or in conductive foam to avoid electrostatic breakdown.

3. Incident Light

CCD sensor is sensitive to infrared light.

Note that infrared light component degrades resolution and PRNU of CCD sensor.

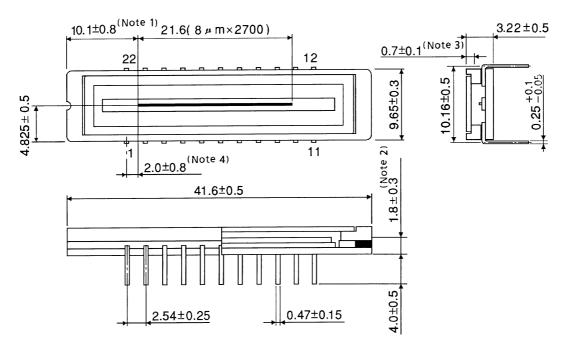
4. Lead Frame Forming

Since this package is not strong against mechanical stress, you should not reform the lead frame. We recommend to use a IC-inserter when you assemble to PCB.



PACKAGE DIMENSIONS

WDIP22-G-400-2.54C Unit: mm



Note 1: No.1 SENSOR ELEMENT (S1) TO EDGE OF PACKAGE.

Note 2: TOP OF CHIP TO BOTTOM OF PACKAGE.

Note 3: GLASS THICKNESS (n = 1.5)

Note 4: No.1 SENSOR ELEMENT (S1) TO EDGE OF No.1 PIN.

Weight: 4.5g (Typ.)