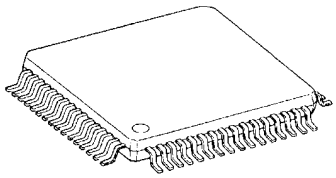
Preliminary

TOSHIBA CMOS Digital Interated Circuit
Silicon Monolithic

T C 9 0 A 3 2 F

Digital Video Encoder

The TC90A32F converts a digital image's Y, Cb and Cr signals, which conform to ITU-R601/656 standards, to analog Y and C composite signals for NTSC and PAL systems.



LQFP64-P-1010-0.50

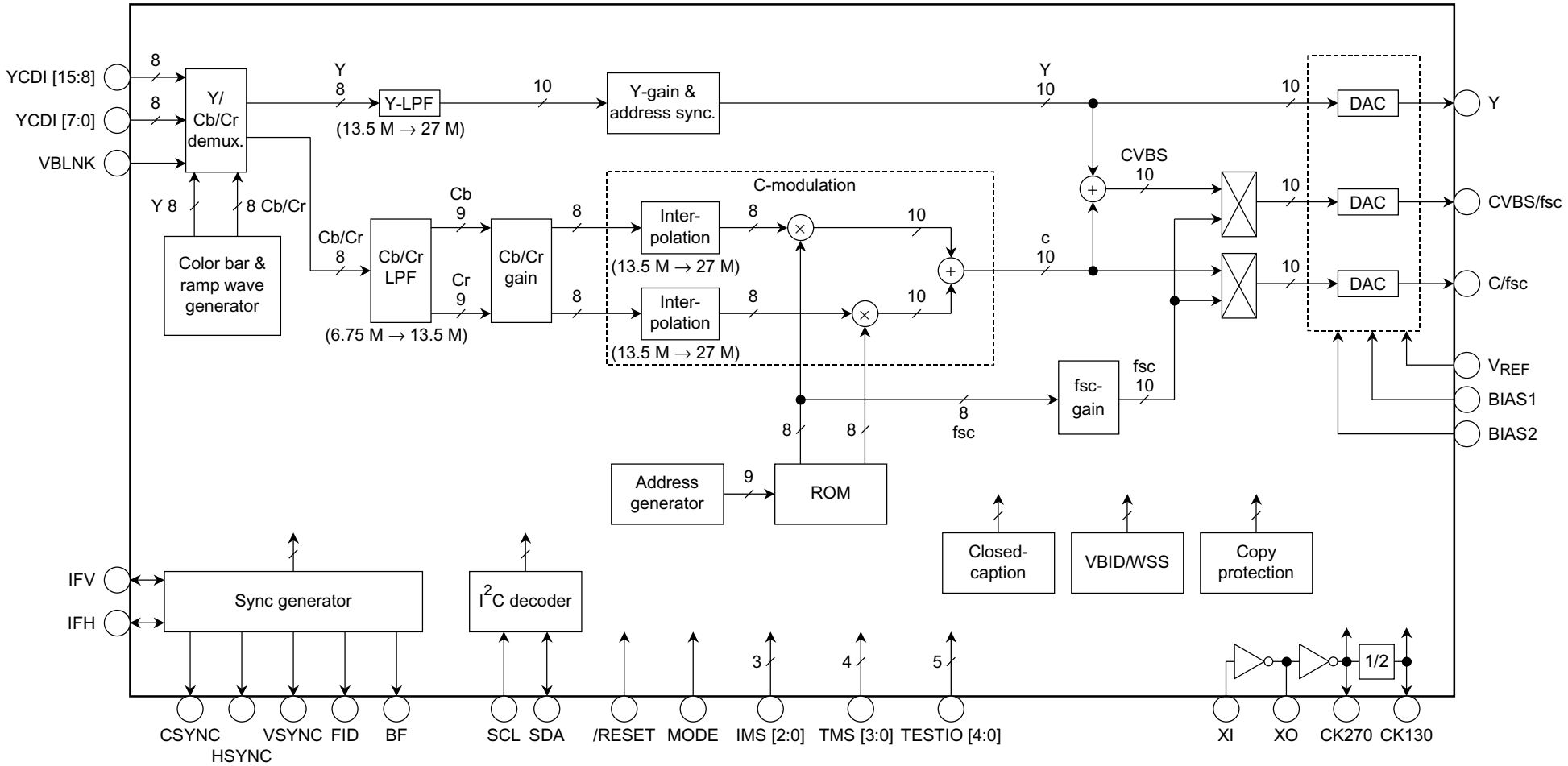
Weight: g (typ.)

Features

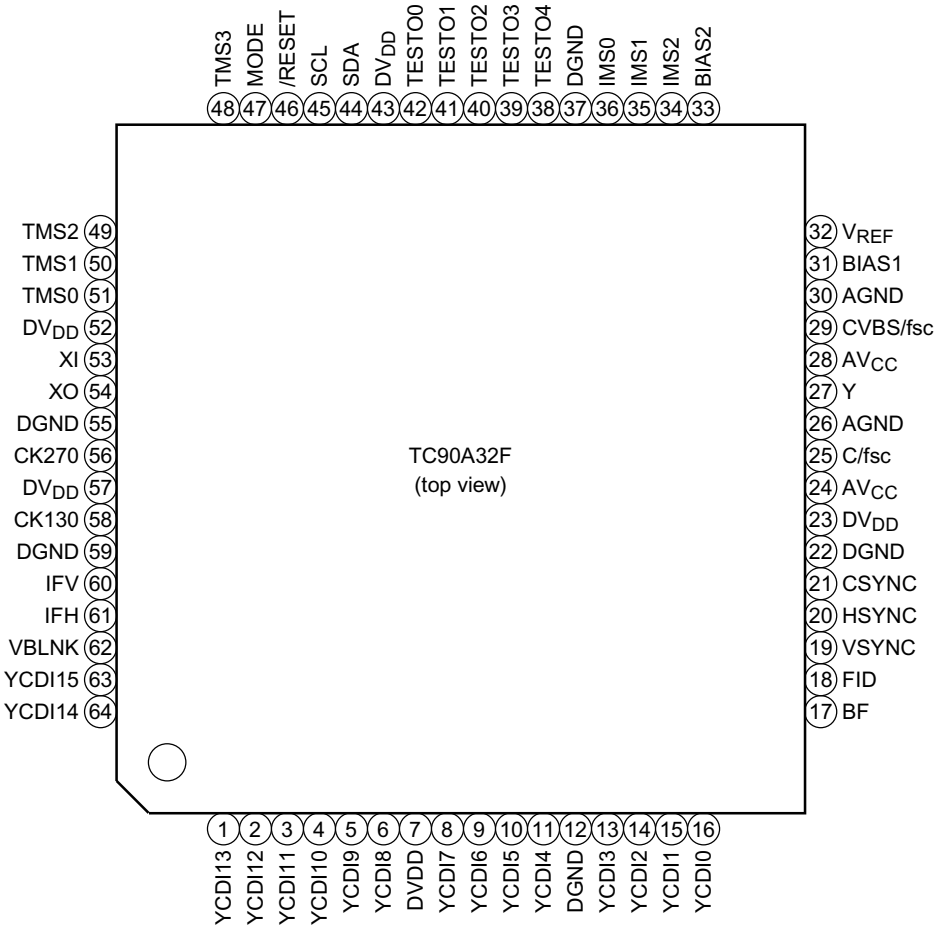
- Encodes ITU-R 601/656 format Y/Cb/Cr digital video signal (8-bit/16-bit) to analog video signal.
- NTSC/PAL (-B, -G, -D, -K, -I) encoder
- Copy protection (MACROVISION Rev. 6.1/7.01)*
- Closed caption, VBID encoding
- Various types of synchronizing signal can be generated.
- Master/Slave Modes
- Built-in 10-bit DAC for CVBS, Y and C
- Y set-up 0/7.5% changeable (NTSC)
- 27-MHz system clock (can be switched between internal oscillation/outside input)
- 13.5-MHz clock output
- Internal digital sub-carrier synthesizer
- Interlaced or non-interlaced support
- Can be controlled by I^2C bus.
- 64-pin QFP
- Single 3.3-V power supply

*: This device is protected by U.S. Patent Numbers 4,631,603, 4,577,216 and 4,819,098 and other intellectual property rights.
The use of Macrovision's copy protection technology in the device must be authorized by Macrovision and is intended for home and other limited pay-per-view uses only, unless otherwise authorized in writing by Macrovision. Reverse engineering or disassembly is prohibited.

Block Diagram



Pin Assignment



Pin Names

Pin No.	Name	I/O	Function	Notes
1	YCDI13	I	Pixel data input pins*1	
2	YCDI12	I		
3	YCDI11	I		
4	YCDI10	I		
5	YCDI9	I		
6	YCDI8	I		
7	DV_{DD}	—	Digital power supply	
8	YCDI7	I	Pixel data input pins*2	
9	YCDI6	I		
10	YCDI5	I		
11	YCDI4	I		
12	DGND	—	Digital GND	
13	YCDI3	I	Pixel data input pins*2	
14	YCDI2	I		
15	YCDI1	I		
16	YCDI0	I		
17	BF	O	Burst flag pulse output (synchronized with analog output)	
18	FID	O	Field ID output (synchronized with analog output)	
19	VSYNC	O	Vertical synchronization signal output (synchronized with analog output)	
20	HSYNC	O	Horizontal synchronization signal output (synchronized with analog output)	
21	CSYNC	O	Composite sync output (synchronized with analog output)	
22	DGND	—	Digital GND	
23	DV_{DD}	—	Digital power supply	
24	AV_{CC}	—	Analog power supply for DAC	For DAC Dynamic range of analog output is set by V_{REF}. Output voltage: 1.5 V_{p-p} max (V_{DD} to V_{DD} – 1.5 V)
25	C/fsc	O	Analog C-signal/fsc output (for testing)	
26	AGND	—	Analog GND for DAC	
27	Y	O	Analog Y-signal output	
28	AV_{CC}	—	Analog power supply for DAC	
29	CVBS/fsc	O	Analog CVBS/fsc output	
30	AGND	—	Analog GND for DAC	
31	BIAS1	—	Bias pin 1 for DAC	
32	V_{REF}	—	Reference voltage input for DAC	
33	BIAS2	—	Bias pin 2 for DAC	
34	IMS2	I	Input mode setting pins MSB	
35	IMS1	I		
36	IMS0	I	LSB	
37	DGND	—	Digital GND	

Pin No.	Name	I/O	Function	Notes
38	TESTO4	O	Output pins for testing (Connect to digital GND.) MSB … LSB	
39	TESTO3	O		
40	TESTO2	O		
41	TESTO1	O		
42	TESTO0	O		
43	DV_{DD}	—	Digital power supply	
44	SDA	I/O	I^2C bus data	*5-V withstand
45	SCL	I	I^2C bus clock	
46	/RESET	I	RESET input (L: RESET)	
47	MODE	I	NTSC/PAL selection (L: NTSC/H: PAL)	
48	TMS3	I	Input pins for testing (Connect to digital GND.) MSB … LSB	
49	TMS2	I		
50	TMS1	I		
51	TMS0	I		
52	DV_{DD}	—	Digital power supply	
53	XI	I	X'tal connection/27-MHz clock input	
54	XO	O	X'tal connection	
55	DGND	—	Digital GND	
56	CK270	O	27-MHz clock output	
57	DV_{DD}	—	Digital power supply	
58	CK130	O	13.5-MHz clock output	
59	DGND	—	Digital GND	
60	IFV	I/O	Vertical synchronous signal for I/F input/output	
61	IFH	I/O	Horizontal synchronous signal for I/F input/output	
62	VBLNK	I/O	Video blanking signal for I/F input/output	
63	YCDI15	I	Pixel data input pins*1	
64	YCDI14	I		

Note1: Pixel data input pins *1 (YCDI [15:8])
ITU-R601 8-Bit Master/Slave Modes, ITU-R656 Mode: Fixed L-input
ITU-R601 16-Bit Master/Slave Modes: 8-bit parallel input pins for Cb/Cr signals

Pixel data input pins *2 (YCDI [7:0])
ITU-R601 8-Bit Master/Slave Modes, ITU-R656 Mode: Y/Cb/Cr 8-bit serial input pins
ITU-R601 16-Bit Master/Slave Modes: 8-bit parallel input pins for Y-signal

Description of Functions

1. Clock Generation Circuit

Generates various clocks for Y/Cb/Cr separation using the video-blanking signal input from VBLNK (pin 62).

2. Y/Cb/Cr Separation Circuit

Separates the ITU-R601 and 656 standard 4:2:2 digital video data input (Cb/Y/Cr/Y) from YCDI [7:0] (pins 8~11 and 13~16) into Y, Cb and Cr.

3. Color Bar/Ramp Waveform Generation Circuit

Generates color bar and ramp waveform for testing.
Color-bar/ramp-waveform generation mode is selected using IMS [2:0] (pins 36~34).

Color Bar Generation Mode IMS [2:0] = 5 (IMS2 = 1, IMS1 = 0, IMS0 = 1)
Ramp Waveform Generation Mode IMS [2:0] = 6 (IMS2 = 1, IMS1 = 1, IMS0 = 0)

Note: Set VBLNK (pin 62) to “H” in test signal genration mode.

4. YLPF Circuit

This is an LPF for the Y-signal. The cut-off frequency for this LPF is 6 MHz.
The YLPF is switched ON/OFF using IIC BUS 01H [YLPF].

5. Y-Level Adjustment and Sync Signal Addition Circuit

The Y-level adjustment and sync signal addition circuit adds the composite sync and blanking signal from the sync generator circuit to the level-adjusted Y.

6. CLPF Circuit

The high-frequency components of the Cb and Cr signals are cut by the CLPF.
The cut-off frequency for this LPF is switched between 1.5 MHz and 3.0 MHz using IIC BUS 01H [CLPFS].
The CLPF is switched ON/OFF using IIC BUS 01H [CLPF].

7. C Generation and Sync Addition Circuit

After increasing the rate of the Cb and Cr signals to 27 MHz by the interpolation filter, this circuit modulates the sub-carrier generated digitally by ROM. Hence, generation of the C signal also adds the color burst and blanking signals.

8. Y/C Addition Circuit

Performs Y/C addition to create a composite video signal.

9. Sync Generation Circuit

Generates various sync signals, the burst flag pulse and the sync signals for the video decoder interface.

10. VBID/WSS Encode Circuit

VBID: For NTSC Mode
Insert a signal denoting a new aspect ratio and various other information into the blanking for 20H and 283H.

WSS: For PAL Mode
Insert a signal denoting a new aspect ratio and various other information into the blanking for 23H.

VBID/WSS encoding is switched ON/OFF using IIC BUS 05H [VBON].

11. Closed-Caption Encoding Circuit

Adds the closed-caption data to 21H and 284H for each field. This is for NTSC Mode only.
Closed-caption encoding is switched ON/OFF using IIC BUS 05H [CCD2, CCD1].

- 0: OFF = default
- 1: encodes field Odd
- 2: encodes field Even
- 3: encodes both field Odd and Even

12. Macrovision Copy Guard Function Encoding Circuit

Generates copy protection signal corresponding to macrovision Rev 6.1/7.01 and adds the signal to the encoded video signal.

The copy guard function can be turned ON and OFF using IIC BUS 23H [MACON].

0 = OFF (default)
1 = ON

The version can be selected using IIC BUS 22H [REV67].

0 = Ver. 7.0.1 (default)
1 = Ver. 6.1

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Reverse engineering or disassembly is prohibited.

13. DAC Circuit

3-channel internal 10-bit DA converter 3 channels (for Y, C and composite video output)

Video I/F

The video I/F format is set using IMS[2:0] as shown in the following table.

IMS2	IMS1	IMS0	Description
0	0	0	ITU-R656 Mode
0	0	1	ITU-R601 8-Bit Master Mode
0	1	0	ITU-R601 8-Bit Slave Mode
0	1	1	ITU-R601 16-Bit Master Mode
1	0	0	ITU-R601 16-Bit Slave Mode
1	0	1	100% Color Bar Generation Mode (test signal generation)
1	1	0	Ramp Wave Generation Mode (test signal generation)
1	1	1	ITU-R656 Mode

(1) ITU-R656 Mode

ITU-R656 standard 8-bit digital video data (Cb/Y/Cr/Y, 27-MHz) is input on YCDI[7:0] (pins 8~11 and 13~16).

The TC90A32F reads the timing reference code in the video data and controls the internal H and V counters.

The H and V sync signals for the video decoder interface are output on IFH (pin 61) and IFV (pin 60) respectively.

(2) 8-Bit Master Mode

ITU-R601 standard 8-bit digital video data (Cb/Y/Cr/Y, 27-MHz) is input.

The H and V sync signals for the video decoder interface are output on IFH and IFV respectively.

(3) 8-Bit Slave Mode

ITU-R601 standard 8-bit digital video data (Cb/Y/Cr/Y, 27-MHz) is input.

The H and V sync signals are input on IFH and IFV respectively.

(4) 16-Bit Master Mode

An ITU-R601 standard 8-bit digital Y-signal (13.5 MHz) is input on YCDI [7:0] and 8-bit digital Cb and Cr signals (Cb/Cr, 13.5 MHz) are input on YCDI[15:8] (pins 1~6, 63 and 64).

The H and V sync signals for the video decoder interface are output.

(5) 16-Bit Slave Mode

An ITU-R601 standard 8-bit digital Y-signal (13.5 MHz) is input on YCDI [7:0] and 8-bit digital Cb and Cr signals (Cb/Cr, 13.5 MHz) are input on YCDI[15:8].

The H and V sync signals are input on IFH and IFV respectively.

NTSC/PAL

The TC90A32F is designed for both NTSC and PAL systems.
The MODE pin (pin 47) is used to switch between NTSC and PAL.
IIC BUS (00H) [NTPAL] can also be used to switch between NTSC and PAL.

0 = NTSC (default)
1 = PAL

Mode	Mode (pin 47)	Field Frequency	Number of Scanning Lines	Line Cycle (number of clock pulses)
NTSC	L	60 Hz	525	63.5 μs (1716 clocks)
PAL	H	50 Hz	625	64 μs (1728 clocks)

Interlace/Non-Interlace

The TC90A32F is designed for both interlace and non-interlace systems. The interlace mode is determined by IIC BUS 00H [INTER]. The number of scanning lines for non-interlace systems is shown below.

Mode	Number of Scanning Lines
NTSC	262
PAL	312

System Clock

The TC90A32F incorporates an oscillator circuit for generating a stable 27-MHz clock.
Connect a 27-MHz X'tal to XI and XO.
The system clock is output on CK270 (pin 56).
Alternatively, the system clock can be directly input on XI (pin 53).

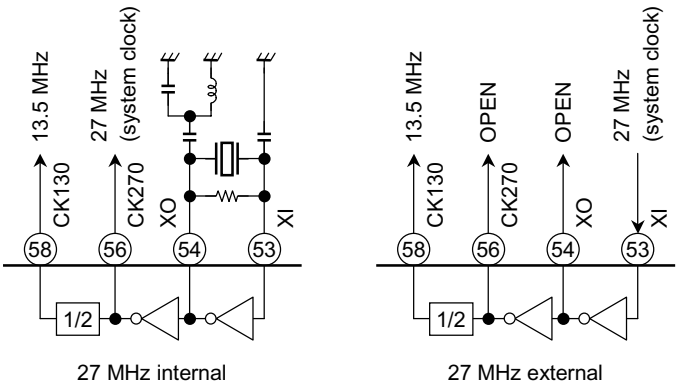


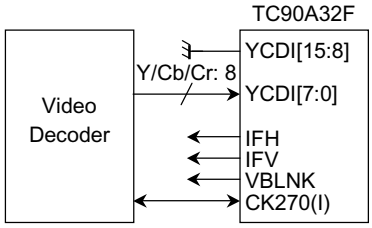
Figure 1 TC90A32F system clock

Video Decoder Interface

The TC90A32F supports both Master and Slave Modes when interfacing with the video decoder. Master and Slave Modes are selected using IMS[2:0] (pins 34~36).

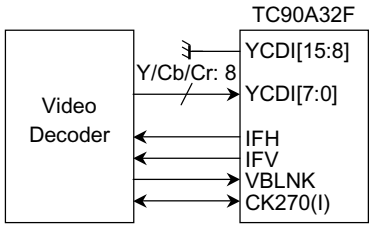
Pin No.	Pin Name	I/O	Description
61	IFH	O	Master Mode: Horizontal sync output At start of line, outputs low level for 128 clock pulses synchronized with rising edge of CK270(I).
		I	Slave Mode: Horizontal sync input At start of line, input low level for at least 8 clock pulses. Sampled on rising edge of CK270(I)
60	IFV	O	Master Mode: Vertical sync output At start of field, outputs low level for 3 lines (NTSC) or 2.5 lines (PAL) synchronized with rising edge of CK270(I).
		I	Slave Mode: Vertical sync input At start of field, input low level for at least 16 clock pulses. Sampled on rising edge of CK270(I)
62	VBLNK	O	Video blanking signal output This internal signal is generated when video decoder does not output blanking signal for valid pixel data input period.
		I	Video blanking signal input Input High signal for valid pixel data input period and Low signal for blanking period. Sampled on rising edge of CK270(I)
8~11, 13~16	YCDI[7:0]	I	8-bit pixel data bus. Input multiplexed video data in sequence Cb/Y/Cr/Y according to ITU-R601 and 656 format. (In 16-Bit Mode: Input 8-Bit Y data.)
1~6, 63, 64	YCDI[15:8]	I	In 16-Bit Mode: input Cb/Cr data. In 8-Bit Mode: set to L.
53	XI	I	Input pin when 27-MHz system clock is input from external source
56	CK270	O	27-MHz system clock output pin when built-in oscillator circuit is used

Video I/F Connection Examples

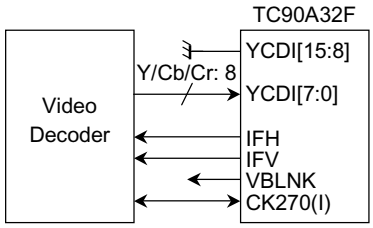


(1) ITU-R656 Mode

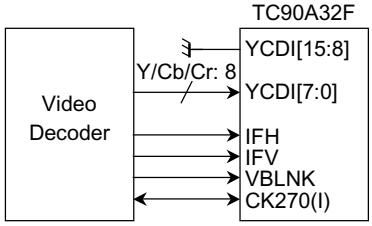
ITU-R656 Mode



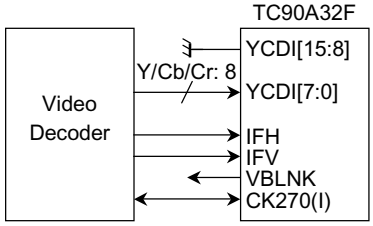
(2) 8-Bit: Master Mode (VBLNK input)



(3) 8-Bit: Master Mode (VBLNK output)

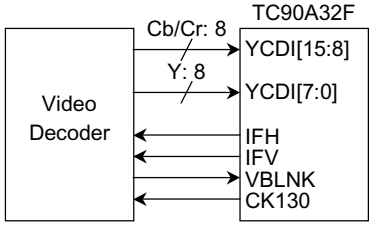


(4) 8-Bit: Slave Mode (VBLNK input)

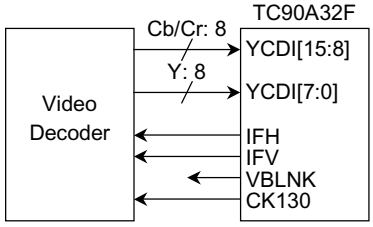


(5) 8-Bit: Slave Mode (VBLNK output)

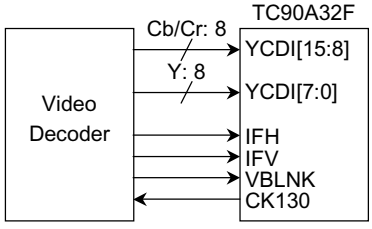
ITU-R601 8-Bit Master/Slave Modes



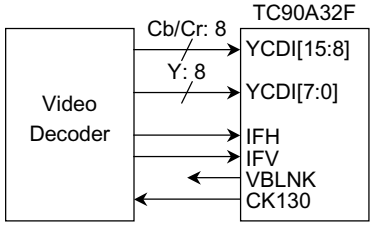
(6) 16-Bit: Master Mode (VBLNK input)



(7) 16-Bit: Master Mode (VBLNK output)



(8) 16-Bit: Slave Mode (VBLNK input)



(9) 16-Bit: Slave Mode (VBLNK output)

ITU-R601 16-Bit Master/Slave Modes

Figure 2 Video I/F connection examples

Internal Filter Characteristics

(1) Y-signal

The device incorporates a 6-MHz cut-off low-pass filter (13.5 MHz → 27 MHz, ×2 oversampling) for the luminance signal (Y-signal).

The filter can be switched ON/OFF using IIC BUS 01H [YLPF].

*: Y-signal pass level: 5.00 MHz = –0.8dB
6.25 MHz = –4.0dB
over 7.50 MHz = under –11.2dB

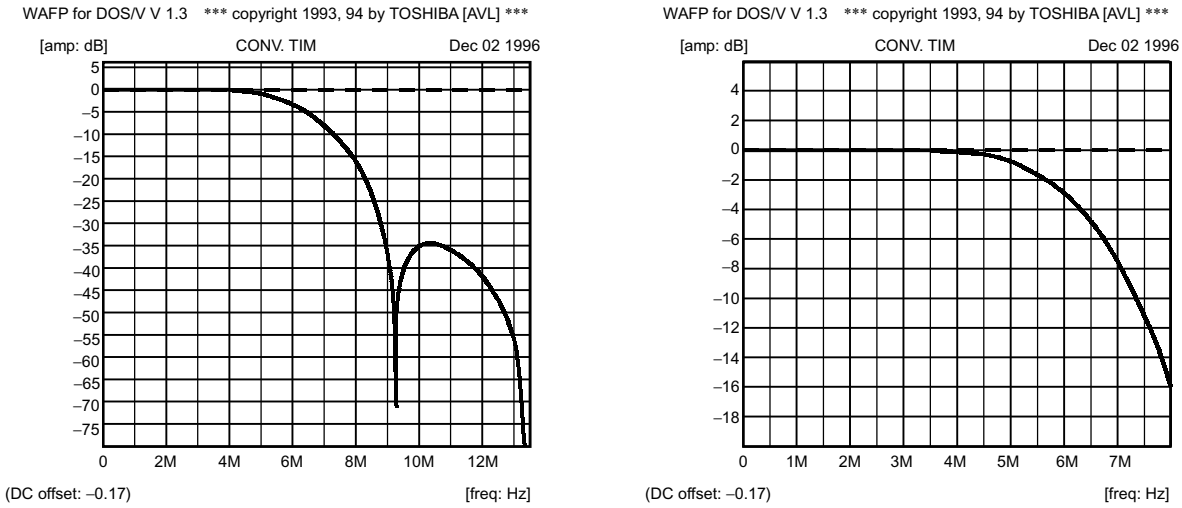


Figure 3 Y-signal 6M-LPF characteristics

(2) C-signal

A low-pass filter for C (Cb/Cr) signal (6.75 MHz~13.5 MHz: ×2 oversampling) is applied.
The cut-off frequency is 1.5 MHz/3.0 MHz. This LPF is switched using IIC BUS 01H [CLPF].
The cut-off frequency is switched between 1.5 MHz and 3.0 MHz using IIC BUS 01H [CLPFS].

① 1.5-MHz LPF

*: C (Cb/Cr) signal pass level: 1.25 MHz = –2.5dB
2.50 MHz = –13.0dB
Over 3.75 MHz = Under –35dB

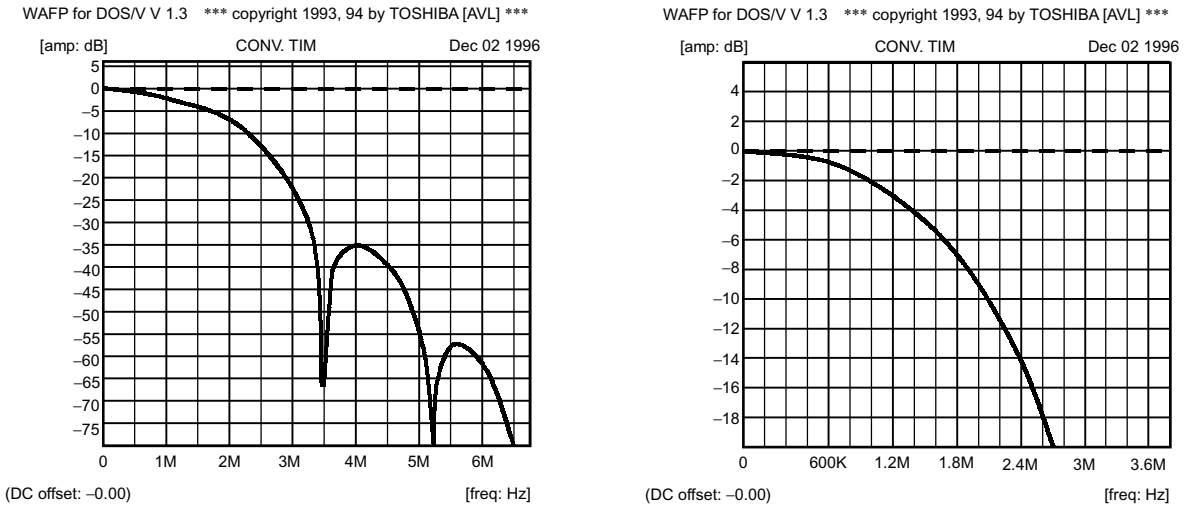


Figure 4-1 C (Cb/Cr) signal 1.5M-LPF characteristics

② 3-MHz LPF

*: C (Cb/Cr) signal pass level: 1.25 MHz = –0.2dB
2.50 MHz = –0.9dB
Over 3.75 MHz = Under –11.5dB

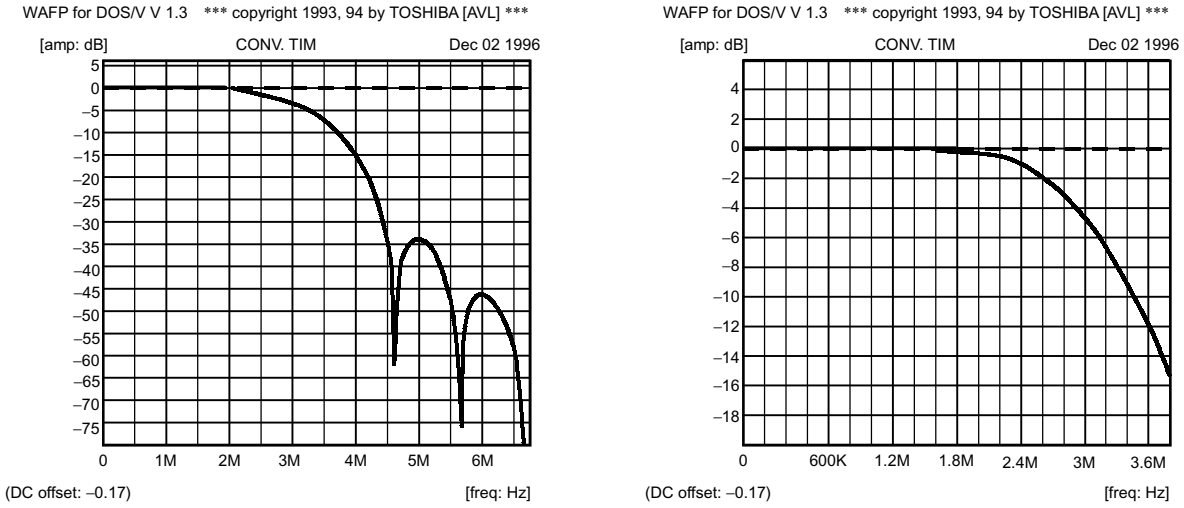


Figure 4-2 C (Cb/Cr) signal 3M-LPF characteristics

Video I/F V-Timings

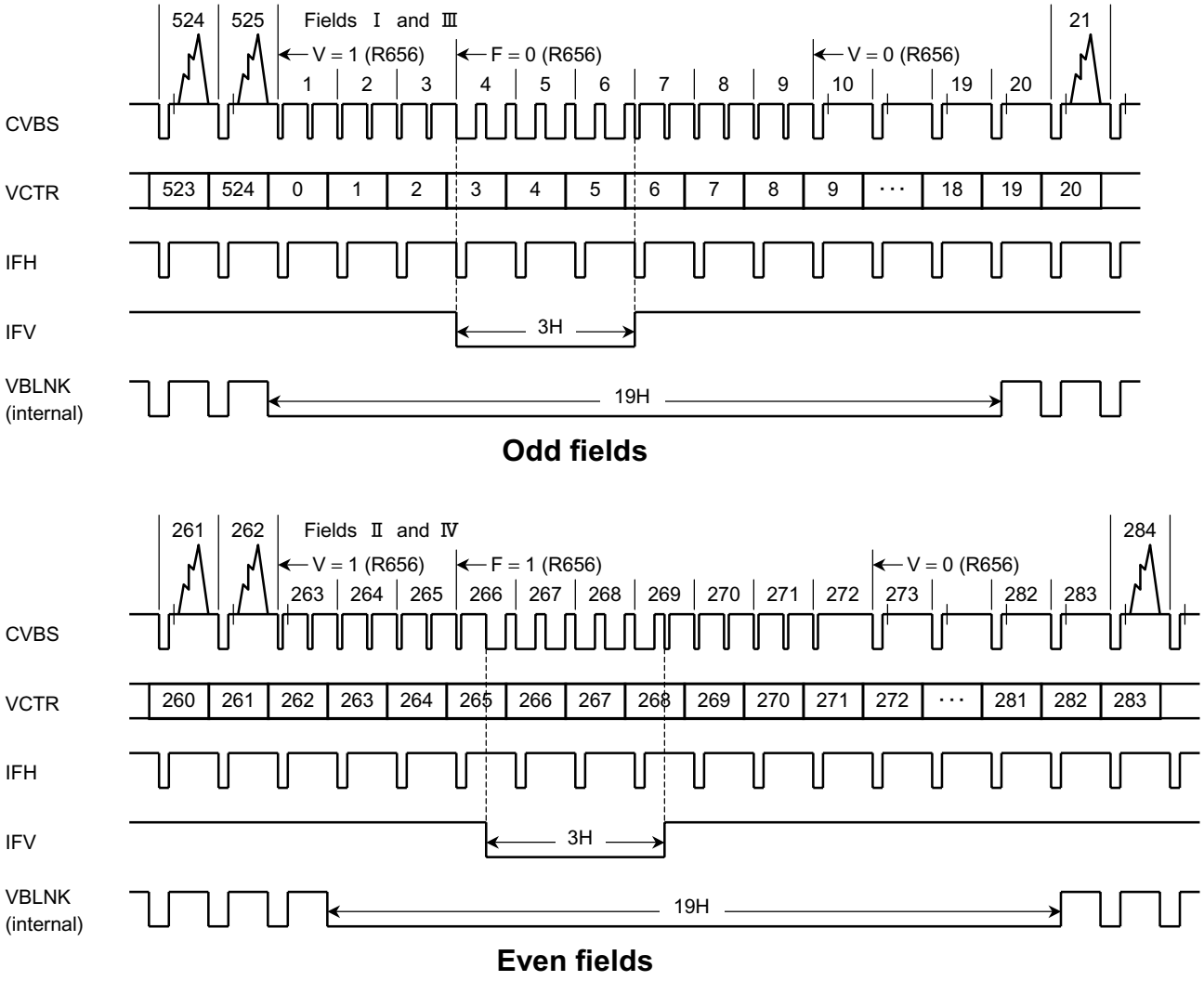


Figure 5-1 I/F V-timing (NTSC)

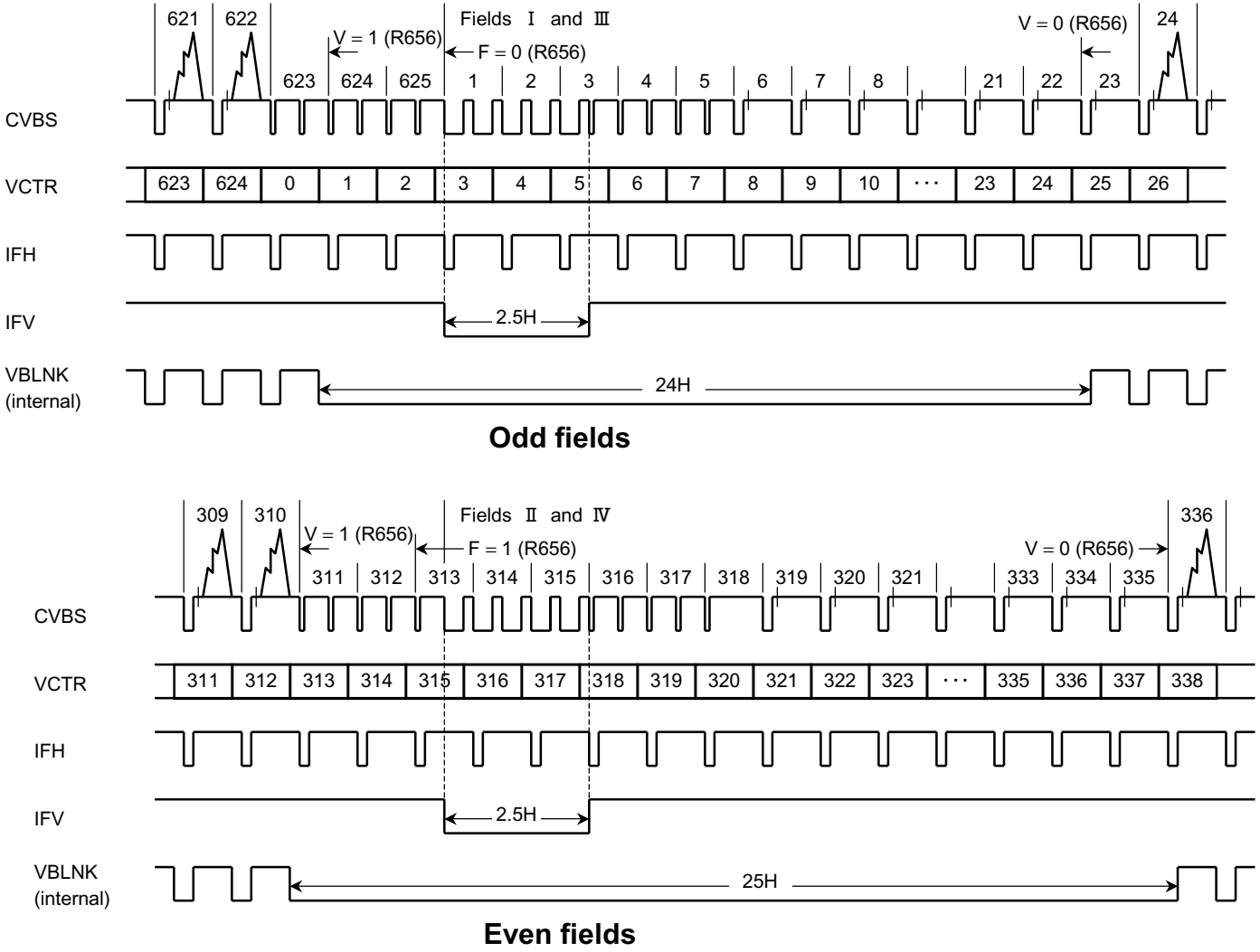


Figure 5-2 I/F V-timing (PAL)

H-Timings

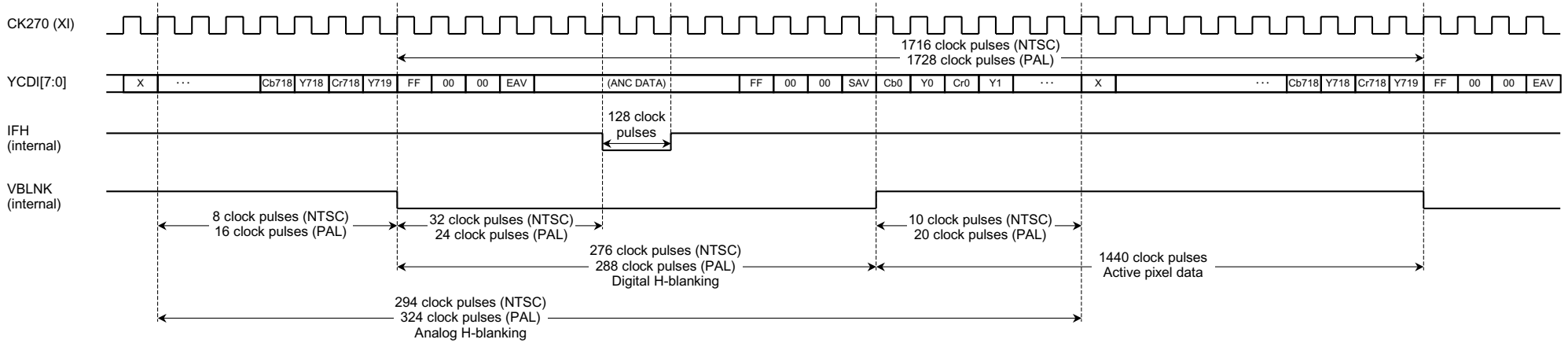


Figure 6-1 ITU-R656 Mode H-timing

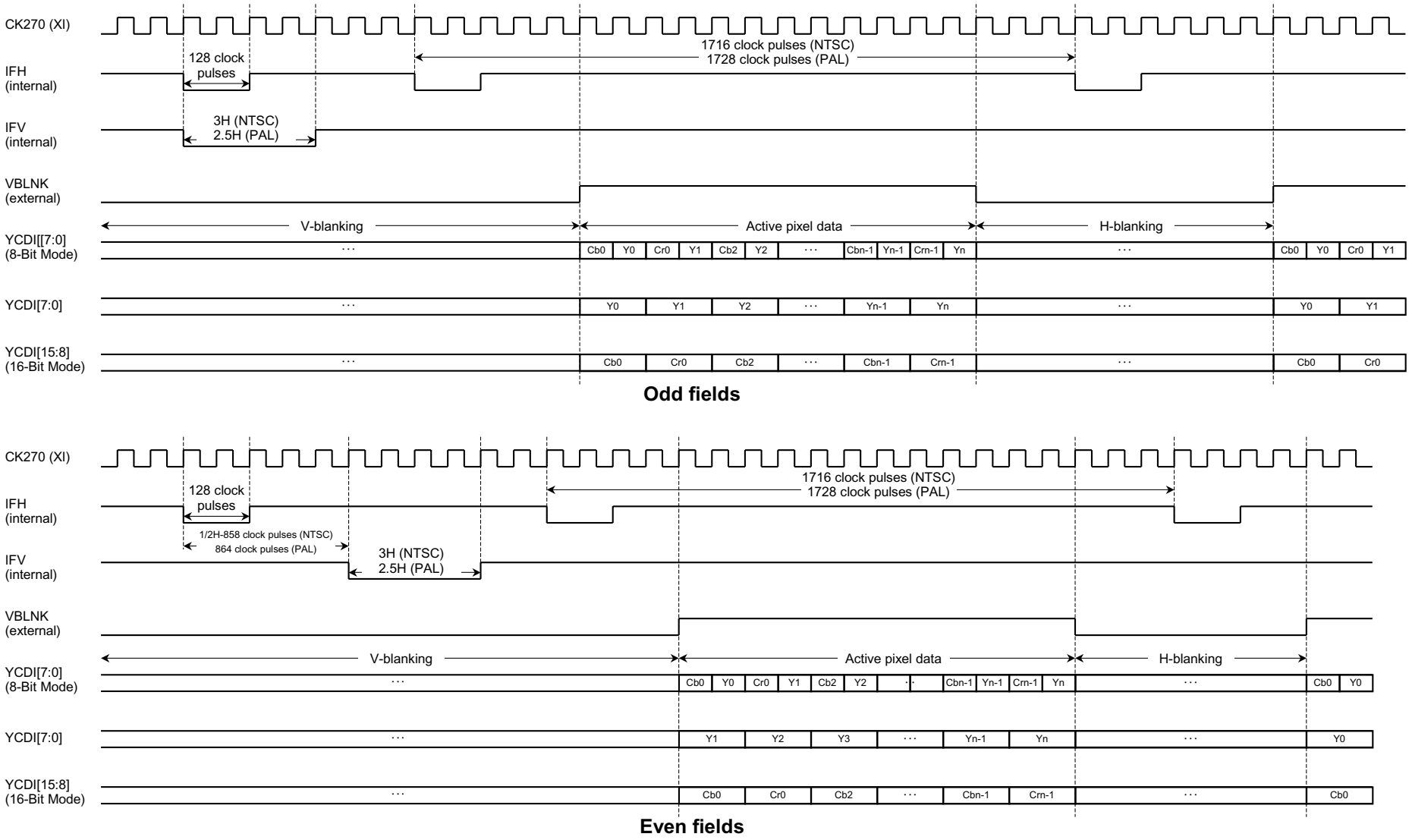
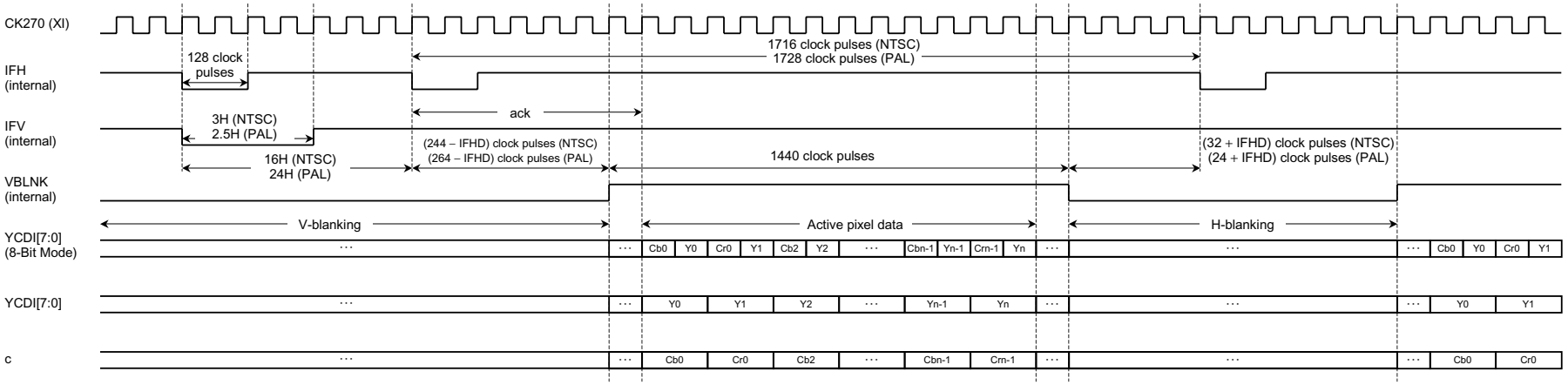
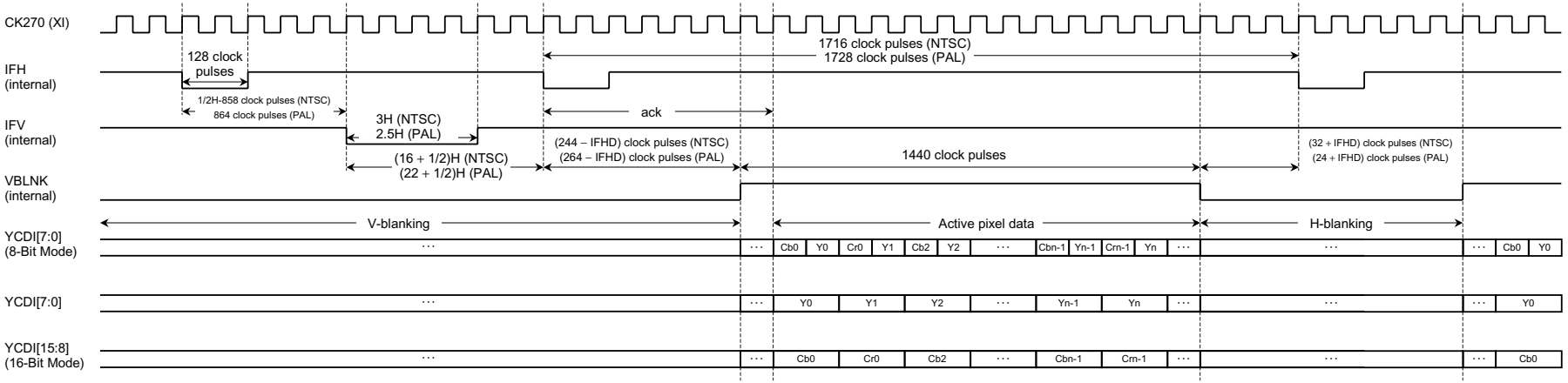


Figure 6-2 Master Mode H-timing (VBLNK external)



Odd fields

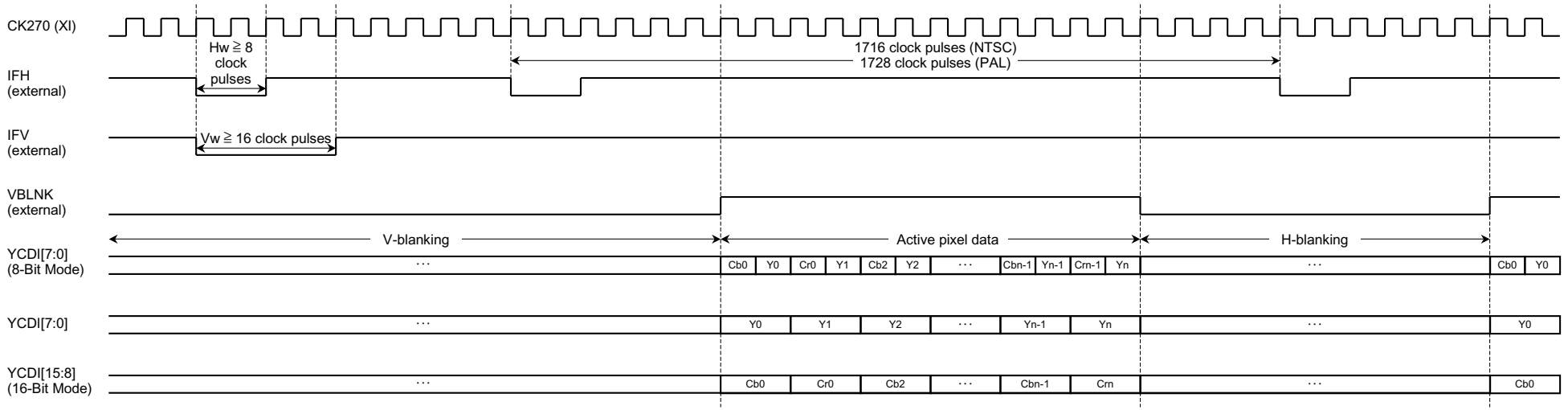


Even fields

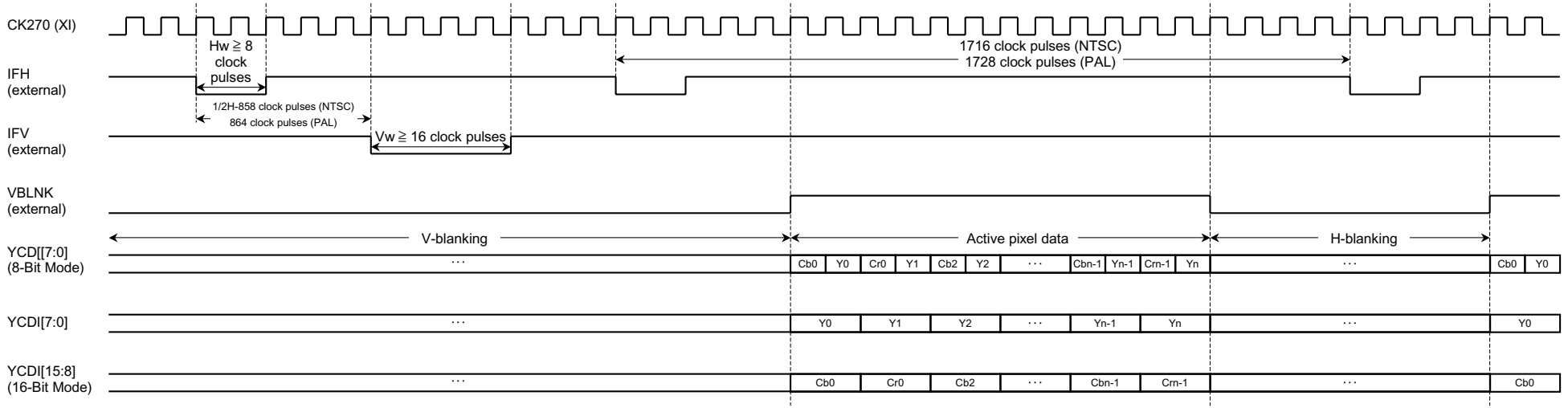
* a is the phase difference between the falling edge and the first pixel data (Cb0).
It can be adjusted using IIC BUS 00-[IFHD1,IFHD0].
(a + IFHD[1:0]) = 4xm clock pulses (m = integer)
e.g.) if a = 245 clock pulses, IFHD[1:0] = 3

* 16-Bit Master Mode
- IFH and IFV are output on the rising edge of CK130.
- YCDI[15:0] are sampled on the rising edge of CK270 (XI).

Figure 6-3 Master Mode H-timing (VBLNK internal)

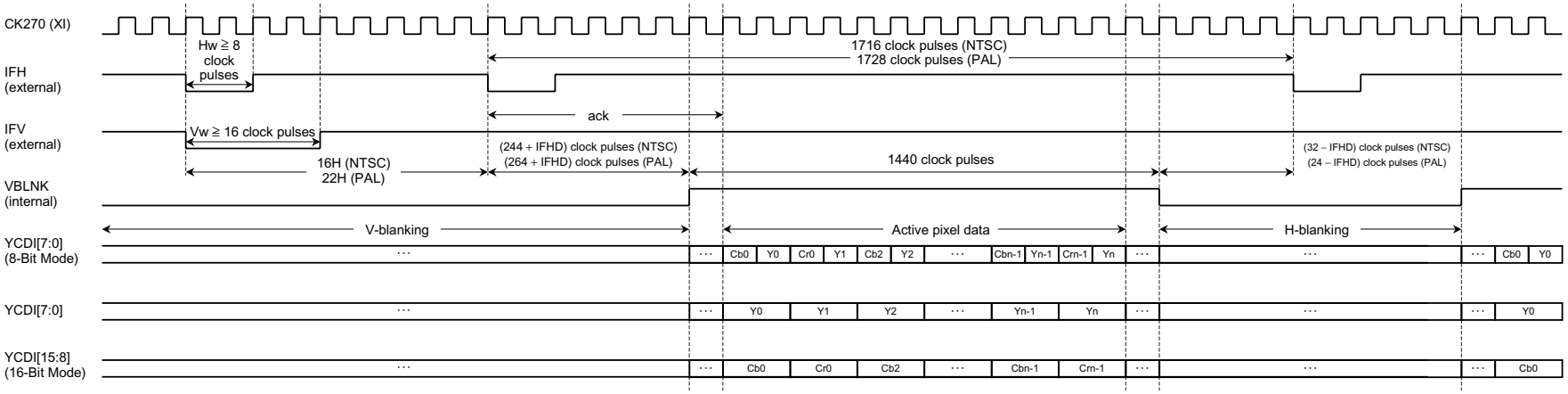


Odd fields

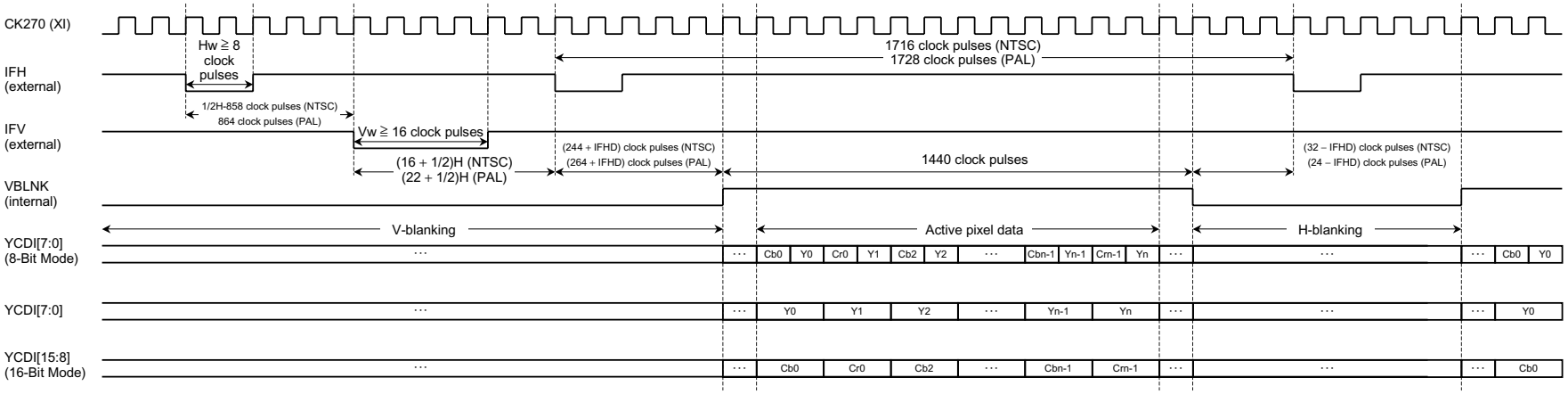


Even fields

Figure 6-4 Slave Mode H-timing (VBLNK-external)



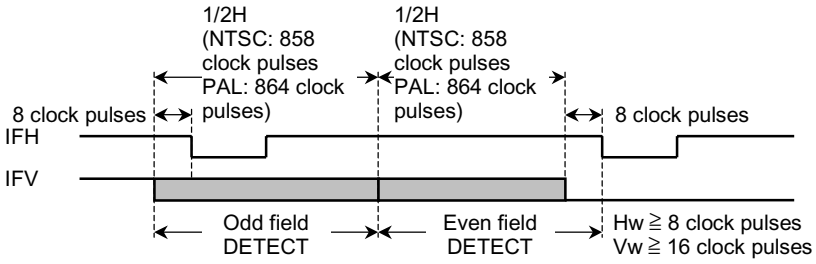
Odd fields



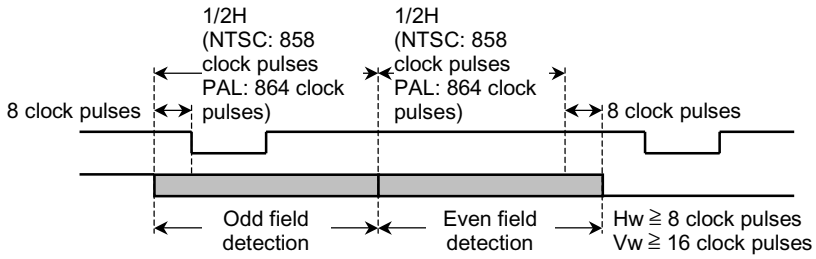
Even fields

Figure 6-5 Slave Mode H-timing (VBLNK- internal)

Slave Mode Detection



Slave Mode (VBLNK external)



Slave Mode (VBLNK-internal)

Figure 7 Slave Mode detection

Sync Signals

The pulse widths of all the sync signals generated by the TC90A32F conform to either the RS-170A standard (for NTSC) or the CCIR Rec. 624-3 standard (for PAL). The following table shows the pulse widths.

NTSC Sync Signals

Signal Name	Function	RS-170A Standard	TC90A32F Pulse Width	TC90A32F Clock Pulses
HSYNC	Horizontal Sync	4.7 ± 0.1 μs	4.70 μs	127
BF	Burst Flag	9 cycles	9 cycles	68
BLK	Horizontal Blanking	10.9 ± 0.2 μs	10.89 μs	294
EQ	Equalization Pulse	2.3 ± 0.1 μs	2.310 μs	62
SR	Serration Pulse	4.7 ± 0.1 μs	4.690 μs	127

PAL Sync Signals

Signal Name	Function	CCIR Rec. 624-3 Standard	TC90A32F Pulse Width	TC90A32F Clock Pulses
HSYNC	Horizontal Sync	4.7 ± 0.1 μs	4.70 μs	127
BF	Burst Flag	10 ± 1 cycle	10 cycles	61
BLK	Horizontal Blanking	12 ± 0.3 μs	12.00 μs	324
EQ	Equalization Pulse	2.35 ± 0.1 μs	2.337 μs	63
SR	Serration Pulse	4.7 ± 0.1 μs	4.701 μs	127

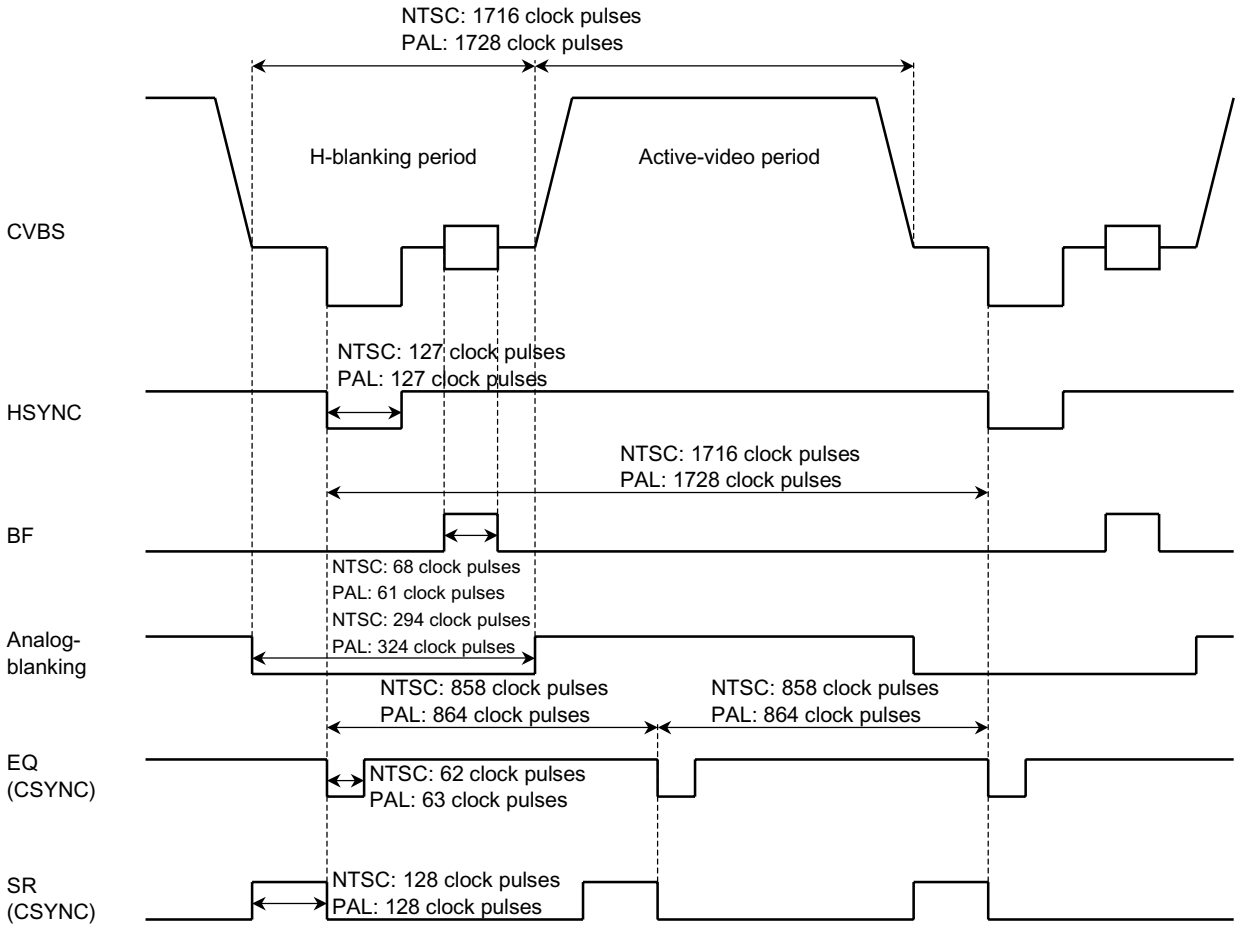


Figure 8 1H-timing

NTSC/PAL V-Timing

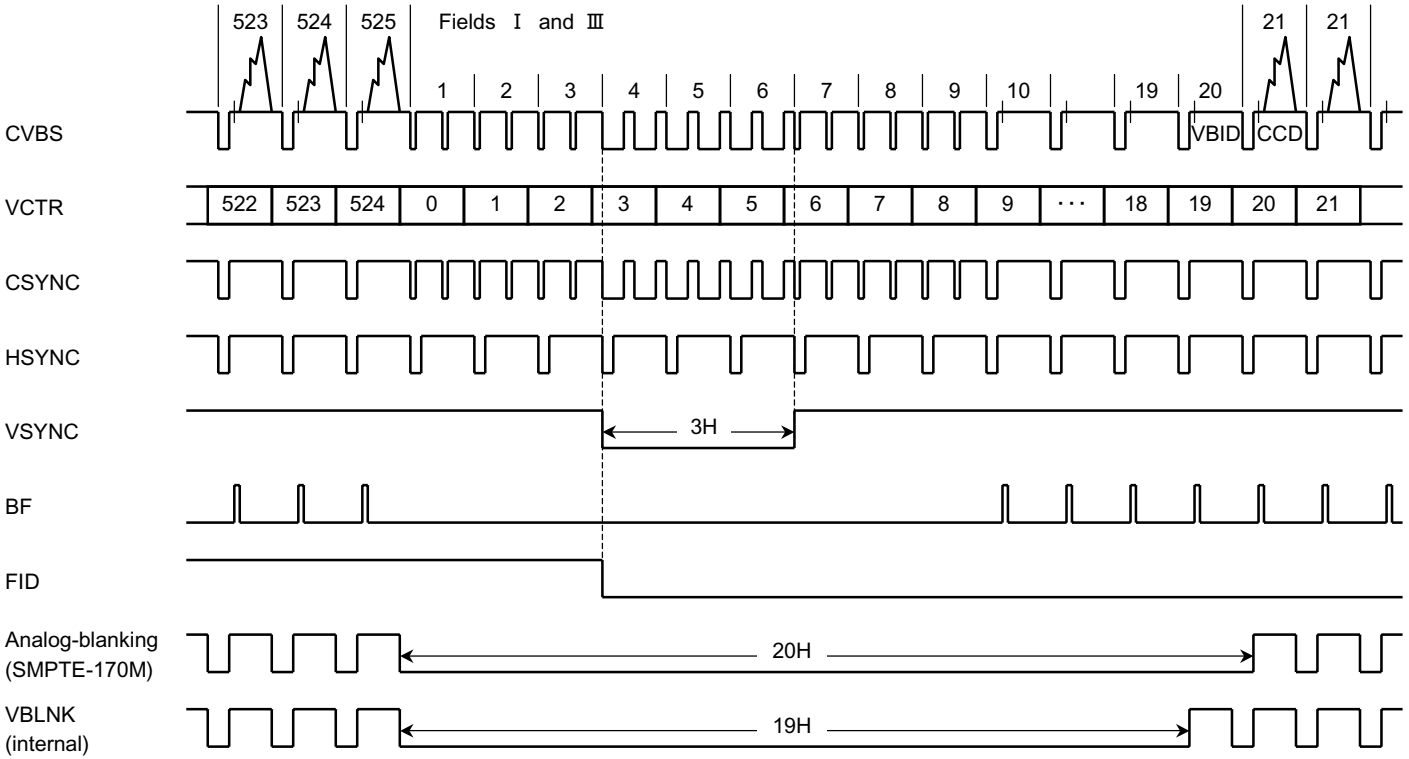


Figure 9-1 NTSC V-timing (odd)

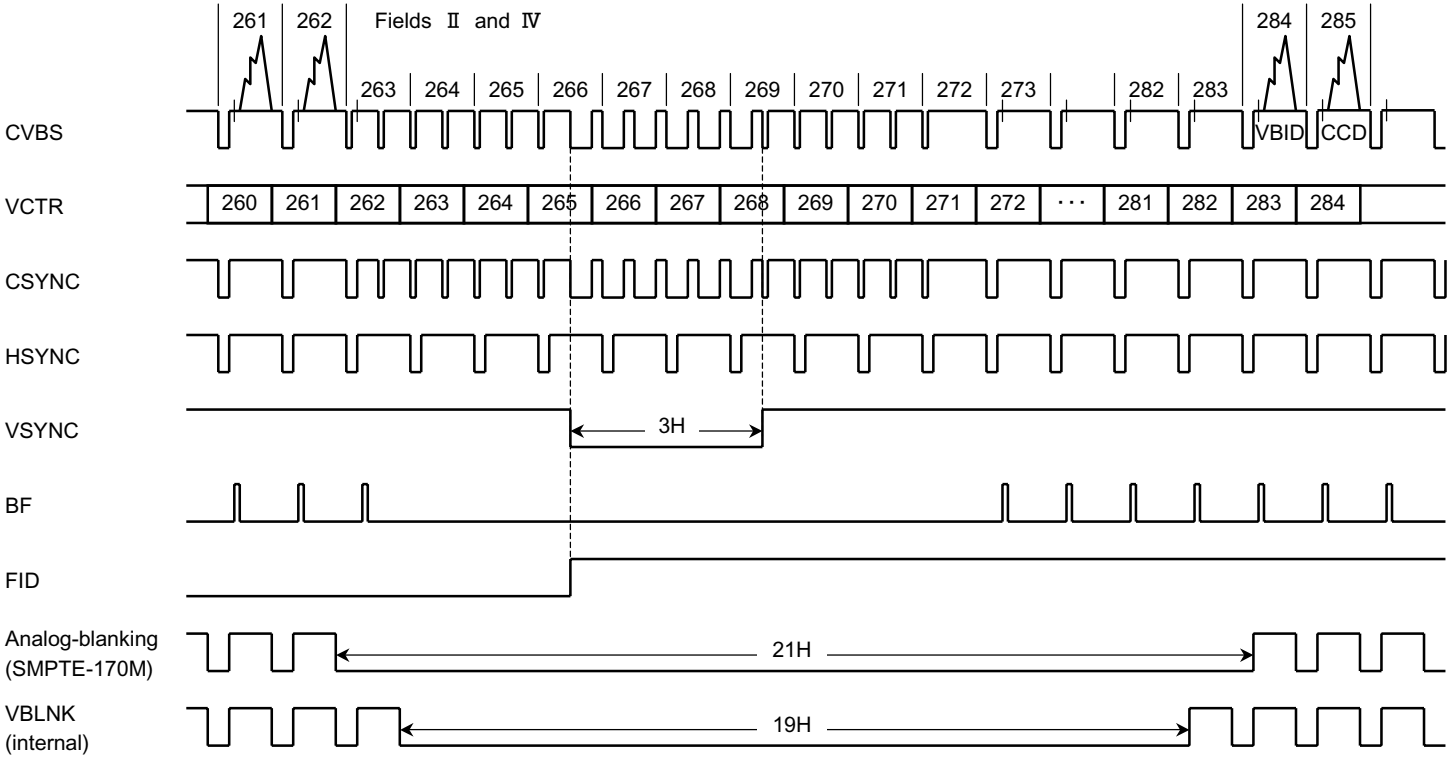


Figure 9-2 NTSC V-timing (even)

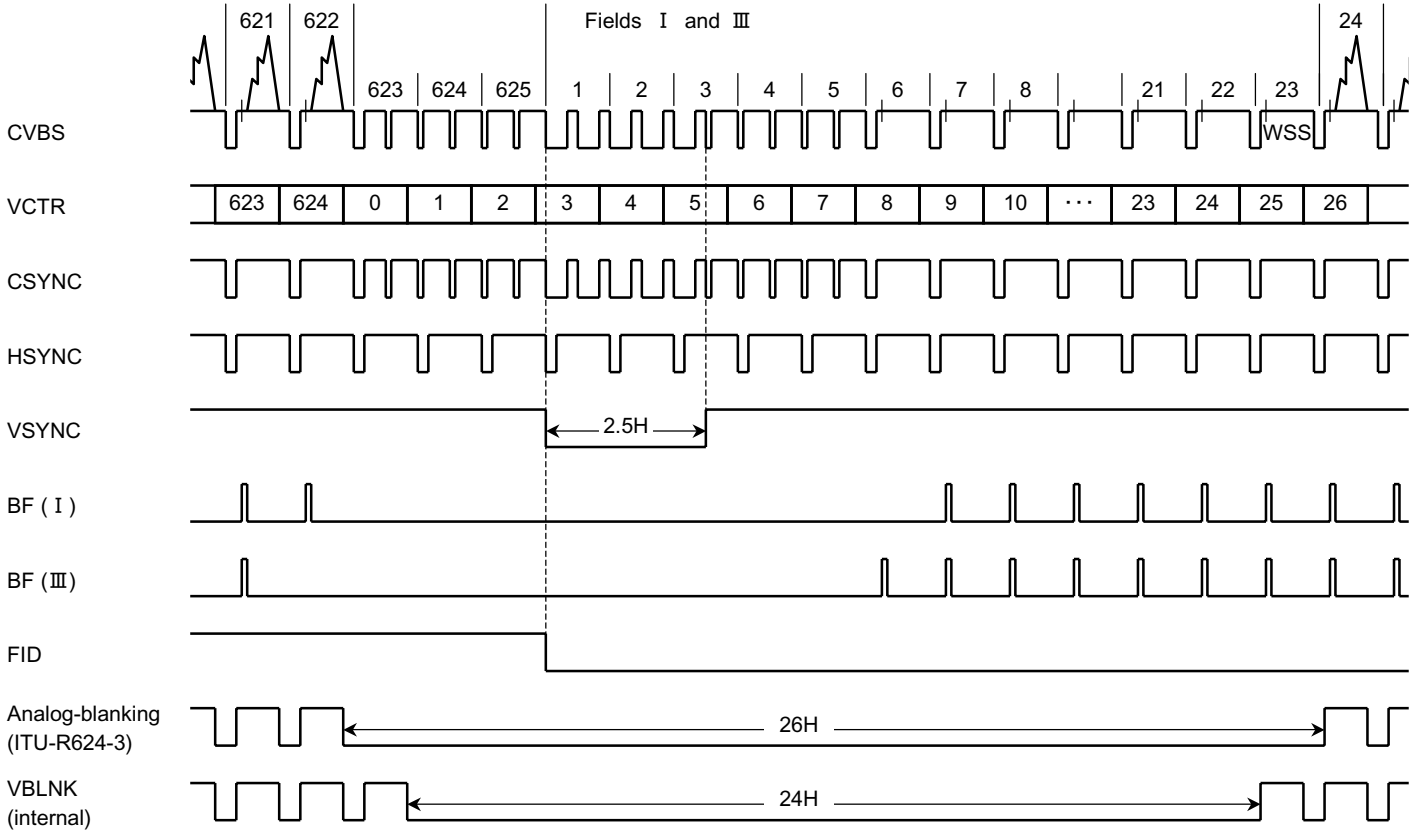


Figure 9-3 PAL V-timing (odd)

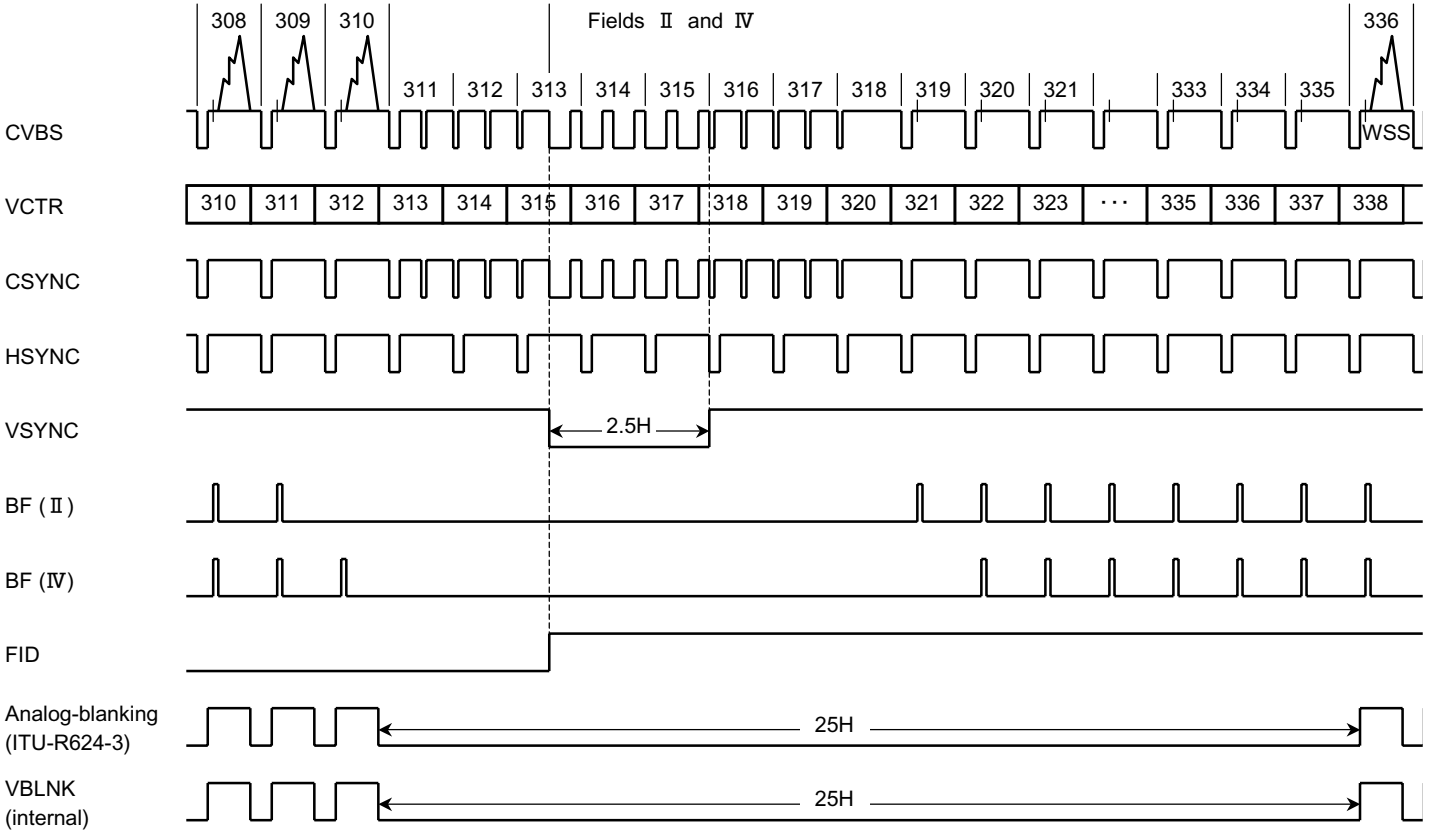


Figure 9-4 PAL V-timing (even)

Video Signal Output Waveforms

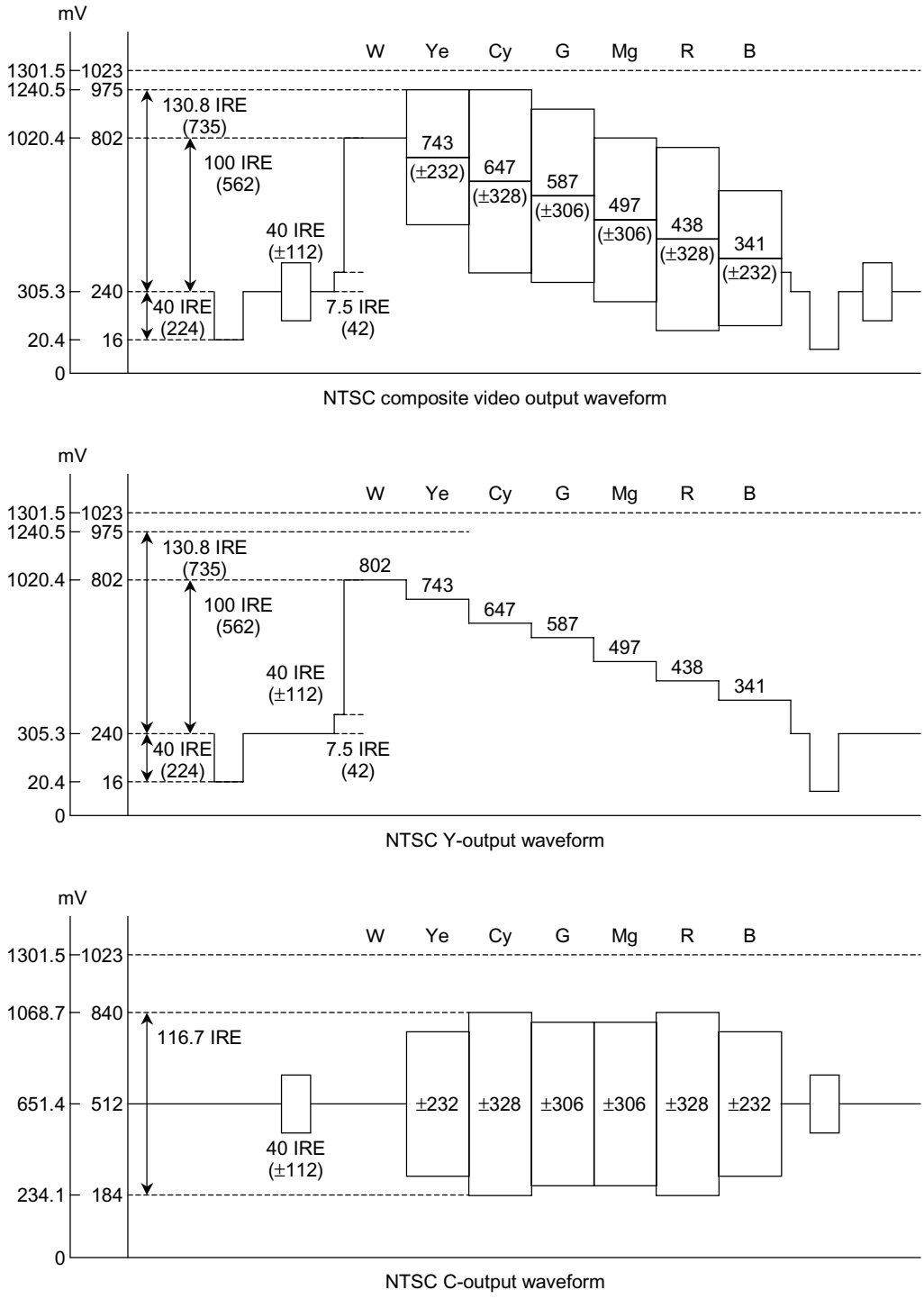


Figure 10-1 NTSC Video Signal Output Waveforms (with 7.5% set-up)

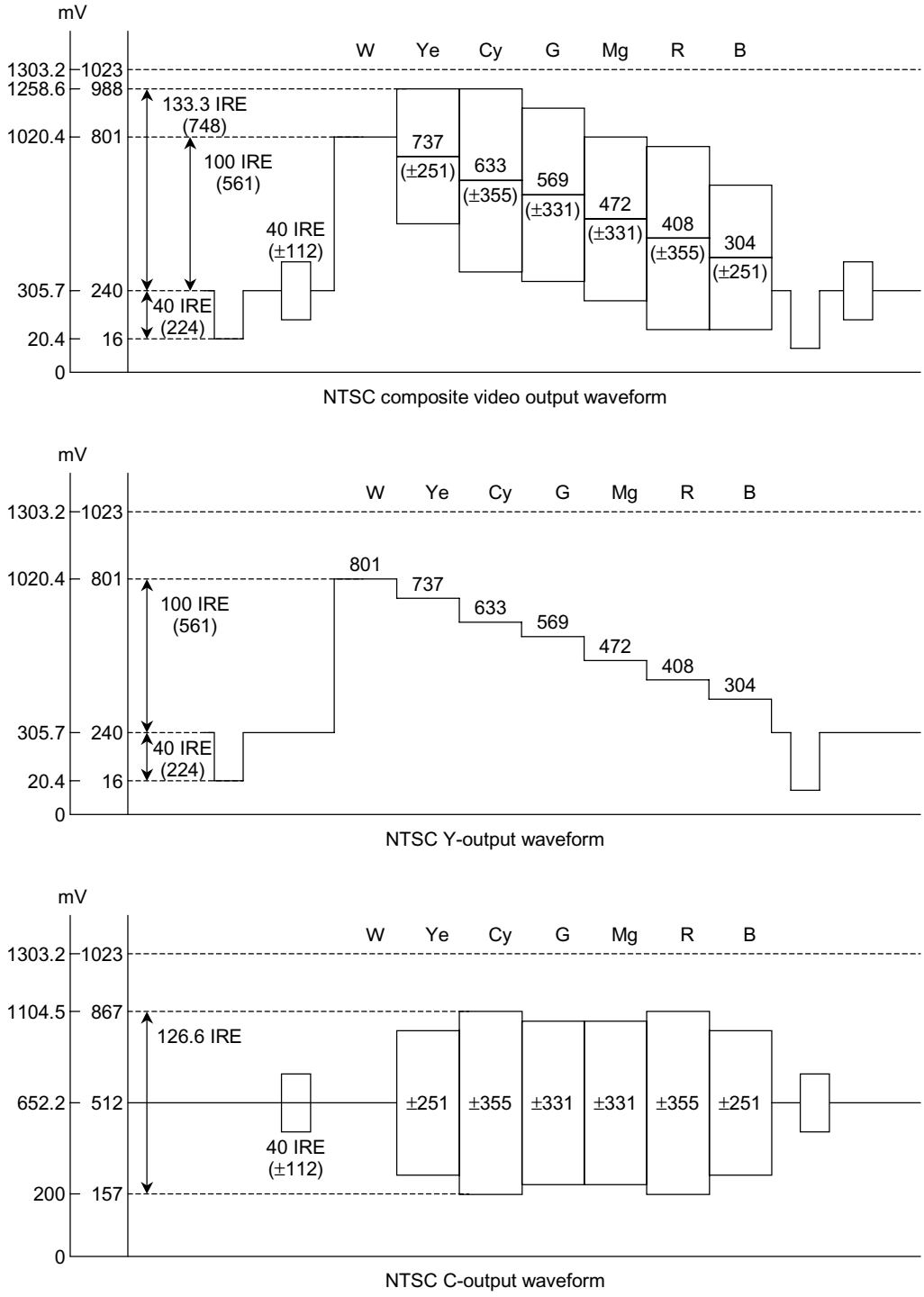


Figure 10-2 NTSC Video Signal Output Waveforms (without 7.5% set-up)

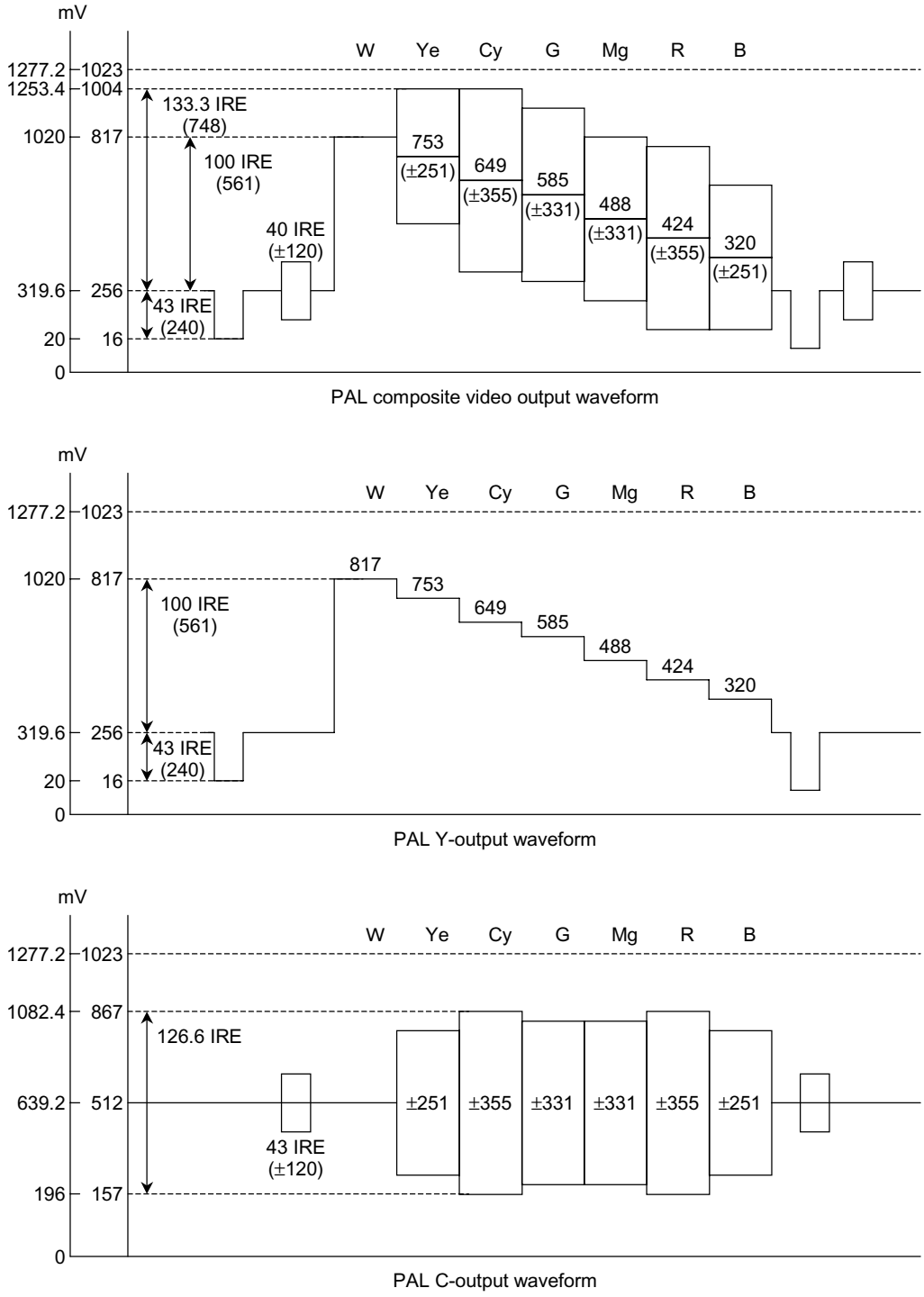
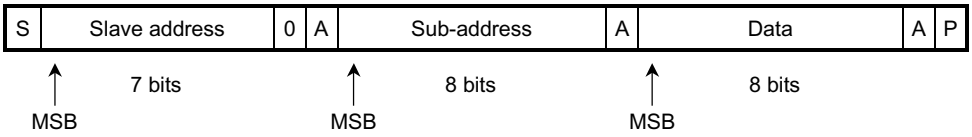


Figure 10-3 PAL Video Signal Output Waveforms

I²C Bus Control Format

The bus control format of the TC90A32F conforms to the Philips I²C bus control format standard.

Data Transfer Format

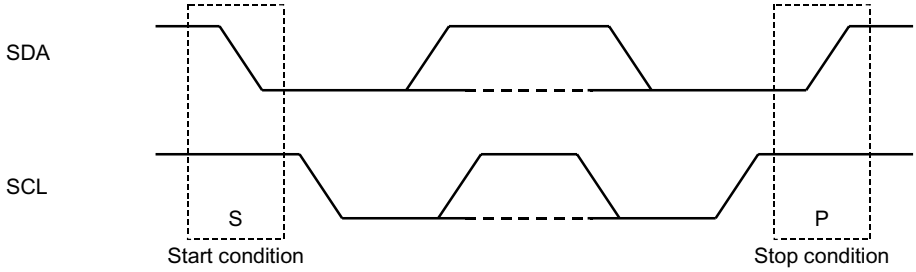


S: Start condition

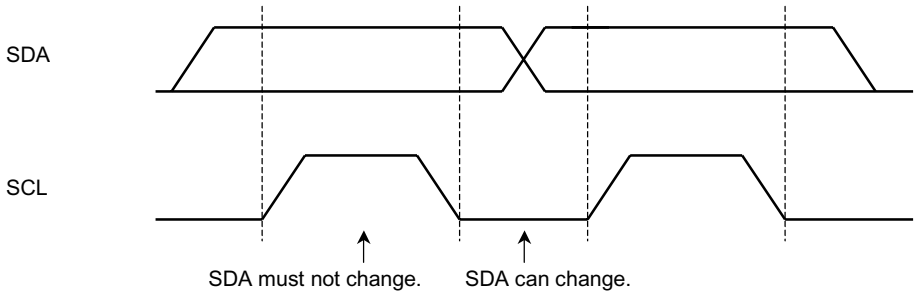
P: Stop condition

A: Acknowledge

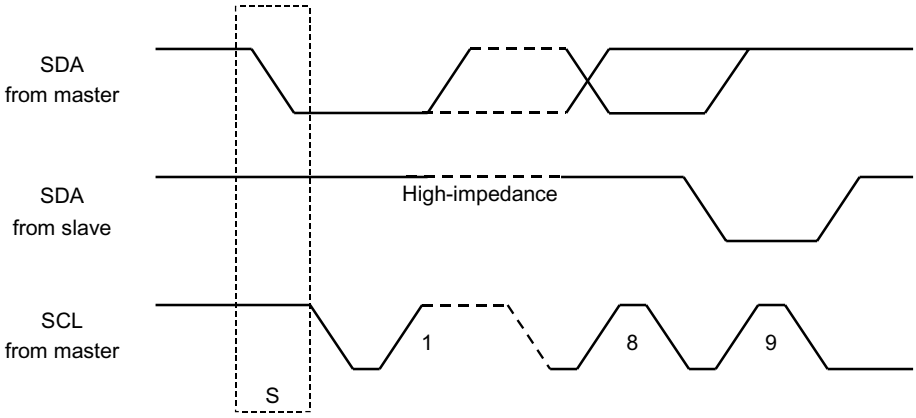
(1) Start condition and stop condition



(2) Bit transfer



(3) Acknowledge



(4) TC90A32F slave address

A6	A5	A4	A3	A2	A1	A0	R/W
0	1	0	0	1	0	0	X

Purchase of TOSHIBA I^2C components conveys a license under the Philips I^2C Patent Right to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by Philips.

I^2C Bus Control Parameters

Parameter	Sub-Address	Register Name	Contents	Default
IFH, IFV Phase Delay Adjustment	00 (H)	IFHD[1:0]	0 to 3 ck	0 ck
IFH Polarity	00	IFHPO	0: Negative polarity 1: Positive polarity	Negative polarity
IFV Polarity	00	IFVPO	0: Negative polarity 1: Positive polarity	Negative polarity
VBLNK Input/Output Selection	01	VBLKIO	0: Input 1: Output	Input
VBLNK Polarity	01	VBLKPO	0: Negative polarity 1: Positive polarity	Positive polarity
Sync Signal ON/OFF Selection	00	SYNDIS	0: ON 1: OFF	ON
Y-Signal ON/OFF Selection	02	YDIS	0: ON 1: OFF	ON
C-Signal ON/OFF Selection	02	CDIS	0: ON 1: OFF	ON
Burst ON/OFF Selection	02	BURDIS	0: ON 1: OFF	ON
YLPF ON/OFF Selection	01	YLPF	0: ON 1: OFF	ON
CLPF ON/OFF Selection	01	CLPF	0: ON 1: OFF	ON
CLPF Characteristics	04	CLPFS	0: 1.5 MHz 1: 3.0 MHz	1.5 MHz
C-Signal ×2 Interpolation ON/OFF Selection	01	CX2OFF	0: OFF 1: ON	ON
Composite Sync Signal Polarity Selection	03	CSPO	0: Negative polarity 1: Positive polarity	Negative polarity
Horizontal Sync Signal Polarity Selection	03	HSPO	0: Negative polarity 1: Positive polarity	Negative polarity
Vertical Sync Signal Polarity Selection	03	VSPO	0: Negative polarity 1: Positive polarity	Negative polarity
Field ID Polarity Selection	03	FIDPO	0: Negative polarity 1: Positive polarity	Negative polarity
Burst Flag Polarity Selection	02	BURPO	0: Negative polarity 1: Positive polarity	Positive polarity
fsc Gain Selection	02	fsc	0.375 V_{p-p}, 0.25 V_{p-p}, 0.5 V_{p-p}	0.375 V_{p-p}
Set-up	01	SETUP	0: Variable 1: Fixed to 7.5%	Variable
Set-up Level Setting	25	SUPD	0 to 42 (0% to 7.5%)	0
Mode Selection	00	NTPAL	0: NTSC 1: PAL	NTSC
Interlace/Non-Interlace Selection	00	INTER	0: Interlace 1: Non-interlace	Interlace
C/fsc Output Selection	03	DAO1	0: C-signal 1: fsc	C-signal
CVBS/fsc Output Selection	03	DAO2	0: CVBS 1: fsc	CVBS
CCD Encoding ON/OFF Selection	05	CCD[2:1]	0: OFF 1: Odd field ON 2: Even field ON 3: Both fields ON	OFF
CCD Parity Bit Internal Operation/Direct Encoding Selection	05	CCDP	0: Internal operation 1: Direct encoding	Internal operation
VBID/WSS Encoding ON/OFF Selection	05	VBON	0: OFF 1: ON	OFF
VBID Parity Bit Internal Operation/Direct Encoding Selection	05	VBIDC	0: Internal operation 1: Direct encoding	Internal operation
VBID Data Encoding Field Selection	05	ODEVON	0: Same data in both fields 1: Data in two fields different	0
WSS Data Encoding Field Selection	28	CHFV	0: Odd field only 1: Both fields	0

I²C Bus Write Registers

Address (H)	MSB Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB Bit 0
00	IFHD1	IFHD0	IFHP0	IFVP0	INTER	SYNDIS	*	NTPAL
01	SETUP	YLPF	CLPF	CLPFS	VBLKIO	VBLKPO	*	*
02	*	*	YDIS	CDIS	BURDIS	BURPO	fsc1	fsc0
03	CSPO	HSPO	VSPO	FIDPO	DAO2	DAO1	*	*
04	CX2OFF	—	*	*	*	*	*	*
05	VBON	CCD2	CCD1	VBIDC	CCDP	—	—	ODEVON
06	VIDA8	VIDA7	VIDA6	VIDA5	VIDA4	VIDA3	VIDA2	VIDA1
07	VIDA14	VIDA13	VIDA12	VIDA11	VIDA10	VIDA9	*	*
08	VIDA20	VIDA19	VIDA18	VIDA17	VIDA16	VIDA15	*	*
09	*	*	*	*	*	*	*	*
0A	CCDP11	CCD116	CCD115	CCD114	CCD113	CCD112	CCD111	CCD110
0B	CCDP12	CCD126	CCD125	CCD124	CCD123	CCD122	CCD121	CCD120
0C	*	*	*	*	*	*	*	*
0D	CCDP21	CCD216	CCD215	CCD214	CCD213	CCD212	CCD211	CCD210
0E	CCDP22	CCD226	CCD225	CCD224	CCD223	CCD222	CCD221	CCD220
0F	*	*	*	*	*	*	*	*
22	REV67	*	*	*	*	*	*	*
23	MACON	*	*	*	*	*	*	*
24	—	—	—	—	—	—	*	*
25	*	*	SUPD5	SUPD4	SUPD3	SUPD2	SUPD1	SUPD0
26	VIDB8	VIDB7	VIDB6	VIDB5	VIDB4	VIDB3	VIDB2	VIDB1
27	VIDB14	VIDB13	VIDB12	VIDB11	VIDB10	VIDB9	*	*
28	VIDB20	VIDB19	VIDB18	VIDB17	VIDB16	VIDB15	*	CHFV
29	*	*	*	*	*	*	*	*
2A	—	—	—	—	—	—	—	—
2B	*	—	—	—	—	—	—	—
2C	—	—	—	—	—	—	—	—
2D	—	—	—	*	—	—	—	—

Note2: * indicates that the valve should be set to 0.

Note3: — indicates that bit setting is for test purposes (default value is 0).

Note4: 10H~21H are for MACROVISION data set.

I²C Bus Read Register

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	*	*	*	*	VBIDW	CCD1W	CCD2W	*

Controls

1. Function Control

SUB 00H (write)

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	IFHD1	IFHD0	IFHPO	IFVPO	INTER	SYNDIS	*	NTPAL
Default	0	0	0	0	0	0	0	0

- IFHD[1:0]: IFH (H sync signal for I/F), IFV (V sync signal for I/F) delay (1 clock pulse = 27 MHz)

IFHD1	IFHD0	Delay	Notes
0	0	+0 clock pulses	1 clock pulse = 27 MHz
0	1	+1 clock pulse	
1	0	+2 clock pulses	
1	1	+3 clock pulses	

- IFHPO: IFH (H sync signal for I/F) polarity selection
  0: Negative polarity 1: Positive polarity

- IFVPO: IFV (V sync signal for I/F) polarity selection
  0: Negative polarity 1: Positive polarity

- INTER: Interlaced or non-interlaced selection
  0: Interlaced 1: Non-interlaced

- SYNDIS: Sync signal ON/OFF selection.
  Applicable to Y and CVBS.
  Outputs CSYNC, HSYNC, VSYNC and FID (monitor output).
  0: ON 1: OFF

- NTPAL: NTSC/PAL mode selection
  0: NTSC 1: PAL

SUB-Address 01H (write)

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	SETUP	YLPF	CLPF	CLPFS	VBLKIO	VBLKPO	*	*
Default	0	0	0	0	0	1	0	0

- SETUP: NTSC set-up level selection
  0: changeable (0 to 7.5%)
  Set-up level from 0~7.5%
  Set-up level is set by SUPD[5:0] (SUB 26H).

  1: fixed at 7.5%

- YLPF: Y-LPF (6 M) ON/OFF selection
  0: ON 1: OFF

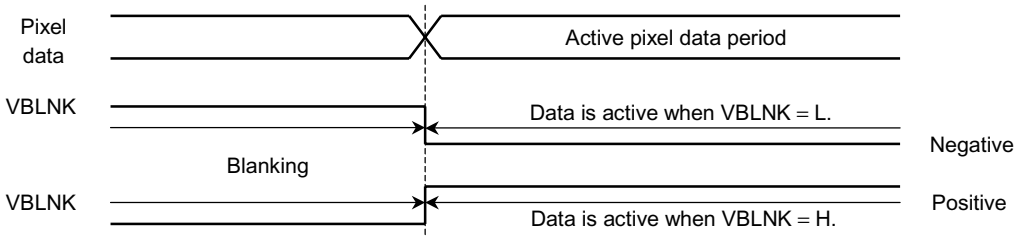
- CLPF: C-LPF (1.5 M/3 M) ON/OFF selection
  0: ON 1: OFF

- CLPFS: C-LPF characteristic selection
  0: 1.5 MHz 1: 3 MHz

- VBLKIO: VBLNK (video blanking signal for I/F) input/output selection
  0: Input 1: Output

- VBLKPO: VBLNK (video blanking signal for I/F) polarity selection
  (polarity of VBLNK for active pixel data input)
  0: Negative polarity 1: Positive polarity

  *: Set to 0 when VBLNK has negative polarity, and to 1 when VBLNK has positive polarity.



Sub-Address 02H (write)

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	*	*	YDIS	CDIS	BURDIS	BURPO	fsc1	fsc0
Default	0	0	0	0	0	1	0	0

- YDIS: Turns Y-signal output ON/OFF.

  Selecting OFF (YDIS = 1) invalidates all Y-signal inputs and outputs at pedestal level.
  Note that all sync signals are output. Applies to Y-signal and composite video signals.
  0: ON 1: OFF

- CDIS: Turns C-signal output ON/OFF.

  Selecting OFF (CDIS = 1) invalidates all Cb/Cr signal inputs and causes them to be output as gray scales.
  Note that burst signals are output. Applies to C-signal and composite video signals.
  0: ON 1: OFF

- BURDIS: Turns burst output ON/OFF.

  The Burst flag (BF) value is output even when this bit is set to OFF.
  Applies to C-signal and composite video signals.
  0: ON 1: OFF

- BURPO: Selects the Burst flag monitor output (BF) polarity.

  0: Negative polarity 1: Positive polarity

- fsc [1:0]: Selects the fsc output gain.

fsc1	fsc0	Gain
0	0	0.375 V_{pp}
0	1	0.25 V_{pp}
1	—	0.5 V_{pp}

Sub-Address 03H (write)

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	CSPO	HSPO	VSPO	FIDPO	DAO2	DAO1	*	*
Default	0	0	0	0	0	0	0	0

- CSPO: Selects the composite sync monitor output (CSYNC) polarity.
  0: Negative polarity 1: Positive polarity
- HSPO: Selects the horizontal sync signal monitor output (HSYNC) polarity.
  0: Negative polarity 1: Positive polarity
- VSPO: Selects the vertical (sync) signal monitor output polarity.
  0: Negative polarity 1: Positive polarity
- FIDPO: FID (field identify signal monitor output) polarity selection
  0: ODD = L 1: ODD = H
  EVEN = H EVEN = L
- DAO2: CVBS/fsc (pin 29) output selection
  0: CVBS output 1: fsc output (for testing purposes)
- DAO1: C/fsc (pin 25) output selection
  0: C output 1: fsc output (for testing purposes)

Sub-Address 04H (write)

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	CX20FF	—	*	*	*	*	*	*
Default	1	0	0	0	0	0	0	0

- CX20FF: C-signal ×2 interpolation ON/OFF selection (CMOD block)
  0: ×2 interpolation OFF 1: ×2 interpolation ON

Sub-Address 25H (write)

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	*	*	SUPD5	SUPD4	SUPD3	SUPD2	SUPD1	SUPD0
Default	0	0	0	0	0	0	0	0

- SUPD [5:0]: Set-up level setting register
  When SETUP (01H[7]) = 0, SETUP can be set in the range 0%~7.5% (0~42).
  If the value of the data is greater than or equal to 42 (i.e. 42~63), forcibly set this value to 42.

2. CCD/VBID/WSS Encoding

Sub-Address 05H (write)

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	VBON	CCD2	CCD1	VBIDC	CCDP	—	—	ODEVON
Default	0	0	0	0	0	0	0	0

- VBON: Turns VBID (NTSC)/WSS (PAL) encoding ON/OFF.
  0: ON 1: OFF

- CCD [2:1]: Selects closed-caption encoding mode.

CCD2	CCD1	Setting
0	0	Closed-caption encoding OFF
0	1	Field 1 (21 lines) encoding ON
1	0	Field 2 (284 lines) encoding ON
1	1	Encoding for both fields ON

- VBIDC: Selects internal operation or direct encoding for the CRC code (bits 14~19) in VBID (NTSC) data or for the parity bit (bit 3) in WSS (PAL) data.
  0: Internal operation (processing is carried out within the IC; the CRC code or parity bit is then inserted into the image data.)
  1: Direct encoding (the microcontroller writes the CRC code or parity bit directly to the IIC BUS register, thus inserting it into the image data).

  *: VID[20:15] of VBID (NTSC) sub-address 08H
  VID4 of WSS (PAL) sub-address 06H

- CCDP: Selects internal operation or direct encoding for the closed-caption parity bit.
  0: Internal operation (processing is carried out within the IC; the closed-caption parity bit is then inserted into the image data)
  1: Direct encoding (the microcontroller writes the closed-caption parity bit directly to the IIC BUS register, thus inserting it into the image data).

  *: Input bit CCDP11 of sub-address 0AH into character #1 of field 1.
  Input bit CCDP12 of sub-address 0BH into character #2 of field 1.
  Input bit CCDP21 of sub-address 0DH into character #1 of field 2.
  Input bit CCDP22 of sub-address 0EH into character #2 of field 2.

- ODEVON: Selects the encoding method for the VBID/WSS data.
  NTSC Mode (VBID):
  0: The same data is encoded in both fields. 1: Data encoded in the two fields is different.

  PAL Mode (WSS):
  Determined in combination with CHFV (sub-address 28H).
  If CHFV = 1:
  0: The same data is encoded in both fields. 1: Data encoded in the two fields is different.

SUB-Address 06 to 08H (write)

- NTSC-VBID data-setting registers (VBID data is added to lines 20H and 283H. (◇ is used for CGMS-A))

  In NTSC Mode, the same data is added to both the odd and even fields. In PAL mode, data is added to the odd field only. If it is required that data be added to both fields in the future, bits VIDB20~VIDB1 of addresses 28H~2AH should be used.

Sub-Address 06H (write)

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	◇VIDA8	◇VIDA7	VIDA6	VIDA5	VIDA4	VIDA3	VIDA2	VIDA1
Default	0	0	0	0	0	0	0	0
	b7	b6	b5	b4	b3	b2	b1	b0

Sub-Address 07H (write)

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	◇VIDA14	◇VIDA13	◇VIDA12	◇VIDA11	◇VIDA10	◇VIDA9	*	*
Default	0	0	0	0	0	0	0	0
	b13	b12	b11	b10	b9	b8		

SUB-Address 08H (write)

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	◇VIDA20	◇VIDA19	◇VIDA18	◇VIDA17	◇VIDA16	◇VIDA15	*	*
Default	0	0	0	0	0	0	0	0
	b19	b18	b17	b16	b15	b14		

- VID [3:1]: WORD0-A (bits [2:0] - identification signal which varies according to video transfer method)

Name	Descripton	0	1
VID1	Aspect ratio	4:3	16:9
VID2	Letterbox	Normal	Letterbox
VID3	Reserved	—	—

- VID [6:4]: WORD0-B (bits [5:3] - identification signal which varies according to video and other signals (e.g. sound) which are transferred with video)

- VID [10:7]: WORD1 (bits [9:6] - identification signal dependent on WORD0)

  ◇VID [8:7]: CGMS

VID7	VID8	Description
0	0	Copying OK
0	1	Not used
1	0	Copying once OK
1	1	No copying

◇VID [10:9]: APS

VID9	VID10	Description
0	0	AGC pulse OFF, Burst invert OFF
0	1	AGC pulse ON, Burst invert OFF
1	0	AGC pulse ON, Burst invert ON (2 lines at a time)
1	1	AGC pulse ON, Burst invert ON (4 lines at a time)

- VID [14:11]: WORD2 (bits [13:10] - identification signal and information dependent on WORD0)

◇VID11: ASB

VID11	Description
0	Analog pre-recording package media not used
1	Analog pre-recording package media

- VID [20:15]: CRC code (bits [19:14]) is effective when Direct Encode (SUB 05H – VBIDC) = 1.

◇VID [20:15]: same as above

PAL-WSS Data-Setting Registers (data is added to line 23H)

Sub-Address 06H (write)

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	VIDA8	VIDA7	VIDA6	VIDA5	VIDA4	VIDA3	VIDA2	VIDA1
Default	0	0	0	0	0	0	0	0
	b7	b6	b5	b4	b3	b2	b1	b0

Sub-Address 07H (write)

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	VIDA14	VIDA13	VIDA12	VIDA11	VIDA10	VIDA9	*	*
Default	0	0	0	0	0	0	0	0
	b13	b12	b11	b10	b9	b8		

*: SUB 08H is not used.

- VID [4:1]: group 1 (bits [2:0] - information relating to aspect ratio, bit 3 is odd parity bit)

VID1	VID2	VID3	VID4	Aspect Ratio	Full Format/Letterbox	Position
0	0	0	1	4:3	Full format	—
1	0	0	0	14:9	Letterbox	Center
0	1	0	0	14:9	Letterbox	Top
1	1	0	1	16:9	Letterbox	Center
0	0	1	0	> 16:9	Letterbox	Top
1	0	1	1	14:9	Letterbox	Center
0	1	1	1	14:9	Full format	Center
1	1	1	0	16:9	Full format	—

*: Parity bit (VID4-b3) is effective when Direct Encode (SUB 05H – VBIDC) = 1.

- VID [8:5]: Group 2 (bits [7:4] - additional information)

  VID5: Film bit

VID5	Description
0	Camera Mode
1	Film Mode

- VID6 : Color-coding bit

VID6	Description
0	Standard coding
1	Motion adaptive color plus

- VID7: Helper bit

VID7	Description
0	No helper
1	Modulated helper

  *: Helper signal may only be present when the aspect ratio is either 16:9 letterbox center or > 16:9 letterbox center.

- VID8: Reserved (should be set to 0.)

- VID9 [11:9]: Group3 (bits [10:8] - information relating to subtitles)

  VID9: Subtitles within teletext selection

VID9	Description
0	No subtitles within teletext
1	Subtitles within teletext

  VID [11:10]: Subtitle mode selection

VID10	VID11	Description
0	0	No subtitles
1	0	Subtitles in active image area
0	1	Subtitles out of active image area
1	1	Reserved

- VID [14:12]: Group 4 (bits [13:11] - other)

  VID12: Surround-sound bit

VID12	Description
0	No surround-sound
1	Surround-Sound Mode

  VID [14:13]: Reserved (should be set to 0.)

Sub-Addresses 26H~28H (write)

- VBID (NTSC)/WSS (PAL) Data Setting Registers

  In cases where the even and odd fields are set to different values (as explained previously), the even-numbered fields are set using the registers shown below.

Sub-Address 26H (write)

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	VIDB8	VIDB7	VIDB6	VIDB5	VIDB4	VIDB3	VIDB2	VIDB1
Default	0	0	0	0	0	0	0	0
	b7	b6	b5	b4	b3	b2	b1	b0

Sub-Address 27H (write)

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	VIDB14	VIDB13	VIDB12	VIDB11	VIDB10	VIDB9	*	*
Default	0	0	0	0	0	0	0	0
	b13	b12	b11	b10	b9	b8		

Sub-Address 28H (write)

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	◇VIDB20	◇VIDB19	◇VIDB18	◇VIDB17	◇VIDB16	◇VIDB15	*	CHFV
Default	0	0	0	0	0	0	0	0
	b19	b18	b17	b16	b15	b14		

CHFV: VBID/WSS data encoding selection
Selects according to the combination with ODEVON (sub-address 05H)
0: encodes the data in the odd field.
1: when ODEVON = 0, encodes the same data in both fields.
1: when ODEVON = 0, encodes different data in each field.

CCD Data Setting Registers

Sub-Address 0AH (write) Closed-caption character #1 data (odd 21H)

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	CCDP11	CCD116	CCD115	CCD114	CCD113	CCD112	CCD111	CCD110
Default	0	0	0	0	0	0	0	0
chara#1	P1	b6	b5	b4	b3	b2	b1	b0

- CCDP11: Closed-caption character #1 data (odd 21H) odd parity bit
  Effective when Direct Encode (SUB 05H – CCDP) = 1
- CCD11 [6:0]: Closed-caption character #1 data (odd 21H)

Sub-Address 0BH (write) Closed-caption character #2 data (odd 21H)

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	CCDP12	CCD126	CCD125	CCD124	CCD123	CCD122	CCD121	CCD120
Default	0	0	0	0	0	0	0	0
chara#1	P2	b6	b5	b4	b3	b2	b1	b0

- CCDP12: Closed-caption character #2 data (odd 21H) odd parity bit
  Effective when Direct Encode (SUB 05H – CCDP) = 1
- CCD12 [6:0]: Closed-caption character #2 data (odd 21H)

Sub-Address 0DH (write) Closed-caption character #1 (even 284H)

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	CCDP21	CCD216	CCD215	CCD214	CCD213	CCD212	CCD211	CCD210
Default	0	0	0	0	0	0	0	0
chara#1	p1	b6	b5	b4	b3	b2	b1	b0

- CCDP21: Closed-caption character #1 data (even 284H) odd parity bit
  Effective when Direct Encode (SUB 05H – CCDP) = 1
- CCD21 [6:0]: Closed-caption character #1 data (even 284H)

Sub-Address 0EH (write) Closed-caption character #2 data (even 284H)

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	CCDP22	CCD226	CCD225	CCD224	CCD223	CCD222	CCD221	CCD220
Default	0	0	0	0	0	0	0	0
chara#2	p2	b6	b5	b4	b3	b2	b1	b0

- CCDP22: Closed-caption character #2 data (even 284H) odd parity bit
  Effective when Direct Encode (SUB 05H – CCDP) = 1
- CCD22 [6:0]: Closed-caption character #2 data (even 284H)

3. Copy Guard Function (MACROVISION)

Sub-Address 22H (write)

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	REV67	*	*	*	*	*	*	*
Default	0	0	0	0	0	0	0	0

- REV67: MACROVISION revision selection
  0: Rev. 7.01 1: Rev. 6.1

Sub-Address 23H (write)

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	MACON	*	*	*	*	*	*	*
Default	0	0	0	0	0	0	0	0

- MACON: Copy guard function ON/OFF
  0: OFF 1: ON

Read Registers

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	*	*	*	*	VBIDW	CCD1W	CCD2W	*

- VBIDW: VBID data can/cannot be written.
  0: Data cannot be written 1: Data can be written

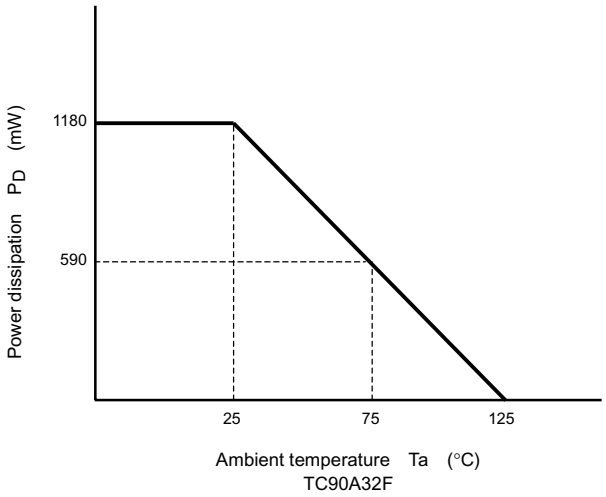
- CCD1W: Closed-caption data (odd 21H) can/cannot be written.
  0: Data cannot be written 1: Data can be written

- CCD2W: Closed-caption data (even 284H) can/cannot be written.
  0: Data cannot be written 1: Data can be written

Absolute maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Supply voltage	V_{DD}	V_{SS} to V_{SS} + 4.5	V
Input voltage	V_{IN}	−0.3 to V_{DD} + 0.3	V
Power dissipation	P_D	1180	mW
Storage temperature	T_{stg}	−55 to 125	°C

Ta-P_D (on-board mounting)



Recommended Operating Conditions

Characteristic	Symbol	Condition	Min	Typ.	Max	Unit
Supply voltage	V_{DD}	—	3.0	3.3	3.6	V
Input voltage	V_{IN}	—	0	—	V_{DD}	V
Operating temperature	T_{opr}	—	−20	—	70	°C

Electrical Characteristics

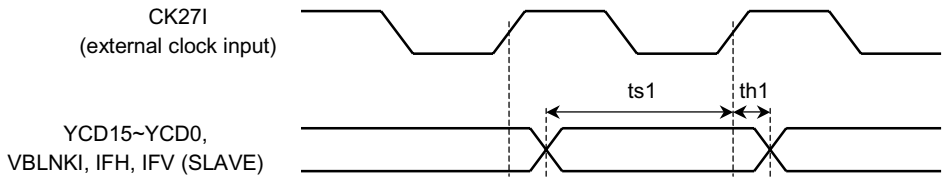
DC Characteristics (V_{DD} = 3.0 V~3.6 V, V_{IN} = 0 V~V_{DD}, Ta = –20°C~75°C, V_{SS} = 0 V)

Characteristics		Symbol	Test circuit	Test condition	Min	Typ.	Max	Unit
Current dissipation		I_{DD}	—	—	—	100	—	mA
High-level input voltage	CMOS	V_{IH}	—	—	2.3	—	—	V
	SCHMITT				2.65	—	—	
Low-level input voltage	CMOS	V_{IL}	—	—	—	—	1.0	V
	SCHMITT				—	—	0.65	
Input current	High-level1	I_{IH1}	—	V_{IN} = V_{DD}	—	—	10	µA
	Low-level1	I_{IL1}	—	V_{IN} = V_{SS}	—	—	10	
	High-level2	I_{IH2}	—	V_{IN} = V_{DD}	—	—	10	
	Low-level2	I_{IL2}	—	V_{IN} = V_{SS}	—	—	10	
Output voltage	High-level1	V_{OH1}	—	I_{OH} = 5.4 mA	2.4	—	—	V
	Low-level1	V_{OL1}	—	I_{OL} = 5.3 mA	—	—	0.4	
	High-level2	V_{OH2}	—	I_{OH} = 10.5 mA	2.4	—	—	
	Low-level2	V_{OL2}	—	I_{OL} = 10.5 mA	—	—	0.4	

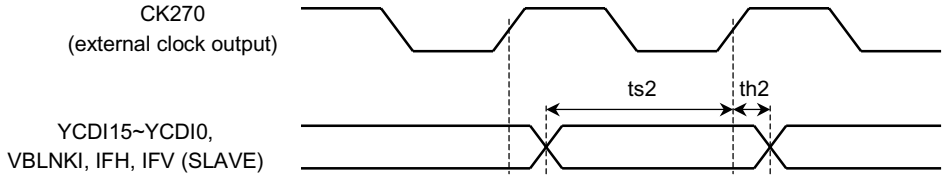
AC Characteristics (V_{DD} = 3.0 V~3.6 V, V_{IN} = 0 V~V_{DD}, Ta = –20°C~75°C, V_{SS} = 0 V)

Characteristics	Symbol	Test circuit	Test condition	Min	Typ.	Max	Unit
Operating frequency conditions	f_{CLK}	—	—	—	27	—	MHz
Input set-up time 1	ts1	—	For YCDI15~YCDI0	3	—	—	ns
			For VBLNKI, IFH, IFV (slave)	2			
Input hold time 1	th1	—	For YCDI15~YCDI0	9	—	—	ns
			For VBLNKI, IFH, IFV (slave)	7			
Input set-up time 2	ts2	—	CK270 output load = 30 pF, for YCDI15~YCDI0 (*1)	14	—	—	ns
			CK270 output load = 30 pF, for VBLNKI, IFH, IFV (slave) (*2)	14			
Input hold time 2	th2	—	(*1)	–1	—	—	ns
			(*2)	–3			
Input set-up time 3	ts3	—	CK130 output load = 30 pF, for YCDI15~YCDI0 (*3)	20	—	—	ns
			CK130 output load = 30 pF, for VBLNKI, IFH, IFV (slave) (*4)	20			
Input hold time 3	th3	—	(*3)	0	—	—	ns
			(*4)	–3			
Output propagation delay time 1	tpd1	—	出力ピン負荷 C_{L3} = 30 pF	8	—	23	ns
Output propagation delay time 2	tpd2		出力ピン負荷 C_{L3} = 30 pF	5	—	16	ns
Output propagation delay time 3	tpd3		出力ピン負荷 C_{L3} = 30 pF	6	—	22	ns

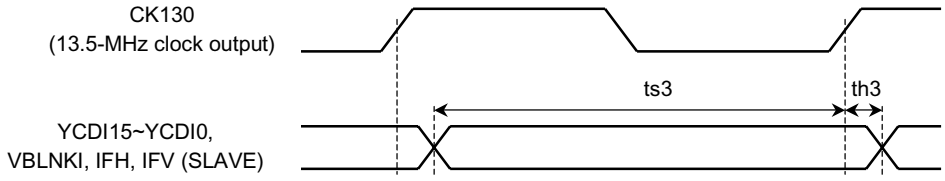
***Input Set-up/Hold Time 1**



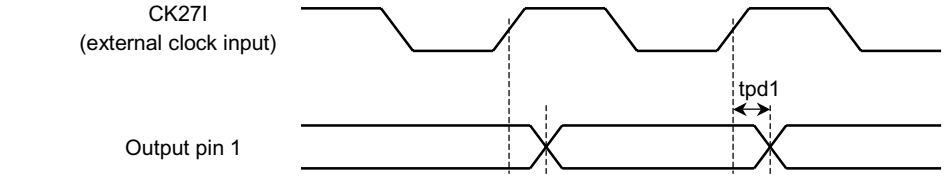
***Input Set-up/Hold Time 2**



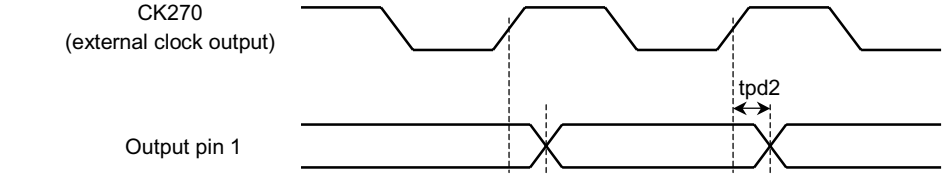
***Input Set-up/Hold Time 3**



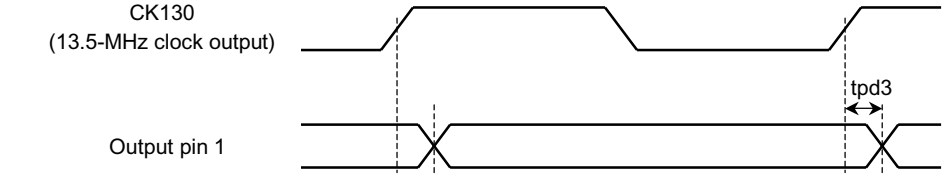
***Output Propagation Delay Time 1**



***Output Propagation Delay Time 2**



***Output Propagation Delay Time 3**



DAC Characteristics (V_{DD} = 3.0~3.6 V, V_{IN} = 0 V~V_{DD}, Ta = –20~75°C, V_{SS} = 0 V)

Characteristics	Symbol	Test circuit	Test condition	Min	Typ.	Max	Unit
Resolution	—	—	—	—	—	10	Bits
Integral linear error	ILE	—	—	—	1	—	LSB
Differential linear error	DLE	—	—	—	1	—	LSB
Output dynamic range	V_{Reg}	—	$V_{REF} = V_{DD} - 1.5$ V (Note5)	—	1.5	—	V_{p-p}
Current dissipation	I_{DD}	—	—	—	10	—	mA

Note5: Please ensure that neither of the following conditions arise:

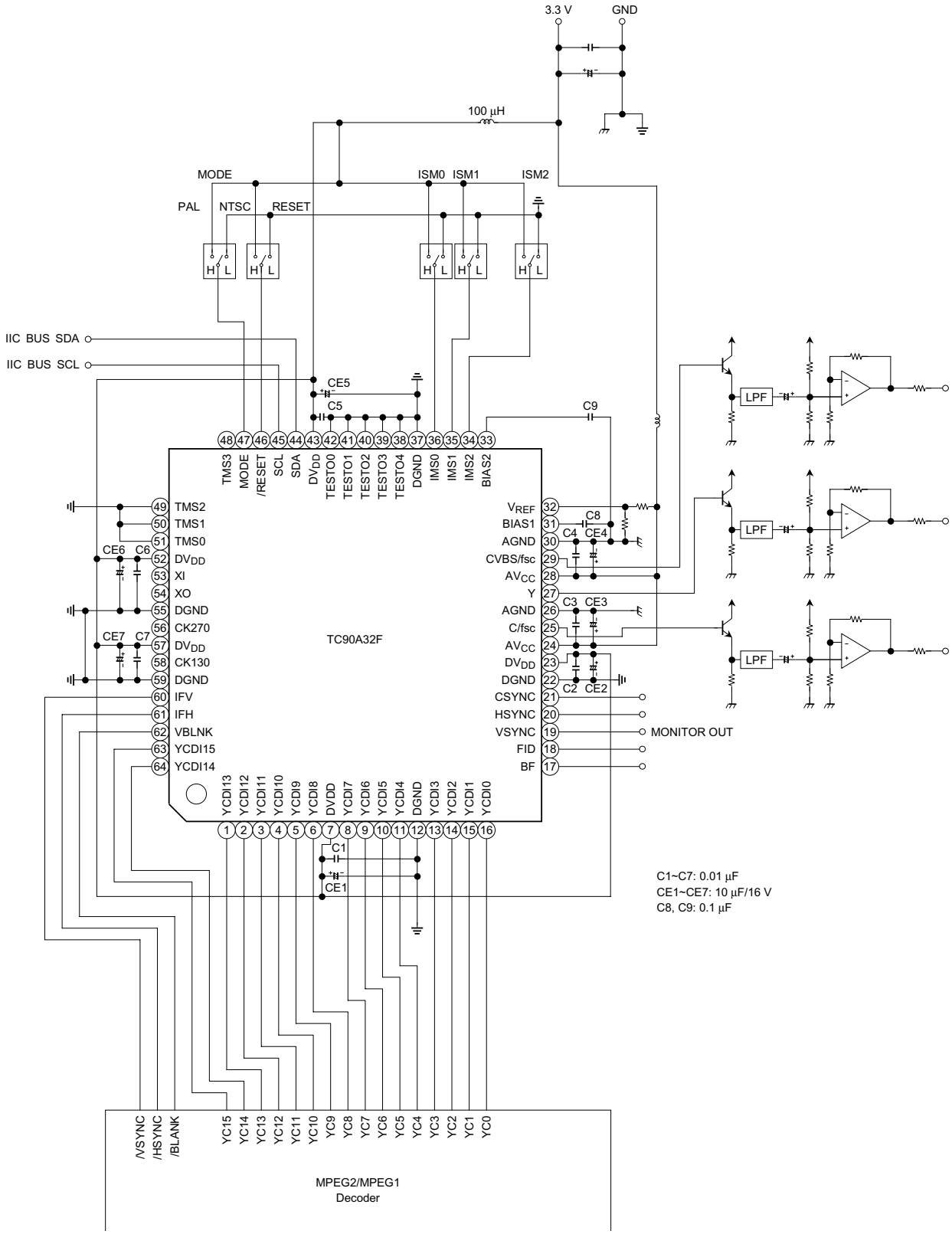
V_{REF} (pin 32) is the reference voltage for the DAC.

(1) $V_{REF} < AV_{DD} - 1.60$ V or $AV_{DD} - V_{REF} > 1.60$ V

(2) Output dynamic range > 1.60 V

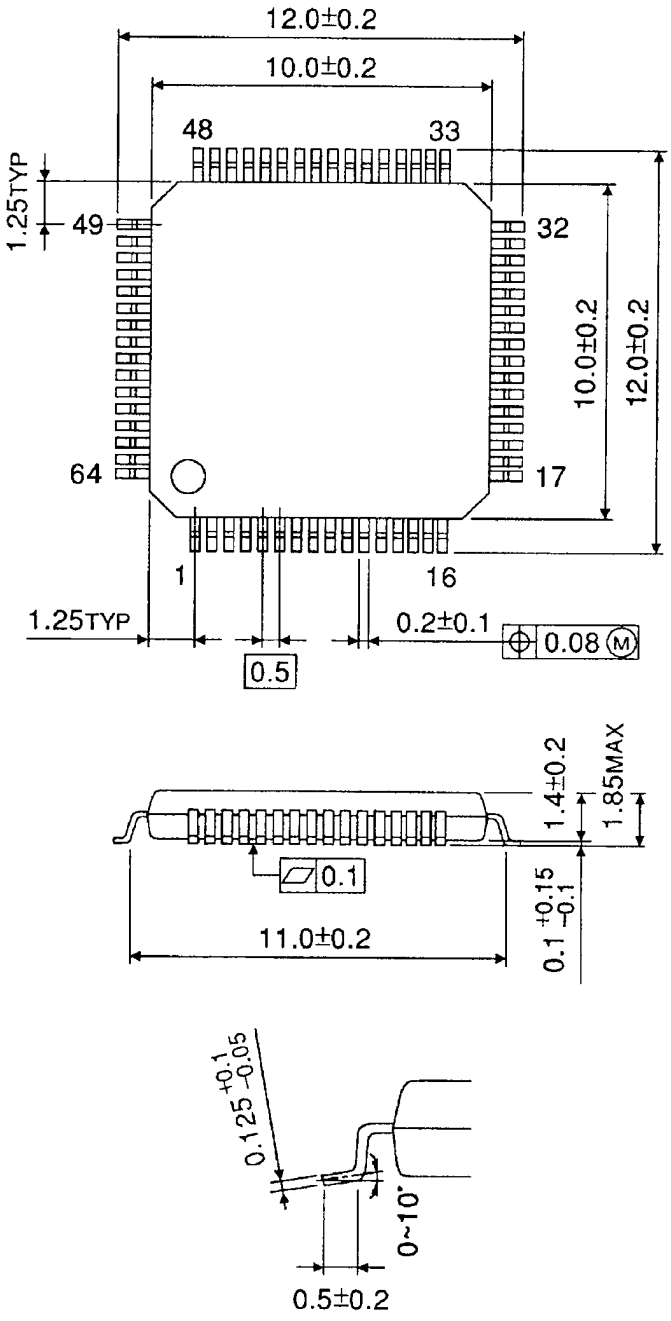
Application Circuit

*: 電源投入時はかならず RESET をかけて下さい.



Package Dimensions

LQFP64-P-1010-0.50 Unit : mm



Weight: g (typ.)