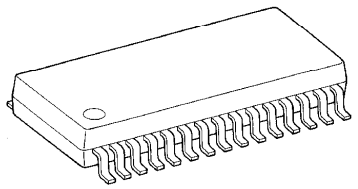
TENTATIVE TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC9335F-001

2-CHANNEL DSP WITH 1-BIT DIGITAL TO ANALOG CONVERTER

The TC9335F-001 is a 2-channel digital signal processor developed for use in digital audio equipment. It contains a 16 k-bit RAM for data delay operation, allowing for 2-channel surround stereo reproduction. Furthermore, it comes with digital tone control, compressor, and bass boost functions, making it possible to accomplish versatile digital effects. What's more, as the TC9335F-001 incorporates a 8-times oversampling filter and a 1-bit DA converter with a built-in filter amp, it can output a direct analog waveform.



SSOP30-P-375-1.00

Weight : 0.4 g (Typ.)

FEATURES

Digital effect unit

- Incorporates a 3-band tone control function.
- Incorporates a selectable bass boost / compressor function.
- The bass boost function provides two boost rates to choose from.
- The compressor function provides two compression rates to choose from.
- Incorporates a 16 k-bit delay RAM.
  The decimation ratio can be selected from 1 / 2 or 1 / 4.
  If you choose a 1 / 4 decimation, it gives you a 92.9 ms delay.
- Incorporates a phase reversing type surround function that gives the listener a great expanse of sound.

Digital filter unit

- Incorporates a 8-times oversampling digital filter.
- Incorporates a digital emphasis function.
- Incorporates a digital attenuator function.

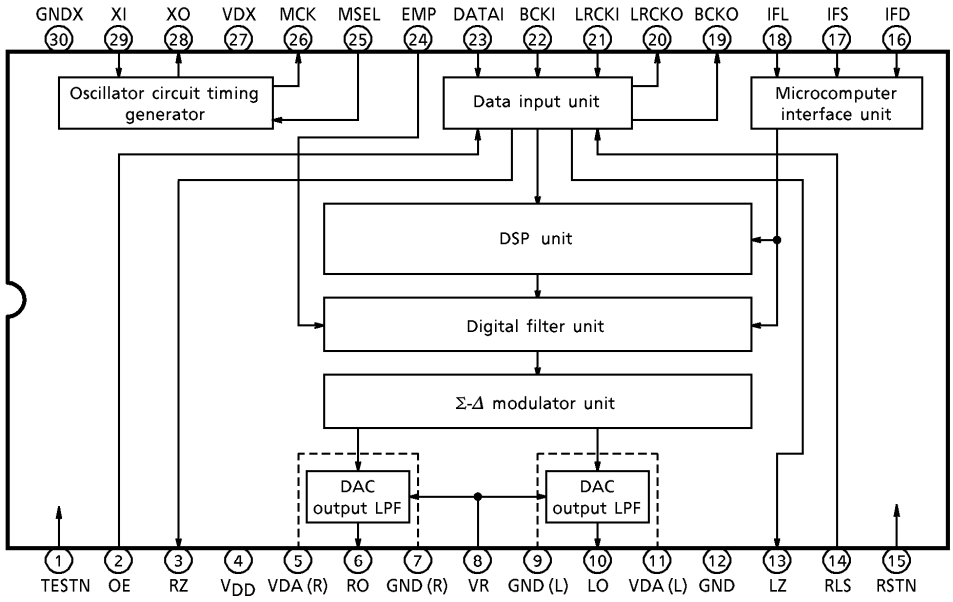
Output unit

- Incorporates a second-order Σ-Δ modulation circuit.
- Incorporates a third-order filter amp.
  THD + N : −80 dB ; S / N ratio : 91 dB at V_{DD} = 3.3 V (Typ.)

Other

- Coefficient data can be set via microcomputer interface.
- Digital data zero detect function is provided independently for the left and right channels.
- The system clock can be selected from 384 fs or 512 fs.
- The device comes in a 30-pin flat package.

BLOCK DIAGRAM



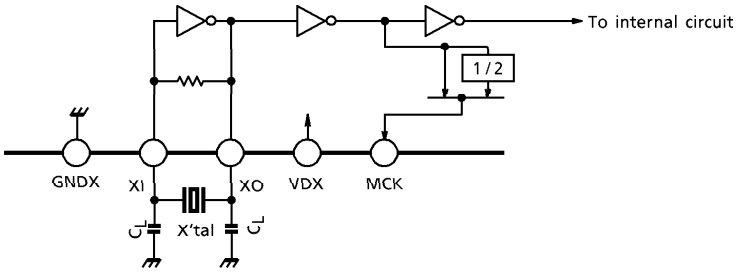
PIN DESCRIPTION

PIN No.	PIN NAME	I / O	FUNCTION	REMARKS
1	TESTN	I	Test mode setup pin.	
2	OE	I	LRCKO and BCKO output enable pin. (Output is enabled when "H" level ; disabled when "L" level.	
3	RZ	O	R-channel zero detect output pin.	
4	V_{DD}	—	Digital power supply pin.	
5	VDA (R)	—	R-channel DAC power supply pin.	
6	RO	O	R-channel analog pin.	
7	GNDA (R)	—	R-channel DAC ground pin.	
8	VR	—	DAC reference voltage pin.	
9	GNDA (L)	—	L-channel DAC ground pin.	
10	LO	O	L-channel output pin.	
11	VDA (L)	—	L-channel DAC power supply pin.	
12	GND	—	Digital ground pin.	
13	LZ	O	L-channel zero detect output pin.	
14	RLS	I	Channel clock polarity select pin. (L-ch = L when "H" level)	
15	RSTN	I	Reset pin	
16	IFD	I	Microcomputer interface data input pin.	
17	IFS	I	Microcomputer interface shift clock input pin	
18	IFL	I	Microcomputer interface latch input pin.	
19	BCKO	O	Bit clock output pin.	
20	LRCKO	O	Channel clock output pin.	
21	LRCKI	I	Channel clock input pin.	
22	BCKI	I	Bit clock input pin.	
23	DATAI	I	Digital audio data input pin.	
24	EMP	I	Deemphasis setup pin.	
25	MSEL	I	Clock output select pin. (Divide-by-2 clock when "L" level)	
26	MCK	O	Clock output pin.	
27	VDX	—	Oscillation circuit power supply pin.	
28	XO	O	Oscillator connecting pin.	
29	XI	I	Oscillator connecting pin.	
30	GNDX	—	Oscillation circuit ground pin.	

CIRCUIT OPERATION

1. Crystal oscillator circuit and timing generator

The clock (384 fs or 512 fs) required for internal device operation can be generated connecting a crystal and capacitor to the device's XI and XO pins as shown below. Or an external source to clock the device can be fed through the XI pin. In this case, however, the external clock must be carefully selected because its jitter, rise / fall characteristics, and duty cycle greatly affect the DA converter's noise distortion and S / N ratio.



Use a crystal whose CI value is low and that has a good startup property.

Fig.1-1. Configuration of crystal oscillator circuit

The timing generator provides the clock required for the digital filter, deemphasis filter, digital attenuator, and Σ-Δ modulator circuits, as well as timing signal for arithmetic and logic operations. Clock selection between 384 fs and 512 fs automatically accomplished.
Furthermore, the polarity of LRCK can be changed by setting the RLS pin as necessary.

Table.1-1. Selection of channel clock polarities

INPUT ON RLS PIN	LRCK POLARITIES	
	L	H
L	R-channel data	L-channel data
H	L-channel data	R-channel data

In addition, the MCK output can be selected from two types as listed below.

Table.1-2. Selection of input clock

MSEL INPUT	MCK OUTPUT
H	XI clock is output directly.
L	XI clock is output after dividing it by 2.

2. Data input circuit

DATAI and LRCKI are latched into the device at the rising edge of BCKI. Therefore, DATAI and LRCKI must be input synchronously with the falling edge of BCKI as shown in Fig.2. Furthermore, since the device is designed in such a way that 16, 18, or 20 bits of DATAI immediately before LRCKI changes are accepted as valid data, data must be "tail-aligned" (with bits filled beginning from the end of each block) as it is input to the device when you are using BCKI = 48 fs or 64 fs. The number of input bits can be set via a microcomputer interface.

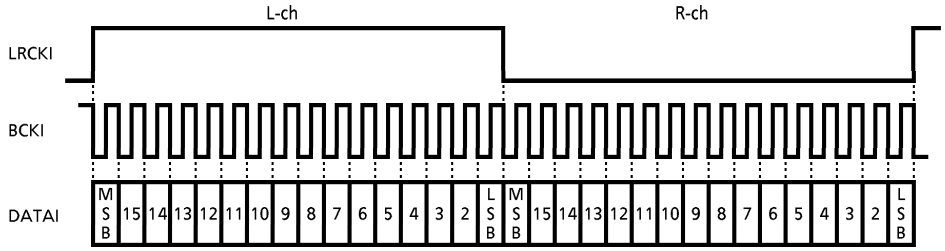


Fig.2-1. Data input timing chart (when input to RLS pin input the low lebel)

If BCKI is 48 fs or 64 fs, make sure that data is "tail-aligned" as shown below.

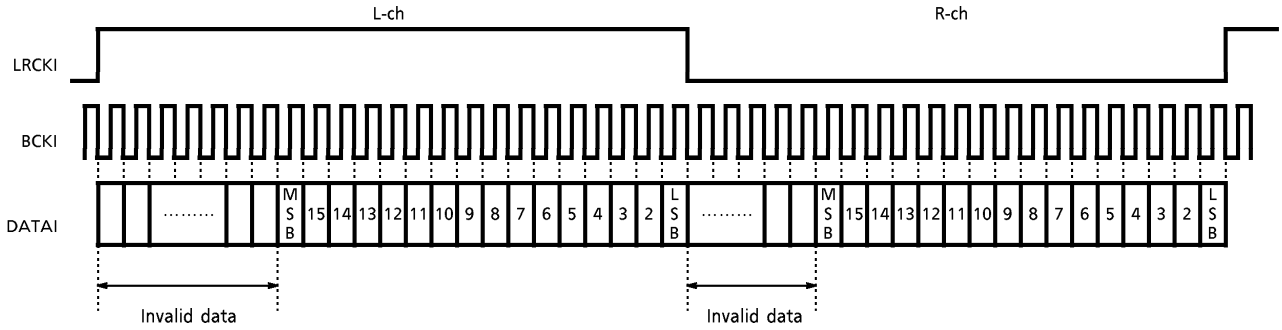


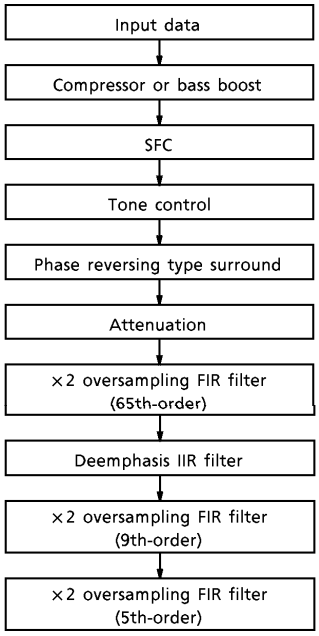
Fig.2-2. Example of input timing chart (When entering 16 bits of data)

3. Digital filter (DF) and various effects (DSP)

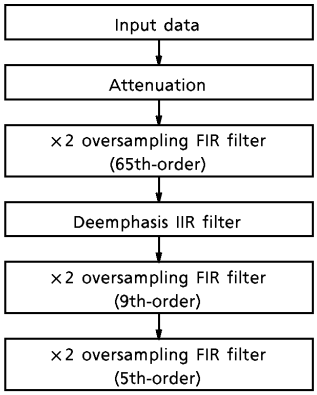
The charts below illustrate the configurations of the ×8 oversampling FIR digital filter, digital effect, and emphasis. Standard operation is accomplished by "DSP + DF" processing or "DF" processing as shown in the flowcharts below. On the other hand, double-speed operation is accomplished by only DF processing. These operations are set via a microcomputer interface.

- Standard operation

(1) When using "DSP + DF" processing

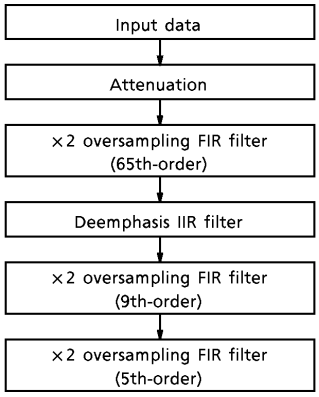


(2) When using "DF" processing



- Double-speed operation

"DF" processing



(Note) : Digital effects (DSP) cannot be used when operating at two times normal speed.

(1) Digital effects (DSP)

① Compressor and bass boost function

The DSP unit has compressor and bass boost functions whichever function can be enabled as you select. These functions can be turned on and off under control via a microcomputer interfase. Fig.3-1. shows the algorithm of compressor and bass boost on / off control. The numbers prefixed by @ denote the coefficient / offset RAM address. [+1b] denotes a 1-bit shift operation.

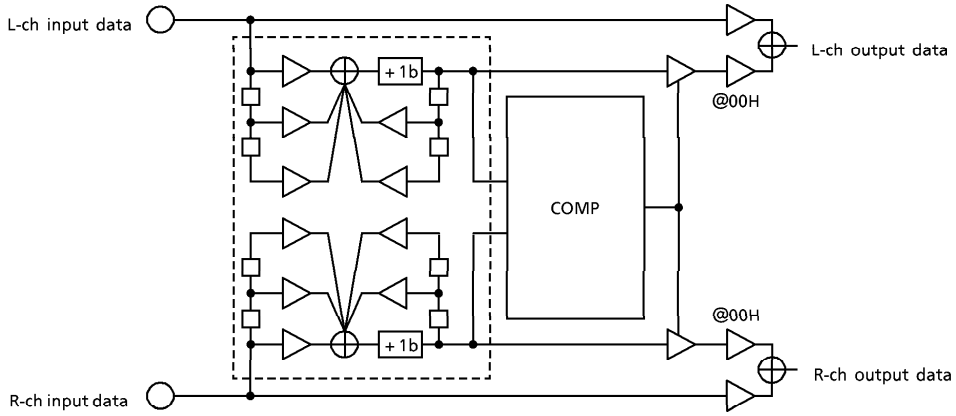


fig.3-1. Compressor / bass boost algorithm

Table.3-1. Compressor / bass boost settings

CM1	CM0	SETTING
0	0	OFF
0	1	Compressor ON
1	0	Bass boost 1
1	1	Bass boost 2

Bass boost 1 and 2 allow you to change the LPF characteristics.

When the compressor is enabled, its compression rate can be selected between two rate settings available. Fig.3-2. shows the compressor's input / output characteristics for each compression rate.

Table.3-2. Compression rate settings

EFFECT	COMPRESSION RATE
0	+ 6 dB
1	+ 12 dB

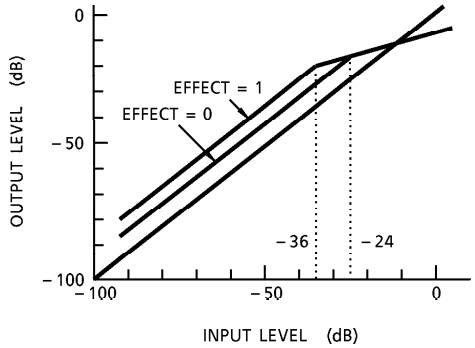


Fig.3-2. Input / output characteristics of compressor

Furthermore, when using the compressor and boss booster, it is possible to switch over the attach time and release time as described below.

Table3-3. Attach time / release time settings

Attach time

EFFECT / CTUP	0	1
0	4 ms	6 ms
1	16 ms	24 ms

Release time

EFFECT / CTDW	0	1
0	0.6 s	1 s
1	6 s	10 s

The output level when using the compressor and the boost add ratio when using the bass booster can be changed by modifying each coefficient RAM data.

② SFC function

The TC9335F-001 allows to perform SFC operation by using its internal 16 k-bit RAM. The diagram below shows the algorithm of this operation.

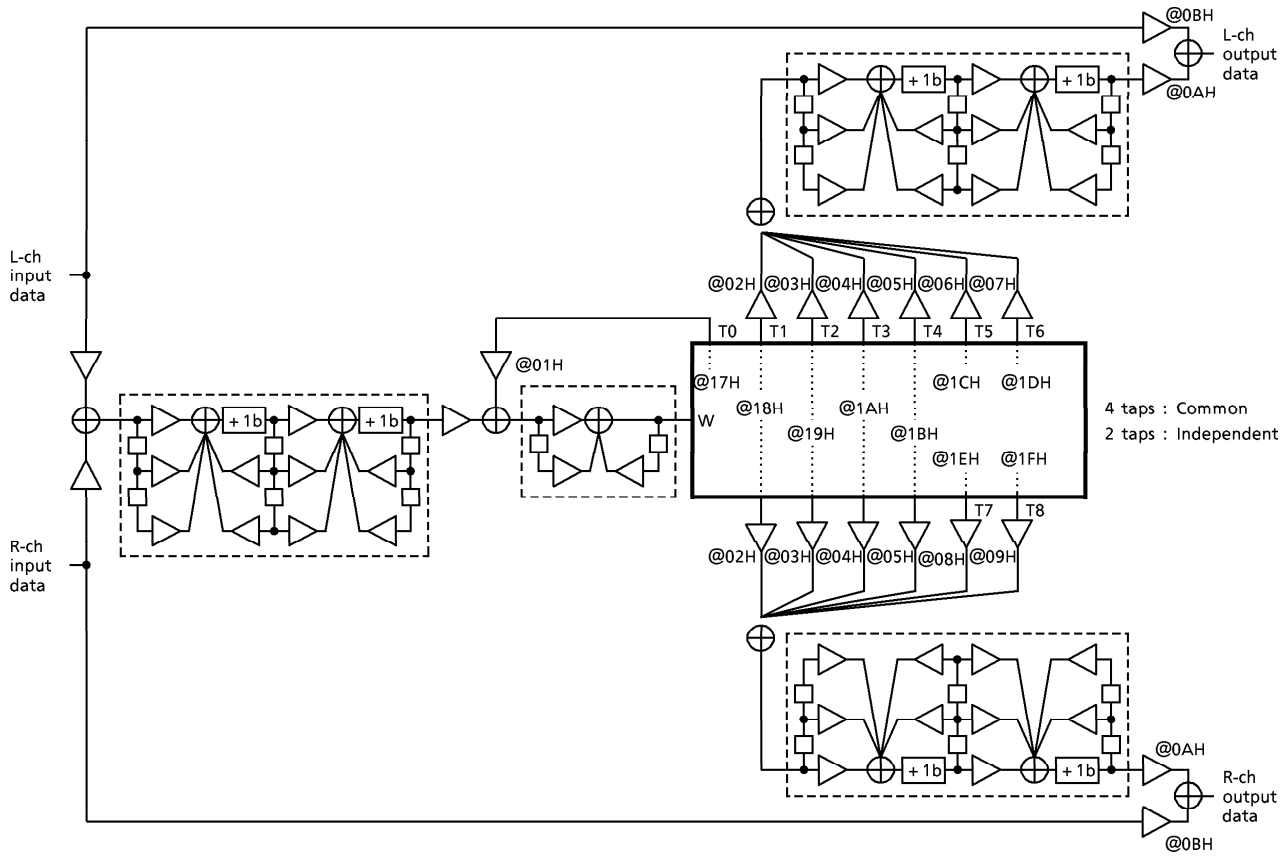


Fig.3-3. Algorithm of SFC operation

The TC9335F-001 uses decimation technology to provide a large delay time. Decimation settings are shown in the table below. By modifying this setting, it is possible to change coefficients for the decimation and interpolation filters to accomplish decimation. Although decimation gives a large amount of delay, the pass band is narrowed accordingly.

Table.3-4. Decimation ratio and add ratio settings

DECI1	DECI0	DECIMATION RATIO	L AND R ADD RATIO
0	0	1 / 2	(L + R) / 2
0	1	1 / 2	(L – R) / 2
1	0	1 / 4	(L + R) / 2

The taps used for the SFC function are available for six taps each on left and right channels. Of this, four taps are the same for both left and right channels. The delay position (offset amount) and coefficient on each tap are set in RAM. The maximum delay time varies with the decimation ratio selected. Table.3-5. lists the maximum amount of delay for each decimation ratio.

Table.3-5. Decimation ratio and maximum amount of delay

DECI1	DECI0	DECIMATION RATIO	MAXIMUM AMOUNT OF DELAY
0	0	1 / 2	46.4 ms
0	1	1 / 2	46.4 ms
1	0	1 / 4	92.9 ms

③ Tone control function

The TC9335F-001 has a tone control function whose algorithm is shown below. It consists of primary IIR + secondary IIR + primary IIR independently for the left and right channels. All of these coefficients are set to coefficient RAM.

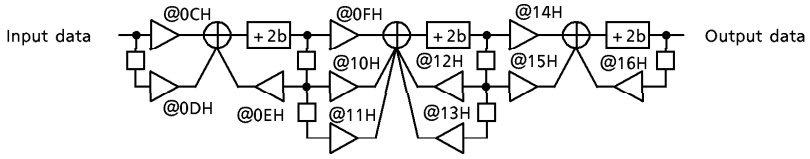


Fig.3-4. Algorithm of tone control function (Same coefficient for both left and right channels)

④ Phase reversing type surround function

To provide a wide expanse of stereo sound reproduction, the DSP unit has in its last stage a phase reversing type surround (stereo wide) function. Its algorithm is as shown below.

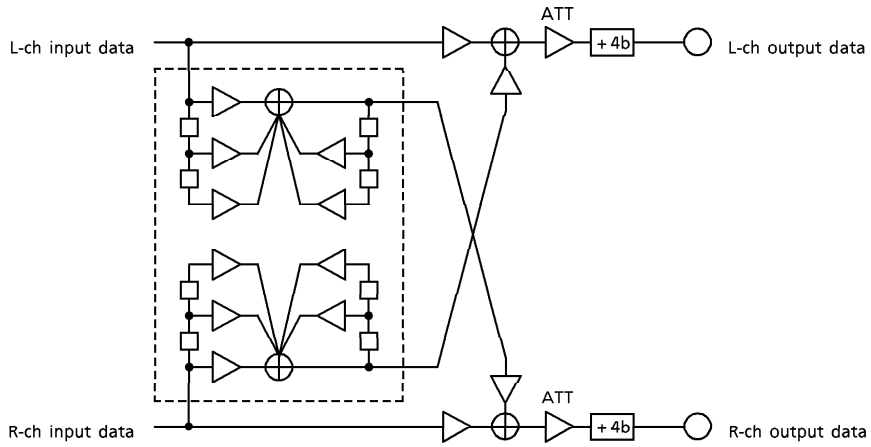


Fig.3-5. Algorithm of phase reversing type surround function

Table.3-6. Phase reversing type surround settings

ROA1	ROA0	SETTING
0	0	OFF
0	1	Stereo Wide 1
1	0	Stereo Wide 2
1	1	Stereo Wide 3

The above IIR filter characteristics are different for Stereo Wide 1 through Stereo Wide 3.

(2) Regarding oversampling filter

The oversampling digital filter is provided independently for three types of fs (44.1 kHz, 32 kHz, and 48 kHz). Furthermore, two types of filters are available for the 44.1 kHz. Switching between these types of filters are accomplished by control through the microcomputer interface.
The table below lists the characteristics of the 44.1 kHz oversampling filter.

Table.3-7. Basic characteristics of oversampling digital filter

RIPPLE WITHIN THE BAND	PASSBAND WIDTH	ATTENUATION
±0.1 dB	20 kHz~24 kHz	– 52 dB

The following graphically illustrates the frequency responses of the oversampling digital filters for each fs.

- 44.1 kHz filter 1

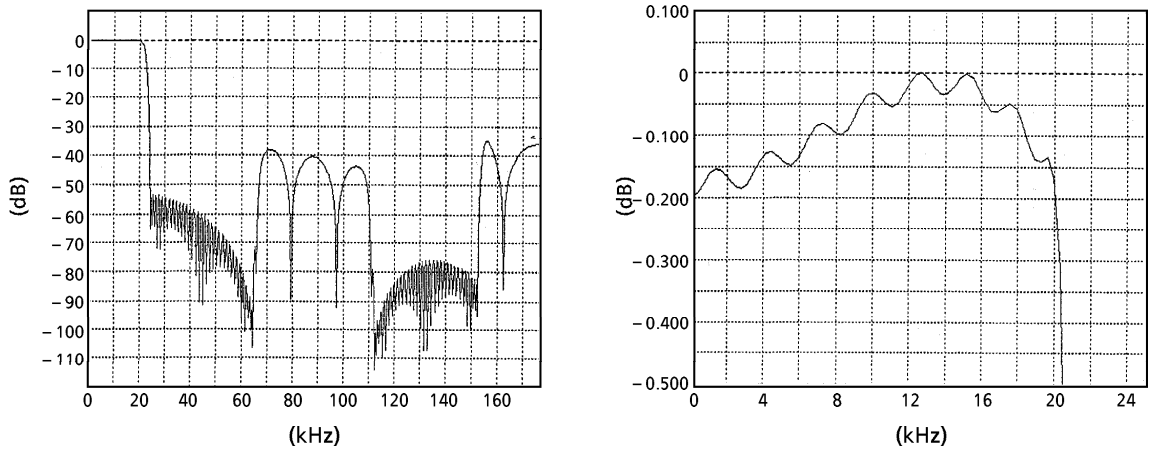
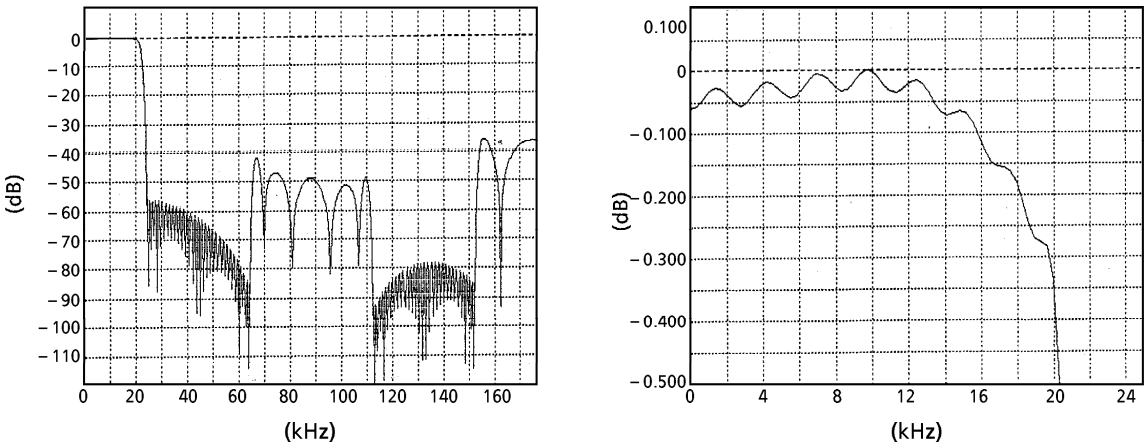
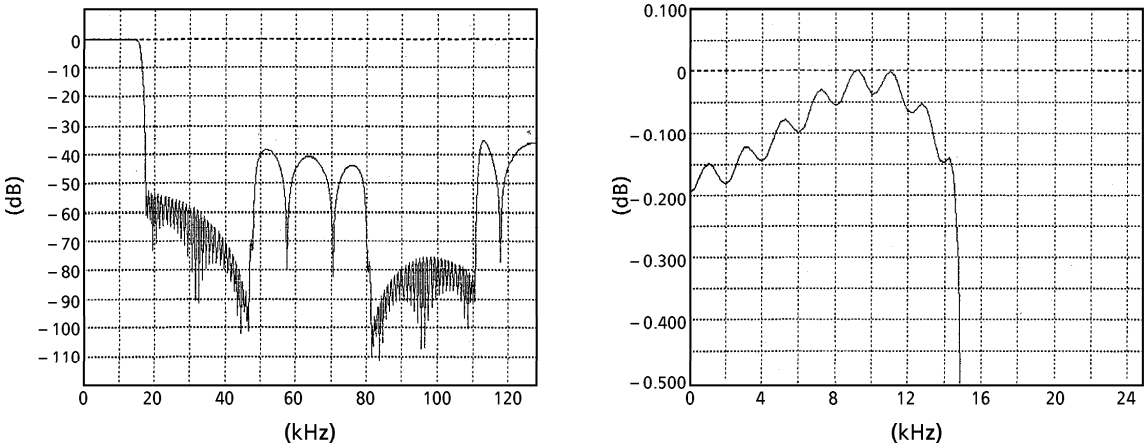


Fig.3-6. Frequency response of oversampling digital filter (1)

- 44.1 kHz filter 2



- 32 kHz filter



- 48 kHz filter

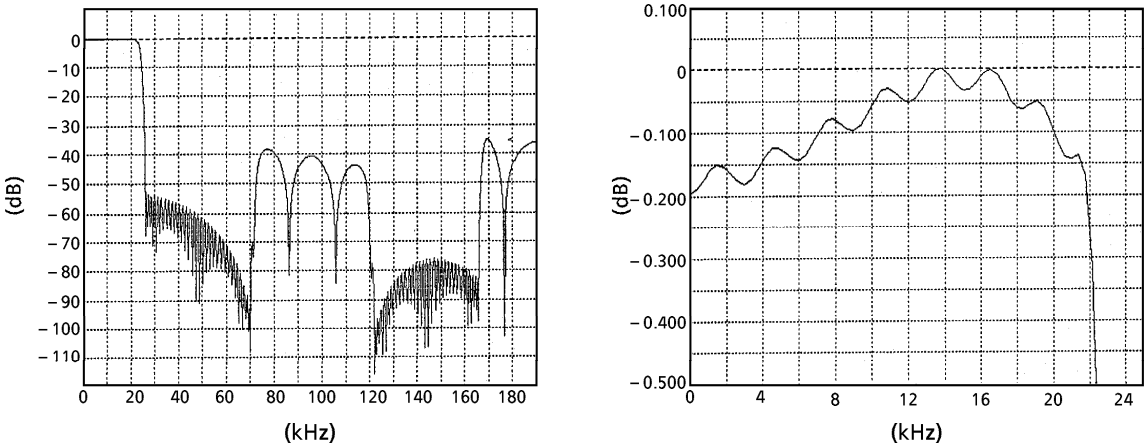


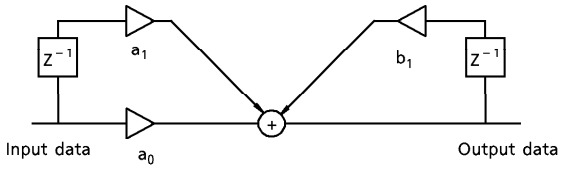
Fig.3-6. Frequency response of oversampling digital filter (2)

(3) Regarding deemphasis filter

Deemphasis filtering is performed during the oversampling filtering operation described above. The deemphasis filter is available for each fs : 44.1 kHz, 32 kHz, and 48 kHz. The table below shows how this filter is set up. This setup is accomplished by setting the external EMP pin and microcomputer bits.

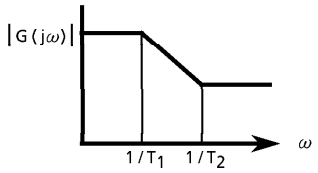
Table.3-8. Deemphasis filter setting

EXTERNAL EMP PIN	MICROCOMPUTER BITS		DEEMPHASIS FILTER
	EM1	EM0	
0	0	0	OFF
0	0	1	44.1 kHz
0	1	0	32 kHz
0	1	1	48 kHz
1	0	0	44.1 kHz
1	0	1	44.1 kHz
1	1	0	44.1 kHz
1	1	1	44.1 kHz



$$\text{Transfer coefficient} = \frac{a_0 + a_1 Z^{-1}}{1 - b_1 Z^{-1}}$$

Fig.3-7. Configuration of deemphasis filter



$T_1 = 50\ \mu s,\ T_2 = 15\ \mu s$

Fig.3-8. Filter characteristics

4. Regarding attenuation

The TC9335F-001 can control the digital attenuation by 7 bits of attenuate data via a microcomputer. The transmit data consists of 7 bits AL6 through AL0. It is possible to set attenuation in 128 steps from 0 dB to $-\infty$ dB by using this data.

Table.4-1. Attenuate data and amount of attenuation

ATTENUATE DATA AL6~0	OUPUT LEVEL
7F [HEX]	0 dB
7E [HEX]	– 0.14 dB
7D [HEX]	– 0.21 dB
…	…
01 [HEX]	– 42.1 dB
00 [HEX]	$-\infty$ dB

The output level changes from 0 dB to $-\infty$ dB at a rate of 1024 / fs seconds.

5. Internal control signals

The TC9335F-001 has the following control signals that can be via a 3-wire serial interface as shown below.

Table.5-1. Microcomputer control bits

INPUT DATA	CONTROL SIGNAL			
	ATTENUATOR	MODE	FILTER	COEFFICIENT / OFFSET
D23	0	0	0	1
D22	0	1	1	IFADR4
D21	AL6	0	1	IFADR3
D20	AL5	PSEL2	CM1	IFADR2
D19	AL4	PSEL1	CM0	IFADR1
D18	AL3	PSEL0	DECI1	IFADR0
D17	AL2	MONO	DECI0	IFRDT17
D16	AL1	CHS	DLRF1	IFRDT16
D15	AL0	BIT2	DLRF0	IFRDT15
D14	—	BIT1	ROA1	IFRDT14
D13	—	—	ROA0	IFRDT13
D12	—	—	OSF1	IFRDT12
D11	—	—	OSF0	IFRDT11
D10	—	—	EM1	IFRDT10
D09	—	—	EM0	IFRDT09
D08	—	—	CTDW	IFRDT08
D07	—	—	CTUP	IFRDT07
D06	—	—	EFFECT	IFRDT06
D05	—	—	—	IFRDT05
D04	—	—	—	IFRDT04
D03	—	—	—	IFRDT03
D02	—	—	—	IFRDT02
D01	—	—	—	IFRDT01
D00	—	—	—	IFRDT00

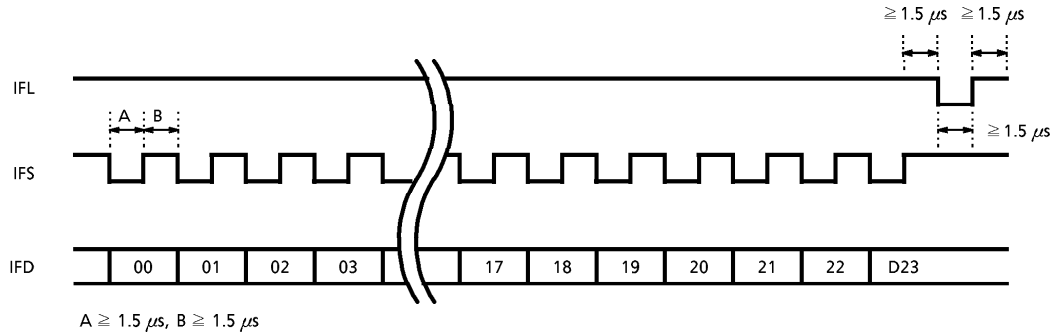


Fig.5-1. Microcomputer data setup timing

Attenuate data settings

AL6~AL0	OUTPUT LEVEL
7F [HEX]	0 dB
7E [HEX]	– 0.14 dB
…	…
00 [HEX]	– ∞ dB

Program & system clock selection

PSEL2	PSEL1	PSEL0	PROGRAM	SYSTEM CLOCK	NORMAL / DOUBLE SPEED
0	0	0	DSP + DF	256 fs	Normal speed
0	1	1	DF only	128 fs	Normal speed
1	0	1	DF only	256 fs	Double speed

Selection of sound multiplex mode

MONO	CHS	OUTPUT LEVEL
0	0	Stereo operation
0	1	Stereo operation
1	0	L-ch monaural
1	1	R-ch monaural

Input bit settings

BIT2	BIT1	NUMBER OF INPUT BITS
0	0	16 bits
0	1	18 bits
1	0	16 bits
1	1	20 bits

Selection of compressor / bass boost

CM1	CM0	SETTING
0	0	OFF
0	1	Compressor ON
1	0	Bass boost 1
1	1	Bass boost 2

Switching between compressor and bass boost

EFFECT	GAIN (LARGE / SMALL)
0	Small (+ 6 dB)
1	Large (+ 12 dB)

Switching of compressor time constant

CTDW	RELEASE TIME CONSTANT
0	Short (.001 dB / fs)
1	Long (.0005 dB / fs)

CTUP	ATTACK TIME CONSTANT
0	Short (.03 dB / fs)
1	Long (.13 dB / fs)

Switching of decimation ratio

DECI1	DECI0	DECIMATION RATIO
0	0	1 / 2
0	1	1 / 2
1	0	1 / 4

Switching of feedback filter

DLRF1	DLRF0	CUT-OFF FREQUENCY OF FILTER
0	0	5.5 kHz
0	1	5.5 kHz
1	0	2.8 kHz
1	1	1.4 kHz

Switching of fs of oversampling filter

OSF1	OSF0	fs OF OVERSAMPLING FILTER
0	0	44.1 kHz-1
0	1	44.1 kHz-2
1	0	32 kHz
1	1	48 kHz

ON / OFF of deemphasis filter

EXTERNAL EMP PIN	MICROCOMPUTER BIT		DEEMPHASIS FILTER
	EM1	EM0	
0	0	0	OFF
0	0	1	44.1 kHz
0	1	0	32 kHz
0	1	1	48 kHz
1	0	0	44.1 kHz
1	0	1	44.1 kHz
1	1	0	44.1 kHz
1	1	1	44.1 kHz

The following explains how the coefficient and offset data are set to RAM. IFADR4 through 0 (D22 through 18) in microcomputer setup bits indicate the RAM addresses to which the data are written. Similarly, IFRDT17 through 00 (D17 through 00) indicate the write data to RAM. Note that when this 18 bits of data is used for offset, only 10 bits from the MSB are used for this purpose, with the other 8 bits ignored.

	COEFFICIENT DATA	OFFSET DATA
IFADR4 … IFADR0	Write address	Write address
IFRDT17 … IFRDT08	18 bits data	10 bits data
IFRDT07 … IFRDT00		Invalid

6. Regarding data zero detect function

The TC9335F-001 has a function to detect digital zero in the input data.
If zero data continues for more than 2^{15} / fs seconds (750 ms when fs = 44.1 kHz), the LZ and RZ pins are driven high.
The diagram shows the timing at which zero detection is cleared by releasing the LZ and RZ pins back low.

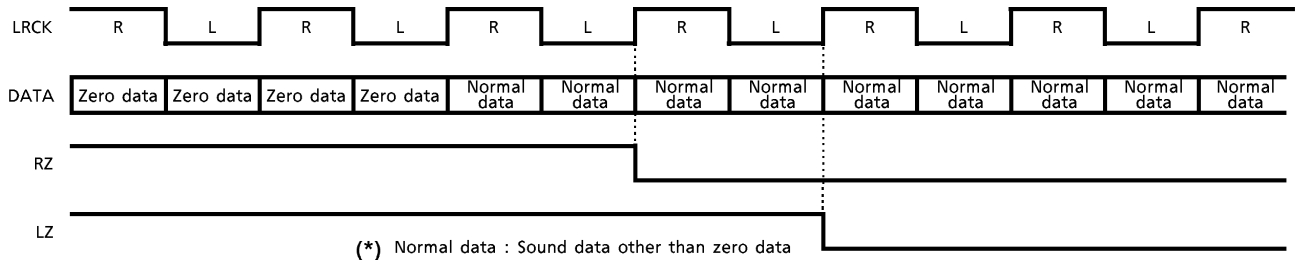


Fig.6-1. Timing at which zero detection is cleared

7. Channel clock and bit clock output

By driving the OE pin high, you can output the channel clock and bit clock to an external device. The table below lists the clock signals thus output.

Table.7-1. Channel clock and bit clock output

OUTPUT PIN	SIGNAL OUTPUT
LRCKO	Clock equivalent to sampling period
BCKO	Clock 64 times sampling period

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{DD}	−0.3~4.8	V
	V_{DA}	−0.3~4.8	V
	V_{DX}	−0.3~4.8	V
Input Voltage	V_{in}	−0.3~V_{DD} + 0.3	V
Power Dissipation	P_D	200	mW
Operating Temperature	T_{opr}	−35~85	°C
Storage Temperature	T_{stg}	−55~150	°C

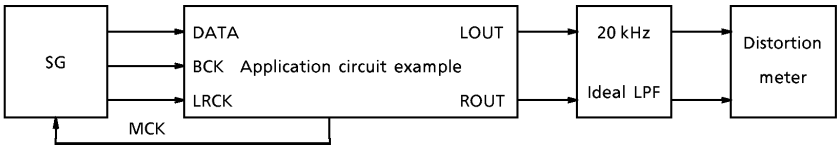
ELECTRICAL CHARACTERISTICS
(Referenced to V_{DD} = V_{DX} = V_{DA} = 3.9 V at Ta = 25°C unless otherwise noted)
DC CHARACTERISTICS

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Power Supply Voltage (1)		V_{DD}	—	Ta = −35~85°C	3.5	3.9	4.3	V
		V_{DX}			3.5	3.9	4.3	
		V_{DA}			3.5	3.9	4.3	
Operating Power Supply Voltage (2)		V_{DD}	—	Ta = −15~50°C (Operating frequency 10 MHz ≦ f_{opr} ≦ 17 MHz)	3.1	3.3	4.3	V
		V_{DX}			3.1	3.3	4.3	
		V_{DA}			3.1	3.3	4.3	
Current Consumption		I_{DD}	—	XI = 16.9 MHz, V_{DD} = 3.3 V	—	15	25	mA
Input Voltage	"H" Level	V_{IH}	—		V_{DD} × 0.7	—	V_{DD}	V
	"L" Level	V_{IL}			0	—	V_{DD} × 0.3	
Input Current	"H" Level	I_{IH}	—		−10	—	10	μA
	"L" Level	I_{IL}						

AC CHARACTERISTICS (Oversampling rate = 192 fs)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Noise Distortion	THD + N	1	1 kHz sine wave, full-scale input $V_{DD} = V_{DX} = V_{DA} = 3.3$ V	—	−80	−78	dB
S/N Ratio	S/N	1	1 kHz sine wave, full-scale input $V_{DD} = V_{DX} = V_{DA} = 3.3$ V	84	91	—	dB
Dynamic Range	DR	1	In terms of 1 kHz sine wave, −60 dB input	82	88	—	dB
Crosstalk	CT	1	1 kHz sine wave, full-scale input	—	−83	−78	dB
Analog Output Level	Aout	1	1 kHz sine wave, full-scale input $V_{DD} = V_{DX} = V_{DA} = 3.3$ V	—	740	—	mV_{rms}
Operating Frequency	f_{opr}	—	$V_{DD} = V_{DA} = V_{DX} \geqq 3.1$ V	10	16.9344	19.2	MHz
Input Frequency	f_{LR}	—	LRCKI duty cycle = 50%	30	44.1	100	kHz
	f_{BCK}		BCKI duty cycle = 50%	0.96	2.1168	4.3	MHz
Rise Time	t_r	—	LRCKI and BCKI pins (10% to 90%)	—	—	15	ns
Fall Time	t_f			—	—	15	
Delay Time	t_d	—	BCKI ↓ falling edge →LRCKI, DATAI	—	—	40	ns

- Test cicuit 1 : A Typ. application circuit is used.

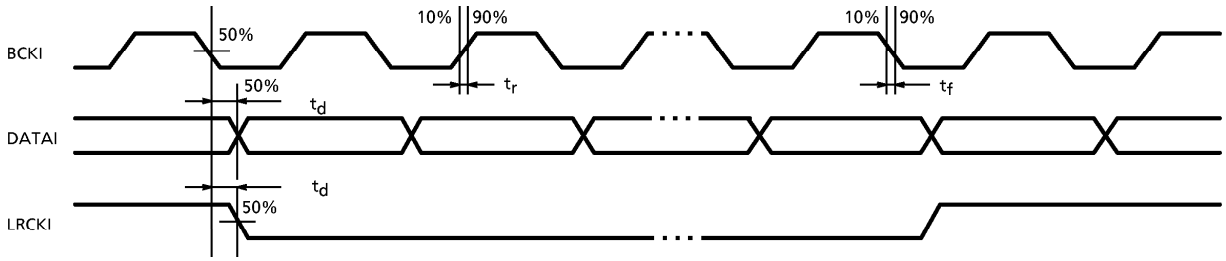


SG : Anritsu MG-22A or equivalent
LPF : Tsubasoku 725C distortion meter built-in filter
Distortion meter : Tsubasoku 725C or equivalent

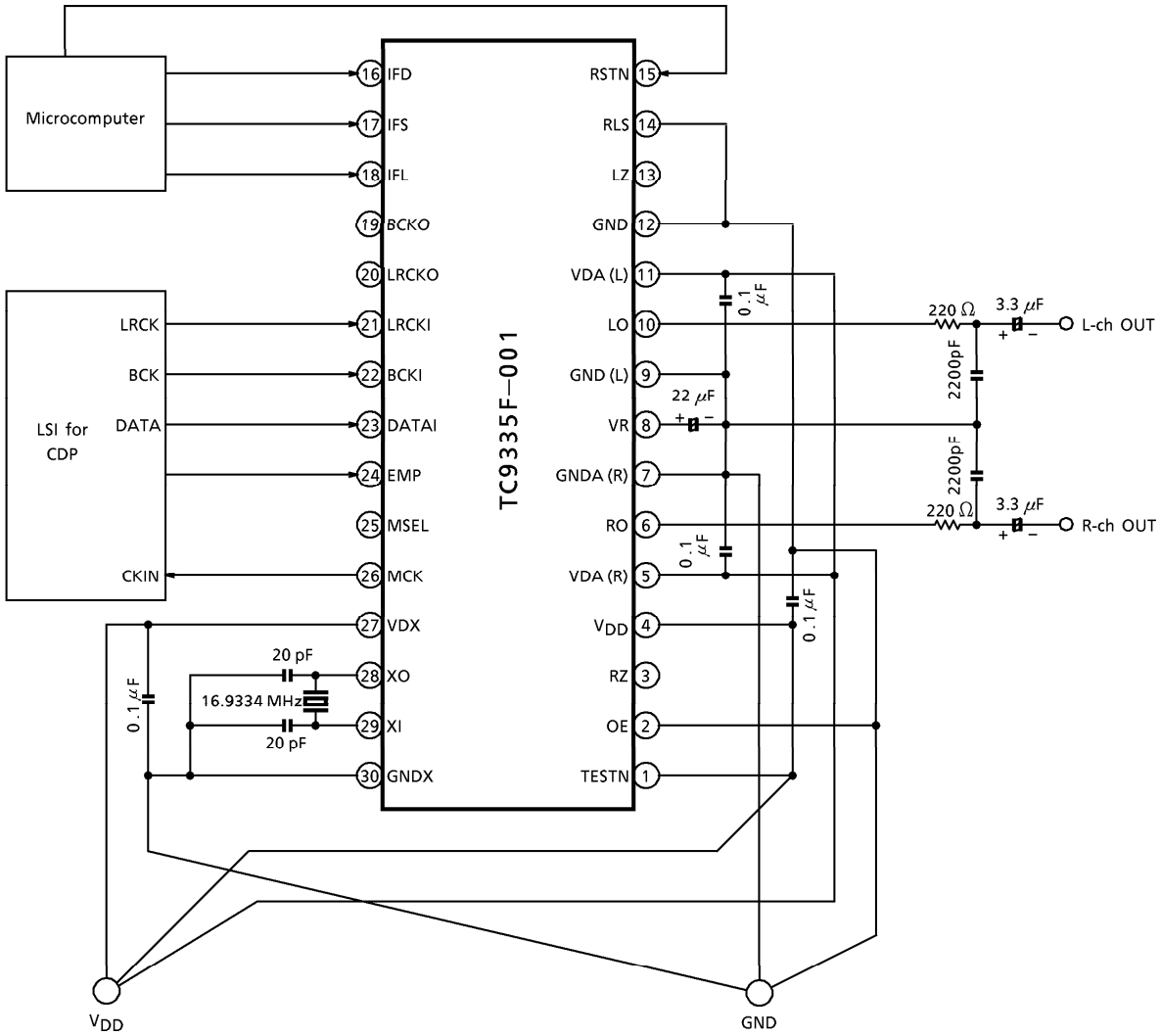
MEASUREMENT ITEM	DISTORTION METER FILTER SETTING A WEIGHTING CURVE
THD + N, CT	OFF
S/N, DR	ON

A Weighting curve
: Equivalent to IEC-A

- AC characteristics stipulated points (Input signals stipulation : LRCKI, BCKI, and DATAI)



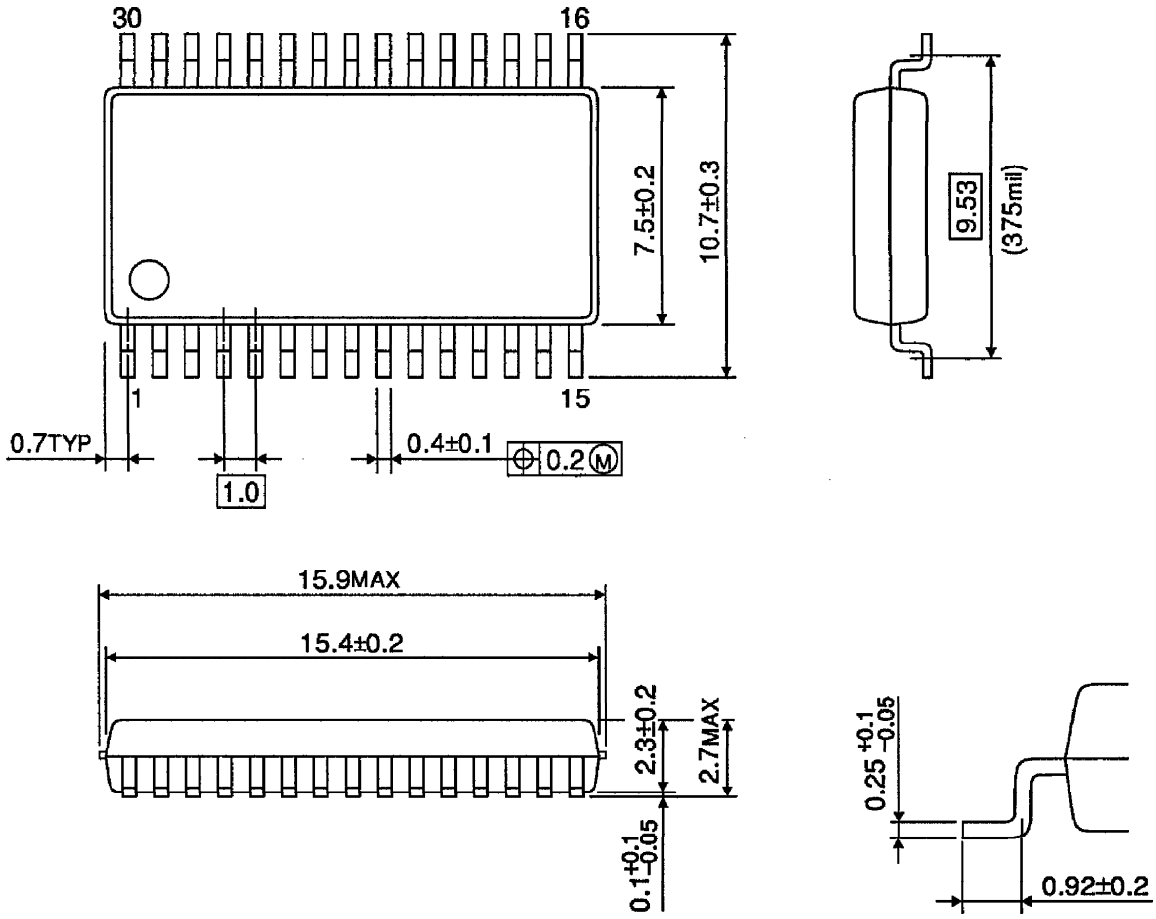
APPLICATION CIRCUIT



OUTLINE DRAWING

SSOP30-P-375-1.00

Unit : mm



Weight : 0.4 g (Typ.)