TOSHIBA CCD LINEAR IMAGE SENSOR CCD(Charge Coupled Device)

# **TCD2503C**

The TCD2503C is a high sensitive and low dark current 5000 elements × 3 line CCD color image sensor.

The sensor is designed for color scanner.

The device contains a row of 5000 elements  $\times$  3 line photodiodes which provide a 16 lines / mm across a A3 size paper. The device is operated by 5 V pulse, and 12 V power supply.

### **FEATURES**

Number of Image Sensing Element

: 5000 elements  $\times$  3 line

Image Sensing Element Size : 14 μm by 14 μm on 14 μm

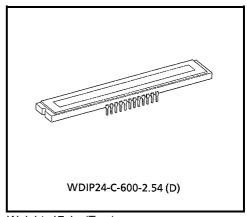
centers

Photo Sensing Region : High sensitive pn

photodiode

Clock : 2 Phase (5 V)
 Distance Between Photodiode Array : 84 µm (6 lines)
 Internal Circuit : Clamp circuit

Package : 24 pin DIPColor Filter : Red, Green, Blue



Weight: 17.1g (Typ.)

### **PIN CONNECTION**

### OS5 OS2 φ2B œ ניו φ2A1 d2A4 61A4 61A1 ø1A3 16 SS ø1A2 62A3 φ2A2 5 0 00 13

(TOP VIEW)

## MAXIMUM RATINGS (Note 1)

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CHARACTERISTIC	SYMBOL	RATING	UNIT	
Clock Pulse Voltage	Vφ			
Shift Pulse Voltage	$V_{SH}$	-0.3~8	V	
Reset Pulse Voltage	$V_{RS}$	0.0 0	v	
Clamp Pulse Voltage	V <sub>CP</sub>			
Power Supply Voltage	V <sub>OD</sub>	-0.3~15	>	
Operating Temperature	T <sub>opr</sub>	0~60	°C	
Storage Temperature	T <sub>stg</sub>	-25~85	°C	

Note 1: All voltage are with respect to SS terminals (Ground).

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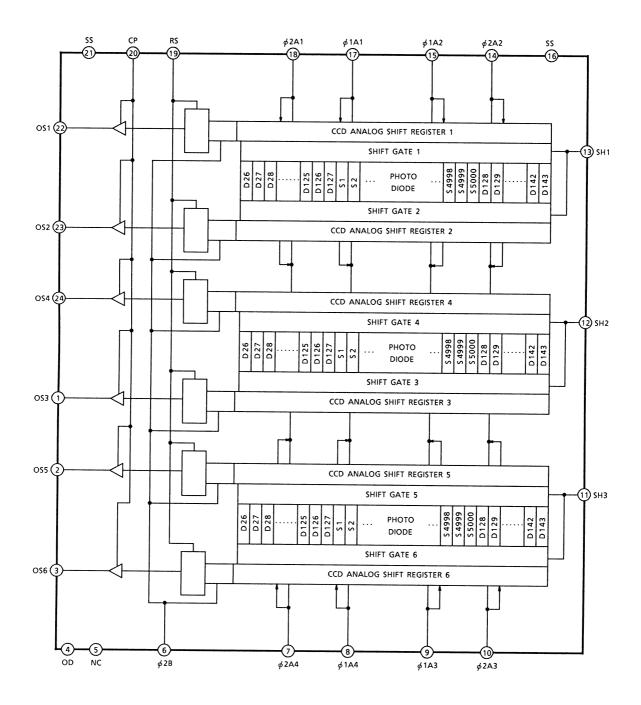
damage to property.

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### **CIRCUIT DIAGRAM**



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## **PIN NAMES**

PIN No.	SYMBOL	NAME	PIN No.	SYMBOL	NAME
1	OS3	Signal Output 3 (Green)	13	SH1	Shift Gate 1
2	OS5	Signal Output 5 (Red)	14	<sub>φ</sub> 2A2	Clock 2 (Phase 2)
3	OS6	Signal Output 6 (Red)	15	<sub>φ</sub> 1A2	Clock 2 (Phase 1)
4	OD	Power (Analog)	16	SS	Ground
5	NC	Non Connection	17	<sub>φ</sub> 1A1	Clock 1 (Phase 1)
6	<sub>φ</sub> 2B	Final Stage clock (phase 2)	18	<sub>φ</sub> 2A1	Clock 1 (Phase 2)
7	<sub>φ</sub> 2A4	Clock 4 (Phase 2)	19	RS	Reset Gate
8	φ1A4	Clock 4 (Phase 1)	20	СР	Clamp Gate
9	φ1A3	Clock 3 (Phase 1)	21	SS	Ground
10	<sub>φ</sub> 2A3	Clock 3 (Phase 2)	22	OS1	Signal Output 1 (Blue)
11	SH3	Shift Gate 3	23	OS2	Signal Output 2 (Blue)
12	SH2	Shift Gate 2	24	OS4	Signal Output 4 (Green)

## **OPTICAL / ELECTRICAL CHARACTERISTICS**

(Ta = 25°C,  $V_{OD}$  = 11V,  $V_{\phi}$  =  $V_{SH}$  =  $V_{RS}$  =  $V_{CP}$  = 5V (pulse),  $f_{\phi}$  = 1MHz LOAD RESISTANCE = 100 k $\Omega$ ,  $t_{INT}$  (INTEGRATION TIME) = 10 ms, LIGHT SOURCE = A LIGHT SOURCE + CM500S FILTER (t = 1.0 mm))

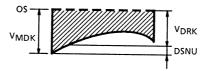
CHARACTERISTIC		SYMBOL	MIN	TYP.	MAX	UNIT	NOTE
	Red	R <sub>R</sub>	12.1	17.3	22.5		
Sensitivity	GREEN	R <sub>G</sub>	15.1	21.7	28.3	V / lx·s	(Note 2)
	BLUE	R <sub>B</sub>	5.0	7.2	9.4		
Photo Response Non Uniformity		PRNU (1)	_	10	20	%	(Note 3)
		PRNU (3)	_	3	12	mV	(Note 4)
Saturation Output Voltage		V <sub>SAT</sub>	2.0	_	_	V	(Note 5)
Saturation Exposure		SE	_	0.18	_	lx·s	(Note 6)
Dark Signal Voltage		V <sub>DRK</sub>	_	1	5	mV	(Note 7)
Dark Signal Non Uniformity		DSNU	_	2	10	mV	(Note 8)
DC Power Dissipation		PD	_	800	1200	mW	
Total Transfer Efficiency		TTE	92	_	_	%	
Output Impedance		Zo	_	0.2	0.5	kΩ	
DC Signal Output Voltage		Vos	4.5	6.0	7.5	V	(Note 9)
Random Noise		$N_{D\sigma}$	_	1.3	_	mV	(Note 10)

- Note 2: Sensitivity is defined for each color of signal outputs average when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature.
- Note 3: PRNU (1) is defined for each color on a single chip by the expressions below when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature.

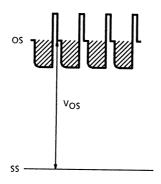
PRNU (1)= 
$$\frac{\Delta \chi}{\overline{\chi}} \times 100(\%)$$

Where  $\overline{\chi}$  is average of total signal outputs and  $\Delta\chi$  is the maximum deviation from  $\overline{\chi}$  .

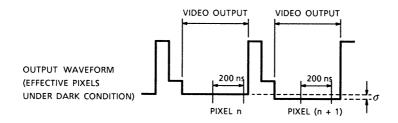
- Note 4: PRNU (3) is defined as maximum voltage with next pixel, where measured 5% of SE (Typ.).
- Note 5: V<sub>SAT</sub> is defined as minimum Saturation Output voltage of all effective pixels.
- Note 6: Definition of SE : SE =  $\frac{V_{SAT}}{R_{G}}$
- Note 7: VDRK is defined as average dark signal voltage of all effective pixels.
- Note 8: DSNU is defined as different voltage between VDRK and VMDK, when VMDK is maximum dark signal voltage.



Note 9: DC Signal Output Voltage is defined as follows:



Note 10: Random noise is defined as the standard deviation (sigma) of the output level difference between two adjacent effective pixels under no illumination (i.e. dark conditions) calculated by the following procedure.



- 1) Two adjacent pixels (pixel n and n + 1) in one reading are fixed as measurement points.
- 2) Each of the output levels at video output periods averaged over 200 ns period to get Vn and V (n + 1).
- 3) V (n + 1) is subtracted from Vn to get  $\Delta V$ .

$$\Delta V = Vn - V(n + 1)$$

4) The standard deviation of  $\Delta V$  is calculated after procedure 2) and 3) are repeated 30 times (30 readings).

$$\overline{\Delta V} = \frac{1}{30} \sum_{i=1}^{30} \! \left| \Delta V i \right| \quad \sigma = \sqrt{\frac{1}{30} \sum_{i=1}^{30} \! \left| \Delta V i \right| - \overline{\Delta V} \right|^2}$$

5) Procedure 2), 3) and 4) are repeated 10 times to get 10 sigma value.

$$\overline{\sigma} = \frac{1}{10} \sum_{j=1}^{10} \sigma_j$$

6)  $\overline{\sigma}$  value calculated using the above procedure is observed  $\sqrt{2}$  times larger than that measured relative to the ground level. So we specify random noise as follows.

Random noise = 
$$\frac{1}{\sqrt{2}}\overline{\sigma}$$



## **OPERATING CONDITION**

CHARACTERISTIC		SYMBOL	MIN	TYP	MAX	UNIT	
Clock Pulse Voltage	"H" Level	V/ A	4.5	5.0	5.5	V	
Clock I dise voltage	"L" Level	$V_{\phi}A$	0	_	0.5		
Final Stage Clock Pulse Voltage	"H" Level	V <sub>φ</sub> B	4.5	5.0	5.5	V	
I mai Stage Clock Fulse Voltage	"L" Level	νφυ	0	_	0.5		
Ole 19 Dude a Maltana (Alata 44)	"H" Level	V <sub>SH</sub>	V <sub>φ</sub> A"H"-0.5	V <sub>φ</sub> A"H"	V <sub>φ</sub> A"H"	V	
Shift Pulse Voltage (Note 11)	"L" Level		0	_	0.5		
Paget Bulga Valtaga	"H" Level	\/	4.5	5.0	5.5	V	
Reset Pulse Voltage	"L" Level	V <sub>RS</sub>	0	_	0.5	V	
Clamp Pulse Voltage	"H" Level	V	4.5	5.0	5.5	V	
Clamp Fulse Voltage	"L" Level	$V_{CP}$	0	_	0.5	v	
Power Supply Voltage		V <sub>OD</sub>	10.5	11.0	13.0	V	

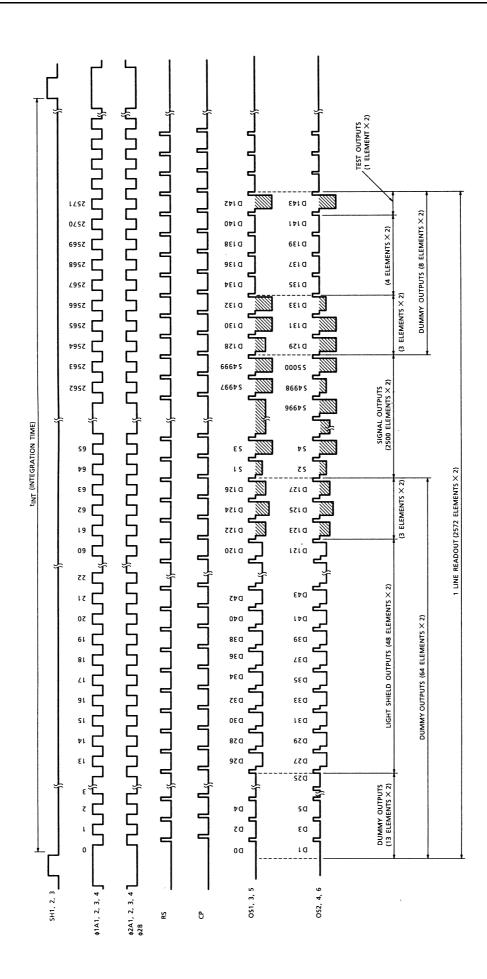
Note 11:  $\,V_{\phi}A\text{``H''}$  means the high level voltage of  $V_{\phi}A$  when SH pulse is high level.

## CLOCK CHARACTERISTICS (Ta = 25°C)

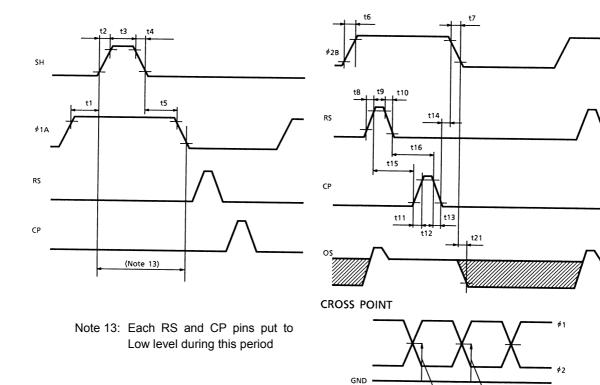
CHARACTERISTIC	SYMBOL	MIN	TYP.	MAX	UNIT
Clock Pulse Frequency	$f_{\phi}$	_	1	13	MHz
Reset Pulse Frequency	f <sub>RS</sub>	_	1	13	MHz
Clamp Pulse Frequency	f <sub>CP</sub>	_	1	13	MHz
Clock Capacitance (Note 12)	C <sub>φ</sub> A	_	250	_	pF
Final Stage Clock Capacitance	C <sub><math>\phi</math></sub> 2B	_	50	_	pF
Reset Gate Capacitance	C <sub>RS</sub>	_	50	_	pF
Shift Gate Capacitance	C <sub>SH</sub>	_	50	_	pF
Clamp Gate Capacitance	C <sub>CP</sub>	_	50	_	pF

Note 12:  $V_{OD} = 12 \text{ V}$ 





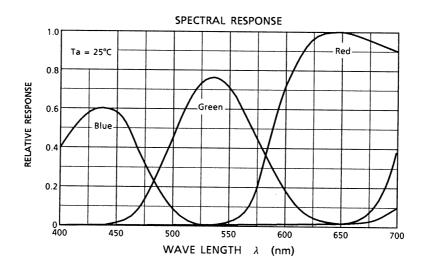
## **TIMING REQUIREMENTS**



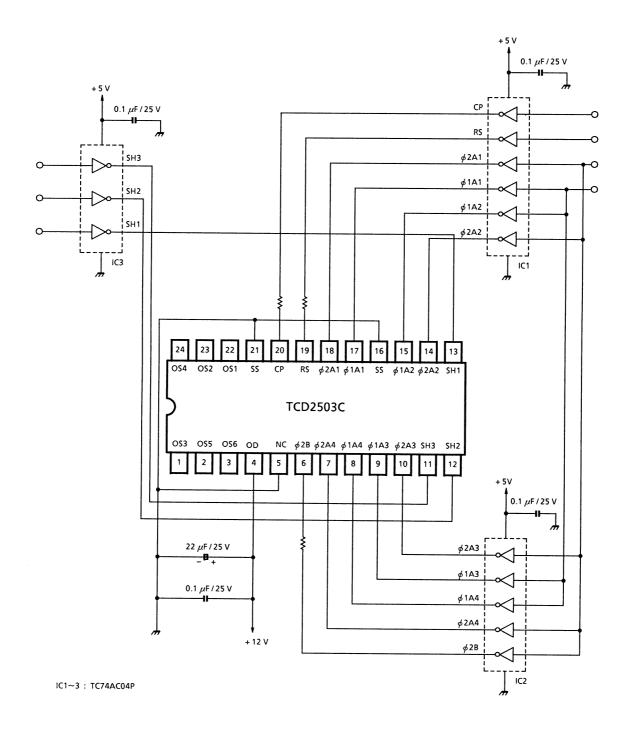
CHARACTERISTIC	SYMBOL	MIN	TYP. (Note 14)	MAX	UNIT	
Pulse Timing of SH and $_\phi$ 1A	t1	0	1000	_	ns	
	t5	500	1000	_	115	
SH Pulse Rise Time, Fall Time	t2, t4	0	50	_	ns	
SH Pulse Width	t3	1000	2000	_	ns	
$_{\phi}$ 1, $_{\phi}$ 2 Pulse Rise Time, Fall Time	t6, t7	0	50	_	ns	
RS Pulse Rise Time, Fall Time	t8, t10	0	20	_	ns	
RS Pulse Width	t9	10	100	_	ns	
CP Pulse Rise Time, Fall Time	t11, t13	0	20	_	ns	
CP Pulse Width	t12	10	100	_	ns	
Pulse Timing of $_\phi 2B$ and CP	t14	5	40	_	ns	
Dulas Timing of DC and CD	t15	0	100	_		
Pulse Timing of RS and CP	t16	10	100	_	ns	
Video Data Delay Time (Note 15)	t21	_	15	_	ns	

Note 14: TYP. is the case of  $f_{RS}$  = 1 MHz. Note 15: Load Resistance is 100 k $\Omega$ .

## **TYPICAL PERFORMANCE CURVES**



## **TYPICAL DRIVE CIRCUIT**



### PRECAUTIONS FOR USE OF CCD IMAGE SENSOR

### 1. Static Electricity

This device has some weakly terminals for static electricity. Therefor, please pay attention to treat this device.

CCD Image Sensor is protected against static electricity, but inferior puncture mode device due to static electricity is sometimes detected. In handling the device, it is necessary to execute the following static electricity preventive measures, in order to prevent the trouble rate increase of the manufacturing system due to static electricity.

- a. Prevent the generation of static electricity due to friction by making the work with bare hands or by putting on cotton gloves and non-charging working clothes.
- b. Discharge the static electricity by providing earth plate or earth wire on the floor, door or stand of the work room.
- c. Ground the tools such as soldering iron, radio cutting plier or pincette. It is not necessarily required to execute all precaution items for static electricity. It is all right to mitigate the precautions by confirming that the trouble rate within the prescribed range.

#### 2. Window Glass

As the dust and station on the glass window of the package will cause black flow on the picture, never fail to clean the glass surface before using. (Blow compressed vapor, and wipe off the dust, and dirt with soft cloth or paper slightly moistened with alcohol).

Fully take care for the handling of the device as the window glass will break or a strong friction is given to the window glass surface.

## 3. Incident Light

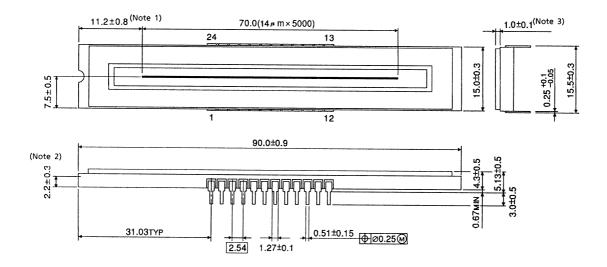
CCD image sensor has sensitivity in a wide range zone of light wave length, but its characteristics will sometimes widely change when used with long wave length input light outside the visual light zone.



## **PACKAGE DIMENSIONS**

WDIP24-C-600-2.54 (D)

Unit: mm



Note 1: No. 1 SENSOR ELEMENT (S1) TO EDGE OF PACKAGE.

Note 2: TOP OF CHIP TO BOTTOM OF PACKAGE.

Note 3: GLASS THICKNES (n = 1.5)

Weight: 17.1 g (Typ.)