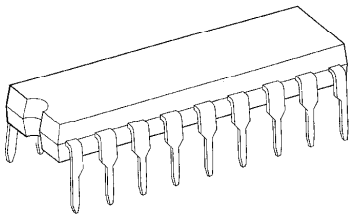
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC9181P, TC9181F

PLL FREQUENCY SYNTHESIZER LSI FOR COMMUNICATION USE

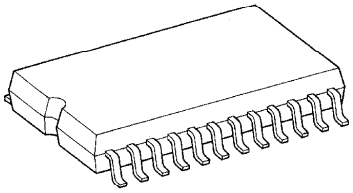
The TC9181P and TC9181F are developed as PLL frequency synthesizer LSI for communication use and has following features.

TC9181P



DIP18-P-300-2.54A

TC9181F



SOP24-P-450-1.27A

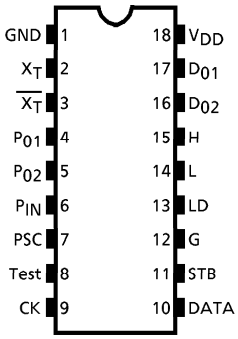
Weight
DIP18-P-300-2.54A : 1.12g (Typ.)
SOP24-P-450-1.27A : 0.44g (Typ.)

FEATURES

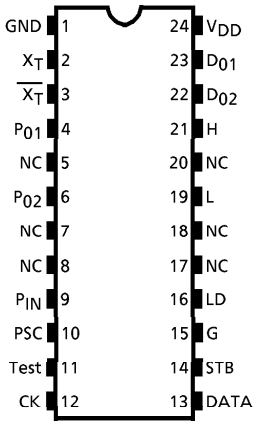
- Enable to be used as PLL LSI in many communication equipments e.g., Personal radio, Mobil telephone, CB radio and so on, because of it's various purposive system design.
- Built in 12 bits programmable counter as a reference frequency divider, so frequency division range of programmable counter is 5~4095 divisions according to serial data.
- Built in swallow type programmable counter to generate very high frequency.
- Phase comparator circuit has 3 types of output and replace of it inputs is possible.
- With 2 wide purposive output ports.
- Enable to be controlled by only 3 serial lines (DATA, CK, STB).

PIN CONNECTION

TC9181P



TC9181F



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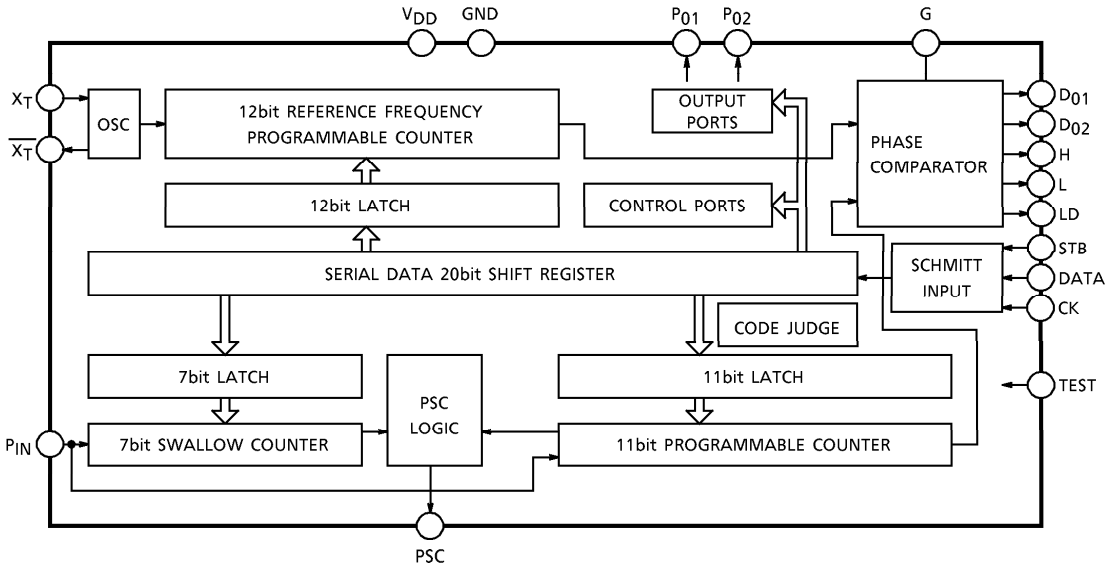
BLOCK DIAGRAM



PIN FUNCTION

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
1	GND	Ground-1	Logic ground terminal.	—
2 3	X_T $\overline{X_T}$	Crystal oscillator terminal	Reference frequency crystal oscillator connection terminal.	—
4 5	P_{01} P_{02}	Wide purposive output port-1, 2	Wide purposive output ports externally controllable by serial data.	—
6	P_{IN}	Programmable counter input	Programmable counter input terminal. Input an external prescaler output through a coupling capacitor.	—
7	PSC	Prescaler control	2 modulus prescaler frequency division ratio switching control terminal. At "H" level, division ratio = P At "L" level, division ratio = P + 1	—
8	Test	Test terminal	Normal operation at "L" level. Test mode operation at "H" level.	—
9 10 11	CK DATA STB	Serial data input	Serial data input terminals to control this LSI externally. Schmitt trigger input.	—
12	G	Ground-2	Ground terminal of phase comparator charge pump.	—
13	LD	Lock detector	Output "H" level signal when phase comparator detects lockout state. Enable to be set compulsorily by data given externally.	—
14 15	L H	Phase comparator output	Phase comparator output terminals to connect external high voltage charge pump.	—
16 17	D_{02} D_{01}	Phase comparator charge pump output	D_{01}, D_{02} are tri-state outputs. D_{01} always outputs and D_{02} is able to be controlled ON / OFF externally. Effective to shorten lock-up time.	—
18	V_{DD}	Power supply	+ 5V power supply terminal.	—

OPERATIONS

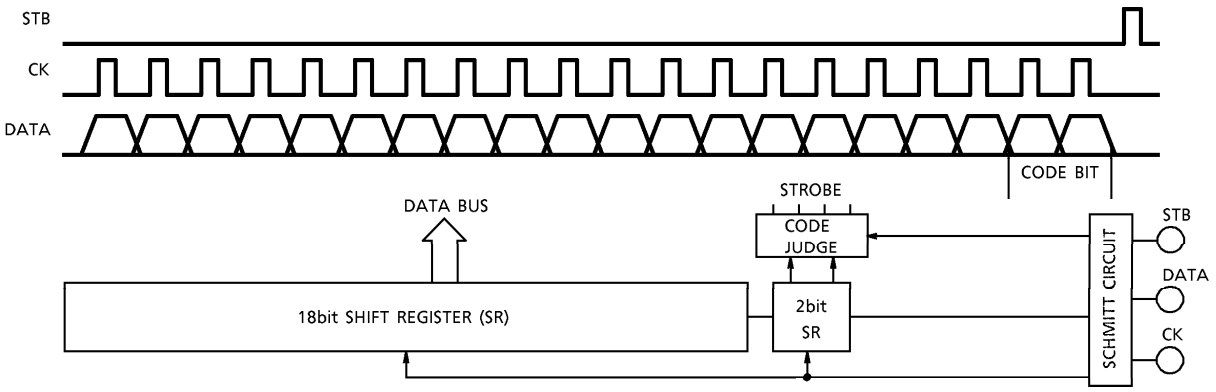
1. Serial data input

Serial data can control 4 group functions separately.
Data is always input from LSB and final 2bit data selects the group.

- Group 1 — Reference divider frequency division ratio.
  Phase comparator S, R inputs replace.
- Group 2 — Programmable counter frequency division ratio.
- Group 3 — Wide purposive output ports.
- Group 4 — Phase comparator D_{02} output ON / OFF control.
  Lock detector compulsory set.

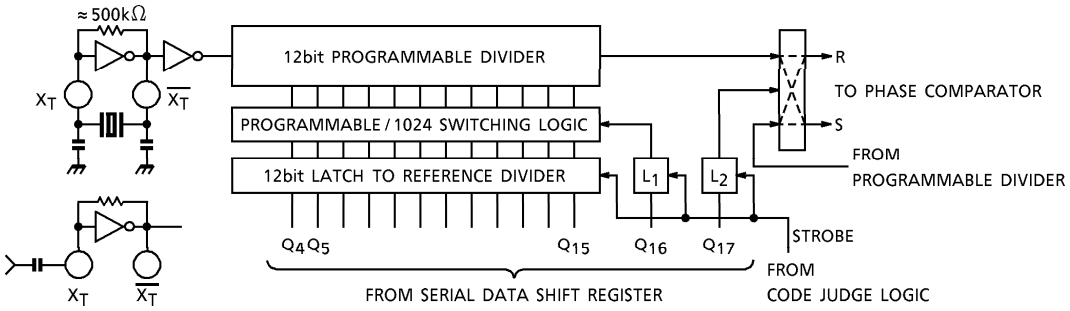
Serial data is composed of 3 lines of DATA, CK and STB.
DATA is input orderly in internal shift register at going rising edge of CK.
By setting STB "H" level after all DATA is input, DATA is transferred to the latch selected by the group code and this LSI can be controlled.
Serial data input 3 terminals build in schmitt trigger circuits that protect from data error by noise.

Concerning the data status of each group, refer to the respective block explanations.



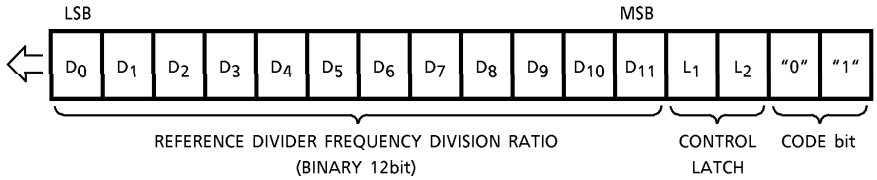
2. Reference divider

This block generates PLL reference frequency and is composed of Crystal oscillation amp, 12bit programmable divider and 2 control ports.



- Crystal oscillation amp allows crystal oscillation up to 15MHz and inputting signal in XT terminal externally up to 15MHz through a coupling capacitor.
- Programmable divider is composed of binary 12bit.
  Voluntary frequency division of range 5~4095 division is possible by serial data given externally. So a crystal to generate reference frequency can be selected freely and common use of the crystal using other purpose is possible.
  By setting Latch-1 (L_1) at "H" level, frequency division ratio is fixed at 1024 division neglecting serial data.
  And at this time serial data becomes brief.
- Latch-2 (L_2) is a control latch to replace reference divider output and programmable counter output before inputting to phase comparator circuit.
  Set L_2 at "L" level when external low pass filter is an inversion type, and set "H" level when not an inversion type.
- Serial data

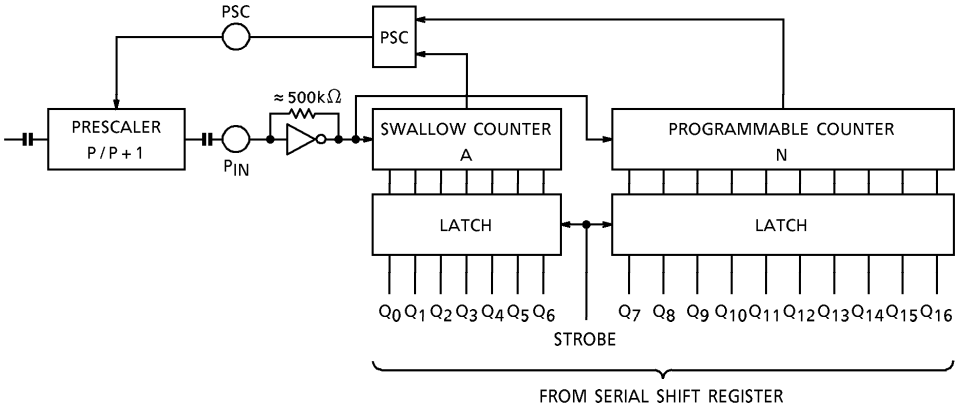
  Serial data to control reference divider block is of 16bit as following construction.



* D_0~D_{11} is binary code N of frequency division ratio intended.
$5 \leqq N \leqq 4{,}095$

3. Programmable counter

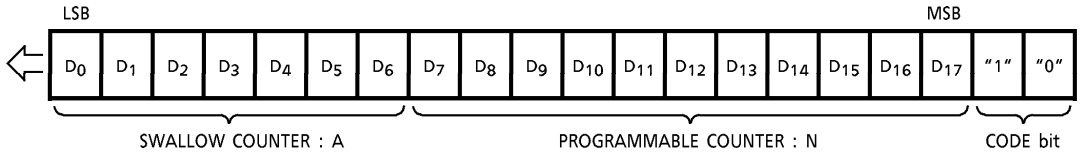
Programmable counter circuit adopts swallow system to generate high frequency and is composed of 7bit swallow counter, 11bit programmable counter and prescaler control logic to switch frequency division ratio of 2 modulus prescaler connected externally.



- Total frequency division ratio is defined as follows.
  Frequency division ratio = $(P+1)\cdot A + P\cdot(N-A)$
  $= P\cdot N + A$ (Note) : $N > A$
- Frequency division ratio of the external prescaler should be "P + 1" when PSC is "L" level and "P" when PSC is "H" level.
- Serial data

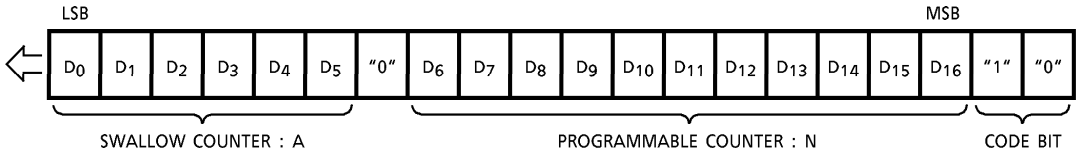
  Serial data which defines frequency division ratio of programmable counter is composed of 20bit but changes according to "P" of external prescaler.

  (1) When used with an external prescaler of P = 128



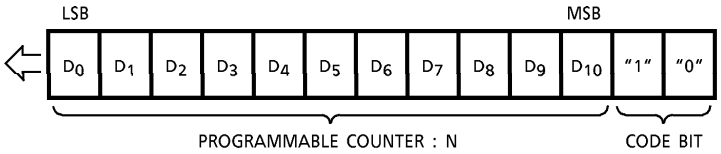
* $D_0 \sim D_{17}$ is binary code D of frequency division ratio intended.
Generally $16{,}384 \leqq D \leqq 262{,}143$

(2) When used with an external prescaler of P = 64



* D_0~D_{16} is binary code D of frequency division ratio intended.
The 7th bit should be fixed at "L".
Generally 4,096 ≦ D ≦ 131,071

(3) When used as a normal programmable counter



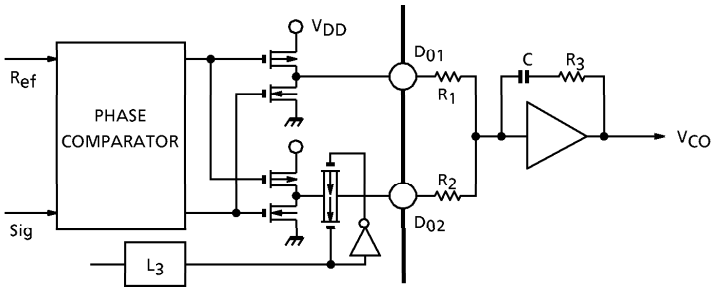
* D_0~D_{10} is binary code D of frequency division ratio intended.
$5 \leqq D \leqq 2{,}047$

4. Phase comparator

Phase comparator converts phase difference of reference divider output and programmable counter output into V_{CO} control voltage and has features as following.

- Always operating ordinary tri-state output (D_{01}).
- Tri-state output (D_{02}) which can be controlled ON / OFF according to serial data given externally.
- Phase comparator outputs (H, L) to connect high voltage charge pump externally.
- Lock detector output (LD) which can be compulsorily set by data given externally.

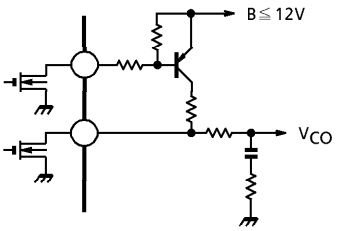
(1) Example use of D_{01}, D_{02} terminal



When change a channel, ON the D_{02} output and make the time constant of the low pass filter smaller to make PLL lock state fastly.
And after PLL is locked, OFF the D_{02} output and make the time constant larger to improve side-band spurious feature and stability.

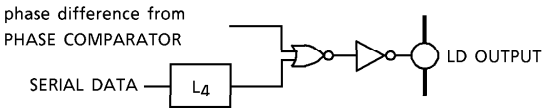
(2) Example use of H, L terminals

When connect an external passive low pass filter, supply voltage of charge pump should be high. In this case connect an external PNP transistor as a right figure.



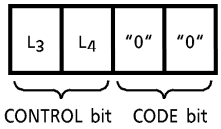
- Lock detector

Lock detector (LD) outputs pulse signal during phase deference time detected by phase detector circuit.
Additionally this lock detector output can be fixed unlocked state compulsorily by serial data given externally.
By fixing LD unlocked state just before channel changing to stop transmission output and canceling unlocked state after a definite time from the channel changing, troubles at channel changing e.g., overshoot can be prevented from.



- Serial data

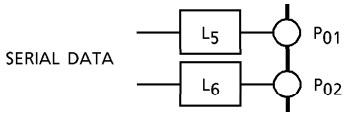
Serial data controls concerning phase comparator circuit are tri-state output ON / OFF control and lock detector compulsory set mentioned before.
They are composed of 4 bits serial data as below.

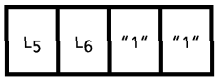


L_3 : D_{02} CONTROL bit
L_4 : LD CONTROL bit

5. Wide purposive output port

P_{01}, P_{02} output ports are available to many functions e.g., transmitter / receiver switching signal, band switching signal, sensibility switching and frequency band switching, according to serial data.





L_5 : P_{01}
L_6 : P_{02}

6. Test circuit

When Test terminal (8 pin) is placed at "H" level, this LSI is placed in the test mode as followings.

1. P_{01} terminal outputs reference divider output.
2. P_{02} terminal outputs programmable counter output.

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	−0.3~7.0	V
Input Voltage	V_{IN}	−0.3~V_{DD} + 0.3	V
Power Dissipation	P_D	300	mW
Operating Temperature	T_{opr}	−30~85	°C
Storage Temperature	T_{stg}	−55~125	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta = 25°C, V_{DD} = 5V)

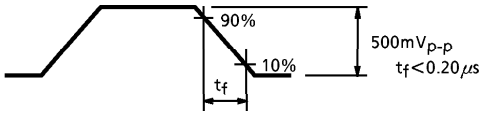
CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage	V_{DD}	—	$f_{OSC} = f_{PIN}$ = 10MHz, $V_{PIN} = 0.5V_{p-p}$, Ta = −30~85°C	4.0	5.0	6.0	V
Operating Supply Current	I_{DD}	—	$f_{OSC} = f_{PIN}$ = 10MHz, $V_{PIN} = 0.5V_{p-p}$, Ta = −30~85°C	—	2.0	5.0	mA
Reference divider block							
X'tal Oscillating Frequency	f_{OSC}	—	V_{DD} = 4~6V	1.0	—	15.0	MHz
X_T Input Frequency	f_{XTin}	—	V_{DD} = 4~6V, V_{XTin} = 100mV_{rms}	1.0	—	15.0	MHz
X_T Input Voltage	V_{XTin}	—	V_{DD} = 4~6V, f_{XT} = 10MHz	100	—	—	mV_{rms}
Programmable counter block							
P_{IN} Frequency	f_{Pin}	—	V_{DD} = 4~6V, $V_{Pin} = 0.5V_{p-p}$	1k	—	10M	Hz
P_{IN} Input Voltage	V_{Pin}	—	V_{DD} = 4~6V, f_{Pin} = 10MHz	0.5	—	—	V_{p-p}
Phase comparator block (D_{01}, D_{02}, LD, H, L)							
Output Current	"H" Level	I_{OH}	—	D_{01}, D_{02}, LD V_{DD} = 5V, V_{OH} = 4V	0.5	1.5	3.0	mA
	"L" Level	I_{OL}	—	D_{01}, D_{02}, LD, H, L V_{DD} = 5V, V_{OL} = 1V	0.5	1.5	3.0	mA
Breakdown Voltage		V_O	—	H, L, V_{DD} = 4~6V	—	—	12.0	V
Off Leak Current		I_L	—	D_{01}, D_{02}, H, L V_{DD} = 6V	—	—	0.1	μA
Output port (P_{01}, P_{02})							
Output Current	"H" Level	I_{OH}	—	V_{DD} = 5V, V_{OH} = 4V	0.5	1.5	3.0	mA
	"L" Level	I_{OL}		V_{DD} = 5V, V_{OL} = 1V	0.5	1.5	3.0	

Serial input (CK, DATA, STB)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage	"H" Level	V_{IH}	—	V_{DD} = 5V	3.8	—	5.0	V
	"L" Level	V_{IL}		V_{DD} = 5V	0.0	—	1.2	
Input Speed		S_{IN}	—	—	5	—	—	μs

(Note 1) X_T : SIN wave input
P_{IN} : SQ wave input

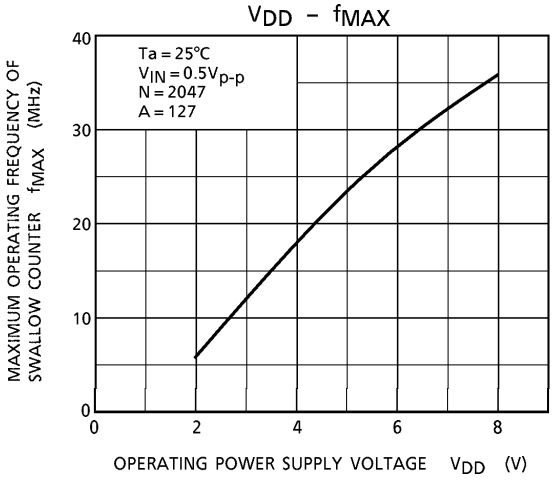
(Note 2) Falling of P_{IN} input wave have a rule as following.

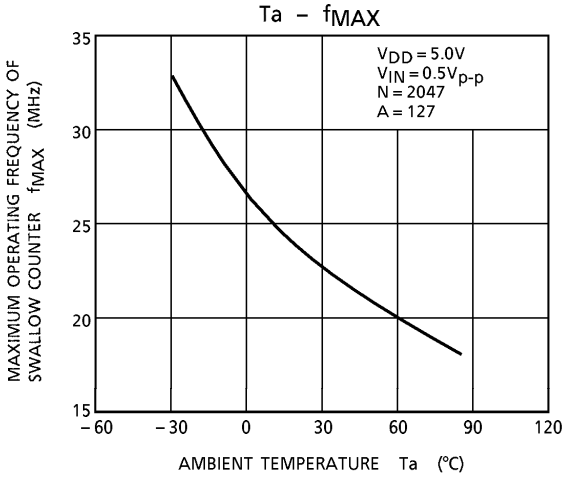


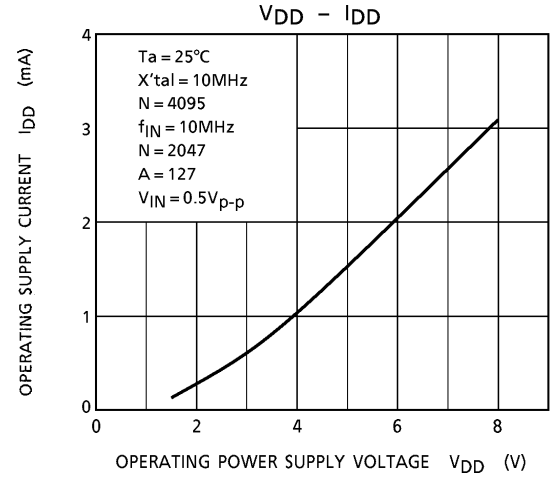
* $t_f < 0.20\mu s$

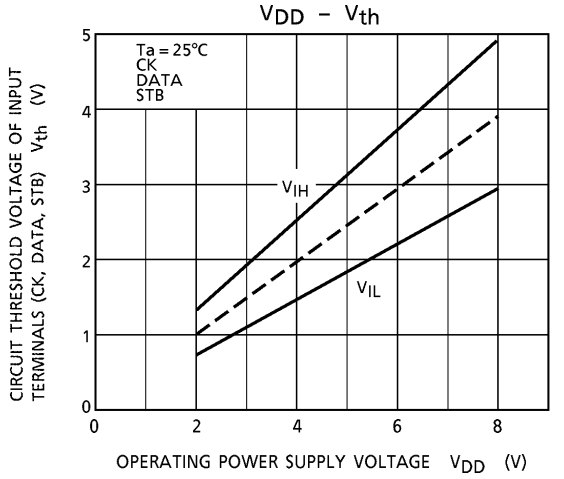
(Note 3) Choose a crystal oscillator that has a small CI value and good startup characteristics.

CHARACTERISTIC DATA





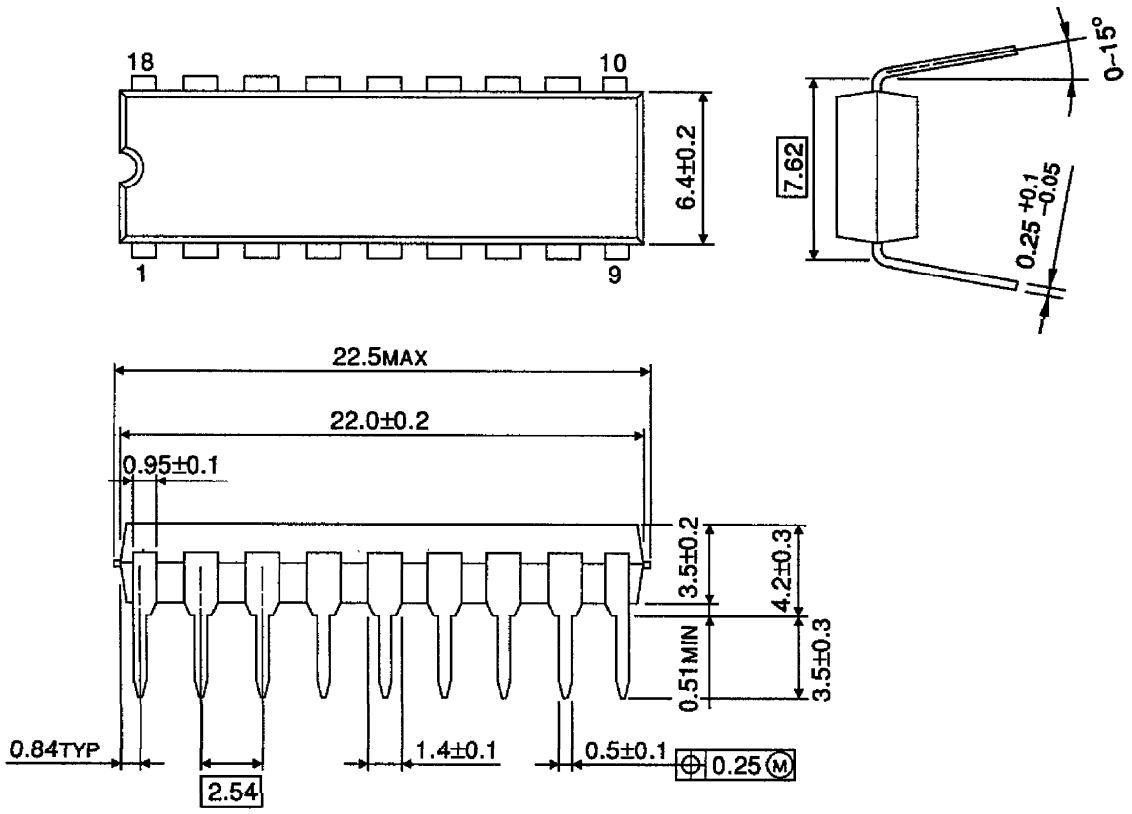




OUTLINE DRAWING

DIP18-P-300-2.54A

Unit : mm

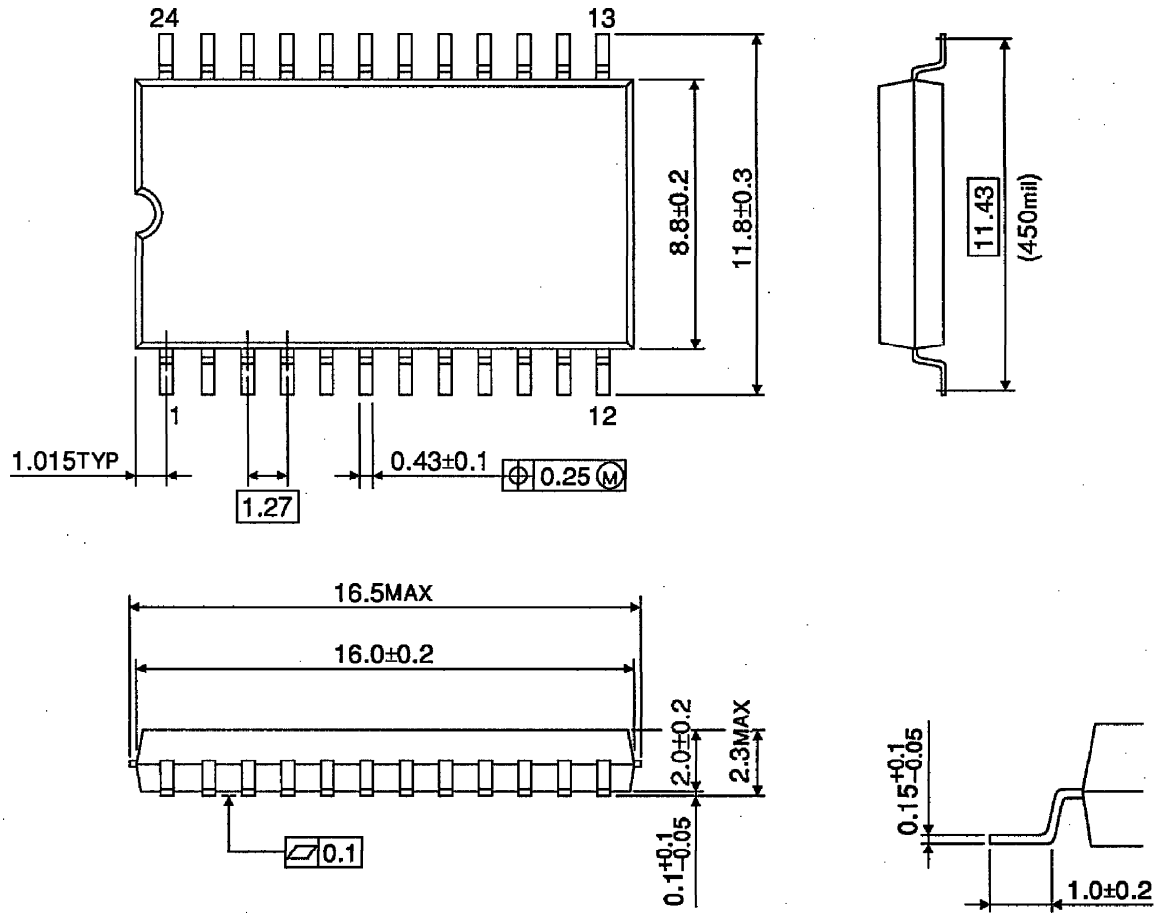


Weight : 1.12g (Typ.)

OUTLINE DRAWING

SOP24-P-450-1.27A

Unit : mm



Weight : 0.44g (Typ.)