INTEGRATED CIRCUIT

TOSHIBA

TECHNICAL DATA

TOSHIBA CCD AREA IMAGE SENSOR

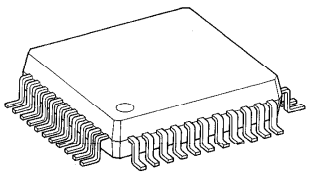
TC6162AU

CCD(Charge Coupled Device)

GENERAL

The TC6162AU is a CMOS LSI chip for generating NTSC television synchronization signals and operating a 400,000- pixel FITCCD area image sensor.

This chip covers the electronic shutter mode of 1/60 to 1/2000 seconds. It has a vertical reset pin that enables synchronizing with an external system.



QFP44-P-1010A

Weight : 0.56g (Typ.)

FEATURES

- Generation of NTSC television synchronization signals.
- Generation of pulses for operation the vertical register of the CCD area image sensor.
- An electronic shutter mode of 1/60 to 1/2000 seconds.
- Synchronization with as external.

MAXIMUM RATINGS (V_{SS} = 0V)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	−0.3~7.0	V
Input Voltage	V_{IN}	−0.3~V_{DD} + 0.3	V
Input Current	I_{IN}	±20	mA
Storage Temperature	T_{stg}	−40~125	°C

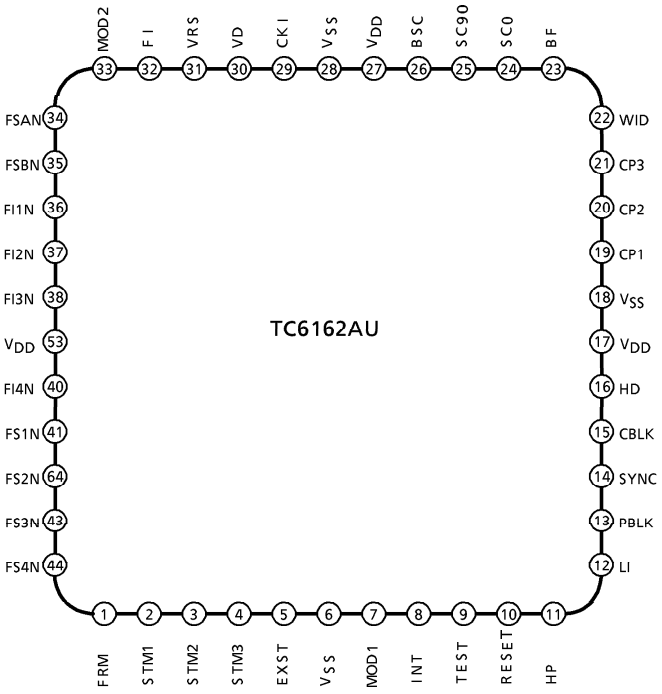
OPERATING CONDITIONS (V_{SS} = 0V)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	4.75~5.25	V
Operating Temperature	T_{opr}	0~70	°C

ELECTRICAL CHARACTERISTICS (V_{SS} = 0V, V_{DD} = 4.75~5.25V, Ta = 0~70°C)

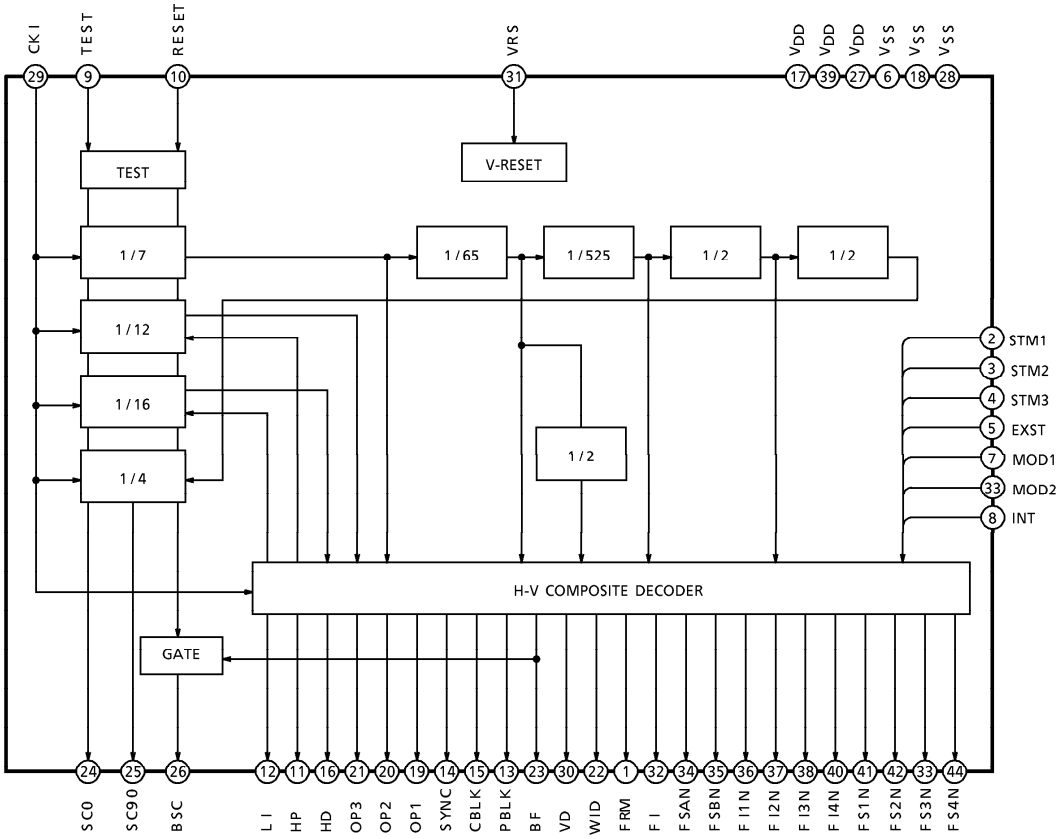
CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage (high)	V_{IH}	VRS	4.0	—	—	V
		All inputs except VRS	3.5	—	—	
Input Voltage (low)	V_{IL}	VRS	—	—	1.0	V
		All inputs except VRS	—	—	1.5	
Input Current (high)	I_{IH}	$V_{IN} = V_{DD}$	− 10	—	10	μA
Input Current (low)	I_{IL}	$V_{IN} = V_{SS}$, CKI	− 10	—	10	μA
		All inputs except CKI	− 200	—	− 10	
Output Voltage (high)	V_{OH}	I_{OH} = − 4mA, HP	2.4	—	—	V
		I_{OH} = − 1mA, WID				
		I_{OH} = − 2mA All output except WID, HP				
Output Voltage (low)	V_{OL}	I_{OL} = 4mA, HP	—	—	0.4	V
		I_{OL} = 1mA, WID				
		I_{OL} = 2mA All output except WID, HP				
Supply Current	I_{DD}	C_L = 0pF	—	20	—	mA

PIN CONNECTION



(TOP VIEW)

BLOCK DIAGRAM



PIN FUNCTIONS

<table>
<tr><th>PIN No.</th><th>SYMBOL</th><th>I/O</th><th>FUNCTION</th></tr>
<tr><td>1</td><td>FRM</td><td>O</td><td>Frame pulse output. This pulse is generated once per frame on the second or fourth field. It remains high for 3H-wide.</td></tr>
<tr><td>2
3
4</td><td>STM1
STM2
STM3</td><td>I</td><td>Inputs on STM1-STM3 set the shutter speed. The set values and shutter speeds are:
<table>
<tr><th>Shutter speed (s)</th><th>STM1</th><th>STM2</th><th>STM3</th></tr>
<tr><td>1/60 (1/30)</td><td>H</td><td>H</td><td>H</td></tr>
<tr><td>1/100</td><td>H</td><td>H</td><td>L</td></tr>
<tr><td>1/120</td><td>H</td><td>L</td><td>H</td></tr>
<tr><td>1/250</td><td>H</td><td>L</td><td>L</td></tr>
<tr><td>1/500</td><td>L</td><td>H</td><td>H</td></tr>
<tr><td>1/1000</td><td>L</td><td>H</td><td>L</td></tr>
<tr><td>1/2000</td><td>L</td><td>L</td><td>H</td></tr>
<tr><td>EXST</td><td>L</td><td>L</td><td>L</td></tr>
</table>
The speed in parentheses is the frame storage mode.</td></tr>
<tr><td>5</td><td>EXST</td><td>I</td><td>An external input on EXST controls the shutter speed. When the input on STM1-STM3 are all low, this pin is enabled. When the input on EXST goes low, shutter speed control is enabled in the range of 1/62 to 1/1386 seconds in increments of 1/15734 seconds.</td></tr>
<tr><td>6</td><td>V_{SS}</td><td>—</td><td>GND</td></tr>
<tr><td>7</td><td>MOD1</td><td>I</td><td>Mode pin 1 that is open for normal use.</td></tr>
<tr><td>8</td><td>INT</td><td>I</td><td>An input on INT changes the storage mode.
High-level input: Field storage mode
Low-level input : Frame storage mode</td></tr>
<tr><td>9</td><td>TEST</td><td>I</td><td>Test input. This pin open for normal use.</td></tr>
<tr><td>10</td><td>RESET</td><td>I</td><td>Reset input. A low-level input on RESET initializes the internal circuits. This pin is open for normal use.</td></tr>
<tr><td>11</td><td>HP</td><td>O</td><td>Horizontal transfer control pulse output. The high-level indicates the period during which horizontal CCD driving pulse ϕH is not generated connected to pin HP of the horizontal driving IC.</td></tr>
<tr><td>12</td><td>LI</td><td>O</td><td>Line identification pulse output. This pulse alternately gone high and low every horizontal cycle, and is reset on the frame cycle.</td></tr>
<tr><td>13</td><td>PBLK</td><td>O</td><td>Pre-blanking signal output. high-level output indicates the blanking period. The pulse is a composite signal that is 9.8μs wide for the horizontal synchronization section and 18H wide for the vertical synchronization section.</td></tr>
<tr><td>14</td><td>SYNC</td><td>O</td><td>Composite synchronized signal output.</td></tr>
<tr><td>15</td><td>CBLK</td><td>O</td><td>Composite blanking signal output. Low-level output indicates the blanking period. The pulse is a composite signal that is 11μs wide for the horizontal synchronization section and 20H wide for the vertical synchronization section.</td></tr>
</table>

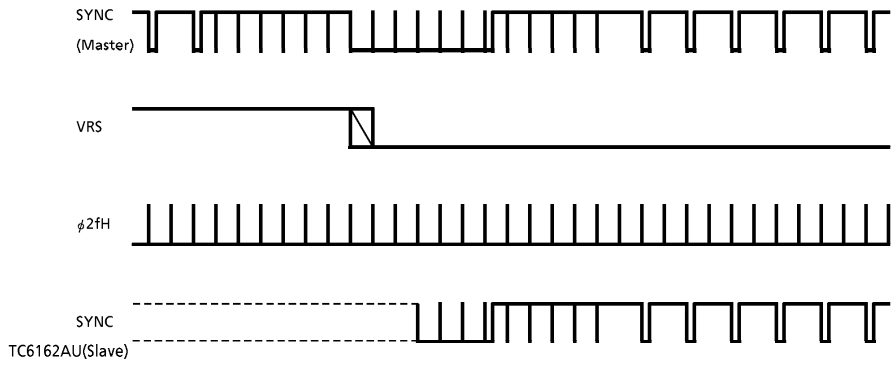
PIN No.	SYMBOL	I/O	FUNCTION
16	HD	O	Horizontal drive output. This pulse is output once per horizontal cycle. The 6.3μs wide pulse goes high from the beginning of the horizontal flyback time.
17	V_{DD}	—	A voltage of 5V ± 0.25V is supplied to this pin.
18	V_{SS}	—	GND
19	CP1	O	Clamp pulse output. This pulse clamps the black reference signal of a CCD output signal. It remains high for 1.5μs. Clamp pulse output is not generated at vertical flyback time when no black reference signal is output.
20	CP2	O	Clamp pulse output. This is a clamp pulse for signal processing. It remains high for 2.0μs.
21	CP3	O	Clamp pulse output. This is a clamp pulse for signal processing. It remains high for 2.9μs.
22	WID	O	Output of the window pulse for sampling the iris control signal. Low-level output indicated the sampling period.
23	BF	O	Bust flag output. This pulse gates a subcarrier. It remains high for 2.6μs.
24 25	SC0 SC90	O	Subcarrier output obtained by dividing the clock input to CKI by 4. The 3.579MHz clock is output. Compared with the pulse on SC0, the pulse on SC90 advances 90degrees in phase.
26	BSC	O	Burst subcarrier output obtained by gating a subcarrier with BF. The phase difference between the phase of the pulse on BSC and that of the pulse on SC0 is 270degrees.
27	V_{DD}	—	A voltage of 5V ± 0.25V is supplied to this pin.
28	V_{SS}	—	GND
29	CKI	I	Master clock input. A clock of 14.31818MHz is input on CKI. An internal pull-up resistor is not connected to this pin.
30	VD	O	Vertical drive output. The pulse is output once per field. It remains high for 3H.
31	VRS	I	Vertical reset input. A negative-going edge on this pin resets the vertical frequency divider. This pin is used for operation in synchronization with an external system. The input operates like a Schmitt-trigger input.
32	FI	O	Field identification pulse output. The pulse alternately goes high and low for each field. High-level output indicates the first or third field. Low-level output indicates the second or fourth field.
33	MOD2	I	Mode pin 2 changes the vertical CCD sweep transfer modes of the image section. The level is low for normal use.

PIN No.	SYMBOL	I/O	FUNCTION
34 35	FSAN FSBN	O	Field shift pulses for driving the vertical CCD. FSAN : ϕI1 FSBN : ϕI3 Each polarity is inverted. The pulses are connected to the vertical clock inverter driver.
36 37 38 40 41 42 43 44	FI1N FI2N FI3N FI4N FS1N FS2N FS3N FS4N	O	Line shift pulses for driving the vertical CCD. FI1N : ϕI1 FS1N : ϕS1 FI2N : ϕI2 FS2N : ϕS2 FI3N : ϕI3 FS3N : ϕS3 FI4N : ϕI4 FS4N : ϕS4 Each polarity is inverted. The pulses are connected to the vertical clock inverter driver.
39	V_{DD}	—	A voltage of 5V ± 0.25V is supplied to the pin.

Unless otherwise specified, internal pull-up resistors are connected to the input pins.

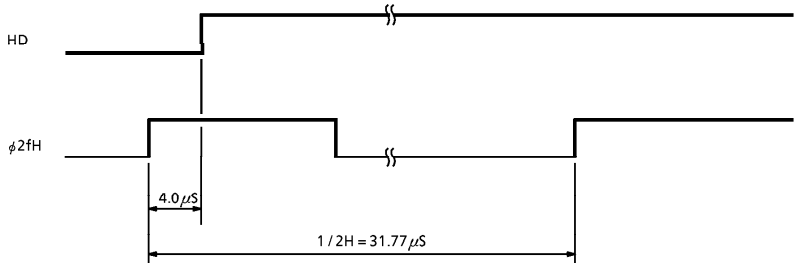
VRS PIN FOR OPERATION IN SYNCHRONIZATION WITH AN EXTERNAL SYSTEM

The VRS pin enables vertical resetting. The VRS pulse is input to the chip on its falling edge. Resetting is performed so that the falling edge of VRS appears for the first 0.5H of SYNC VS output.



The reset pulse is generated on ϕ2fH, which is not sent out of the chip. If the VRS pulse goes high around the ϕ2fH rising edge, reset time may fluctuate 0.5H. See the timing chart for the phase of the ϕ2fH pulse.

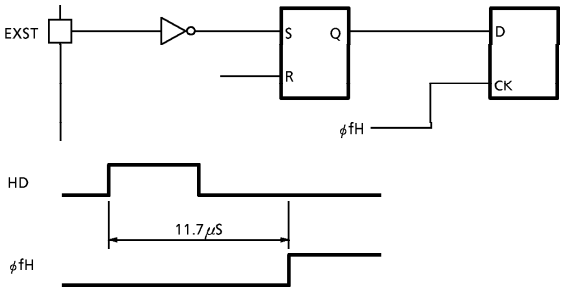
The VRS pin enables resetting in 0.5H units (minimum).
If the chip is synchronized with as external system, H synchronization by PLL is required.



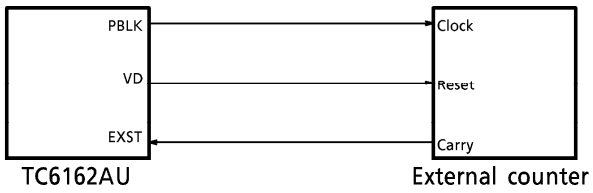
EXTERNAL SHUTTER MODE

If inputs on STM1-STM3 are all low, the external shutter mode is enabled and the shutter speed can be controlled by the timing of an input on EXST.

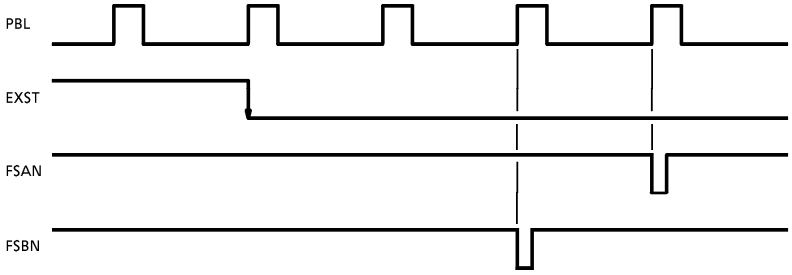
The input on EXST sets the internal RS-flip-flop on the falling edge, and the output of the flip-flop is processed on ϕfH. If the input on EXST goes low around the ϕfH rising edge, the shutter speed may fluctuate 1H.



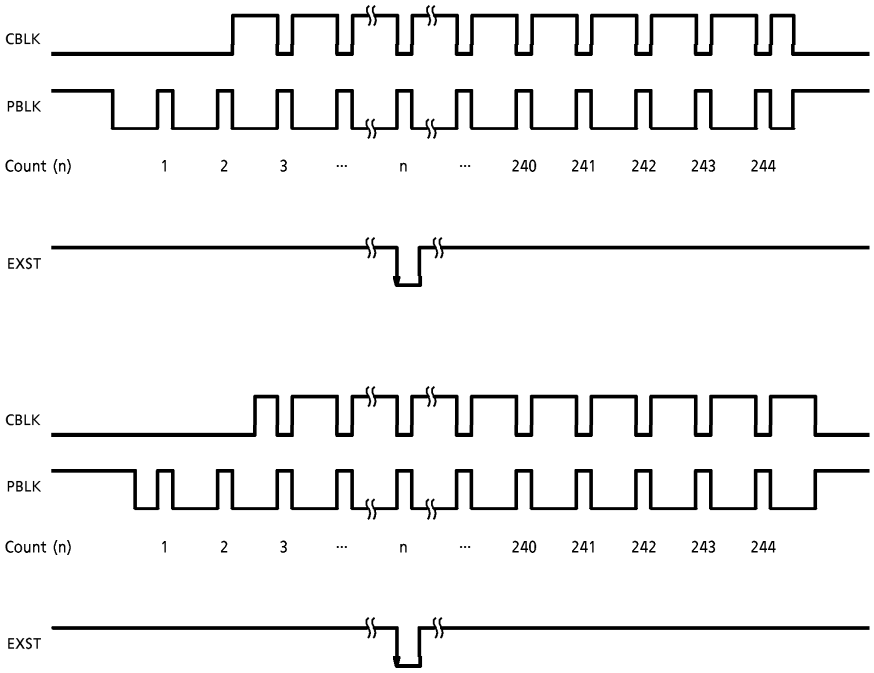
Generating the EXST pulse requires an external counter circuit. The external counter used the rising edge of the HD pulse as a clock, and is reset by the VD pulse.



The following chart shows the relationship between the falling edge of the EXST input and field shift pulse. When the EXST input goes low, the FSBN pulse is generated after 2H, and the FSAN pulse is generated after 3H.

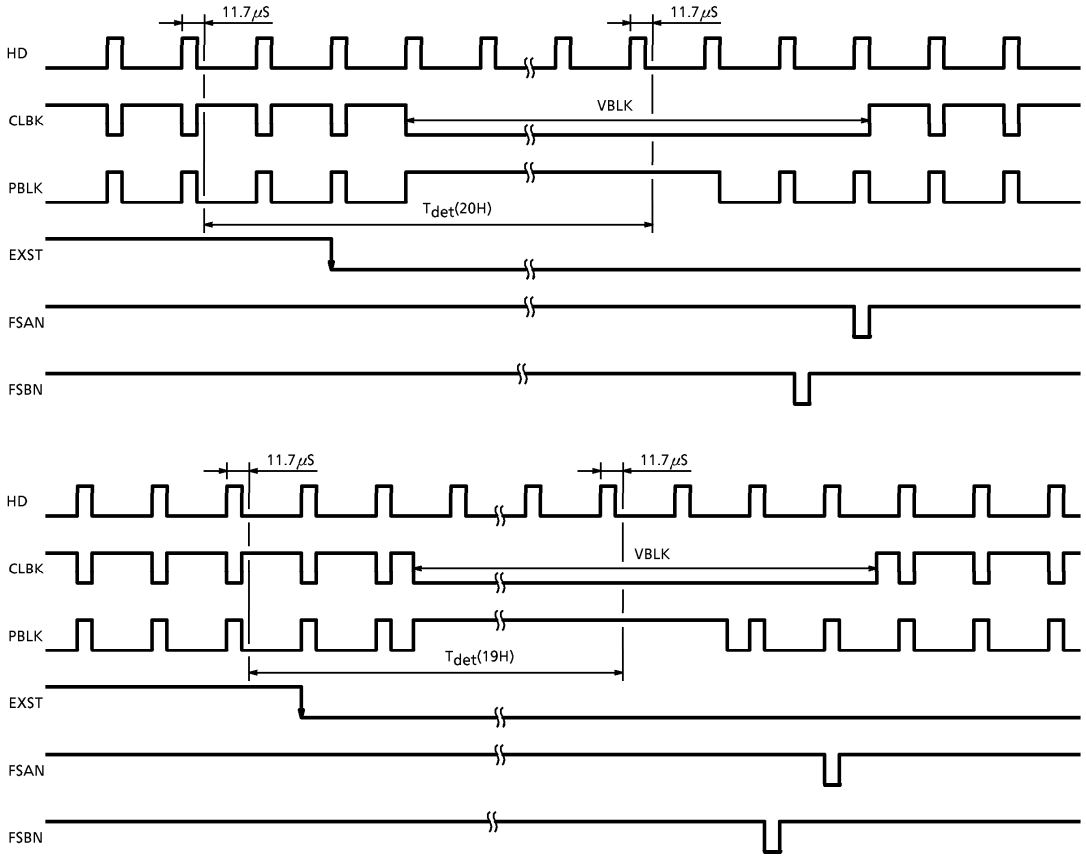


The shutter speed can be calculated with the count (n) of the external counter as follows:



$$\text{shutter speed} = \frac{253.5 - n}{15734.26} \text{ (s)}$$

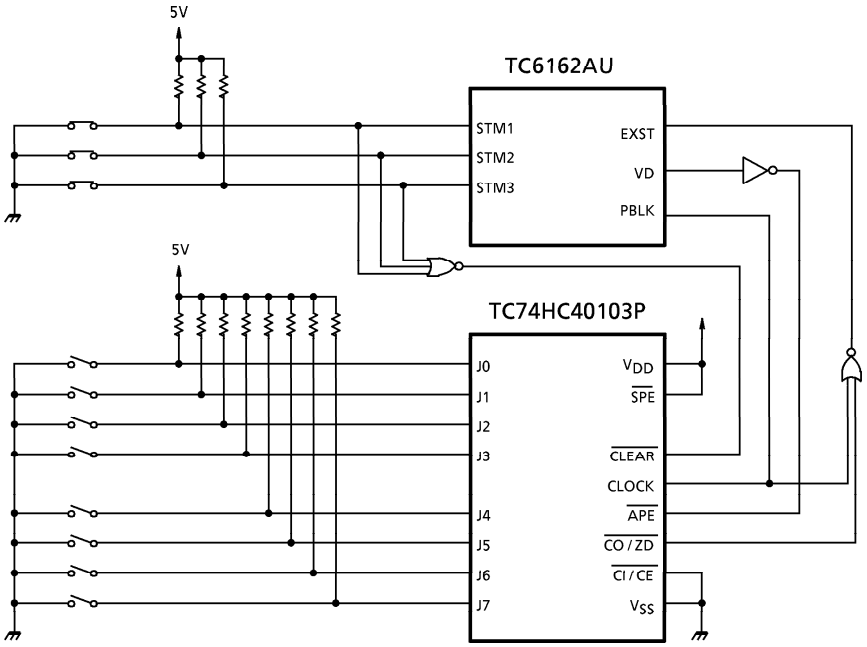
A shutter speed from 1/62 to 1/1368 s can be set in the external shutter mode. If the EXST input goes low for a period that does not conform to the range (Td period), the shutter speed is fixed to 1/62 s.



In the external shutter mode, the falling edge of the EXST pulse must be input for each field. The shutter-on field shift pulse is not generated unless a timing pulse is input to the EXST pin. Therefore, the storage time is 1/59.8 s for the first field and 1/60.0 s for the second field, so fricker occur to CCD output.

The EXST falling edge should not be input two or more times within one-field period. If the shutter-on field shift pulse is generated two or more times, an unnecessary charge increases overly in the vertical CCD, and it may fail to be removed from the CCD. The following shows an example of the counter circuit in the external shutter mode.

EXAMPE OF THE COUNTER CIRCUIT IN THE EXTERNAL SHUTTER MODE



Set values for J0~J7 and each storage time.

SET VALUE										STORAGE TIME	
DEC (I)	HEX	BIN								Lines	Time (s)
		J7	J6	J5	J4	J3	J2	J1	J0		
0	00	0	0	0	0	0	0	0	0	252.5H	1/62.31
1	01	0	0	0	0	0	0	0	1	251.5H	1/62.56
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
I		↓	↓	↓	↓	↓	↓	↓	↓	(252.5 – I) H	(252.5 – I)/ 15734.26
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
241	F1	1	1	1	1	0	0	0	1	11.5H	1/1368
242	F2	1	1	1	1	0	1	0	0	254.5H	1/61.82
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓		
244	F4	1	1	1	1	0	1	0	0		
245	F5	1	1	1	1	0	1	0	1	Must not be set	
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓		
256	FF	1	1	1	1	1	1	1	1		

STORAGE MODES

Storage modes can be changed with the INT pin.

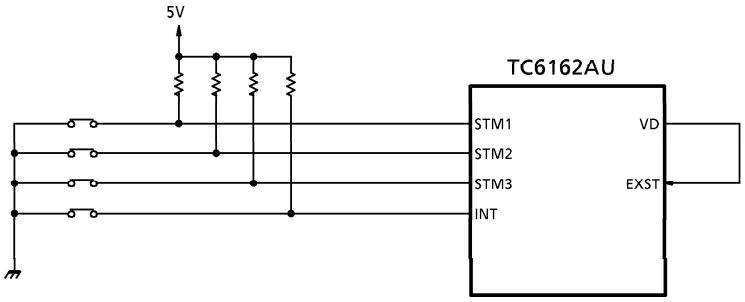
High-level input : Field storage mode.

Low-level input : Frame storage mode.

In the frame storage mode, the storage time is set to 1/30 s when inputs on shutter speed setting pins STM1 to STM3 are all high.

In the frame storage mode, the storage time cannot be set to 1/60 s. If the VD pin is connected to the EXST pin, and if inputs on STM1 to STM3 are all low (external shutter mode), however, the shutter speed can be set to 1/62 s.

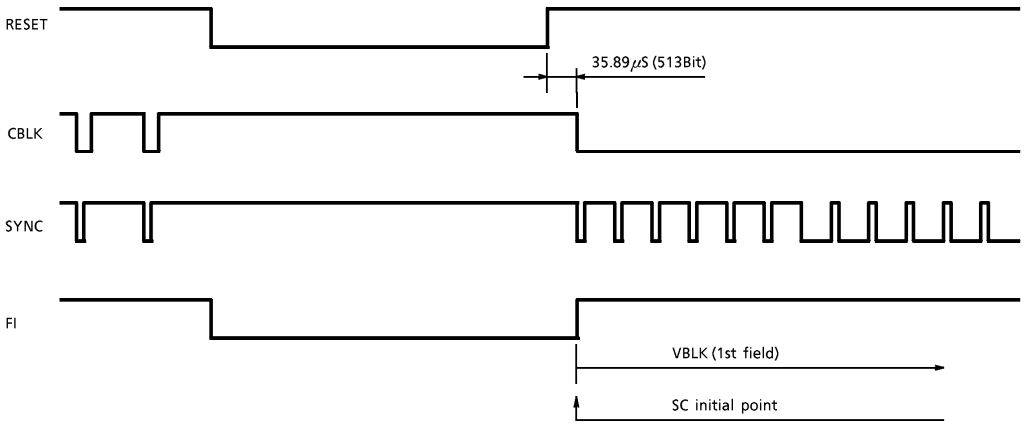
The sensitivity in the frame storage mode is half of that in the field storage mode at electronic shutter mode.



Setting the electronic shutter speed to 1/62 s.

RESET OPERATION

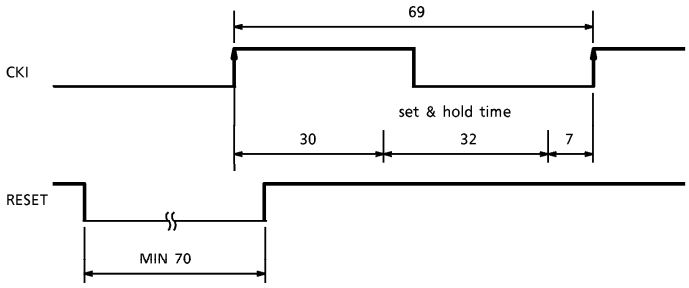
When the input on the RESET pin goes low, the internal circuit is reset, and all operations are stopped for the period of the low-level pulse. When the input on the RESET pin then goes high, the VBLK operation (first field) starts after 35.89μs (513 bits). (The SC output is reinitialized immediately after the VBLK operation starts.)



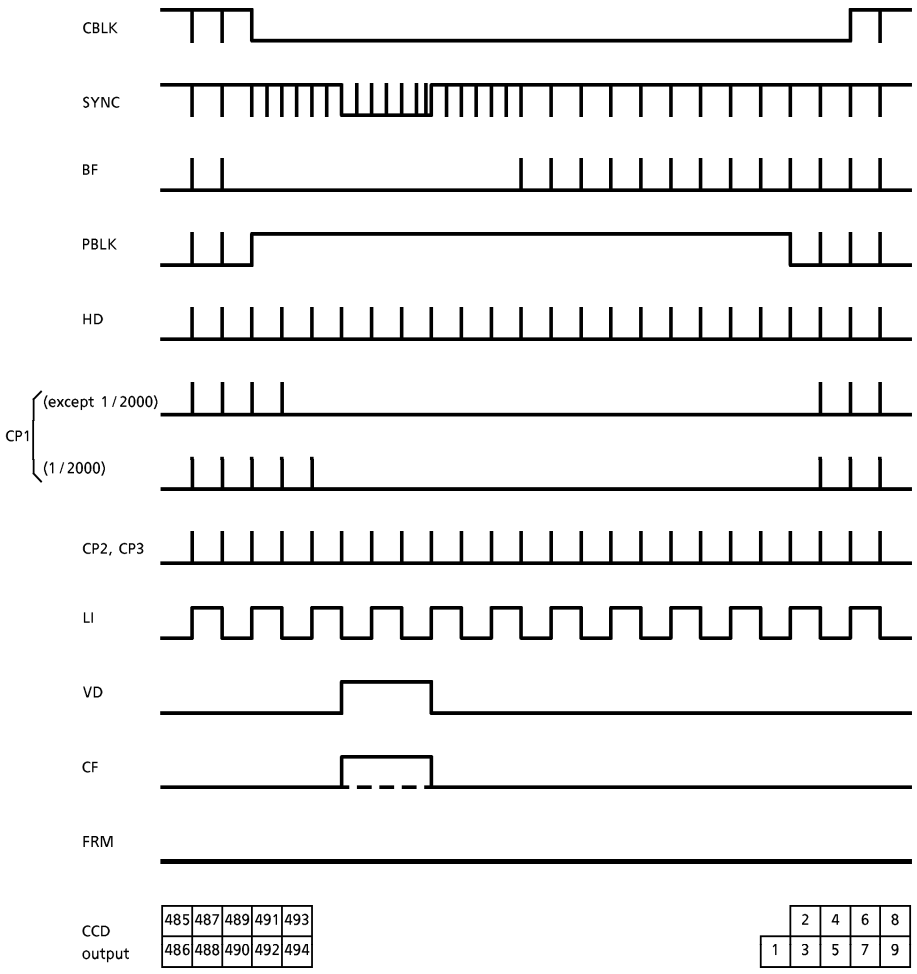
When the RESET pulse goes high within the set and hold time of the clock input on the CKI pin, the reset timing may shift one bit.

At least 70 ns is required for the period of the low-level input on RESET pulse.

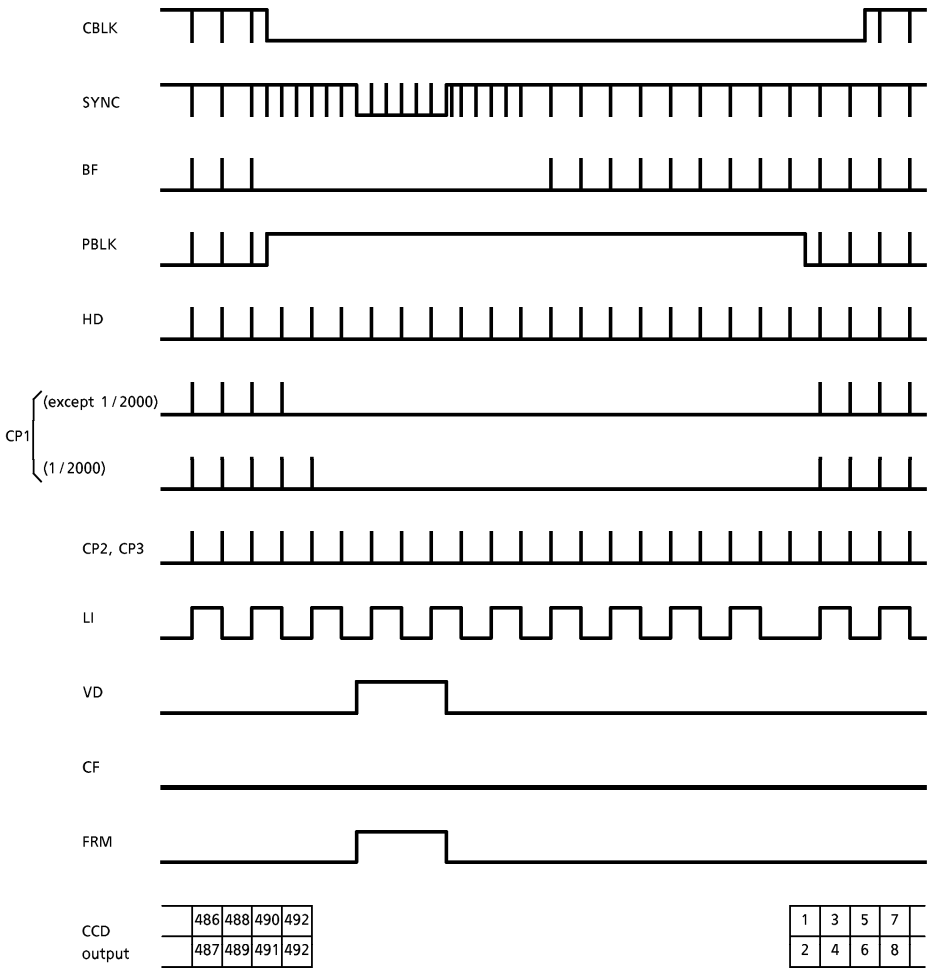
Unit : ns



TIMING CHART Ⅰ, Ⅲ field

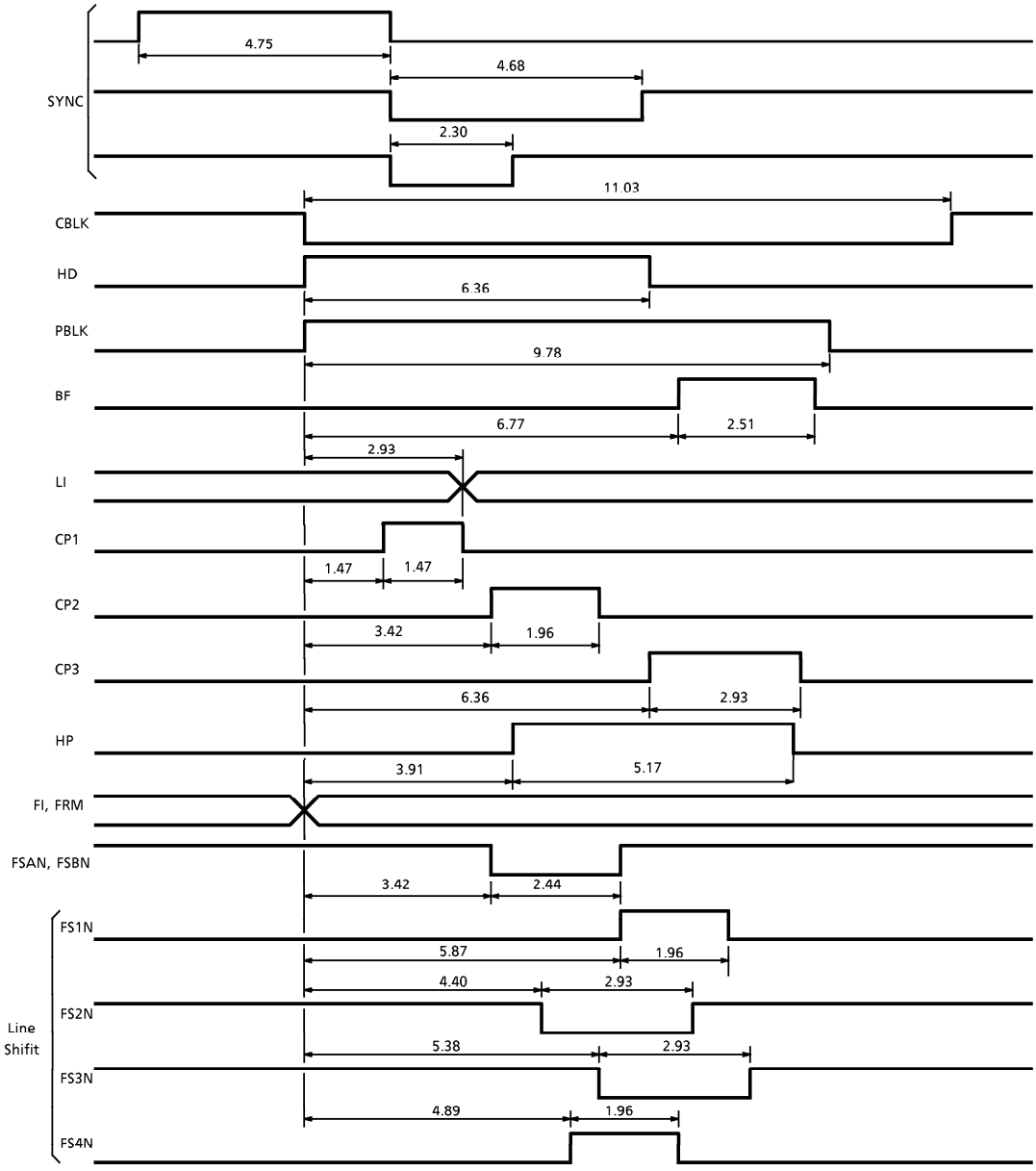


TIMING CHART Ⅱ, Ⅳ field



TIMING CHART

Unit : μs

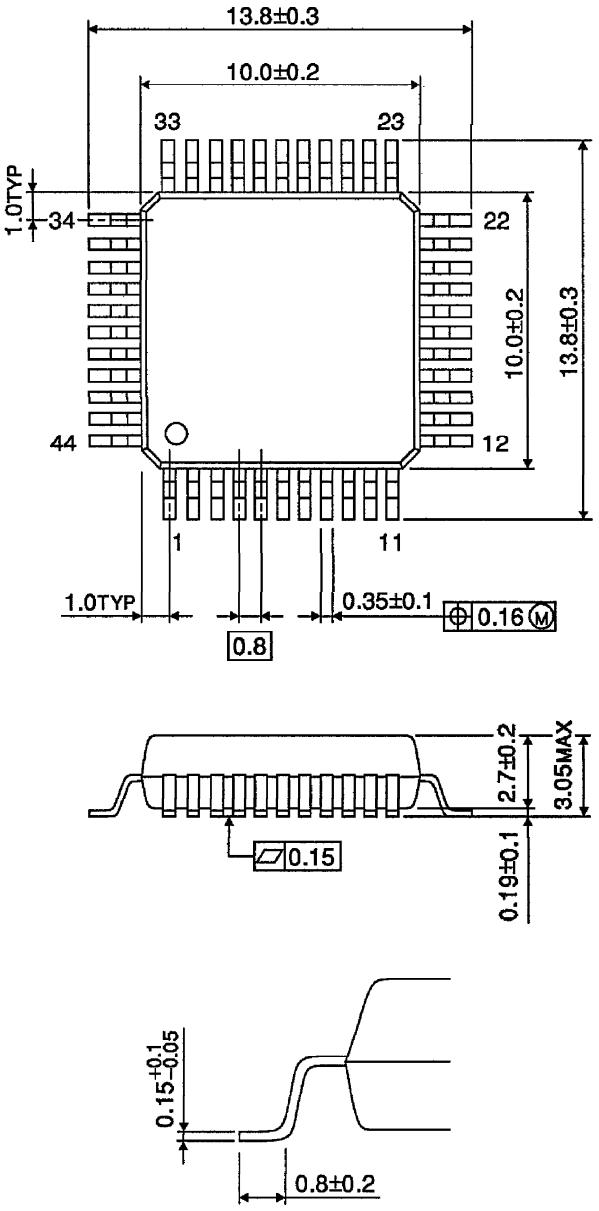


The values indicate periods converted from designed counts.

OUTLINE DRAWING

QFP44-P-1010A

Unit : mm



Weight : 0.56g (Typ.)

TC6162AU – 18*
1994 – 10 – 24
TOSHIBA CORPORATION