INTEGRATED CIRCUIT

TOSHIBA

TECHNICAL DATA

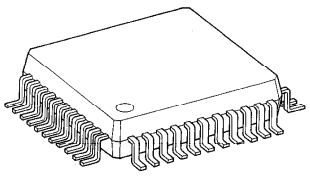
TOSHIBA CCD AREA IMAGE SENSOR

TC6024AU

CCD(Charge Coupled Device)

GENERAL

The TC6024AU is a CMOS LSI chip for driving CCD area image sensor.
When used with an IC for generating synchronizing signals, the TC6024AU can generate multiple timing signals.
The TC6024AU has the following features:



QFP44-P-1010A

Weight : 0.05g (Typ.)

FEATURES

- Horizontal CCD driving pulses H1A, H1B and H2 for the CCD area image sensor and reset gate driving pulse RS are generated to drive the CCD directly.
- CDS and color separation pulses are generated for the TA8790F, an IC for noise reduction and color separation.
- A 1/3 divider is included for eliminating the flickering of the fluorescent lamps.
- A clock input is divided by four and eight to generate outputs for driving delay lines.

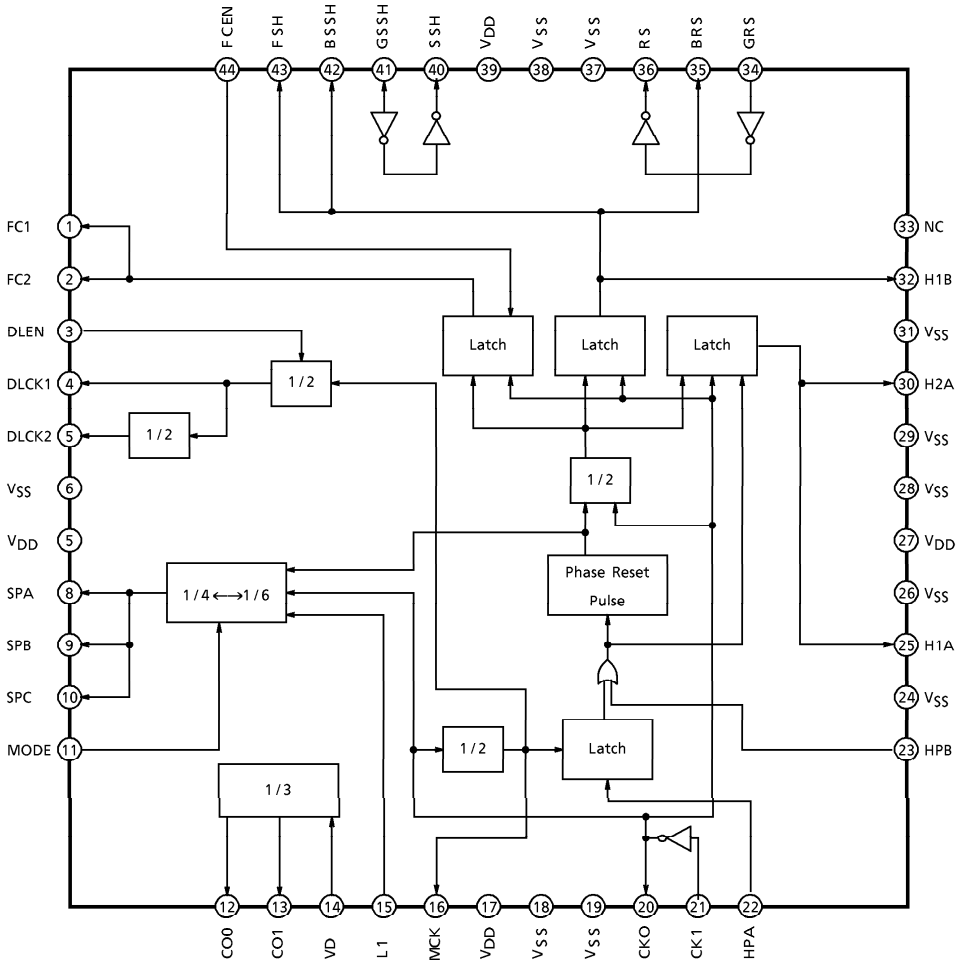
MAXIMUM RATINGS (V_{SS} = 0V)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	−0.3~7.0	V
Input Voltage	V_{IN}	−0.3~V_{DD} +0.3	V
Input Current	I_{IN}	±20	mA
Storage Temperature	T_{stg}	−20~125	°C

OPERATING CONDITIONS (V_{SS} = 0V)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	4.5~5.25	V
Operating Temperature	T_{opr}	0~70	°C

BLOCK DIAGRAM



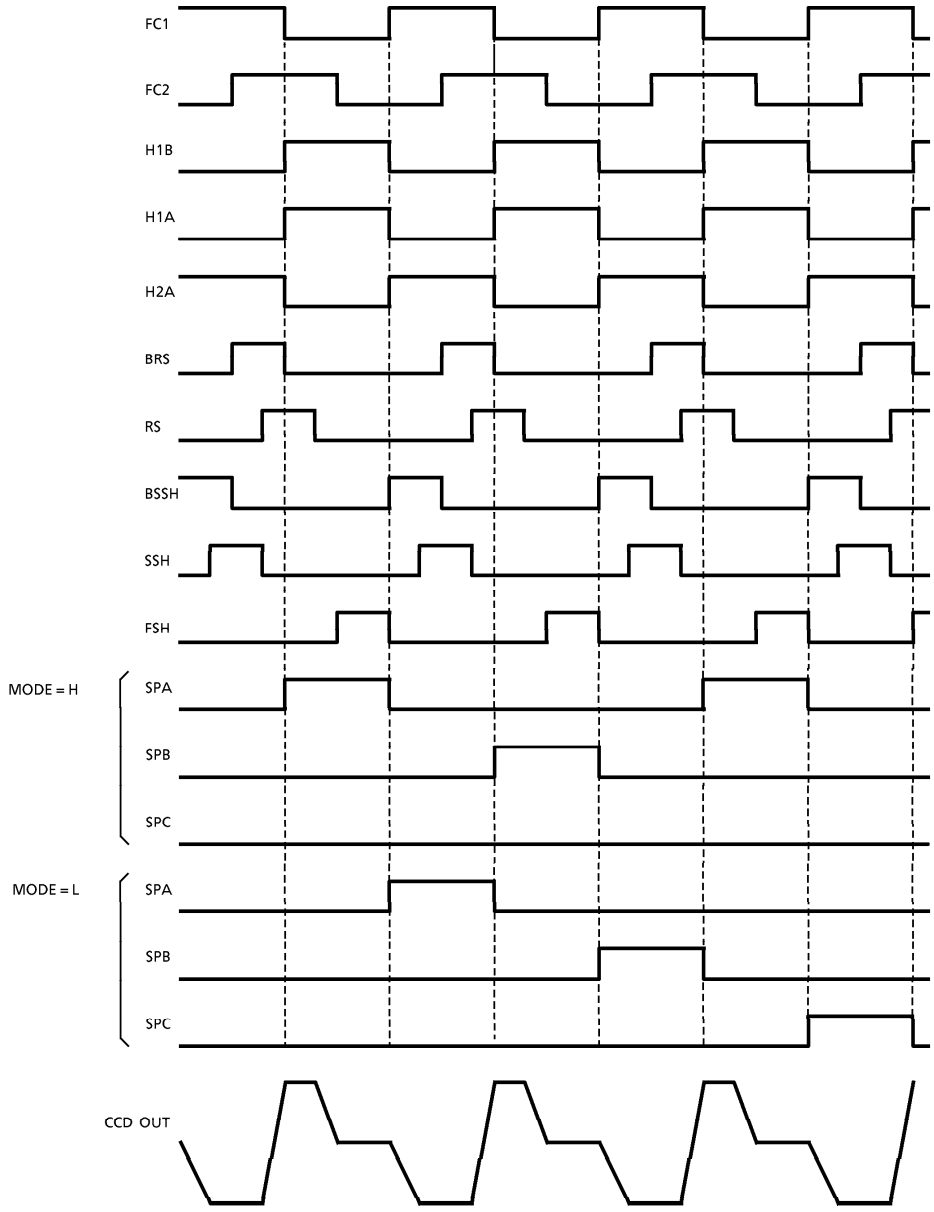
PIN FUNCTIONS

PIN No.	SYMBOL	I/O	FUNCTION
CLOCKS			
21	CKI	I	Clock input. The frequency of the CKI input is twice as high as that of the horizontal CCD driving signal (fck). No internal pull-up resistor is provided for this input.
20	CKO	O	The output on CKO is an inverted clock of the clock input on CKI. CKO is used for clock waveform shaping or for supplying a clock to the IC for generating synchronizing signals.
16	MCK	O	The output on MCK is a clock obtained by dividing the CKI input clock by two. Usually this clock is supplied to the IC for generating synchronizing signals.
CCD DRIVING PULSES			
22	HPA	I	The inputs on HPA and HPB control horizontal transfer for the CCD. A high input to HPA or HPB stops horizontal CCD driving pulses H1A and H2A. The HPA input is captured on the rising edge of the MCK output, and the HPB input is captured on the rising edge of the CKO output. Usually these pins are connected to horizontal transfer control pulses HP, VP and (VHP) output from the IC for generating synchronizing signals.
23	HPB	I	
25	H1A	O	Horizontal CCD driving pulse outputs. They are connected to the ϕH1A and ϕH2A pins of the CCD sensor. When inputs to HPA and HPB are both low, a clock obtained by dividing the CKI input by two is output on H1A and H2A. Whenever the HPA input or HPB input is high, H1A is high and H2A is low.
30	H2A	O	
32	H1B	O	Pulse output for driving last horizontal block in the CCD. H1B is connected to the ϕH1B pin of the CCD sensor. On H1B, a clock obtained by dividing the CKI input by two is output, independently of the HPA and HPB input.
36	RS	O	Reset gate driving pulse output. It is connected to the ϕRS pin of the CCD sensor through a capacitor of approximately 0.1μF.
35	BRS	I	Reference pulse output for generating the RS pulse. BRS is connected to the GRS input through capacitors and resistors, if necessary, to cause a delay.
34	GRS	O	Gate input for generating the RS pulse. The GRS input is buffered, then output on RS. No internal pull-up resistor is provided for this input.

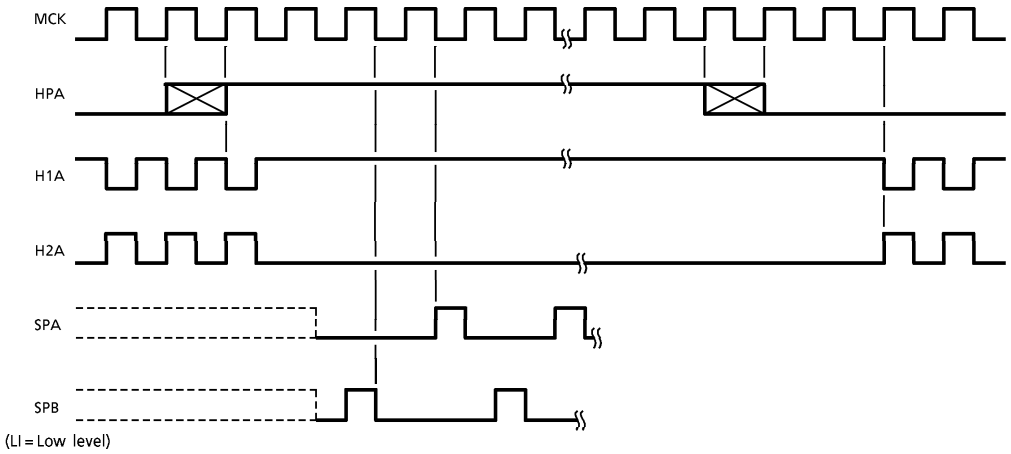
PIN No.	SYMBOL	I/O	FUNCTION
CDS AND COLOR SEPARATION PULSE			
43	FSH	O	Pulse output used to the feed through level of the CCD output. Usually FSH connected to the FCP pin of the TA8790F.
40	SSH	O	Pulse output used to sample an optical signal output from the CCD. Usually SSH is connected to the FCDS pin of the TA8790F.
42	BSSH	O	Reference pulse for generating the SSH pulse. It is connected to the GSSH input through capacitors and resistors, if necessary, to cause a delay.
41	GSSH	I	Gate input for generating the SSH pulse, It is buffered, then output on SSH. No internal pull-up resistor is provided for GSSH.
8	SPA	O	Sampling pulse output for color separation. When an input to MODE is high (open), the CCD output signal is sampled for each pixel on SPA and SPB alternately. An input to LI reverses the phase relationship between SPA and SPB. Usually this mode is used for a CCD sensor using the complementary color difference line sequence method. SPA and SPB are connected to SP1 and SP2 of the TA8790F. When an input to MODE is low, every third signal of the CCD output signal is sampled on SPA, SPB and SPC. In this case, the phase relationship between SPA, SPB and SPC remains unchanged independently of the LI input.
9	SPB	O	
10	SPC	O	
15	LI	I	When an input to MODE is high, the LI input, if connected to the LI output of the IC for generating synchronizing signals, changes the phase relationship between the color separation sampling pulses to match the color filters of the CCD sensor. For monochrome cameras, the LI pin must be left open.

PIN No.	SYMBOL	I/O	FUNCTION
OTHER PULSES			
1	FC1	O	A clock applied to CKI is divided by two, then output on FC1 and FC2 when input to FCEN is low. The FC1 and FC2 output are synchronized with the CCD transfer clock, so they can be used for peripheral application circuits. When these pins are not used, FCEN must be left open.
2	FC2	O	
44	FCEN	I	Enable input for the FC1 and FC2 outputs.
4	DLCK1	O	Clock outputs for delaying line. They output when DLEN is low. The output on DLCK1 is obtained by dividing a clock input to CKI by four, and the DLCK2 output is obtained by dividing the clock to CKI by eight. When they are not used.
5	DLCK2	O	
3	DLEN	I	Enable input for DLCK1 and DLCK2
12	CO0	O	Outputs on CO0 and CO1 control analog switches for eliminating flickering in the fluorescent lamps.
13	CO1	O	
14	VD	I	Clock input for the 1/3 divider to generate CO0 and CO1 outputs. To eliminate flickering, the VD signal from the IC for generating synchronizing signals is applied to the VD pin. When this pin is not used, it must be left open.

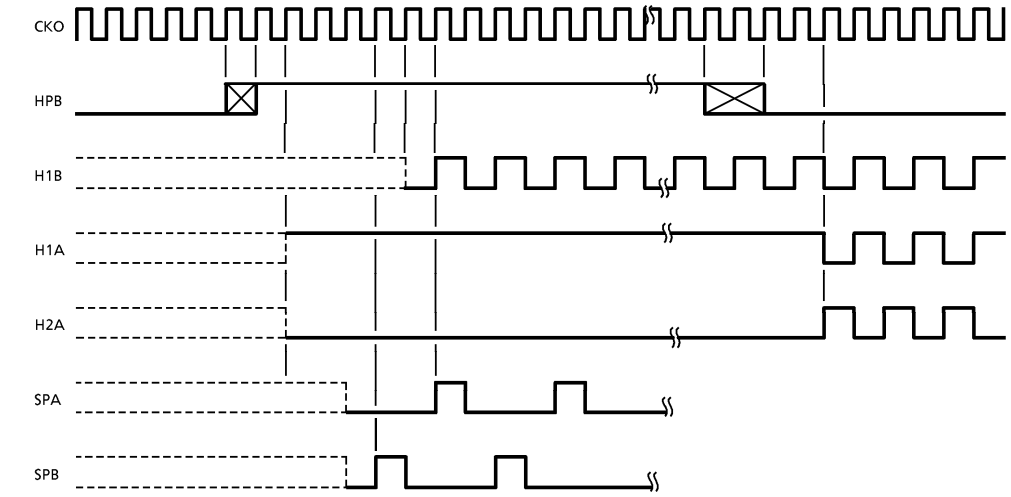
TIMING CHART (1)



TIMING CHART (2)

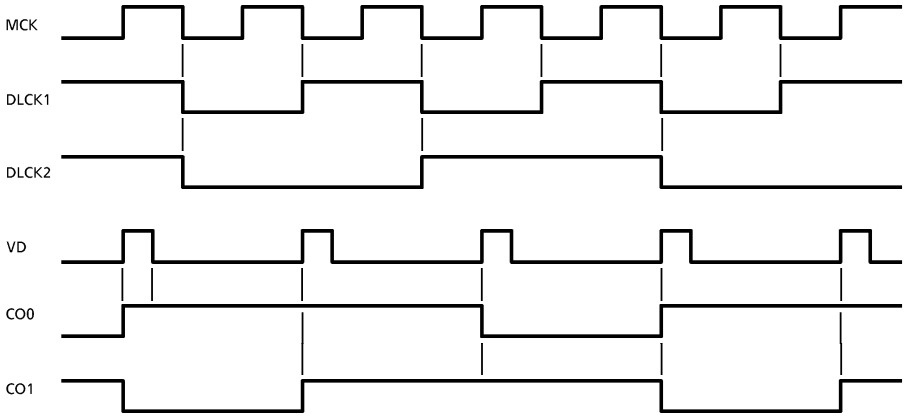


(LI = Low level)



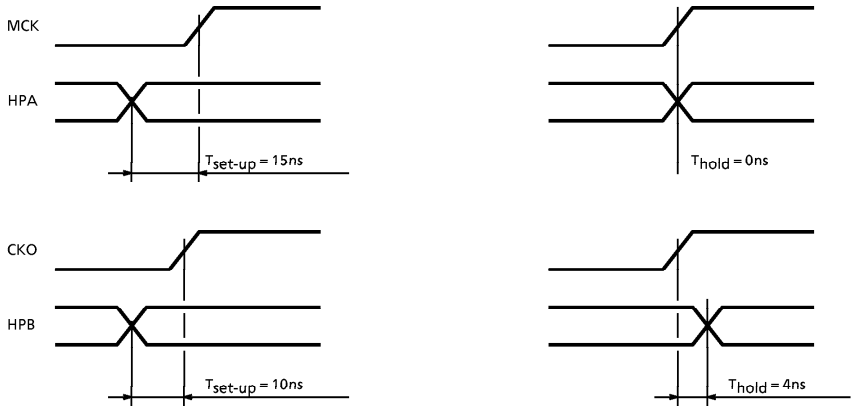
(LI = Low level)

TIMING CHART (3)



HPA AND HPB SET-UP AND HOLD TIMES

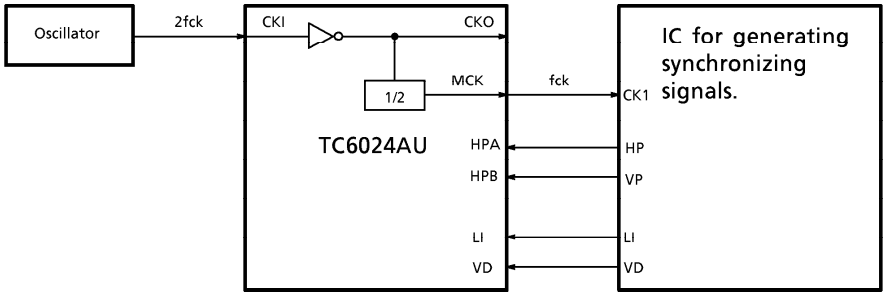
The minimum set-up time and hold time of HPA with respect to MCK, and those of HPB with respect to CKO are shown below.



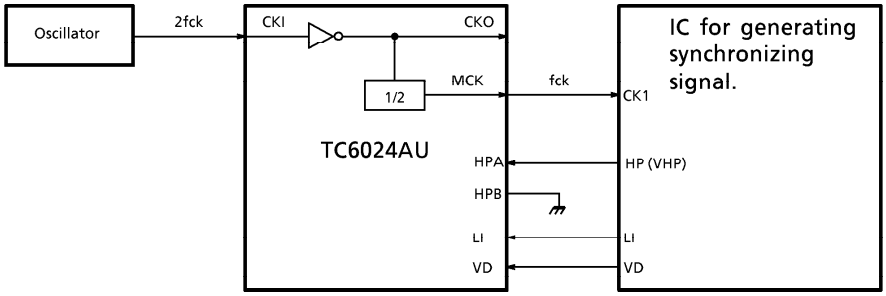
CONNECTING THE TC6024AU TO AN IC FOR GENERATION SYNCHRONIZING SIGNALS.

To drive the CCD, the TC6024AU must be connected to an IC for generating signals. There are three combinations and connection procedures, as shown below.
They depend on the CCD sensor used.

① The IC for generating synchronizing signals has HP and VP outputs.

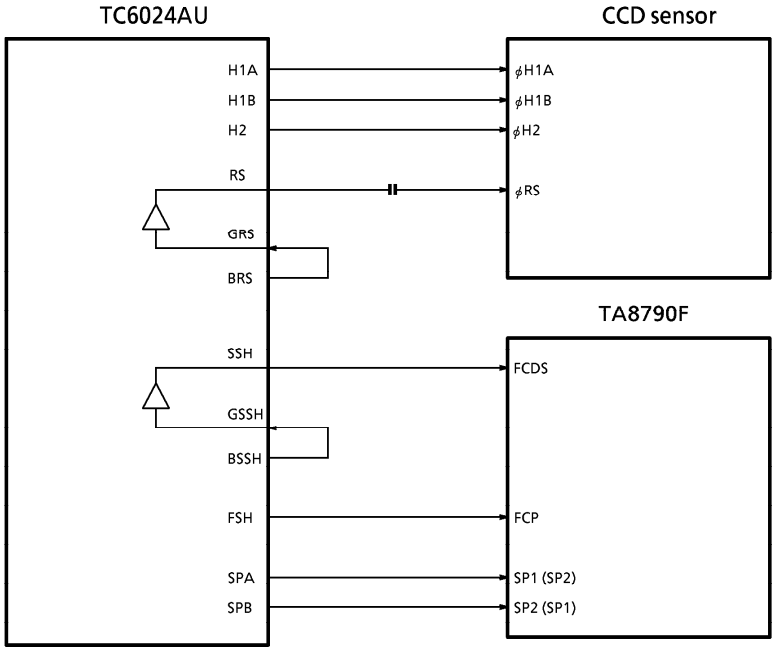


② The IC for generating synchronizing signals does not output the VD signal or it outputs the VHP signal which is a composite signal of HP and VP.



CONNECTING THE TC6024AU TO THE CCD SENSOR AND TA8790F

Horizontal CCD driving pulses H1A, 2HA, H1B, and H2 are connected to the CCD sensor directly. Reset gate pin RS is connected to the CCD sensor through a capacitor. CDS sampling pulses FSH, SSH and color separation pulses SPA and SPB are connected to FCP, FCDS, SP1 and SP2 of the TA8790F.

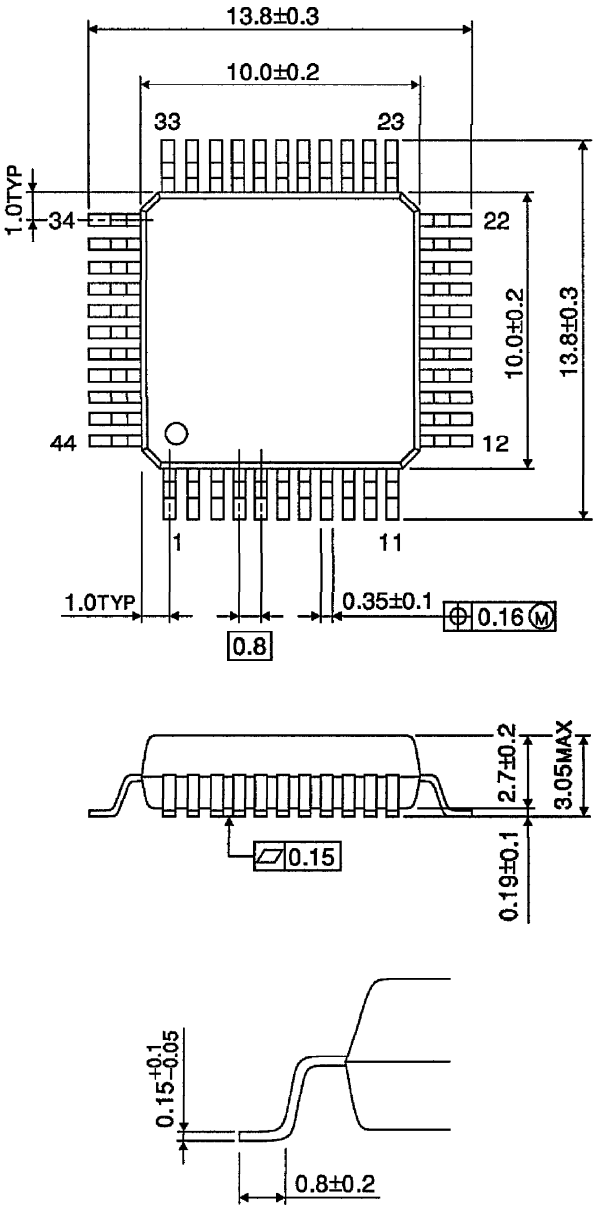


The RS signal is obtained by connecting BRS and GRS, and the SSH signal is obtained by connecting BSSH and GSSH.

OUTLINE DRAWING

QFP44-P-1010A

Unit : mm



Weight : 0.55g (Typ.)

TC6024AU – 11*
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TOSHIBA CORPORATION