TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

T6C84

COLUMN AND ROW DRIVER LSI FOR A DOT MATRIX GRAPHIC LCD

The TOSHIBA T6C84 is a driver for a small−or medium−scale dot matrix graphic LCD. It includes the functions of the TOSHIBA T9841B (column driver) and the TOSHIBA T9842B (row driver). It has an 8−bit interface circuit and a serial interface circuit. It generates all the timing signals for the display using an on−chip oscillator. It receives 8−bit data from an MPU, latches the data to an on−chip RAM, and displays the image on the LCD (the data in the display RAM correspond to the dots on the display).
The device has 136 column driver outputs and 34 row driver outputs enabling it to drive a 136−dot by 34−dot LCD. In addition, there are resistors to divide the bias voltage, a power supply op−amp, DC−DC converter (doubler, tripler, quadruplexer) and contrast control circuit enabling the LCD to be driven by a single power supply.

Unit: mm

T6C84	LEAD PITCH	
	IN	OUT
(UCW, 5NS)	0.8	0.26

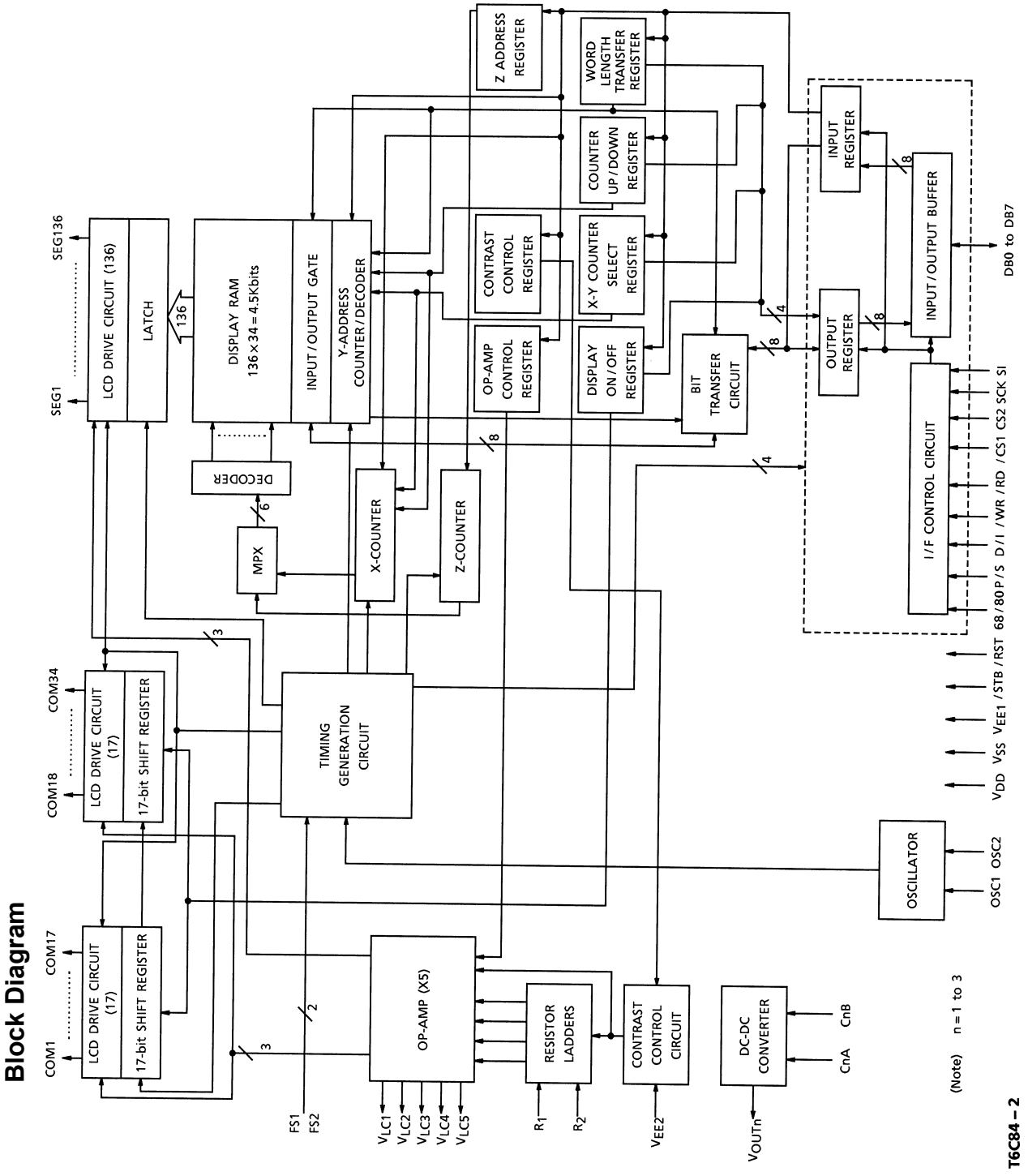
Please contact Toshiba or an authorized dealer for information on package dimensions.

TCP (Tape Carrier Package)

Features

- On−chip display RAM capacity: 136 × 34 = 4624 bits
- Display RAM data
  (1) Display data = 1 .....LCD turns on.
  (2) Display data = 0 .....LCD turns off.
- 1 / 34 duty cycle
- Word length of display data can be switched between 8−bit / word and 6−bit / word according to the character font.
- LCD driver outputs: 136 column driver outputs and 34 row driver outputs
- Interface with 80−Series MPU, 68−Series MPU and 4−bit MPU
- On−chip oscillator with one external resistor
- Low power consumption
- On−chip resistors to divide bias voltage, on−chip operational amplifier for LCD supply, on−chip DC−DC converter, on−chip contrast control circuit
- CMOS process
- Operating voltage: 2.7 V to 5.5 V
- Operating voltage for LCD drive signal:
  The following condition must be maintained: $V_{DD} - V_{EE1} \leq 16.0$ V, $V_{DD} - V_{EE2} \leq 16.0$ V, $V_{EE1} \leq V_{EE2}$
- Package: TCP (Tape Carrier Package)

Block Diagram



000707EBE2

- Polyimide base film is hard and thin. Be careful not to injure yourself on the film or to scratch any other parts with the film. Try to design and manufacture products so that there is no chance of users touching the film after assembly, or if they do , that there is no chance of them injuring themselves. When cutting out the film, try to ensure that the film shavings do not cause accidents. After use, treat the leftover film and reel spacers as industrial waste.
- Light striking a semiconductor device generates electromotive force due to photoelectric effects. In some cases this can cause the device to malfunction.
  This is especially true for devices in which the surface (back), or side of the chip is exposed. When designing circuits, make sure that devices are protected against incident light from external sources. Exposure to light both during regular operation and during inspection must be taken into account.
- The products described in this document are subject to the foreign exchange and foreign trade laws.
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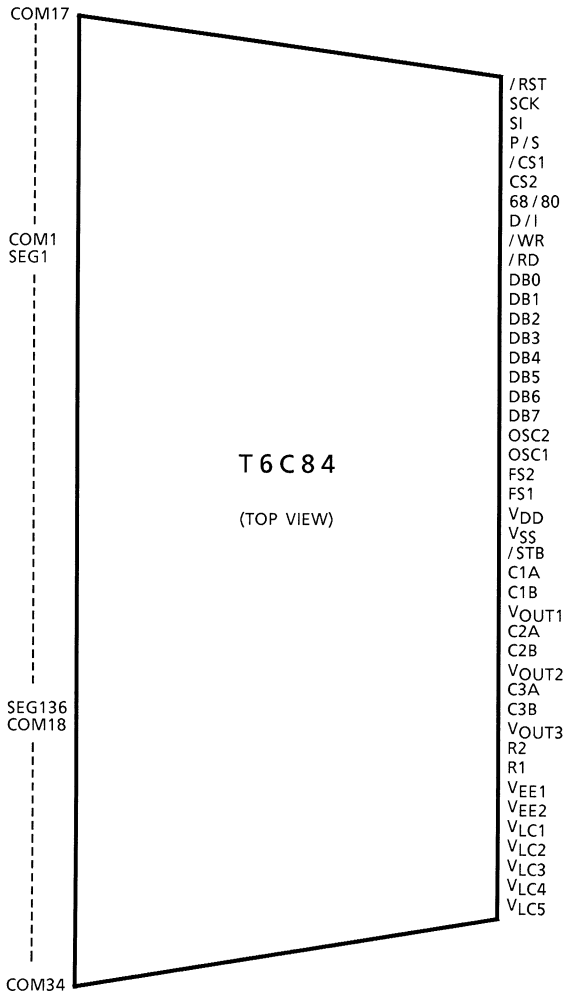
Pin Assignment



Note: The above diagram shows the pin configuration of the LSI Chip; it does not show the configuration of the tape carrier package.

Pin Functions

Pin Name	I / O	Functions
SEG1 to SEG136	Output	Column driver output
COM1 to COM34	Output	Row driver output
DB0 to DB7	I / O	Data bus
P / S	Input	Input for parallel interface / serial interface select signal ● P / S = H → Parallel interface is selected. SI and SCK must be connected to V_{DD} or V_{SS}. ● P / S = L → Serial interface is selected. DB0 to DB7 must be open. / WR and / RD must be connected to V_{DD} or V_{SS}.

<table>
<tr><th>Pin Name</th><th>I / O</th><th>Functions</th></tr>
<tr><td>68 / 80</td><td>Input</td><td>Input for 68−Series MPU / 80−Series MPU select signal
● 68 / 80 = H→ 68−Series MPU is selected.
● 68 / 80 = L → 80−Series MPU is selected.</td></tr>
<tr><td>/ CS1, CS2</td><td>Input</td><td>Input for chip select signal
● / CS1 = L and CS2 = H → Selection state</td></tr>
<tr><td>D / I</td><td>Input</td><td>Input for data / instruction select signal
● D / I = H → indicates that the data on DB0 to DB7 or SI is display data.
● D / I = L → Indicates that the data on DB0 to DB7 or SI is instruction data.</td></tr>
<tr><td>/ WR (R / W)</td><td>Input</td><td>Input for write enable signal (input for read / write select signal)
● When 80−Series MPU is selected, data on DB0 to DB7 is latched on the rising edge of / WR.
● When 68−Series MPU is selected, this pin is used to indicate whether read operation or write operation is performed.</td></tr>
<tr><td>/ RD (E)</td><td>Input</td><td>Input for read enable signal (input for enable signal)
● When 80−Series MPU is selected, data appears on DB0 to DB7 while / RD = L.
● When 68−Series MPU is selected, this pin is used for input enable signal.</td></tr>
<tr><td>SI</td><td>Input</td><td>Input for serial data</td></tr>
<tr><td>SCK</td><td>Input</td><td>Input for serial clock</td></tr>
<tr><td>/ RST</td><td>Input</td><td>Input for reset signal
● / RST = L → Reset state</td></tr>
<tr><td>/ STB</td><td>Input</td><td>Input for standby signal
● Usually connected to V_{DD}
● / STB = L → T6C84 is in standby state and cannot accept any commands or data. Column driver signal and row driver signal are at the V_{DD} level.</td></tr>
<tr><td>OSC1, OSC2</td><td>—</td><td>When using the internal clock oscillator, connect a resistor between OSC1 and OSC2.
When using an external clock, connect the clock to OSC1 and leave OSC2 open.</td></tr>
<tr><td>FS1, FS2</td><td>Input</td><td>Inputs for frequency selection
<table>
<tr><th>FS1</th><th>FS2</th><th>f_{OSC} (kHz)</th><th>f_{COM} (Hz)</th></tr>
<tr><td>0</td><td>0</td><td>28.56</td><td>35</td></tr>
<tr><td>0</td><td>1</td><td>57.12</td><td>35</td></tr>
<tr><td>1</td><td>0</td><td>228.48</td><td>35</td></tr>
<tr><td>1</td><td>1</td><td>456.96</td><td>35</td></tr>
</table></td></tr>
</table>

PS	68 / 80	Interface Type	/ CS1	CS2	D / I	/ WR	/ RD	SI	SCK	DB0 to DB7
H	L	80−Series MPU	/ CS1	CS2	D / I	/ WR	/ RD	L / H	L / H	DB0 to DB7
	H	68−Series MPU	/ CS1	CS2	D / I	R / W	E	L / H	L / H	DB0 to DB7
L	L / H	Serial interface	/ CS1	CS2	D / I	L / H	L / H	SI	SCK	Open

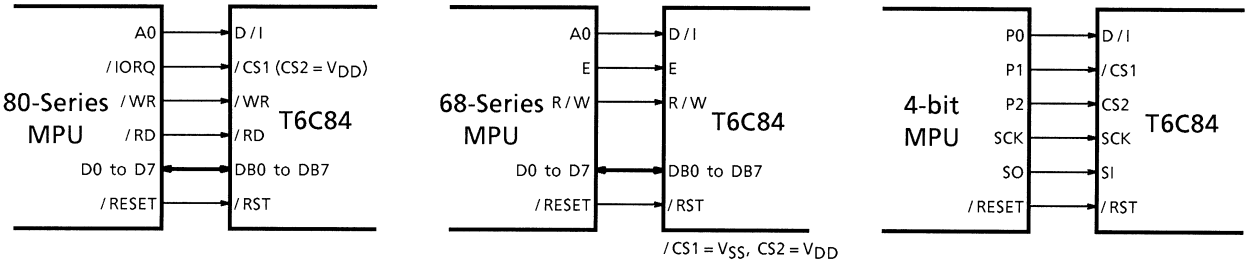
Note: “H” denotes the V_{DD} level; “L” denotes the V_{SS} level.

Pin Name	I / O	Functions
R1, R2	Input	Connect with external resistor.
C1A, C1B	—	Connect using a capacitor for doubler.
V_{OUT1}	—	DC−DC converter output (×2 Level)
C2A, C2B	—	Connect using a capacitor for tripler.
V_{OUT2}	—	DC−DC converter output (×3 Level)
C3A, C3B	—	Connect using a capacitor for quadruplexer.
V_{OUT3}	—	DC−DC converter output (×4 Level)
V_{EE1}, V_{EE2}	—	Power supply for LCD driver circuit • When using on−chip DC−DC converter, connect V_{EE1} and V_{EE2} to V_{OUT}.
V_{LC1} to V_{LC5}	—	Power supply for LCD driver circuit
V_{DD}, V_{SS}	—	Power supply for logic circuit. Reference: Ground

Function of Each Block

• Interface logic

The T6C84 can be operated with an 80−Series MPU, a 68−Series MPU or a 4−bit MPU.
Fig. 1 shows an example of the interface.



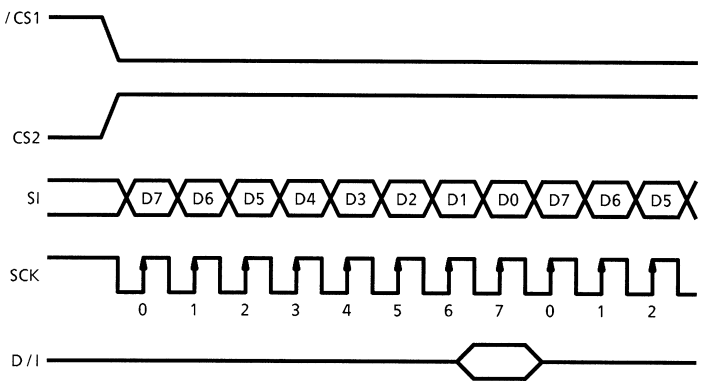


Fig. 1

- **Input register**

  This register stores 8−bit data from the MPU. The D / I signal distinguishes between command data and display data.

- **Output register**

  This register stores 8−bit data from the display RAM. When display data is read, the display data specified by the address in the address counter is stored in this register. After that, the address is automatically incremented or decremented. Therefore, when an address is set, the correct data does not appear as the first data item that is read. The data in the specified address location appears as the second data item that is read.

- **X−address counter**

  The X−address counter is a 34−up / down counter. It holds the row address of a location in the display RAM. Writing data to or reading data from the display RAM causes the X−address to be automatically incremented or decremented.

- **Y− (page) address counter**

  The Y− (page) address counter is a 17−up / down counter, when the word length is eight bits, or a 23−up / down counter, when the word length is six bits. It holds the column address of a location in the display RAM. Writing data to or reading data from the display RAM causes the Y−address to be automatically incremented or decremented.

- **Z−address counter**

  The Z−address counter is a 34−up counter that provides the display RAM data for the LCD drive circuit. The data stored in the Z−address register is sent to the Z−address counter as the Z start address.
  For instance, when the Z start address is 16, the counter increments like this: 16, 17, 18···, 32, 33, 0, 1, 2···14, 15, 16. Therefore, the display start line is line 16 of the display RAM.

- **Up / down register**

  The 1−bit datum stored in this register selects either up or down mode for the X−and Y− (page) address counters.

- **Counter select register**

  The 1−bit datum stored in this register selects the X−address counter or Y− (page) address counter.

- **Display ON / OFF register**

  This 1−bit register holds the display ON / OFF state. In the OFF state, the output data from the display RAM is cleared. In the ON state, the display RAM data is displayed. The display ON / OFF state does not affect the data in the display RAM.

- **Z−address register**

  This 6−bit Hregister holds the data which specifies the display start line.

- **Word length register**

The 1−bit datum stored in this register selects the word length: eight bits per word or six bits per word.

- **Word length change circuit**

This circuit is controlled by the word length register. When the word length is eight bits, data is transferred eight bits at a time. When the word length is six bits, the data transfer method is as shown in Fig. 2 below.

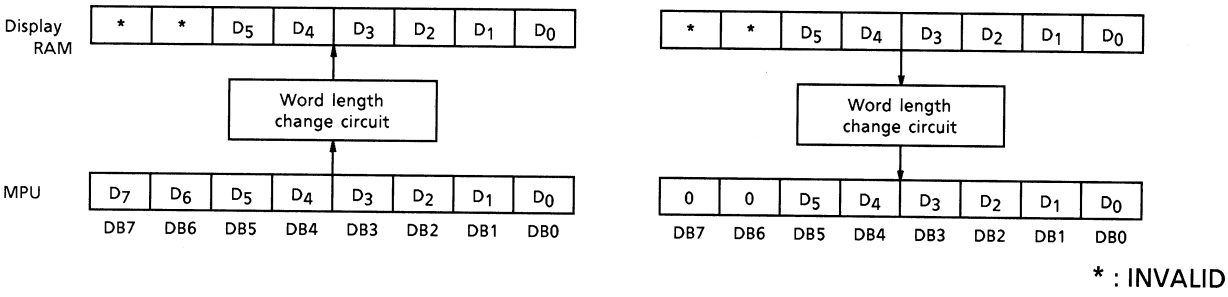


Fig. 2

- **Oscillator**

The T6C84 includes an on−chip oscillator. When using this oscillator, connect an external resistor between OSC1 and OSC2 as shown in Fig. 3. When using an external clock, connect the clock input to OSC1 and leave OSC2 open.

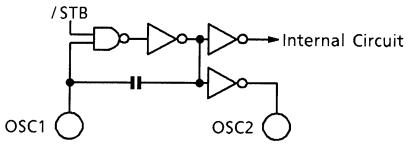


Fig. 3

- **Timing generation circuit**

This circuit divides the signals from the oscillator and generates the display timing signals and the operating clock signal.

- **Shift register**

The T6C84 has two 17−bit shift register. These two 17−bit shift registers can be combined to form a 34−bit shift register.

- **Latch circuit**

The latch circuit latches data from the display RAM.

- **Column driver circuit**

The column driver circuit consists of 136 driver circuits. One of the four LCD driving levels is selected by the combination of the internal M signal and the display data transferred from the latch circuit. Details of the column driver circuit are shown in Fig. 4.

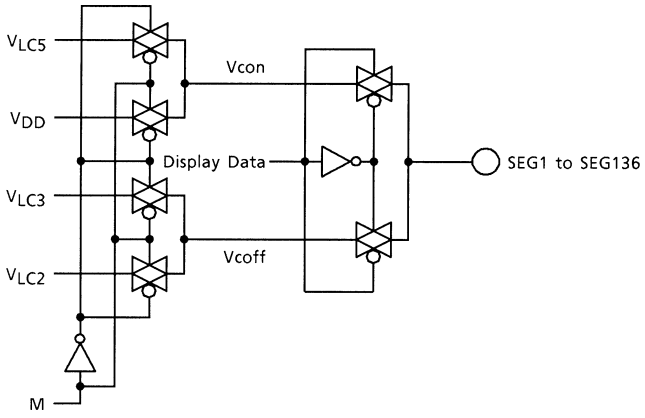


Fig. 4

- **Row driver circuit**

The row driver circuit consists of 34 driver circuits. One of the four LCD driving levels is selected by the combination of the internal M signal and the data from the shift register. Details of the row driver circuit are shown in Fig. 5.

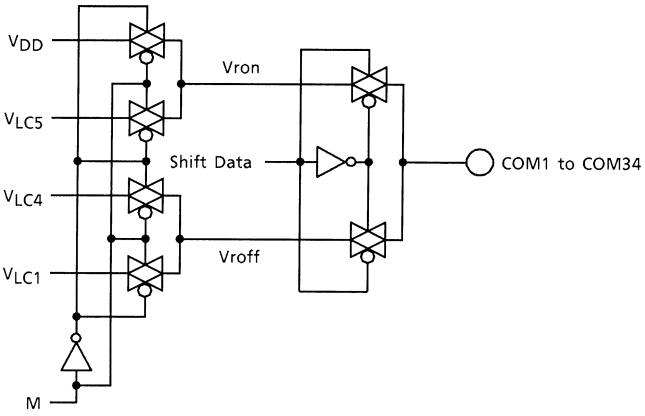


Fig. 5

- **DC−DC converter**

The T6C84 has an on−chip DC−DC converter. The DC−DC converter generates a ×2, ×3 or ×4 output level. See Fig. 6.
When / STB = L, V_{OUT1}, V_{OUT2} and V_{OUT3} = 0 (V).
The recommended value for the capacitor is 2.2 μF.

(1) Doubler (×2) mode

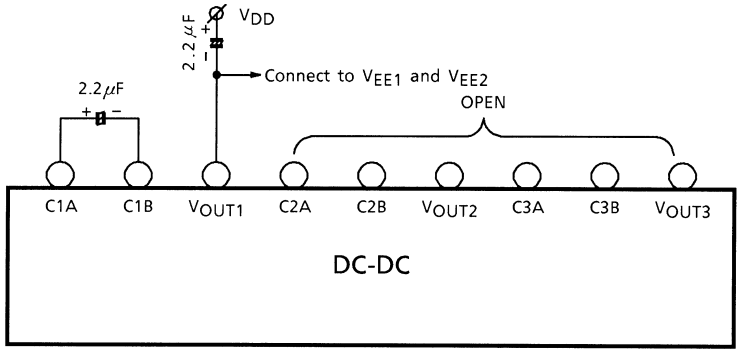


Fig. 6−1

(2) Tripler (×3) mode

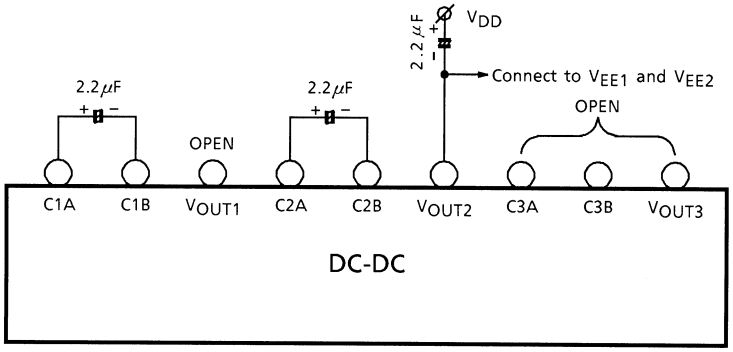


Fig. 6−2

(3) Quadruplexer (×4) mode

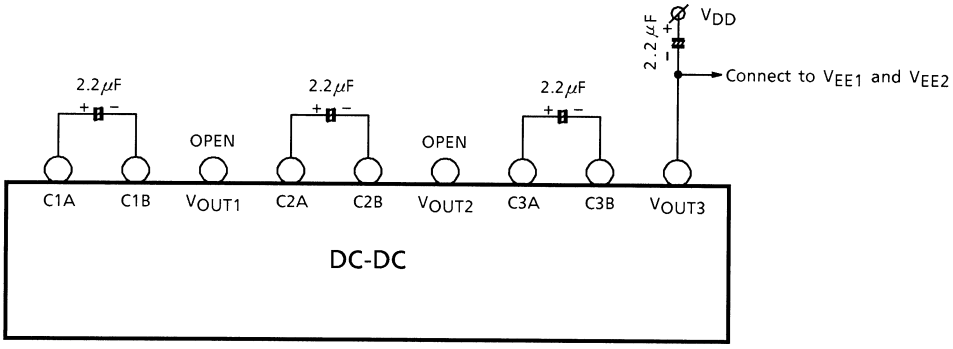


Fig. 6−3

When using an external power supply, input the voltage to V_{EE1} and V_{EE2} and do not connect the capacitors.

- **Voltage divider resistors, contrast control circuit**

The T6C84 has on−chip resistors which include op−amps, that divide the bias voltage, and a contrast control circuit. The voltage bias is modified by the value of the external resistor between R_1 and R_2. These resistors and the contrast control circuit are shown in Fig. 7 below.

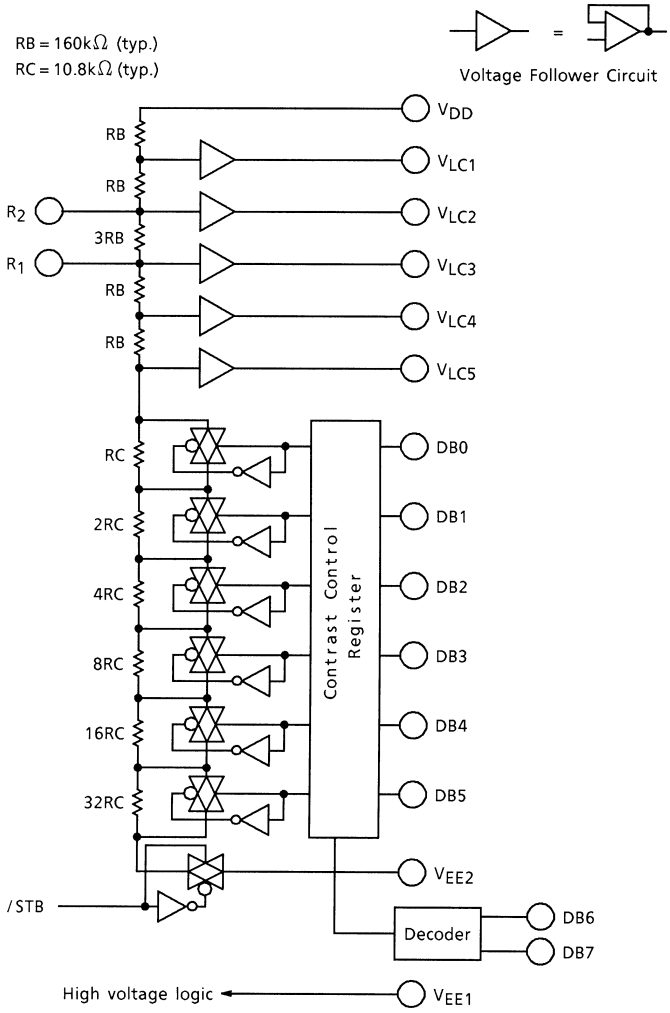


Fig. 7

● Op−amp, op−amp control register

The T6C84 has five operational amplifiers which determine the LCD driving levels. The power supplied by these op−amps is modified by the contents of the op−amp control register to match the LCD panel.
The op−amp can also be controlled in such a way that it supplies full current on the rising edge of SEG and a reduced current otherwise.
To maintain good LCD contrast, connect a capacitor between the op−amp output and V_{DD}.
The value of the capacitor should normally be in the range 0.1 to 1.0 µF.

● Display RAM

The display RAM consists of 34 rows × 136 columns for a total of 4624 cells. It is directly bit−mapped to the LCD. The relation between the display RAM and LCD is shown in Fig. 8.
When the word length is set to eight bits, the display RAM is arranged in 17 pages and each page contains 34 words. When the word length is set to six bits, the display RAM is arranged in 23 pages and each page contains 34 words. See Fig. 9.

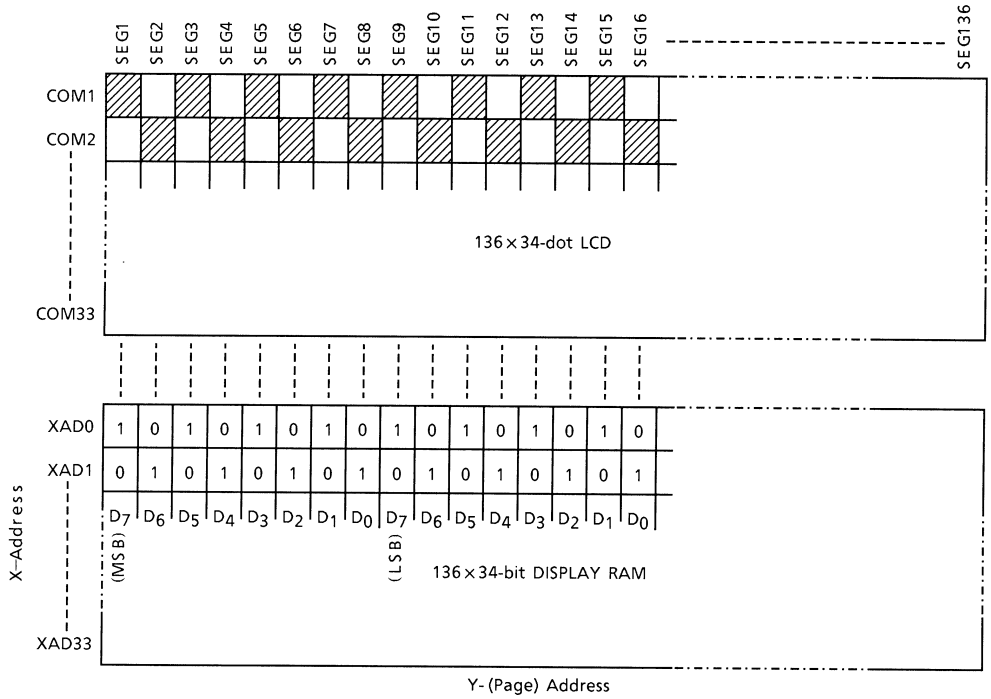
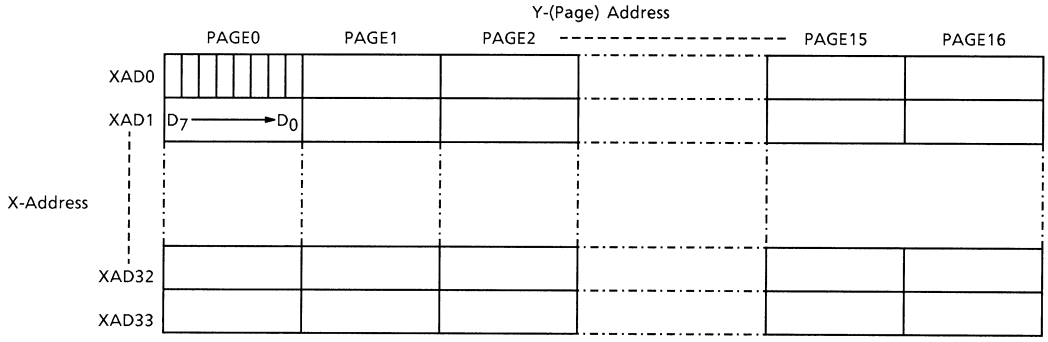


Fig. 8

(1) 8−bits−per−word mode



(2) 6−bits−per−word mode

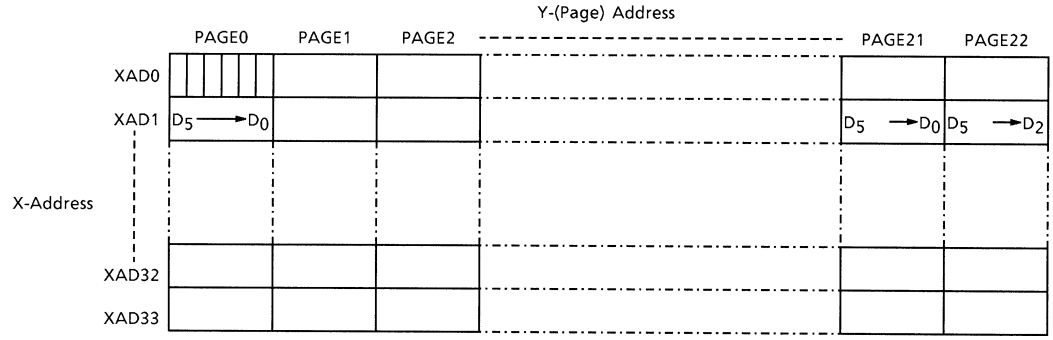


Fig. 9

Command Definitions

Command Name	D / I	/ WR	/ RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function
DPE	0	0	1	0	0	0	0	0	0	1	1 / 0	Display ON (1) / OFF (0)
86E	0	0	1	0	0	0	0	0	0	0	1 / 0	Word Length: 8 bits (1) / 6 bits (0)
UDE	0	0	1	0	0	0	0	0	1	1 / 0	1 / 0	Counter Select: DB1 Y (1) / X (0) Mode Select: DB0 UP (1) / DOWN (0)
CHE	0	0	1	0	0	0	1	1	*	*	*	Test Mode Select
OPA1	0	0	1	0	0	0	1	0	*	1 / 0	1 / 0	Op−Amp Power Control 1
OPA2	0	0	1	0	0	0	0	1	*	1 / 0	1 / 0	Op−Amp Power Control 2
SYE	0	0	1	0	0	1	Y−Address (0 to 22)					Y− (Page) Address Set
SZE	0	0	1	0	1	Z−Address (0 to 33)						Z−Address Set
SXE	0	0	1	1	0	X−Address (0 to 33)						X−Address Set
SCE	0	0	1	1	1	CONTRAST CONTROL (0 to 63)						Contrast Set
STRD	0	1	0	B	8 / 6	D	R	0	0	Y / X	U / D	Status Read
DAWR	1	0	1	Write Data								Display Data Write
DARD	1	1	0	Read Data								Display Data Read

*: INVALID

- **Display ON / OFF select (DPE)**

D / I	/ WR	/ RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	1	0	0	0	0	0	0	1	1	Display ON (03H)
0	0	1	0	0	0	0	0	0	1	0	Display OFF (02H)

This command turns display ON / OFF. It does not affect the data in the display RAM.
When the "Display OFF" command is input, V_{LC1} to V_{LC5} are all set to V_{DD}.

Note: An L input on / RST turns display OFF.

- **Word length 8 bits / 6 bits select (86E)**

D / I	/ WR	/ RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	1	0	0	0	0	0	0	0	1	8−bit word mode (01H)
0	0	1	0	0	0	0	0	0	0	0	6−bit word mode (00H)

This command sets the word length for display RAM data to either six bits or eight bits

Note: An L input on / RST sets the word length to eight bits per word.

- **X / Y (page) counter, up / down mode select (UDE)**

D / I	/ WR	/ RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	1	0	0	0	0	0	1	0	0	X−Counter / Down Mode (04H)
0	0	1	0	0	0	0	0	1	0	1	X−Counter / Up Mode (05H)
0	0	1	0	0	0	0	0	1	1	0	Y−Counter / Down Mode (06H)
0	0	1	0	0	0	0	0	1	1	1	Y−Counter / Up Mode (07H)

This command selects the counter and the up / down mode. For instance, when X−counter / up mode is selected, the X−address is incremented in response to every data read and write. However, when X−Counter / up mode is selected, the address in the Y− (page) counter will not change. Hence the Y−address must be set (with the SYE command) before it can be changed.

Note: An L input on / RST sets the Y−counter to up mode.

- **Test mode select (CHE)**

D / I	/ WR	/ RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	1	0	0	0	1	1	*	*	*	*: INVALID

This command selects the test mode. Do not use this command.

- **Set Y− (page) address (SYE)**

D / I	/ WR	/ RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	A	A	A	A	A

Range: 8−bit / Word: 20H to 30H (Page 0 to Page 16)
6−bit / Word: 20H to 36H (Page 0 to Page 22)

When operating in 8−bits−per−word mode, this command selects one of the 17 pages in the display RAM. Do not try to select a page outside this range. When operating in 6−bits−per−word mode, this command selects one of the 23 pages in the display RAM.

Note: An L input on / RST sets the Y−address to page 0.

- **Set Z−address (SZE)**

D / I	/ WR	/ RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	A	A	A	A	A	A

Range: 40H to 61H (ZAD0 to ZAD33)

This command sets the top row of the LCD screen, irrespective of the current X−address.
For instance, when the Z−address is 16, the top row of the LCD screen is address 16 of the display RAM, and the bottom row of the LCD screen is address 15 of the display RAM.

Note: An L input on / RST sets the Z−address to 0.

- **Set X−address (SXE)**

D / I	/ WR	/ RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	A	A	A	A	A	A

Range: 80H to A1H (XAD0 to XAD33)

This command sets the X−address (in the range 0 to 33). An L input on / RST sets the X−address to 0.

- **Set Contrast (SCE)**

D / I	/ WR	/ RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	A	A	A	A	A	A

Range: C0H to FFH

This command sets the contrast for the LCD. The LCD contrast can be set in 64 steps. The command C0H selects the brightest level; the command FFH selects the darkest.

- **Op−amp control 1 (OPA1)**

D / I	/ WR	/ RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	1	0	0	0	1	0	*	A	A	*: INVALID

Range: 10H to 13H (when DB2 = 0)

This command sets the power supply strength for the operational amplifier. This command selects one of four levels. The command 10H selects the lowest power supply strength and the command 13H selects the maximum power supply strength.

Note: An L input to / RST sets the op−amp power supply strength to the lowest level.

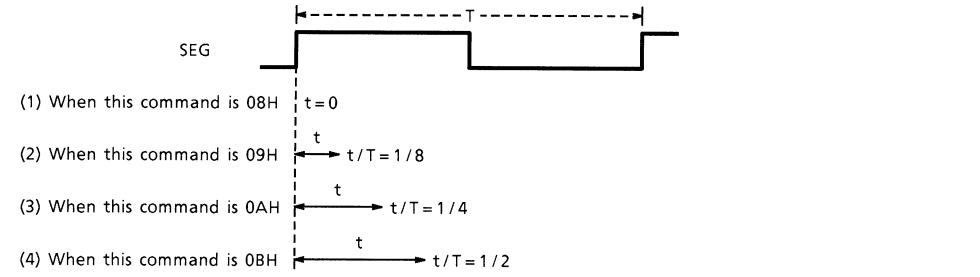
- **Op−amp control 2 (OPA2)**

D / I	/ WR	/ RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	1	0	0	0	0	1	*	A	A	*: INVALID

Range: 08H to 0BH (when DB2 = 0)

This command enhances the power supply strength of the operational amplifier over a short period from the rising edge of SEG. This command selects one of four levels of strength.

Note: An L input to / RST sets t to 0 for the op−amp.
It is not possible to select the combination OPA1 = 10H and OPA2 = 08H. After a Reset, set OPA1 and OPA2 according to the application.



The amplifier's strength is enhanced over the period denoted by ↔, starting on the rising edge of SEG.

Fig. 10

- **Status read (STRD)**

D / I	/ WR	/ RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	B	8 / 6	D	R	0	0	Y / X	U / D

B (Busy) : When B = 1 the T6C84 is executing an internal operation and no instruction can be accepted except STRD.
When B = 0 the T6C84 can accept an instruction.

8 / 6 (Word Length): When 8 / 6 = 1 the word length of the display data is eight bits per word.
When 8 / 6 = 0 the word length of the display data is six bits per word.

D (Display) : When D = 1 display is ON.
When D = 0 display is OFF.

R (Reset) : When R = 1 the T6C84 is in reset state.
When R = 0 the T6C84 is in operating state.

Y / X (Counter) : When Y / X = 1 the Y counter is selected.
When Y / X = 0 the X counter is selected.

U / D (Up / down) : When U / D = 1 the X and Y counters are in up mode.
When U / D = 0 the X and Y counters are in down mode.

- **Write / read display data (DAWR / DARD)**

D / I	/ WR	/ RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
1	0	1	D	D	D	D	D	D	D	D	DAWR: Display Data Write
1	1	0	D	D	D	D	D	D	D	D	DARR: Display Data Read

The command DAWR writes the display data to the display RAM. The command DARD outputs the display data from the display RAM. However, when a data read is executed, the correct data does not appear on the first data reading. Therefore, ensure that the T6C84 performs a dummy data read before reading the actual data.

Function Description

- **X−address counter and Y− (page) address counter**

Fig. 11 shows a sample operation involving the X−address counter.
After Reset is executed, the X−address (XAD) becomes 0, then X−counter / up mode is selected. Next, the X−address is set to 32 using the SXE command.
After data has been written or read, the X−address is automatically incremented by 1.
After X−counter / down mode has been selected and data has been written or read, the X−address is automatically decremented by 1.
When the X−counter is selected, the Y−counter is not incremented or decremented.

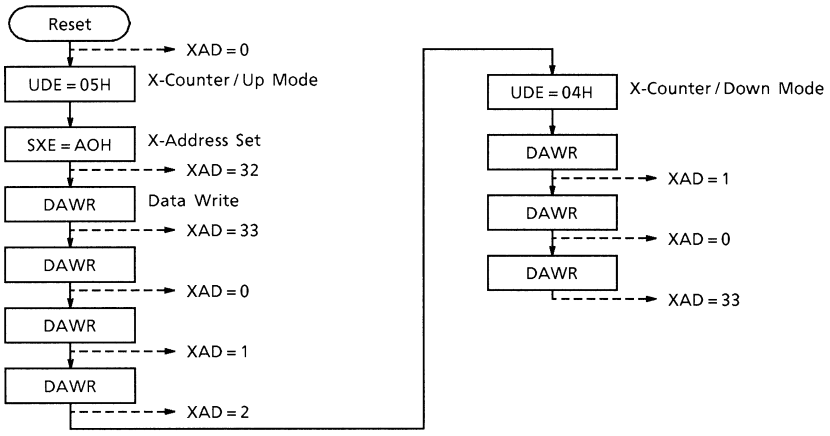


Fig. 11

Fig. 12 shows a sample operation involving for the Y−address counter in 8−bit word length mode.
After Reset is executed, the Y− (page) address (Page) becomes 0, then Y− (page) counter / up mode and 8−bit word length mode are selected. After data has been written or read, the Y− (page) address counter is automatically incremented by 1.
After Y− (page) counter / down mode has been selected and data has been written or read, the Y− (page) address is automatically decremented by 1.
When the Y− (page) counter is selected, the X−counter is not incremented or decremented.

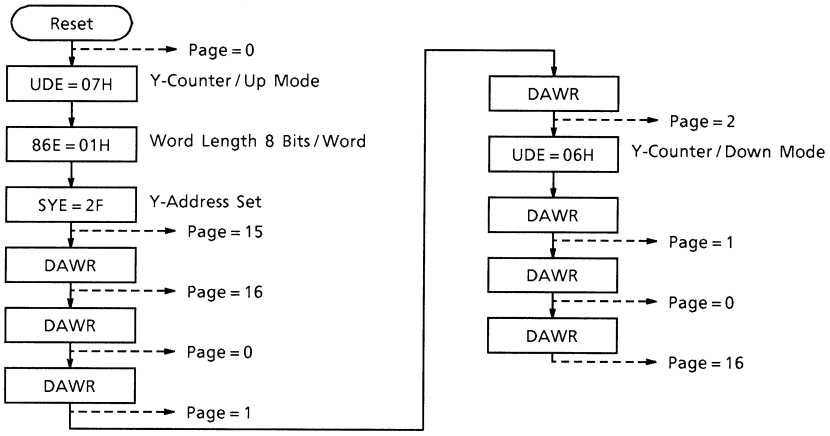


Fig. 12

When operating in 6−bits word length mode, the Y− (page) address counter can count up to 22.
If Page = 22 in up mode, after data has been written or read, the Y− (page) address (Page) becomes 0.
If Page = 0 in down mode, after data has been written or read, the Y− (page) address (Page) becomes 22.

- **Data read**

When reading data, there are some cases when dummy data must be read. This is because when the data read command is invoked, the data pointed to by the address counter is transferred to the output register; the contents of the output register are then transferred by the next data read command.
Therefore when reading data straight after power−on or straight after an address−setting command, such as SYE or SXE, a dummy data read must be performed. See Fig. 13.

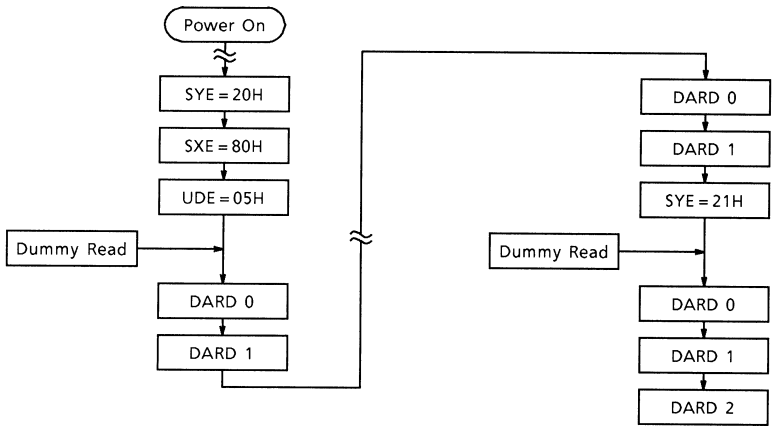


Fig. 13

● Reset function

When / RST = L, the reset function is executed and the following settings are made.

(1) Display ····· OFF
(2) Word length ····· 8 bits / word
(3) Counter mode ····· Y–counter / up mode
(4) Y– (page) address ····· Page = 0
(5) X–address ····· XAD = 0
(6) Z–address ····· ZAD = 0
(7) OPA1 ····· min
(8) OPA2 ····· min

● Standby function

When / STB = L, the T6C84 is in standby state. The internal oscillator is stopped, power consumption is reduced, and the power supply level for the LCD (V_{LC1} to V_{LC5}) becomes V_{DD}.

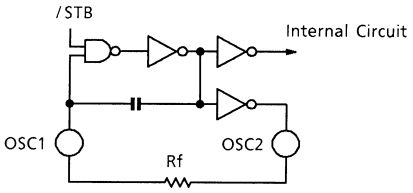
● Busy flag

When the T6C84 is executing an internal operation (other than the STRD command), the busy flag is set to logical H. The state of the busy flag is output in response to the STRD command. While the busy flag is H, no instruction can be accepted (except the STRD command). The busy state period (T) is as follows.

$2 / f_{OSC} \leq T \leq 4 / f_{OSC}$ [seconds] f_{OSC}: Frequency of OSC1

● Oscillation frequency

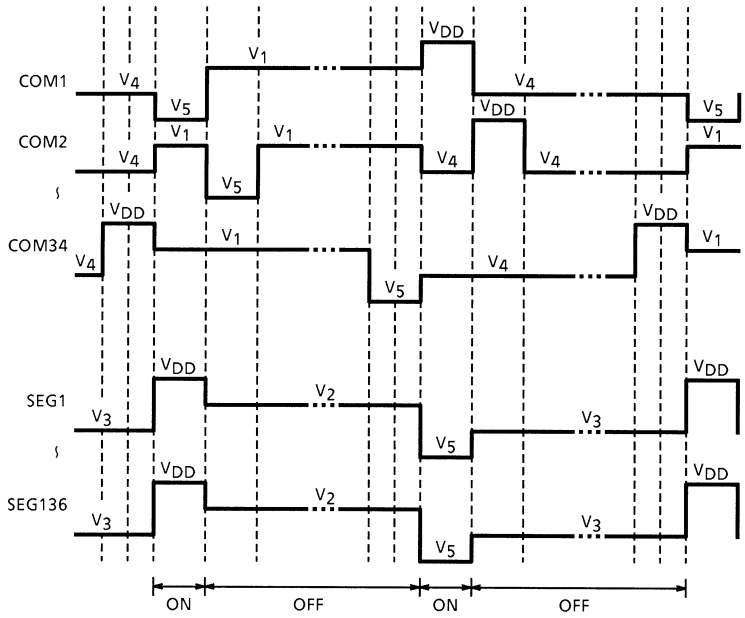
The frequency select pins (FS1 and FS2) are used to set the relation between the oscillation frequency (f_{OSC}) and the frequency of the internal M signal (f_M), as shown in the table below.



Rf (kΩ)	f_{OSC} (kHz)	f_M (Hz)	FS1	FS2
1100	28.56	35	0	0
530	57.12	35	1	0
140	228.48	35	0	1
70	456.96	35	1	1

Note: The resistance values are typical values.
The oscillation frequency depends on how the device is mounted. It is necessary to adjust the oscillation frequency to a target value.

LCD Driver Waveform



LCD driver timing chart (1/34 duty)

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage (1)	V_{DD} (Note 1)	−0.3 to 7.0	V
Supply Voltage (2)	$V_{LC1, 2, 3, 4, 5}$ V_{EE1}, V_{EE2} (Note 3)	V_{DD} − 18.0 to V_{DD} + 0.3	V
Input Voltage	V_{IN} (Note 1, 2)	−0.3 to V_{DD} + 0.3	V
Operating Temperature	T_{opr}	−20 to 75	°C
Storage Temperature	T_{stg}	−55 to 125	°C

Note1: Referenced to V_{SS} = 0 V

Note2: Applies to all data bus pins and input pins except V_{EE1}, V_{EE2}, V_{LC1}, V_{LC2}, V_{LC3}, V_{LC4} and V_{LC5}.

Note3: Ensure that the following condition is always maintained.

$V_{DD} \geq V_{LC1} \geq V_{LC2} \geq V_{LC3} \geq V_{LC4} \geq V_{LC5} \geq V_{EE2} \geq V_{EE1}$

Electrical Characteristics
DC Characteristics
Test Conditions (1)
(Unless otherwise noted, V_{SS} = 0 V, V_{DD} = 3.0 V ± 10%, V_{LC5} = 0 V, Ta = −20 to 75°C)

Item		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Pin Name
Operating Supply (1)		V_{DD}	—	—	2.7	—	3.3	V	V_{DD}
Operating Supply (2)		V_{LC5} $V_{EE1, 2}$	—	—	V_{DD} − 16.0	—	V_{DD} − 4.0	V	V_{LC5}, V_{EE1}, V_{EE2}
Input Voltage	H Level	V_{IH}	—	—	0.8 V_{DD}	—	V_{DD}	V	DB0 to DB7, D / I, / WR, / RD, / CS1, CS2, / RST, / STB, FS1, FS2, SI, SCK, P / S, 68 / 80
	L Level	V_{IL}	—	—	0	—	0.2V_{DD}	V	
Output Voltage	H Level	V_{OH}	—	I_{OH} =−400 µA	V_{DD} − 0.2	—	V_{DD}	V	DB0 to DB7
	L Level	V_{OL}	—	I_{OL} = 400 µA	0	—	0.2	V	
Column Driver Output Resistance		Rcol	—	V_{DD} − V_{LC5} = 11.0 V Load current = ± 100 µA	—	—	7.5	kΩ	SEG1 to SEG136
Row Driver Output Resistance		Rrow	—	V_{DD} − V_{LC5} = 11.0 V Load current = ± 100 µA	—	—	1.5	kΩ	COM1 to COM34
Input Leakage		I_{IL}	—	V_{IN} = V_{DD} to GND	−1	—	1	µA	DB0 to DB7, D / I, / WR, / RD, / CS1, CS2, / RST, / STB, FS1, FS2, SI, SCK, P / S, 68 / 80
Operating Freq.		f_{OSC}	—	—	20	—	500	kHz	OSC1
External Clock Freq.		f_{ex}	—	—	20	—	500	kHz	OSC1
External Clock Duty		f_{duty}	—	—	45	50	55	%	OSC1
External Clock Rise / Fall Time		t_r / t_f	—	—	—	—	50	ns	OSC1
Current Consumption (1)		I_{DD1}	—	(Note 1)	—	300	420	µA	V_{DD}
Current Consumption (2)		I_{DD2}	—	(Note 2)	—	400	530	µA	V_{DD}
Current Consumption (3)		I_{DDSTB}	—	(Note 3)	−1	—	1	µA	V_{DD}
Output Voltage (Tripler Mode)		VO2	2	(Note 4)	−4.50	−4.90	—	V	V_{OUT2}
Output Voltage (Quadruplexer Mode)		VO3	3	(Note 5)	−6.75	−7.50	—	V	V_{OUT3}

Note 1: V_{DD} = 3.0 ± 10%, $V_{EE1, 2}$ = V_{OUT2} (tripler mode), no data access
R_f = 62 kΩ, no load, 1 / 7 bias, FS1, 2 = H, OPA1 = 10H, OPA2 = 09H

Note 2: V_{DD} = 3.0 ± 10%, $V_{EE1, 2}$ = V_{OUT2} (tripler mode), data access cycle f / $_{CE}$ = 1 MHz,
R_f = 62 kΩ, no load, 1 / 7 bias, FS1, 2 = H, OPA1 = 10H, OPA2 = 09H

Note 3: V_{DD} = 3.0 ± 10%, V_{DD} − $V_{EE1, 2}$ = 16.0 V, / STB = L

Note 4: V_{DD} = 3.0 V, I_{Load} = 500 µA, $V_{EE1, 2}$ = − 6.0 V (external power supply)
CnA − CnB = 2.2 µF, V_{DD} − V_{OUT2} = 2.2 µF, R_f = 62 kΩ, Ta = 25°C

Note 5: V_{DD} = 3.0 V, I_{Load} = 500 µA, $V_{EE1, 2}$ = − 9.0 V (external power supply)
CnA − CnB = 2.2 µF, V_{DD} − V_{OUT3} = 2.2 µF, R_f = 62 kΩ, Ta = 25°C

Test Conditions (2)
(Unless otherwise noted, V_{SS} = 0 V, V_{DD} = 5.0 V ± 10%, V_{LC5} = 0 V, Ta = −20 to 75°C)

Item		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Pin Name
Operating Supply (1)		V_{DD}	—	—	4.7	—	5.5	V	V_{DD}
Operating Supply (2)		V_{LC5} $V_{EE1, 2}$	—	—	V_{DD} − 16.0	—	V_{DD} − 4.0	V	V_{LC5}, V_{EE1}, V_{EE2}
Input Voltage	H Level	V_{IH}	—	—	0.7 V_{DD}	—	V_{DD}	V	DB0 to DB7, D / I, / WR, / RD, / CS1, CS2, / RST, / STB, FS1, FS2, SI, SCK, P / S, 68 / 80
	L Level	V_{IL}	—	—	0	—	0.3V_{DD}	V	
Output Voltage	H Level	V_{OH}	—	I_{OH} = − 400 µA	V_{DD} − 0.2	—	V_{DD}	V	DB0 to DB7
	L Level	V_{OL}	—	I_{OL} = 400 µA	0	—	0.2	V	
Column Driver Output Resistance		Rcol	—	V_{DD} − V_{LC5} = 11.0 V Load current = ± 100 µA	—	—	7.5	kΩ	SEG1 to SEG136
Row Driver Output Resistance		Rrow	—	V_{DD} − V_{LC5} = 11.0 V Load current = ± 100 µA	—	—	1.5	kΩ	COM1 to COM34
Input Leakage		I_{IL}	—	V_{IN} = V_{DD} to GND	−1	—	1	µA	DB0 to DB7, D / I, / WR, / RD, / CS1, CS2, / RST, / STB, FS1, FS2, SI, SCK, P / S, 68 / 80
Operating Freq.		f_{OSC}	—	—	20	—	500	kHz	OSC1
External Clock Freq.		f_{ex}	—	—	20	—	500	kHz	OSC1
External Clock Duty		f_{duty}	—	—	45	50	55	%	OSC1
External Clock Rise / Fall Time		t_r / t_f	—	—	—	—	50	ns	OSC1
Current Consumption (1)		I_{DD1}	—	(Note 1)	—	510	640	µA	V_{DD}
Current Consumption (2)		I_{DD2}	—	(Note 2)	—	620	830	µA	V_{DD}
Current Consumption (3)		I_{DDSTB}	—	(Note 3)	−1	—	1	µA	V_{DD}
Output Voltage (Doubler Mode)		VO1	1	(Note 4)	−4.25	−4.50	—	V	V_{OUT1}
Output Voltage (Tripler Mode)		VO2	2	(Note 5)	−8.50	−9.00	—	V	V_{OUT2}

Note 1: V_{DD} = 5.0 ± 10%, $V_{EE1, 2}$ = V_{OUT1} (doubler mode), no data access
R_f = 62 kΩ, no Load, 1 / 7 bias, FS1, 2 = H, OPA1 = 10H, OPA2 = 09H

Note 2: V_{DD} = 5.0 ± 10%, $V_{EE1, 2}$ = V_{OUT2} (doubler mode), data access cycle f / $_{CE}$ = 1 MHz,
R_f = 62 kΩ, no load, 1 / 7 bias, FS1, 2 = H, OPA1 = 10H, OPA2 = 09H

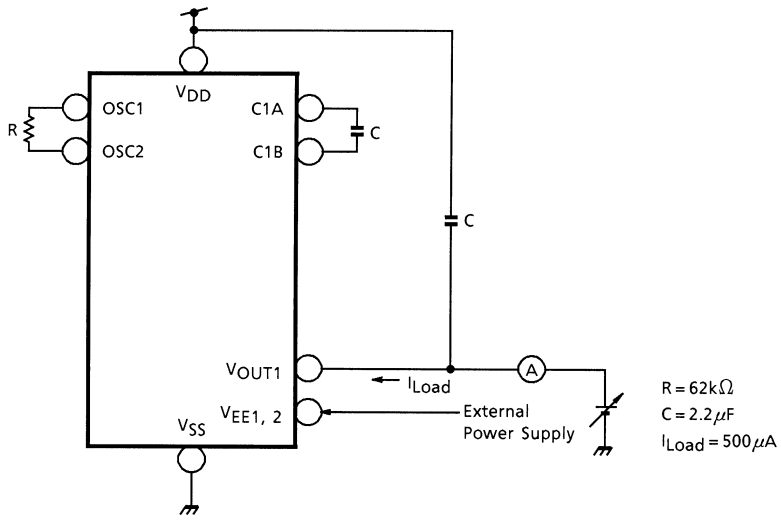
Note 3: V_{DD} = 5.0 ± 10%, V_{DD} − $V_{EE1, 2}$ = 16 V, / STB = L

Note 4: V_{DD} = 5.0 V, I_{Load} = 500 µA, $V_{EE1, 2}$ = − 5.0 V (external power supply)
CnA − CnB = 2.2 µF, V_{DD} − V_{OUT1} = 2.2 µF, R_f = 62 kΩ, Ta = 25°C

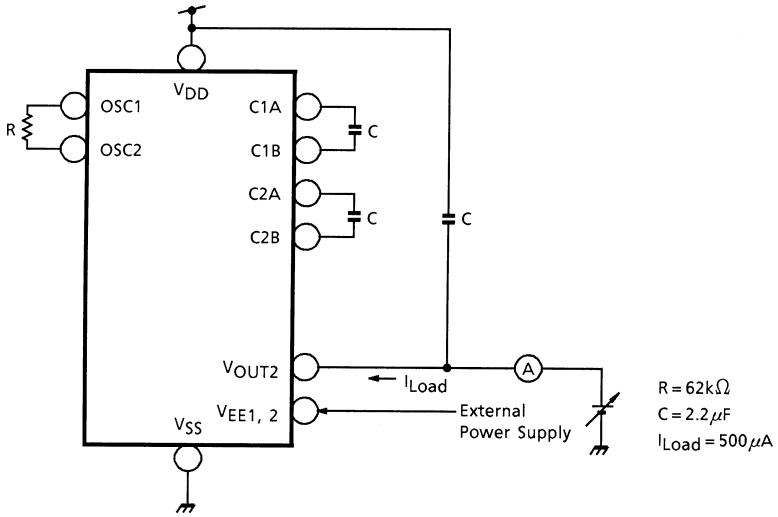
Note 5: V_{DD} = 5.0 V, I_{Load} = 500 µA, $V_{EE1, 2}$ = − 10.0 V (external power supply)
CnA − CnB = 2.2 µF, V_{DD} − V_{OUT2} = 2.2 µF, R_f = 62 kΩ, Ta = 25°C

Test Circuit

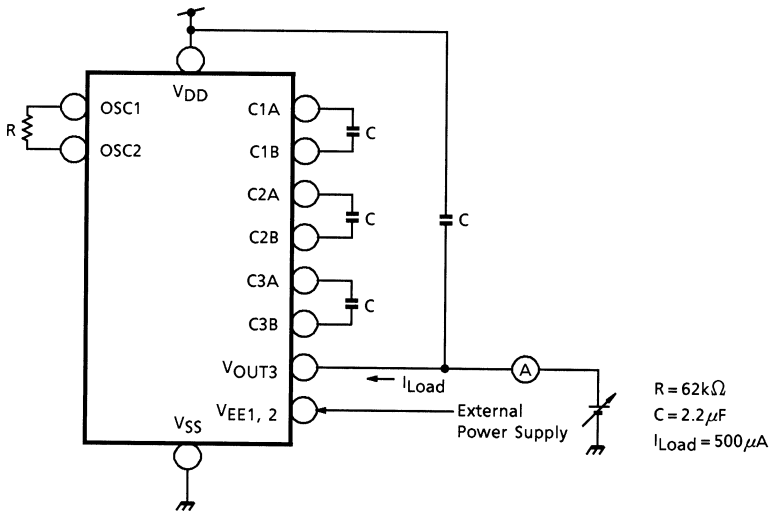
1. Doubler mode



2. Tripler mode

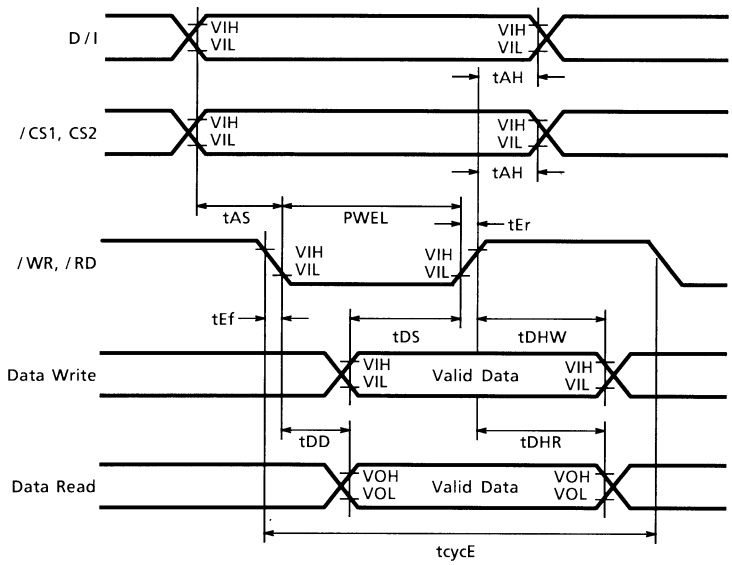


3. Quadruplexer mode



AC Characteristics

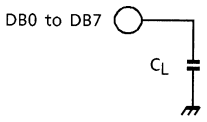
- **80−Series MPU 8−bit interface**



Test Conditions (1) (V_{SS} = 0 V, V_{DD} = 3.0 V ± 10%, V_{LC5} = 0 V, Ta = −20 to 75°C)

Item	Symbol	Min	Max	Unit
Enable Cycle Time	tcycE	1000	—	ns
Enable Pulse Width	PWEL	450	—	ns
Enable Rise / Fall Time	tEr, tEf	—	25	ns
Address Set−up Time	tAS	100	—	ns
Address Hold Time	tAH	0	—	ns
Data Set−up Time	tDS	280	—	ns
Data Hold Time	tDHW	20	—	ns
Data Delay Time	tDD (Note)	—	350	ns
Data Hold Time	tDHR (Note)	20	—	ns

Load Circuit



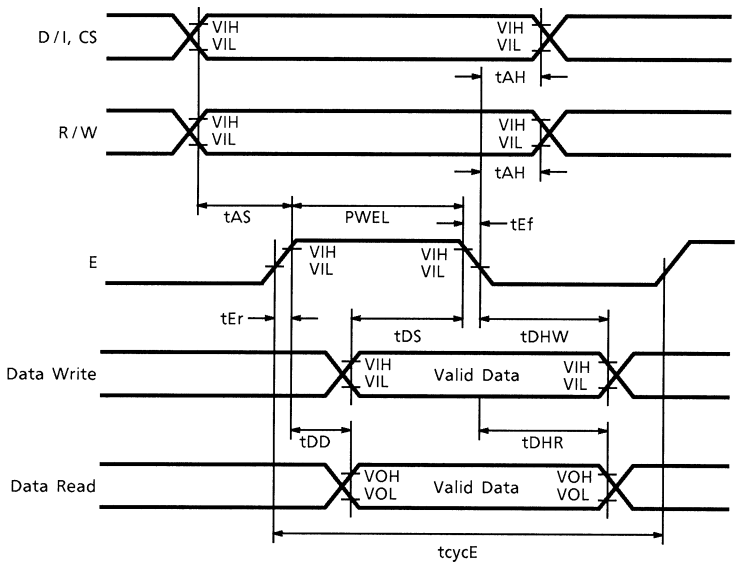
C_L = 100pF
(including wiring capacitance)

Test Conditions (2) (V_{SS} = 0 V, V_{DD} = 5.0 V ± 10%, V_{LC5} = 0 V, Ta = −20 to 75°C)

Item	Symbol	Min	Max	Unit
Enable Cycle Time	tcycE	500	—	ns
Enable Pulse Width	PWEL	220	—	ns
Enable Rise / Fall Time	tEr, tEf	—	20	ns
Address Set−up Time	tAS	60	—	ns
Address Hold Time	tAH	0	—	ns
Data Set−up Time	tDS	60	—	ns
Data Hold Time	tDHW	10	—	ns
Data Delay Time	tDD (Note)	—	160	ns
Data Hold Time	tDHR (Note)	20	—	ns

Note: With load circuit connected

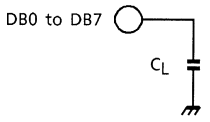
- **68−Series MPU 8−bit interface**



Test Conditions (1) (V_{SS} = 0 V, V_{DD} = 3.0 V ± 10%, V_{LC5} = 0 V, Ta = −20 to 75°C)

Item	Symbol	Min	Max	Unit
Enable Cycle Time	tcycE	1000	—	ns
Enable Pulse Width	PWEL	450	—	ns
Enable Rise / Fall Time	tEr, tEf	—	25	ns
Address Set−up Time	tAS	100	—	ns
Address Hold Time	tAH	0	—	ns
Data Set−up Time	tDS	280	—	ns
Data Hold Time	tDHW	20	—	ns
Data Delay Time	tDD (Note)	—	350	ns
Data Hold Time	tDHR (Note)	20	—	ns

Load Circuit



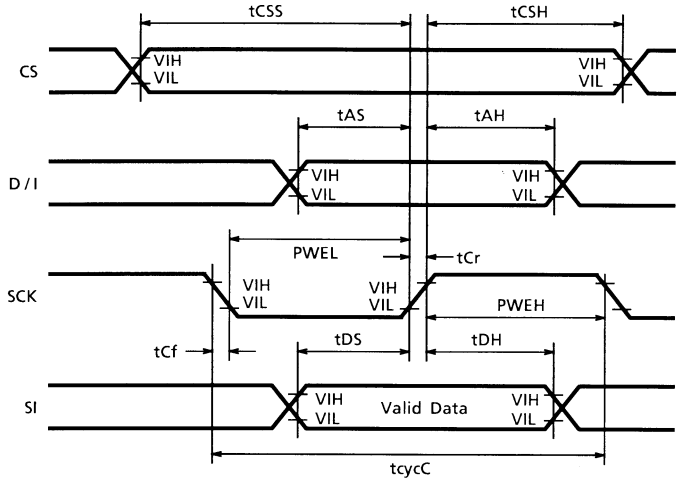
C_L = 100pF
(including wiring capacitance)

Test Conditions (2) (V_{SS} = 0 V, V_{DD} = 5.0 V ± 10%, V_{LC5} = 0 V, Ta = −20 to 75°C)

Item	Symbol	Min	Max	Unit
Enable Cycle Time	tcycE	500	—	ns
Enable Pulse Width	PWEL	220	—	ns
Enable Rise / Fall Time	tEr, tEf	—	20	ns
Address Set−up Time	tAS	60	—	ns
Address Hold Time	tAH	0	—	ns
Data Set−up Time	tDS	60	—	ns
Data Hold Time	tDHW	10	—	ns
Data Delay Time	tDD (Note)	—	160	ns
Data Hold Time	tDHR (Note)	20	—	ns

Note: With load circuit connected

- **Serial interface**



Test Conditions (1) (V_{SS} = 0 V, V_{DD} = 3.0 V ± 10%, V_{LC5} = 0 V, Ta = −20 to 75°C)

Item	Symbol	Min	Max	Unit
Clock Cycle Time	tcycC	1000	—	ns
Clock Pulse Width	PWCL, PWCH	450	—	ns
Clock Rise / Fall Time	tCr, tCf	—	25	ns
CS Set−up Time	tCSS	120	—	ns
CS Hold Time	tCSH	800	—	ns
Address Set−up Time	tAS	250	—	ns
Address Hold Time	tAH	400	—	ns
Data Set−up Time	tDS	250	—	ns
Data Hold Time	tDH	100	—	ns

Test Conditions (2) (V_{SS} = 0 V, V_{DD} = 5.0 V ± 10%, V_{LC5} = 0 V, Ta = −20 to 75°C)

Item	Symbol	Min	Max	Unit
Clock Cycle Time	tcycC	500	—	ns
Clock Pulse Width	PWCL, PWCH	220	—	ns
Clock Rise / Fall Time	tCr, tCf	—	20	ns
CS Set−up Time	tCSS	60	—	ns
CS Hold Time	tCSH	400	—	ns
Address Set−up Time	tAS	120	—	ns
Address Hold Time	tAH	200	—	ns
Data Set−up Time	tDS	120	—	ns
Data Hold Time	tDH	50	—	ns

Application Circuit

- Oscillation frequency is at a minimum.
- LCD drive bias is 1 / 7.
- DC−DC converter (in doubler mode) is used.
- 80−Series MPU is used.