TOSHIBA

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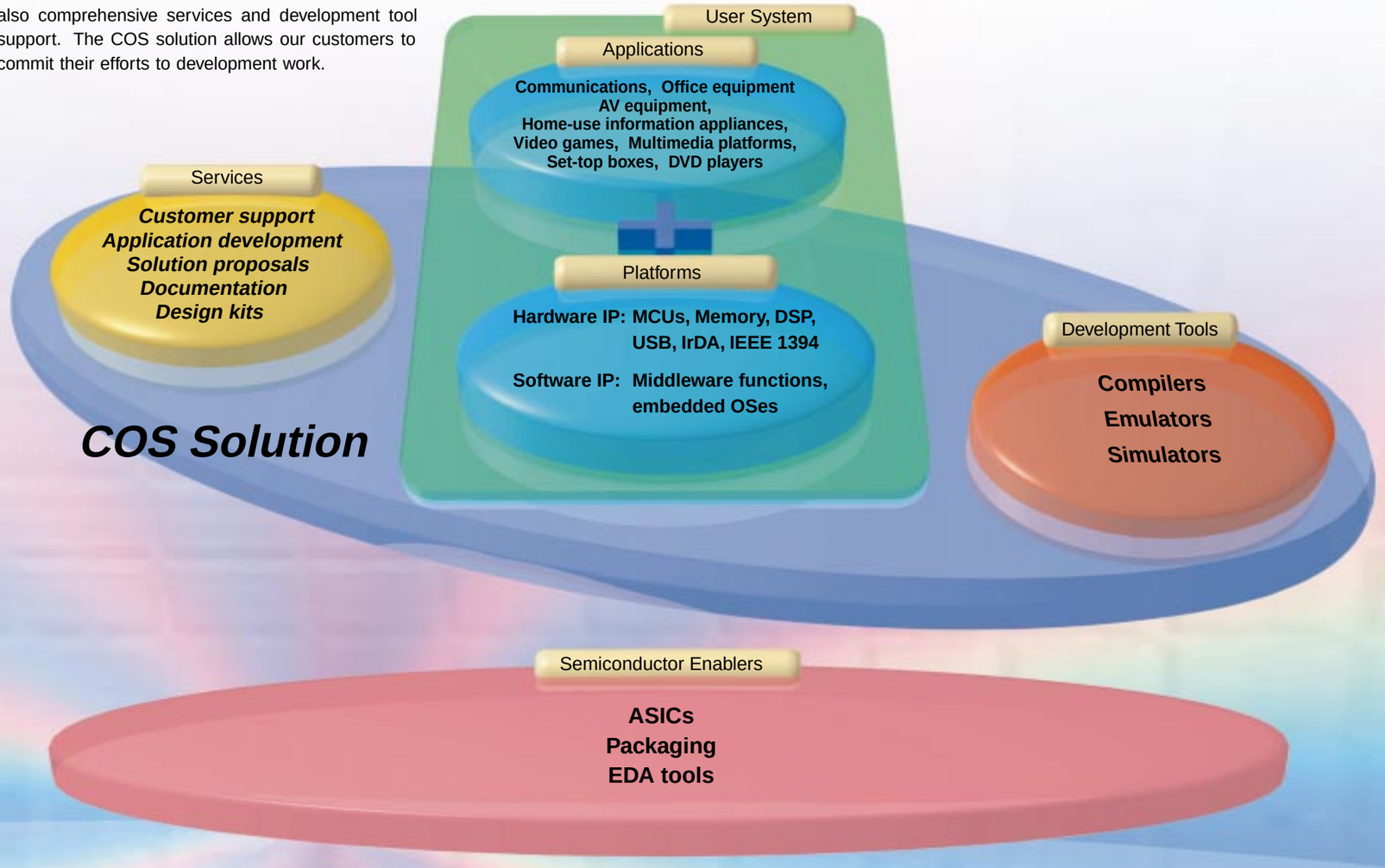
RISC/CISC ASIC

PRODUCT GUIDE

The Dawn of the “Computer -on-Silicon” Age

Specialized microcontrollers are increasingly used to control devices of all kinds such as automobiles, home and office appliances, handheld equipment, etc. With this trend getting into high gear, application software is customized more often than ever before to fit specific needs of target systems.

Toshiba offers a computer-on-silicon (COS) solution to help its customers improve the time-to-market for their new processor-based systems. The combination of Toshiba’s world-class computer and silicon technologies provides its customers with a total solution - a partnership with Toshiba brings you not only the performance of our hardware and software IP, but also comprehensive services and development tool support. The COS solution allows our customers to commit their efforts to development work.



To meet diverse customer needs, Toshiba provides a broad range of Reduced Instruction Set Computer (RISC) and Complex Instruction Set Computer (CISC) processors. Our RISC and CISC processors are available either as ASIC-ready cores or as standard products. Toshiba's ASIC core portfolio includes a gallery of 32- and 64-bit **TX** families of RISC cores as well as Toshiba's proprietary 16-bit CISC processor families such as **TLCS-900/H** and **TLCS900/L1**. Also included among ASIC-ready cores are a variety of hardware and software IP cores targeted for consumer, computer, and communications applications. All these cores give you great flexibility in the design of advanced multimedia products.

Gateway to the COS Age – RISC/CISC ASICs from Toshiba.

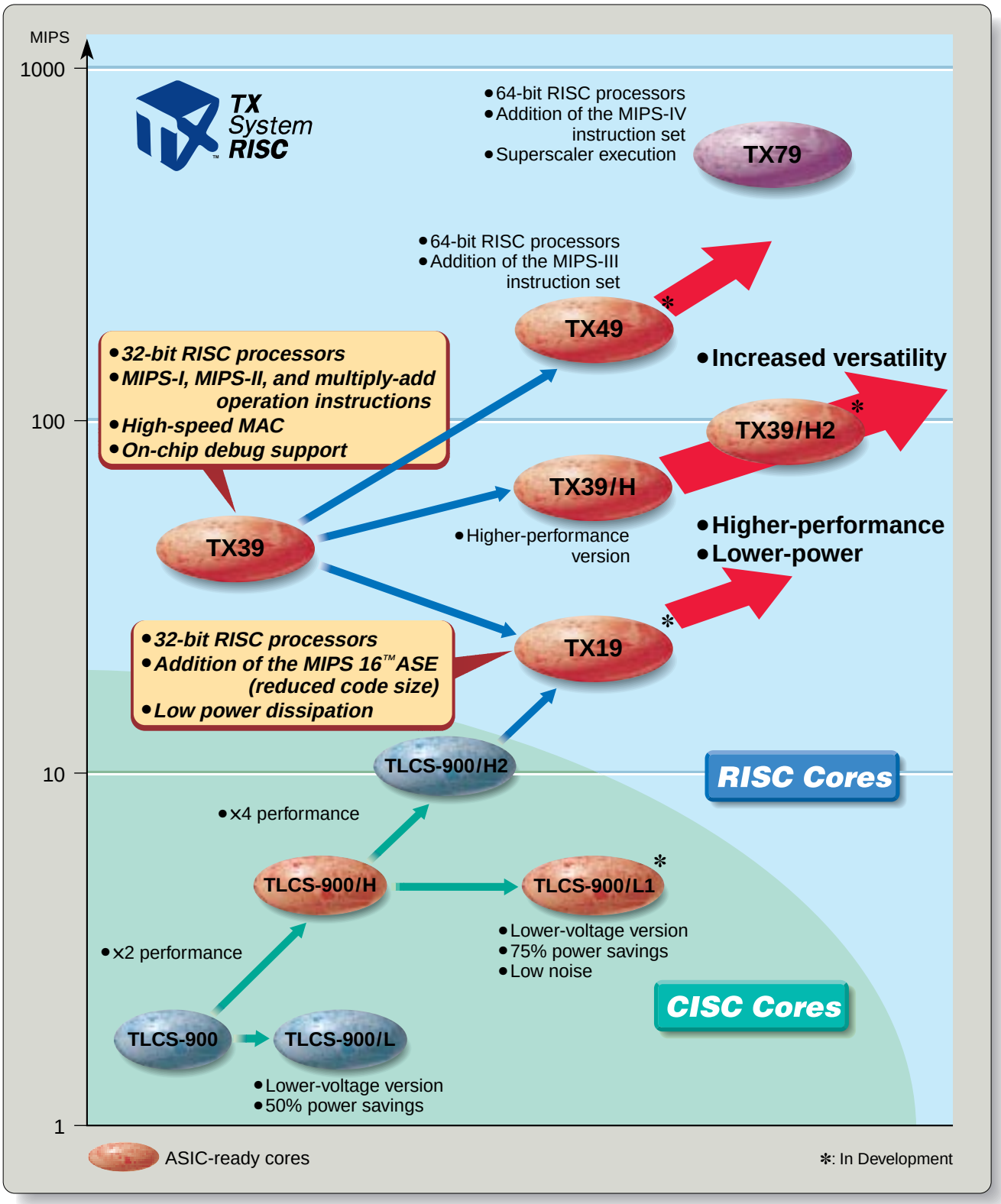
Computer On Silicon

TX System RISC™

CONTENTS

Continuous Evolution of Toshiba's MPU Cores

The following road map shows a whole suite of Toshiba's ASIC-ready MPU cores. Toshiba offers a broad and varied range of RISC and CISC options to suit your unique needs, including applications, power dissipation, and performance requirements. Encompassing Toshiba's MPU core offerings are the **TLCS-900** CISC family and the **TX19**, **TX39**, **TX49**, and the next-generation RISC families.



✵ MIPS16 is a trademark of MIPS Technologies, Inc.

ASIC-Ready RISC Cores

TX System RISC TX39 Family

The **TX39** family is a high-performance 32-bit microprocessor for embedded applications developed by Toshiba based on the MIPS R3000A architecture. The **TX39** family can be used as a foundation for embedded array or cell-based ASIC designs.

Microprocessor Core

- R3000A architecture
- High-performance:
  TX39/H: ***74 MIPS*** (at 70 MHz operation)
  TX39/H2 (in development):
  105 MIPS (at 100 MHz operation)
  based on Dhrystone 2.1 VAX-11/780 benchmarking
- Built-in cache memory
  Separate instruction and data caches
- Non-blocking load function
  Avoids performance degradation by executing the next instruction while the data cache is being refilled.
- DSP function
  One-cycle Multiply-Accumulate (MAC) supporting 32-bit × 32-bit multiply-add operations

Low Power

- Multiple power saving modes of operation, including Reduced-Frequency (RF), Doze, Halt modes, etc.
- The PLL oscillation can be halted externally (standby mode)

Functions for Embedded Applications

- Improved code density and performance
  Branch-likely instructions
  Hardware interlock

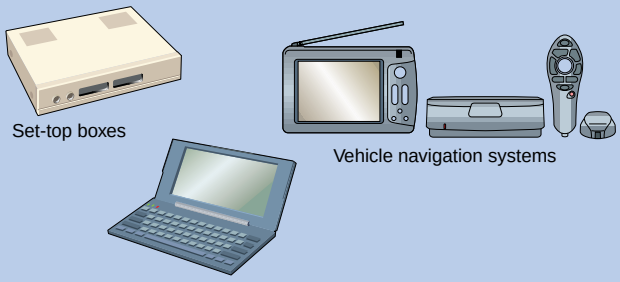
Development Tool Support

- C/C++ compiler, assemblers/linkers
- External real-time debug system support
  Provides for real-time debug with caches enabled.
- Support of various real-time OSes
- Standard board applicable to evaluation and user application

ASIC Support

- Proven EDA environment with RTL Verilog models
- Peripherals add-ons provided as megacells
- MPU core availability:
  - **GR39WAD**: **TX39/H** core (TC220)
  - **PTX3904A**: Functionally-equivalent to **TMPR3904A** (TC220)
  - **PTX39WAD**: **TX39/H2** core (TC240, in development)

Applications



❋ R3000A is a trademark of MIPS Technologies, Inc.

TX39 Family ASSP Products

Product Number	Applications	Clock Frequency	Voltage	Package
TMPR3901AF-70	Standard MPU	70 MHz	3.3 V	QFP160
TMPR3903AF	Vehicle navigation systems	40 MHz	3.3 V	QFP208
TMPR3904AF-66*	Peripherals added to the standard MPU	66 MHz	3.3 V	QFP208
TMPR3907F	Peripherals and a PCI controller added to the standard MPU	66 MHz	3.3 V	QFP208
TMPR3912AU/XB	Personal information communicators (PIC)	92 MHz	3.3 V	LQFP208 / FBGA217
TMPR3922AU/XB	Personal information communicators (PIC)	129/148* MHz	I/O: 3.3 V Core: 2.7 V	LQFP208 / FBGA217

*: In Development

ASIC-Ready RISC Cores

TX System RISC TX19 Family

The **TX19** family is an extremely compact, high-performance 32-bit microprocessor developed by Toshiba based on the MIPS R3000A architecture. The **TX19** family added support for MIPS16™ Application-Specific Extension (ASE), a highly efficient code compression mechanism, to the **TX39** family. Toshiba has been introducing application-specific standard products (ASSPs) in stages that integrate the **TX19** processor core and various peripheral building blocks on the same chip. In addition, the **TX19** processor core can be used in ASIC designs for high-performance embedded systems.

Microprocessor Core

- R3000A architecture
- High-performance: ***42 MIPS*** (at 40 MHz operation)
  based on Dhrystone 2.1 VAX-11/780 benchmarking
- Built-in cache memory and high-speed data RAM
- Non-blocking load function
  Avoids performance degradation by executing the next instruction while the data cache is being refilled.
- DSP function
  Fast Multiply-Accumulate (MAC)
  supporting 32-bit × 32-bit multiply-add operations

Low Power

- Optimized design implemented using a low-power cell library
- Power saving modes
  Clock gearing function (Reduced-Frequency mode)
  Various standby modes

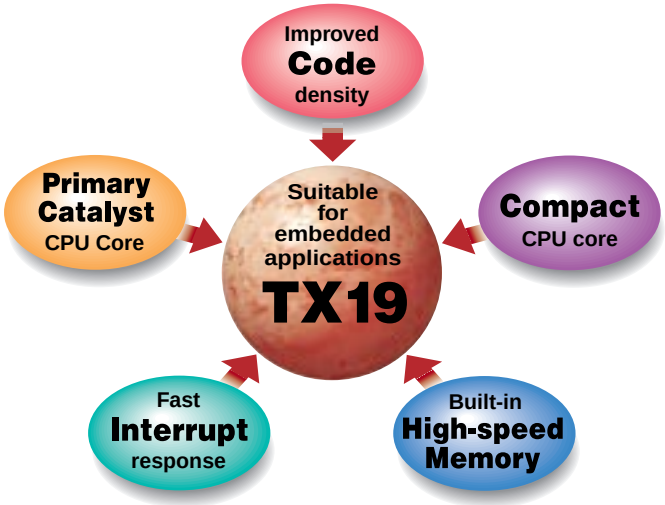
Functions for Embedded Applications

- Compatible with MIPS16™ ASE
- Real-time performance
  Minimizes an interrupt response time (e.g. through one-clock-access RAM)
  Instruction/data cache locking function

※ R3000A and MIPS16 are trademarks of MIPS Technologies, Inc.

ASIC Support

- Implemented with the **TC240** technology process
- Requires a very small die area
- Upgrading development tools



Intermixing 16-and 32-bit instructions provides all the performance benefits of an embedded 32-bit microprocessor while offering reduced code size associated with the 16-bit instruction set.

32-bit instruction code

- Provides performance gains.
- Object-compatible with TX39.
- Supports multiply-add and coprocessor instructions.

Switched by an instruction

16-bit instruction code

- Provides excellent code density.
- Supports PC-relative instructions.

Applications

- Handheld devices: **Personal information communicators (PIC), electronic organizers, digital cellulars**
- PC peripheral equipment: **HDD, DVD-ROM, printers**
- Home appliances: **DVD players, DVC-based systems, digital still cameras (DSC)**

ASIC-Ready CISC Cores

900 Family

The **900** family is a high-performance 16-bit microcontroller (MCU) with high C code efficiency. The **900** family offers a wide range of features to fit a variety of requirements for different products ranging from office equipment such as printers and facsimiles to high-end consumer electronic products like digital still cameras (DSC) and DVC-based systems to portable equipment that mandates low power dissipation. To significantly reduce the time and expense of controller design, a wide range of powerful and consistent development tools are available from Toshiba and several third-party development tool vendors.

The **900** family contains two product series: high-performance **900/H** and low-power, low-noise **900 /L1**.

Suitable for high-end office equipment

High-Performance CISC Core

- Minimum instruction execution time: 160 ns (at 25 MHz)
- 32-bit ALU
- 4-bit barrel shifter

Compact Core

- Reduced die size due to a very lean set of instructions selected for embedded applications

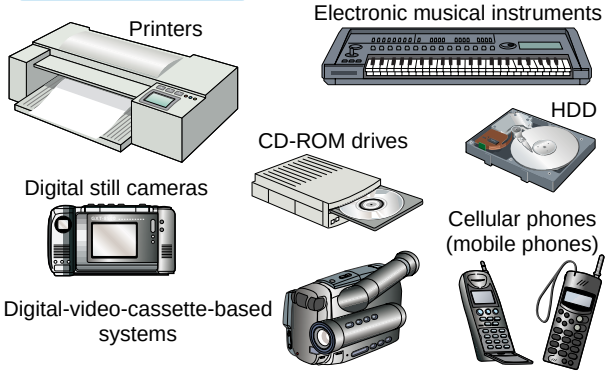
Suitable for applications with low-power and low-noise requirements

Low Power (900/L1)

Tentative Specifications

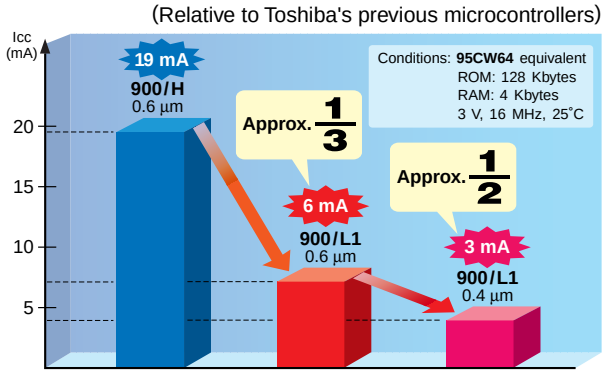
- Operating voltage range: 1.8 to 5.5 V
- Minimum instruction execution time: 250 ns (at 16 MHz, Vcc ≥ 2.7 V) 400 ns (at 10 MHz, Vcc ≥ 1.8 V)
- Low power dissipation: 3.0 mA typical (16 MHz, 3.0V, NORMAL mode)
- Clock gearing function: (fc, fc/2, fc/4, fc8, fc/16)
- Dual clock function
- Three standby modes
- Low-power design techniques (e.g. gated clocks)

Applications

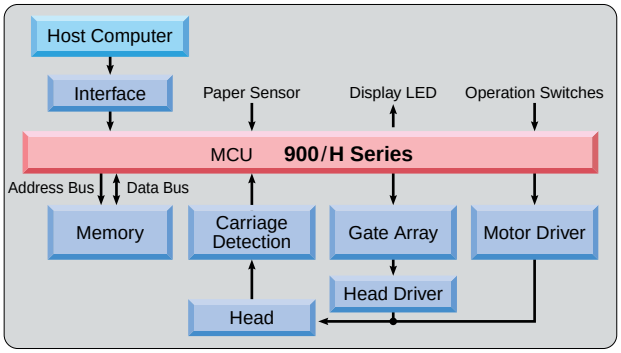


Reduction of Power Dissipation

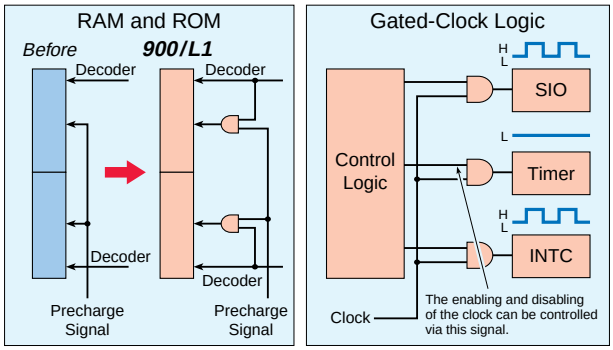
(Relative to Toshiba's previous microcontrollers)



Serial Printer Block Diagram

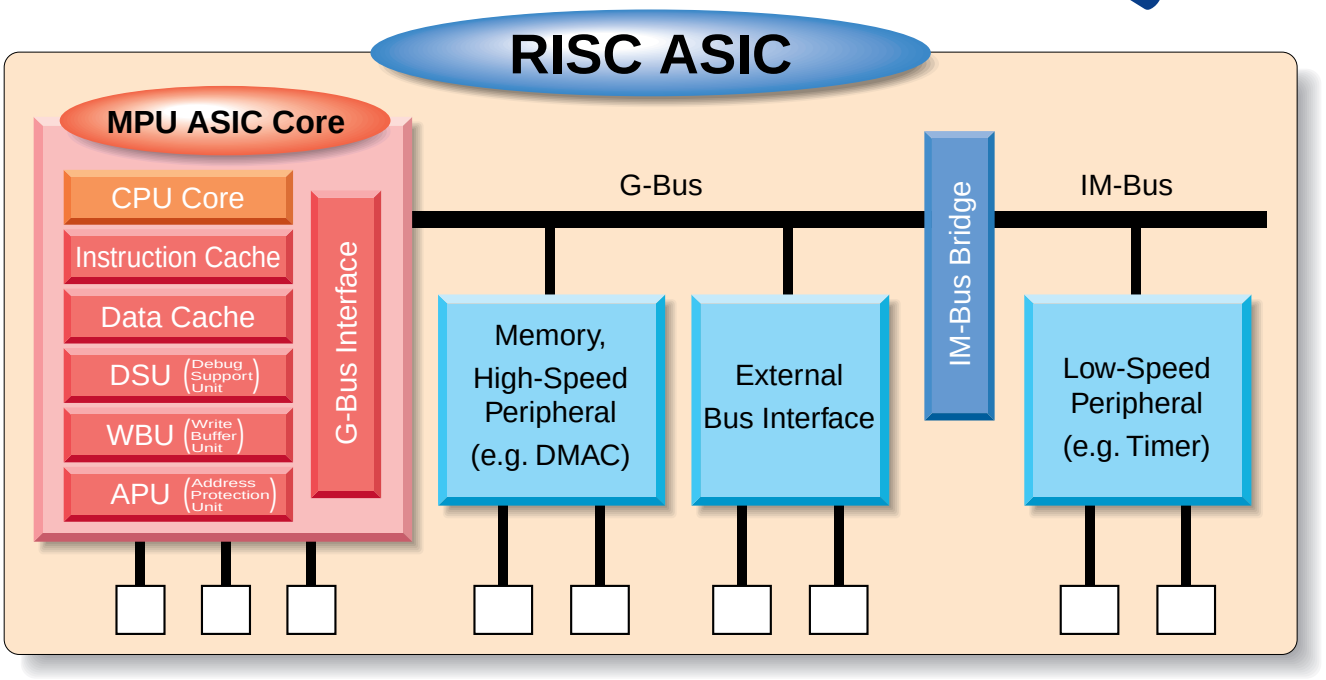


Examples of Low-Power Design Techniques



RISC ASIC

RISC ASIC Configurations



- The RISC ASIC allows designers to integrate a **TX System RISC** megacell (or system CPU) with peripheral IP cores and/or user-defined logic on one chip.
- The integral G-bus directly connects system components together, such as a DMA controller acting as a bus master, a memory controller, a interrupt controller, etc. The specification of G-bus is provided to users of a **TX System RISC** megacell.
- Low-speed peripherals like a timer and a UART block are connected through IM-Bus via a bridging logic.
- Currently, the **TX System RISC** megacells are available in two versions: **GR39WAD** which integrates a **TX39** CPU core with a Address Protection Unit (APU), Write Buffer Unit (WBU), and a Debug Support Unit (DSU) and **PTX3904A** which is functionally equivalent to **TX3904A**. The high-performance megacell, **PTX39WAD**, is in development using the **TC240** technology.
- The **TX39-based ASIC** chip requires a package with at least 160 pins.

Application Example

Digital BS Receiver
MPEG-2 Decoder IC: **TC81220F**

Toshiba's **TC81220F** integrates a **TX39** core, a MPEG-2 video decoder, a MPEG-1/2 audio decoder, a programmable transport processor, standard peripherals, a memory controller, etc.

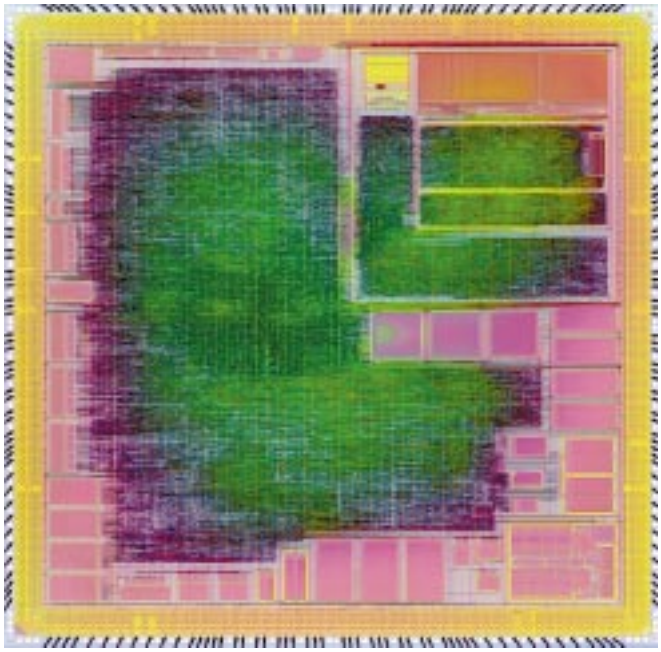
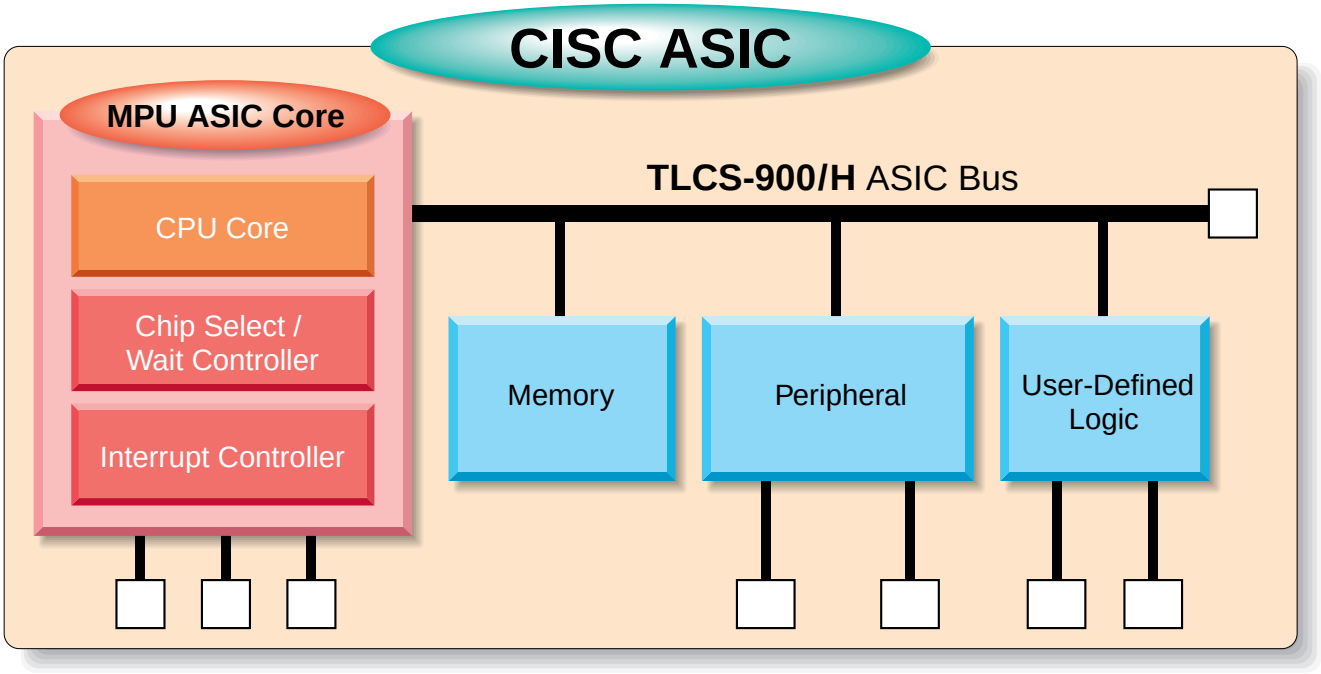


Photo of the **TC81220F**

CISC ASIC

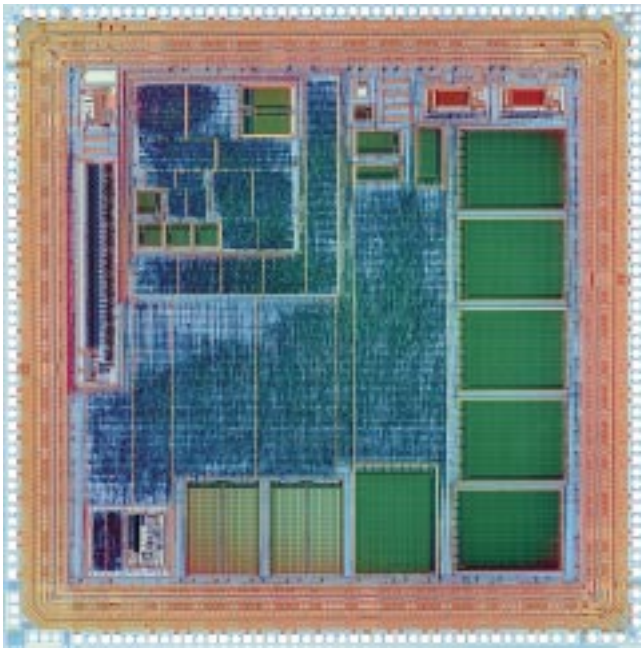
CISC ASIC Configurations



- The CISC ASIC offers a megacell, **SMC95C001**, which integrates a **900/H** core with such built-in functions as a chip-select/wait controller and an interrupt controller. The SMC95C001 is functionally equivalent to Toshiba's standard product **TMP95C001**.
- The **TLCS-900/H** Bus, which is the standard bus specification for all **900/H** products, connects the **900/H** core with memories (RAMs, ROMs, etc.), peripheral I/O functions, and user-defined logic.
- The **TLCS-900/H** Bus is routed off-chip, so the same emulator can be used to test both the standard **TMP95C001** product and **900/H** core-based ASICs.

Application Example

Toshiba used its CISC ASIC solution to integrate a **900/H** core with ROM, RAM, standard peripherals, and A/D converters to build a communications IC. This IC is fabricated using the **TC222C** technology. While the I/O interfaces with 3 V, the core operates at 2 V, reducing power dissipation.



Communications IC Implemented as a CISC-Processor-Core-Based ASIC

IP Core Lines

- A broad range of high-density, high-performance IP cores is an essential element for the success of advanced ASIC designs for all consumer, communications, and data processing applications.
- For true systems-on-a-chip, the supporting ASIC silicon technologies cover a full spectrum of application requirements with a wide range of power, density, and speed solutions.
- IP core offerings meet the requirements of system chips. Hardware IP libraries include cores that implement RISC and CISC processors as well as multimedia, network, and protocol functions. Software (or synthesizable) IP libraries include cores that implement middleware functions such as JPEG, speech processing, and fax modem as well as real-time embedded operating systems and software drivers.

IP Core Availability

(Cores in development are included.)

Software

Middleware	Image processing MH / MR / MMR, JBIG, JPEG Audio processing ADPCM, CELP Human-machine interface Speech recognition, Speech synthesis, Handwriting recognition Communication and PC interface Software modems, IEEE1394, USB, IrDA, PCMCIA, TCP/IP, PPP, SNMP, DOS filesystem
Real-time Embedded OSes	µITRON/UDEOS, pSOSystem®, Windows® CE, Tornado™

Hardware

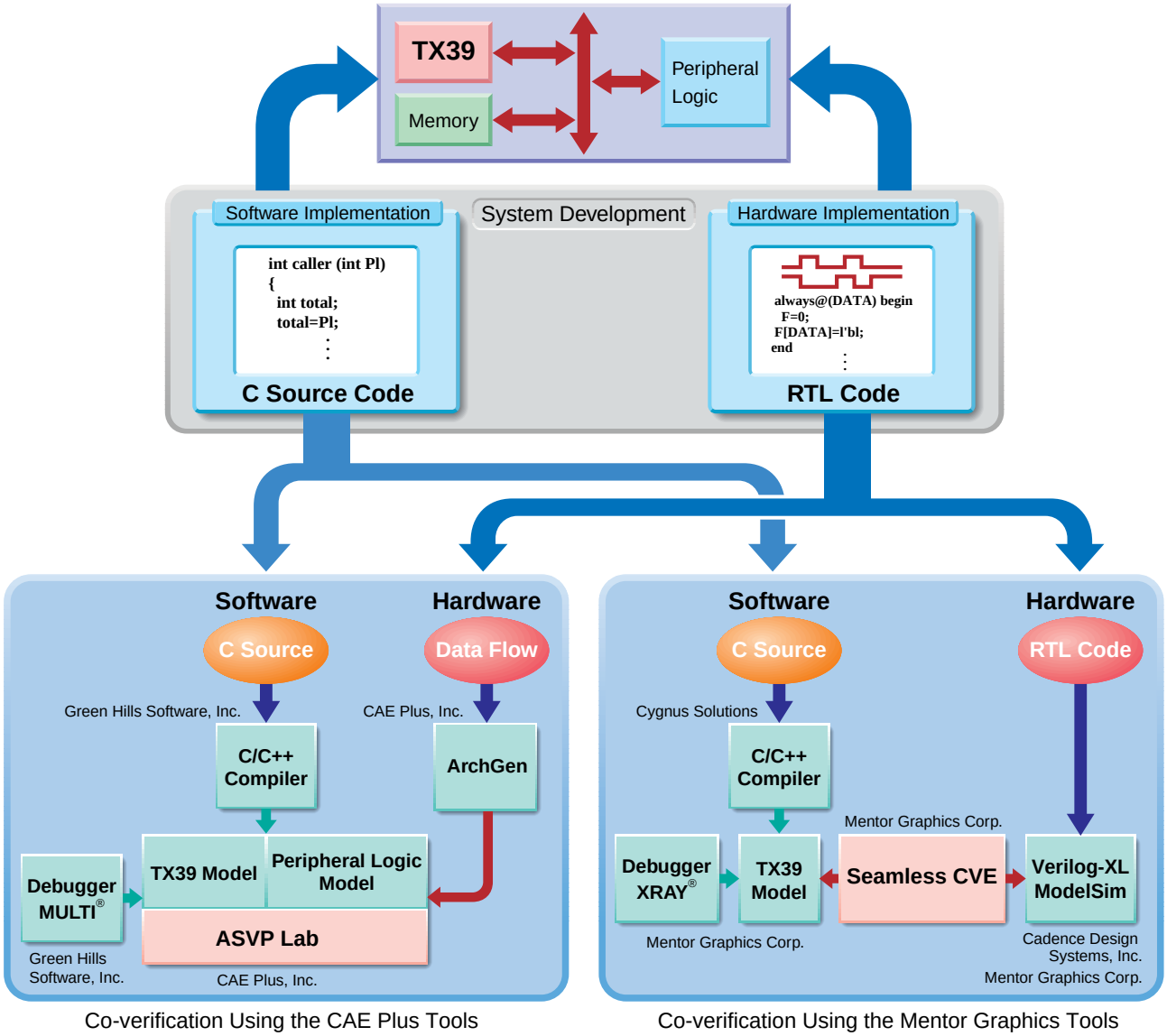
Multimedia	JPEG core, MPEG-2 decoder, NTSC/PAL video encoder, MPEG-4 core
Networking	Ethernet 10/100 MHz MAC, Ethernet 100 MHz PHY, 155 MHz CDR
Protocols	IEEE1394, IEEE1284, PCI controller, TCP/IP, USB, IrDA (V1.1), PCMCIA, CardBUS, AGP, SSFDC interface, ATAPI
High-Performance I/O	622MHz SCI-LVDS, SSTL-3 (SDRAM interface), 66 MHz PCI, USB, AGP, Direct RAC (1.6 GBps Rambus™ASIC cell)
RISC Processors	**TX49** (64-bit), **TX39** (32-bit), **TX19** (32-bit),
CISC Processors	**TLCS-900** (16-bit), **TLCS-Z80** (8-bit)
Peripherals	DRAM controller, ROM controller, Interrupt controller, Timer, DMAC, Serial interface (UART), Parallel interface, External bus interface
Analog Cores	A/D converters, D/A converters, PLL
Memory	DRAM, SRAM, FIFO, ROM, E^2PROM, Flash E^2PROM
Standard ASIC Cells	Primitive cells, I/O cells

Hardware/Software Co-verification Environment

Seamless Co-verification Flow

The traditional approach to the development of system chips with an embedded CPU core is usually a series of sequential and independent steps. This means system development is fragmented into task-oriented specialties like hardware and software designs. Detailed analysis of interactions between hardware and software is only possible after hardware prototyping. While software errors are relatively easy to fix, errors in hardware can cause significant delays if design rework is needed. Today's increasingly complex designs and shortened design cycles make the traditional approach unsuitable.

The hardware/software co-verification environment addresses the problems of the traditional design cycle by linking software and hardware verification together. Toshiba supports ASVP Lab from CAE Plus and Seamless CVE from Mentor Graphics by offering the C model of the **TX39** core. ASVP Lab provides all-C model hardware and software debugging by assembling ArchGen C models of user-defined logic and the **TX39 C** model into a high-speed virtual prototype. Seamless CVE delivers high-performance system verification environment by combining embedded software development tools with behavioral and logic simulation.



Co-verification Using the CAE Plus Tools

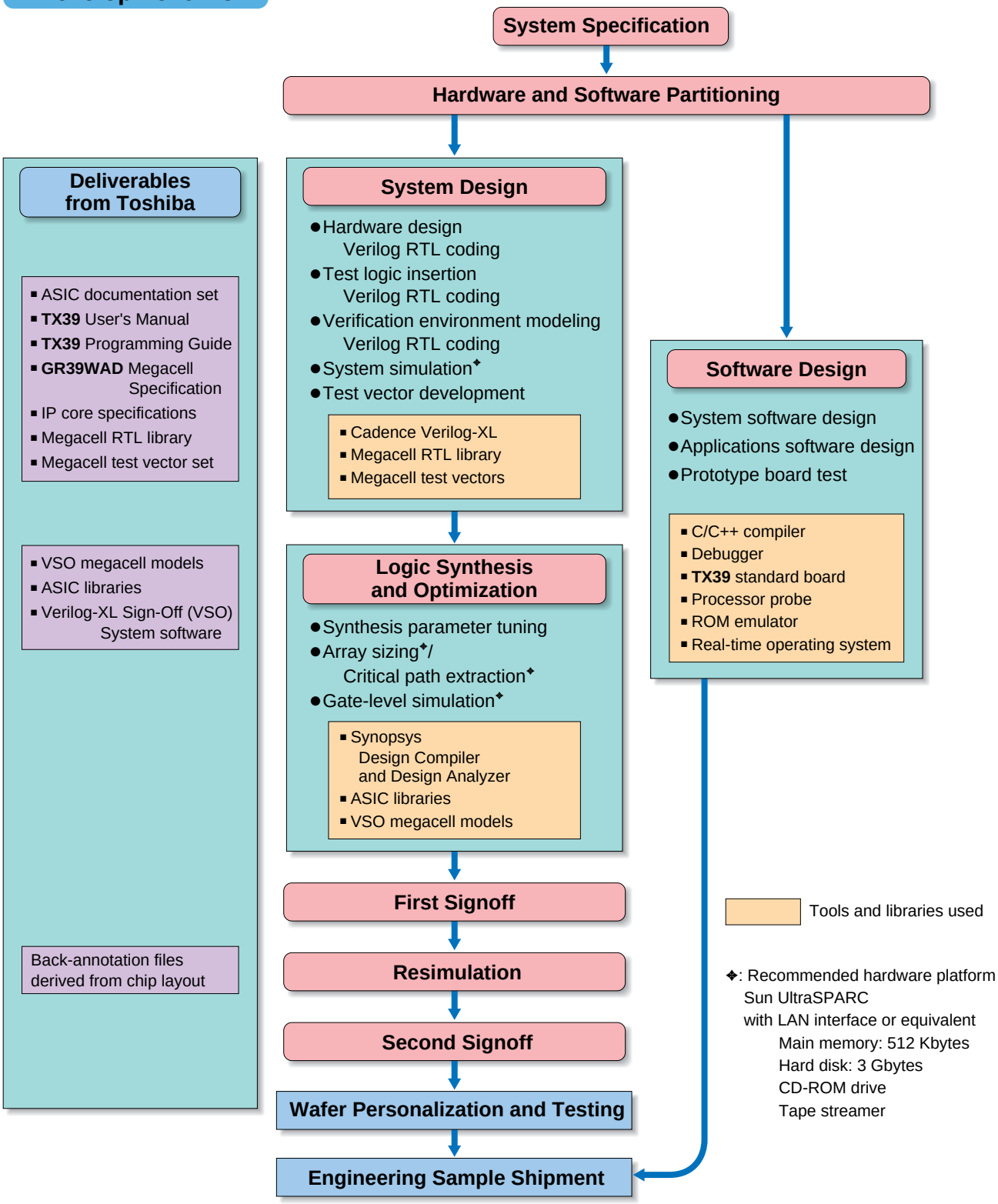
Co-verification Using the Mentor Graphics Tools

∗ Company names and product names may be trademarks or registered trademarks by their respective companies.

Development Flow

The following flowchart shows a typical process for developing an ASIC with an integrated **TX39** family RISC processor core, **GR39WAD**. For support of EDA tools not shown in the flowchart, please contact your local Toshiba customer support group.

■ Development Flow

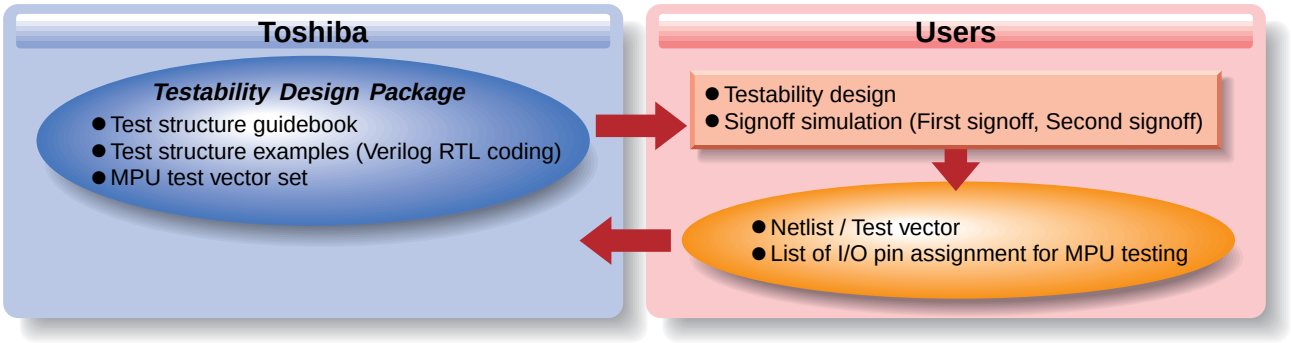


Test Methodologies

There are two issues for testing of a chip with embedded blocks such as an MPU core. One is testing of the block itself. In the case of a large, complex block like an MPU core, it is necessary to test the block separately from the rest of the chip. The figure below shows a direct access approach where the MPU core is isolated from the user-defined logic by providing an access collar around it. All inputs and outputs of the MPU core are made directly accessible and observable for testing by connecting multiplexers to package pin test points. A test vector set for the stand-alone test of an embedded core is provided by Toshiba.

Testability Design Flow

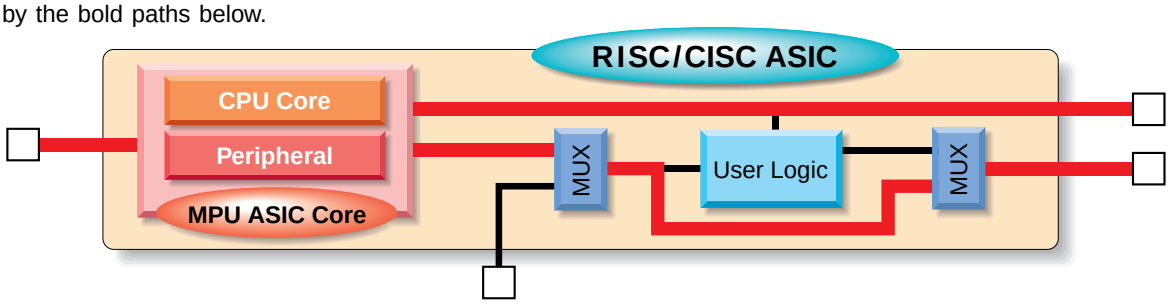
- Test structures need to be designed as part of the user-defined logic.
- Test structure examples coded at RTL are provided by Toshiba.
- An automated test synthesis system is being planned.



Isolating the MPU Core

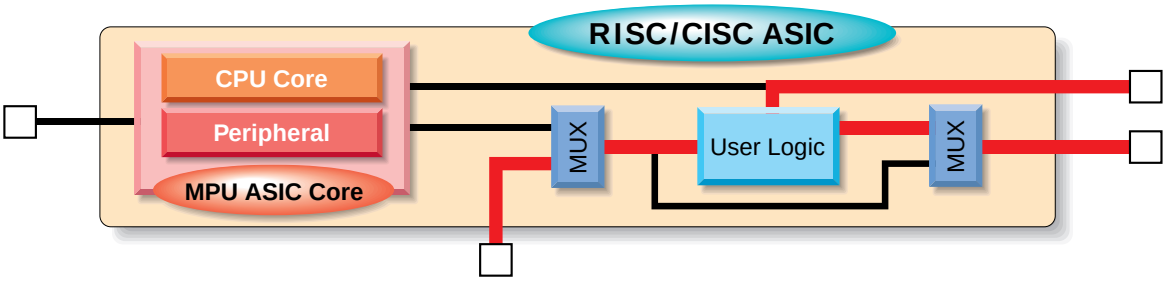
Stand-alone Testing of the MPU

- The MPU core is isolated from the rest of the design during testing. Test vectors for the MPU core are provided by Toshiba and multiplexed through a set of I/O pins. The flow of data while the MPU core is tested is shown by the bold paths below.



Testing of the User-Defined Logic

- The user-defined logic is isolated from the MPU core for testing purposes. Test vectors for the user-defined logic are created by the designer, and internal signals are routed as necessary to ASIC I/O pins to improve testability. The flow of data while the user-defined logic is tested is shown by bold paths below.

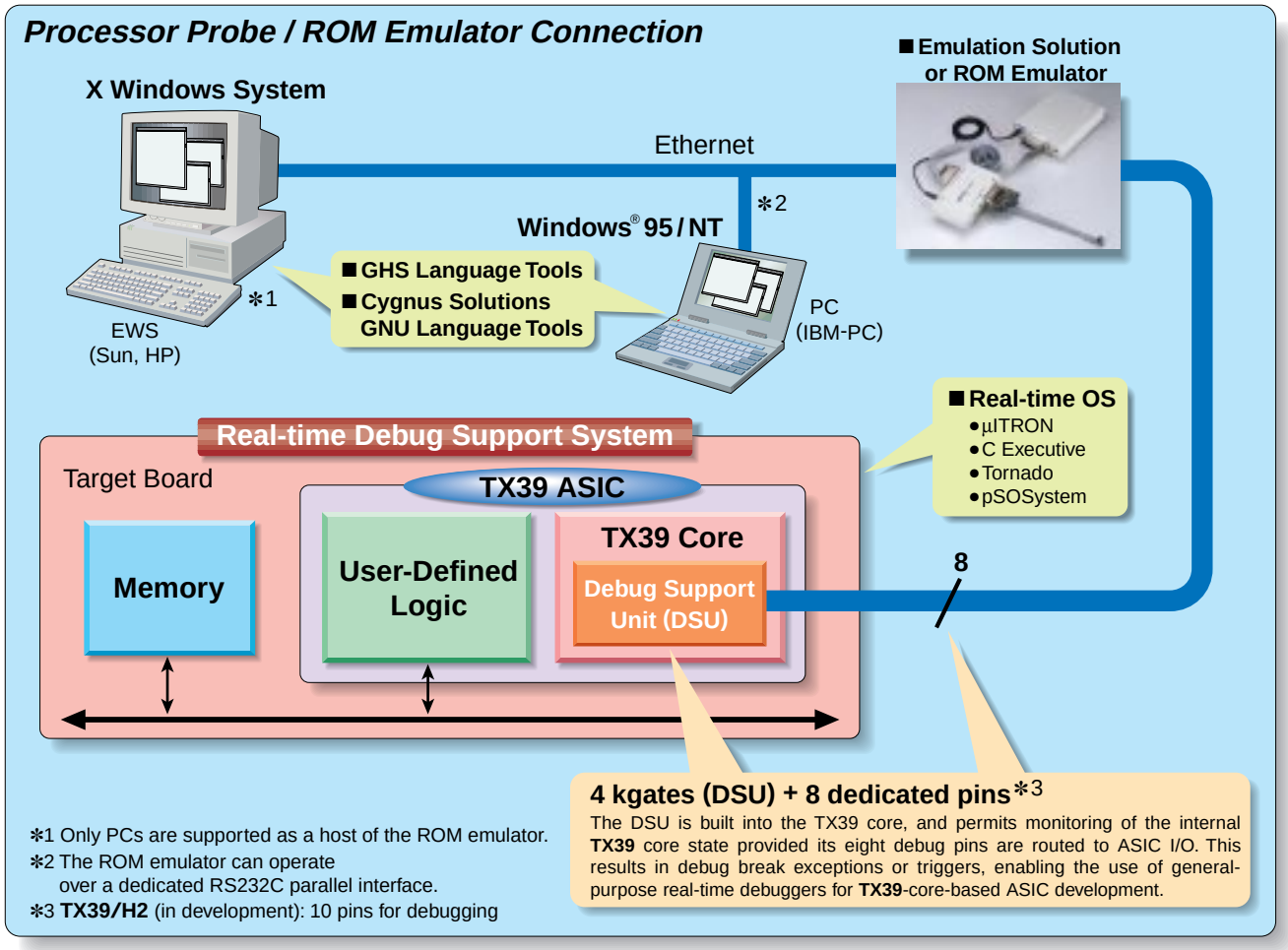


Software Development Tools for RISC ASICs

■ Software Development Environment

Exactly the same suite of tools are supported for the software development of RISC ASICs as for standard **TX family** products. To significantly reduce the time and expense of processor-based design, a wide range of powerful and consistent development tools, including compilers, debuggers, real-time operating systems, and processor probes, are available from Toshiba and several third-party development tool vendors.

Processor Probe / ROM Emulator Connection



∗1 Only PCs are supported as a host of the ROM emulator.
∗2 The ROM emulator can operate over a dedicated RS232C parallel interface.
∗3 **TX39/H2** (in development): 10 pins for debugging

Third-Party Development Tools for TX39

Real-time OS	Language Tools	Debuggers	Emulators	Monitors / Evaluation Boards
Wind River Systems, Inc. **Tornado™**	Cygnus Solutions **GNU C/C++gcc**	Cygnus Solutions **GNU Debugger**		DENSAN Systems, Inc. **DVE-R3900 DVE-R3904/20**
	Green Hills Software, Inc. **C/C++ Compiler**	Green Hills Software, Inc. **MULTI®**	Hewlett-Packard Company **E5900A, E5901A E5902A, E5903A**	
Integrated Systems, Inc. **pSOSystem®**	Integrated Systems, Inc. (Green Hills Software + MULTI [1.8.7CI]) **pRISM+**		Lightwell Co., Ltd. **MDX700**	

Third-Party Development Tools

TX39

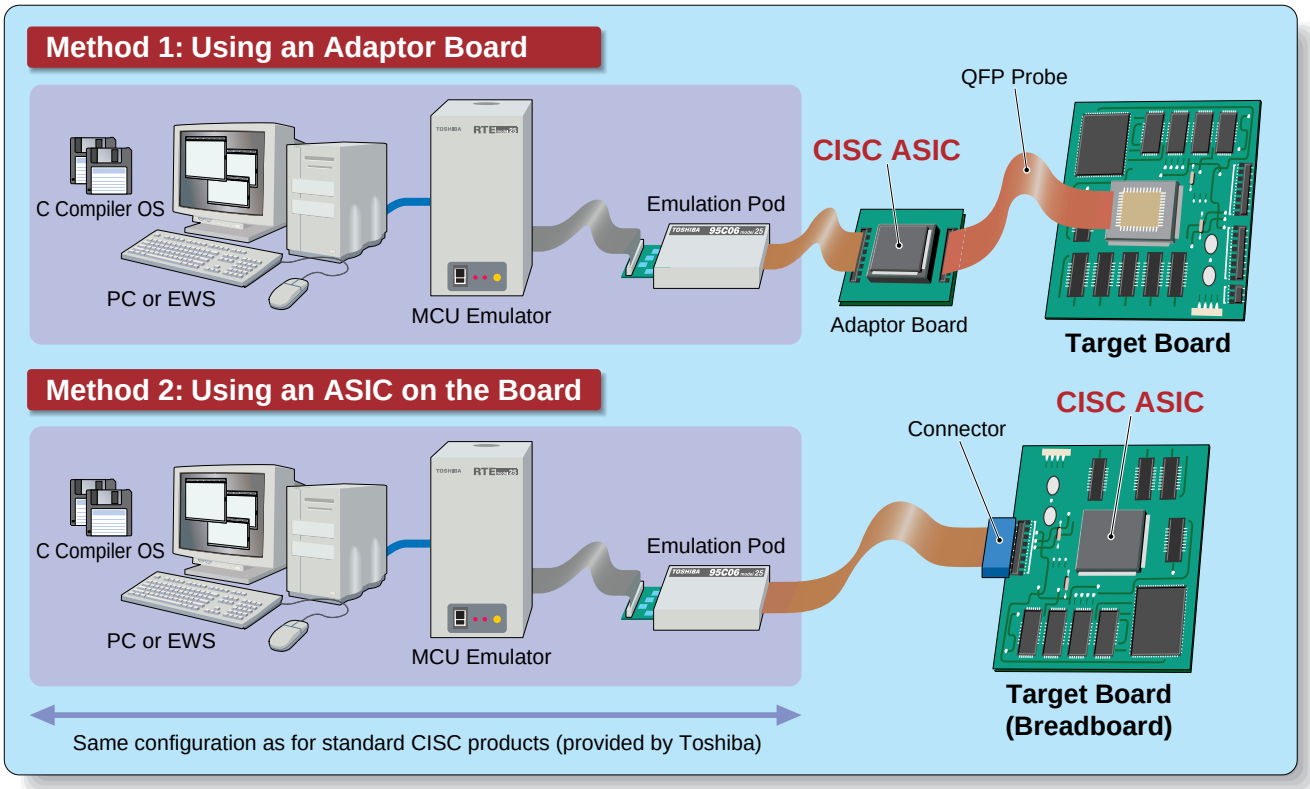
Vendor	Tool	Product Name
Green Hills Software, Inc.	Language Tool Debugger	C/C++ CROSS MIPS COMPILER MULTI®
Integrated Systems, Inc.	Real-time OS	pSOSystem®
Wind River Systems, Inc.	Real-time OS	Tornado™
DENSAN Systems, Inc.	Evaluation Board	DVE-R3904/20 DVE-R3900/20A DVE-R3900/20
Cygnus Solutions	Language Tool Debugger	GNU Pro™ Tool kit GDB
Hewlett-Packard Company	Processor Probe	HPE3492B

TX19 (Under Development)

Vendor	Tool	Product Name
Green Hills Software, Inc.	Language Tool Debugger	C/C++ CROSS MIPS COMPILER MULTI®
Integrated Systems, Inc.	Real-time OS	pSOSystem®
Cygnus Solutions	Language Tool Debugger	GNU Pro™ Tool kit GDB
Hewlett-Packard Company	Processor Probe	HP Distributed Emulation System
Yokogawa Digital Computer	In-circuit Emulator	IDB Analyzer

Software Development Tools for CSIC ASICs

Software Development Environment



Toshiba's Software Development System

TLCS-900/H

Supported MCU Product	Embedded Software Controller	Language Tool	Test Tool		
				Real-time Emulator	
				model 25	model 15
TMP95C001F	Real-time OS	Assembler, C Compiler	Debugger		

Note: For details, please consult the *Microcomputer DEVEOPMENT SYSTEM GUIDE* brochure.

Third-Party Software Development Tools

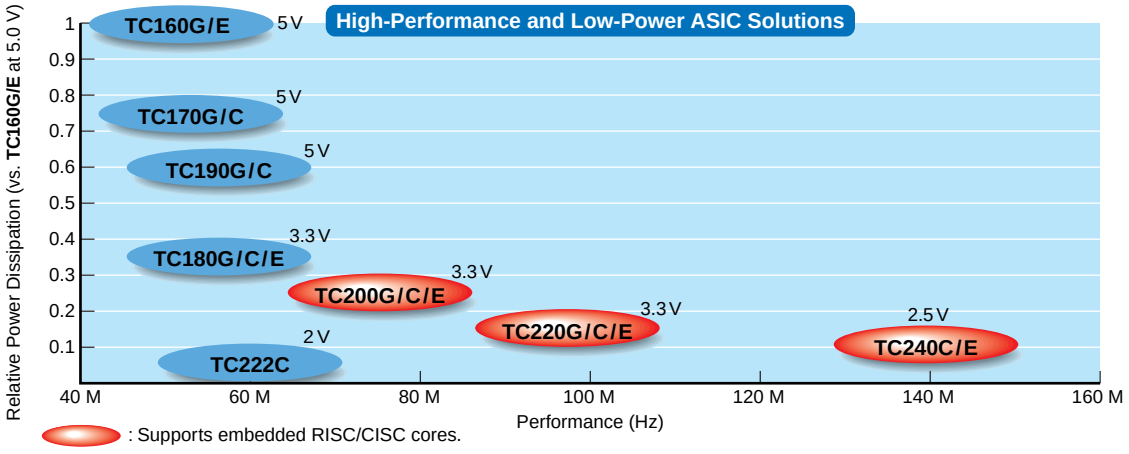
TLCS-900/H

Vendor	Tool	Product Name
IAR Systems AB	Assembler C Compiler Simulator Debugger Emulator Debugger	Development kit C-SPY/S 900
GAIO TECHNOLOGY Co., Ltd.	C Compiler ICE Debugger	XASS-V Series
Yokogawa Digital Computer	In-circuit Emulator	ADViCE

Toshiba ASIC Road Map

Toshiba ASIC Trend

In keeping with our overriding commitment to meeting customers' present and future needs, Toshiba continuously pursues new goals in the exploration of both silicon technologies and design techniques. For true system-scale integrations, ASIC silicon technologies must cover a full spectrum of application requirements with a broad range of power, density and speed solutions, complete with support of core functions and high-performance I/O.



Embedded Array Product Lines

Product Family		I/O: 3.3 V Core: 3.3 V		I/O: Mixed 3.3/5 V Core: 3.3 V	
		TC220E	TC200E	TC223E	TC203E
Process		0.3 µm	0.4 µm	0.3 µm	0.4 µm
Delay Time★	Fanout = 1	0.07 ns	0.11 ns	0.07 ns	0.11 ns
	Fanout = 2 + typical interconnect	0.15 ns	0.19 ns	0.15 ns	0.19 ns
Usable Random Gates		1.9 M	704 k	193 k	694 k
I/O Pads	Wirebond	512	512	504	504
	TAB	768	776	768	768
Power Dissipation★★		0.65 µW	1.14 µW	0.65 µW	1.14 µW
Masterslices		38	39	40	38

★: High-drive 2-input NAND gate
★★: µW/gate/MHz (3.3 or 5 V), 2-input NAND, fanout = 1

Cell-Based IC Product Lines

Product Family		I/O: 3.3 V Core: 3.3 V		I/O: Mixed 3.3/5 V Core: 3.3 V	
		TC220C	TC200C	TC223C	TC203C
Process		0.3 µm	0.4 µm	0.3 µm	0.4 µm
Delay Time★	Fanout = 1	0.06 ns	0.10 ns	0.06 ns	0.10 ns
	Fanout = 2 + typical interconnect	0.14 ns	0.17 ns	0.14 ns	0.17 ns
Usable Random Gates		2.1 M	729 k	2.1 M	718 k
I/O Pads	Wirebond	512	512	504	504
	TAB	768	768	768	768
Power Dissipation★★	ND2 (Fanout = 1)	0.41 µW	0.91 µW	0.41 µW	0.91 µW
	ND2R (Fanout = 1)	0.24 µW	0.48 µW	0.24 µW	0.48 µW
Masterslices		40	39	40	38

★: High-drive 2-input NAND gate
★★: µW/gate/MHz (2, 3.3, or 5 V), ND2: 2-input NAND, NR2R: Low-power 2-input NAND

Note: The above tables give only the product families supporting embedded RISC and CISC cores.

TC240 Family Product Summary

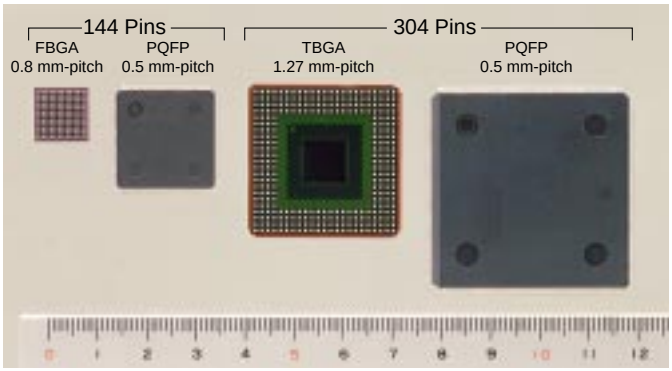
Process Technology		0.25 µm						
		HC2MOS Si-gate five layer metal						
Series		Embedded Arrays			Cell-Based IC			
Maximum Usable Gates★ (with four metals)		8.8 Mgates			10.2 Mgates			
Cell Name★★		GND2X1	GND2X2	GND2X4	CND2XL	CND2X1	CND2X2	CND2X4
Delay Time (ps)	Fanout = 1	77	68	61	87	70	55	54
	Fanout = 1 + typical interconnect	141	101	79	218	118	83	68
Power Dissipation (µW/MHz, Fanout = 1)		0.156	0.270	0.487	0.107	0.170	0.296	0.563
Operating Voltage		Core: 2.5 V I/O: 2.5 V/3.3 V						

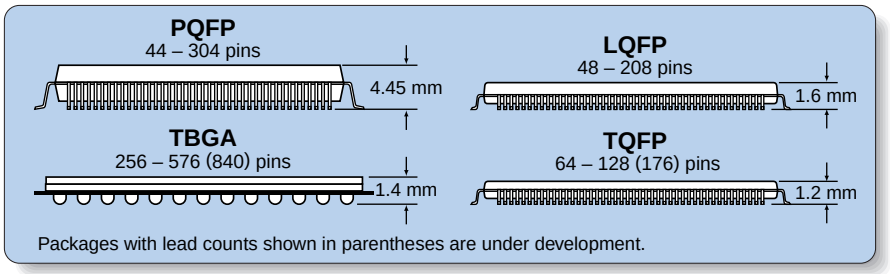
★: Depends on design configurations.
★★: ❑ND2X1: 2-input NAND gate, ×1 drive ❑ND2X2: 2-input NAND gate, ×2 drive ❑ND2X4: 2-input NAND gate, ×4 drive ❑ND2XL: 2-input NAND gate, ×1/2 drive

Packaging

High-Density Packages

BGAs provide the highest I/O-to-body-size ratio, with solder balls formed on the bottom in an area array format and a ball pitch of 1.27 or 0.8 mm. In spite of increased ball pitches, BGAs result in smaller footprints than PQFPs. The photo at right shows an FBGA and a TBGA, in contrast to PQFPs with the same lead counts. Formally known as chip scale packages (CSPs), the fine-pitch BGA (FBGA) is generally defined as having a package body size no larger than 1.2 times the die size. Tape BGA (TBGA) packages support ultra-high pin count applications. TBGAs combine the fine die pad pitch interconnect advantages of TAB with the assembly ease of BGAs. The center balls of the TBGA is depopulated to allow room for the face-down TAB bonded and encapsulated die.





Thin and Light Packages

LQFP and TQFP packages provide a thin, lightweight surface mount solution to system miniaturization. The package height is 1.4 mm (seating height = 1.6 mm) for the LQFP lines and 1.0 mm (seating height = 1.2 mm) for the ultra-thin TQFP lines. Also, TBGAs support both the low-profile and ultra-high-pin-count requirements. With their excellent heat dissipation, low profile, and low cost, TBGAs can handle a wide variety of applications.

Lead Count Chart

Package Family	# I/O / Lead Pitch	100	200	300	400	500	600	700	800	900
TBGA	1.27 mm			256	304	352	420	480	576	
	1.0 mm				336	400	480	560	648	768
	0.8 mm					432	520	620	720	840
PBGA	1.5 – 1.27 mm			225	256					
PFBGA (CSP)	0.8 mm	85 97 109	141 145	169 177 181 201 205 217 241	301					
	0.5 mm			177	209 241 273 305	337				
LQFP	0.5 mm	48 64 80 100		144	176					
	0.4 mm	64	100 120	144						
LQFP [Cu]	0.5 mm		128	144	176	208				
	0.4 mm			176	216	256				
TQFP	0.5 mm	64 80 100								
	0.4 mm		100 120 128							
TQFP [Cu]	0.5 mm			144						
	0.4 mm			144	176					
PQFP	1.0 mm	R64								
	0.8 mm	44 60 R80 100	120							
	0.65 mm	R100		144 160	184					
	0.5 mm	100		144	176	208	240	304		
PQFP [Cu]	0.65 – 0.5 mm			160	208					
PQFP [TAB/Cu]	0.5 – 0.4 mm				208	240 256	304			
HQFP	0.65 mm			160	184					
	0.5 mm				208	240				
	0.4 mm						296			
CQFP	0.8 mm		100	120						
	0.65 mm			144 160	184					
	0.5 mm			176	208	240	304			
CQFP [AℓN]	0.65 mm			160						
	0.5 mm				208	240	304			
CPGA	2.54 mm	64 69 85 101	121	145	181	225				
CPGA [CD]	2.54 mm			155	223	299				
	1.27 mm						391			

Not all die sizes are available with all packaging options. When your need for an ASIC arises, please contact the nearest ASIC service group.

● : Available ■ : In Development ▲ : Planned

Toshiba Documents

Brochures

- CMOS ASICs Product Guide
- ASIC Packaging
- 32-Bit TX System RISC TX19 Family
- 32-Bit TX System RISC TX39 Family
- 64-Bit TX System RISC TX49 Family
- Microcomputers Product Guide
- Microcomputer Development System Guide

TX39

- 32-Bit RISC Microprocessor TLCS-R3900 Family (Architecture TMPR3901F)
- 32-Bit TX System RISC TX39 Family User's Manual (Hardware)
- 32-Bit TX System RISC TX39 ASIC Design Guide

TX19

- 32-Bit TX System RISC TX19 User's Manual (Architecture)

TX49

- 64-Bit RISC Microprocessor TX49 User's Manual

TLCS-900/H and TLCS-900/L1

- 16-Bit Microcontroller TLCS-900/H Series User's Manual (1)
- Development System Manual (ASSEMBLER)
- Development System Manual (C COMPILER)
- Microcomputer Development System Real-time OS (User's Manual)
- 16-Bit Microcontroller TLCS-900/H, TLCS-900/L APPLICATION NOTE

Design Handbooks

- User's manuals for various EDA tools
- CMOS ASIC Design Manual
- Design-for-Test Handbook
- ASIC Packaging

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