

TOSHIBA

ASICs with Embedded DRAM

PRODUCT GUIDE

Embedded DRAM Cores

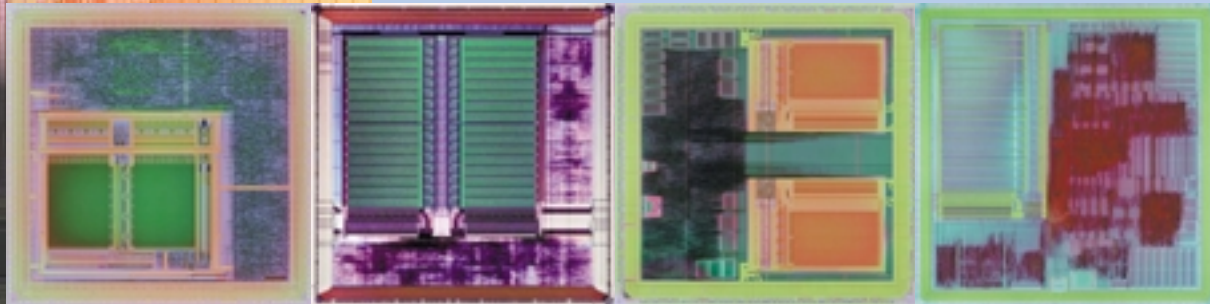
SLI ASICs with Embedded DRAM for High-Performance, High-Density and Low-Power Applications

The ever-increasing ASIC complexity and the drive for system-level integration (SLI) demand the capability to integrate memory blocks, IP cores and random logic on a single chip. We see embedded DRAM as one of the essential technologies for next-generation products. With its differentiating memory capabilities, Toshiba has a proven track record in ASICs with embedded DRAM.

Embedded DRAMs technology integrate traditional DRAM with digital logic on the same chip. Such integration offers the following features and benefits:

- **Excellent DRAM core granularity and bus width flexibility**
- **High bandwidth due to wide and fast memory buses**
- **Low power dissipation due to low-capacitance on-chip connections**
- **Optimal sizing of the DRAM core using a DRAM generator**
- **Discrete-type DRAM test strategy and redundancy in the DRAM core**

The performance and density characteristics of Toshiba's Embedded DRAM hits the sweet spot of today's digital communication, networking and graphics applications and is also ideal for portable equipment that requires low power dissipation with a small silicon footprint.



DRAM Core Features

Trench Process

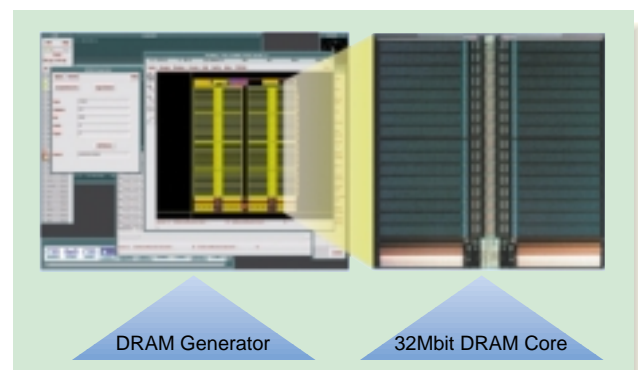
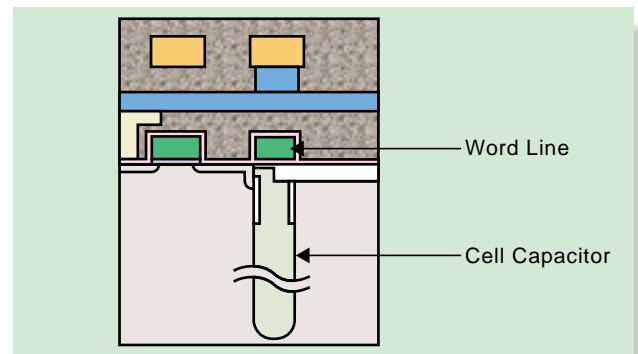
The one-transistor (1T) DRAM cell structure utilizes the same renowned trench process as employed in Toshiba's advanced discrete DRAMs. The trench capacitor, which is formed beneath the surface of the silicon, requires no additional manufacturing steps between the gate and metal. This allows for a planar surface topology that enhances reliability without compromising logic performance.

High Bandwidth

For wide-buses with discrete DRAMs, the large number of pins and packages can be a challenge for both system designers and manufacturing, and power dissipation can be a problem. Freed from these I/O restrictions, embedded DRAM cores provide high memory bandwidth with a synchronous interface and a bus width selectable from 64, 128 and 256 bits.

DRAM Generator

The DRAM Generator automatically constructs fully assembled DRAMs from user-supplied high-level parameters, enabling accurate sizing of the amount of DRAM required in a particular application. The DRAM Generator also generates a timing model in Verilog or VHDL format and Design Compiler format.



DRAM Cores for the TC260 Family

TC260

DRAM cores are offered for use in system-level integration (SLI) ASICs based on the 0.14-micron TC260E embedded array and TC260C cell-based ASIC families. ASICs with combined logic and DRAM are implemented in TC260E/C embedded DRAM technology; however, designers use the same logic libraries as TC260E/C pure logic technology, without degrading any performance.

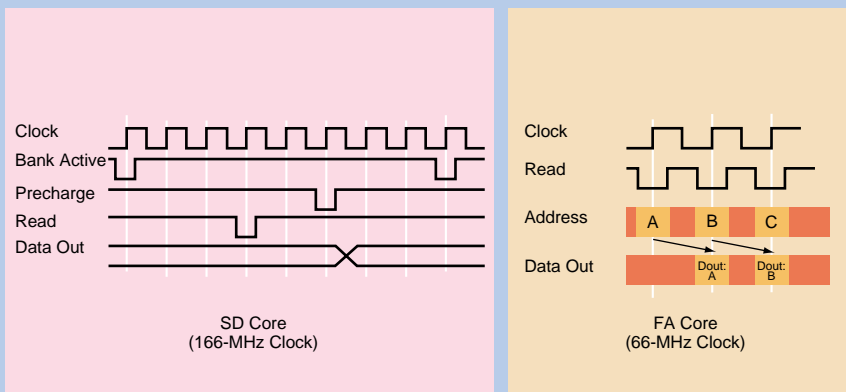
The TC260 offers two types of DRAM cores.

1 Standard Synchronous DRAM (SD) Cores

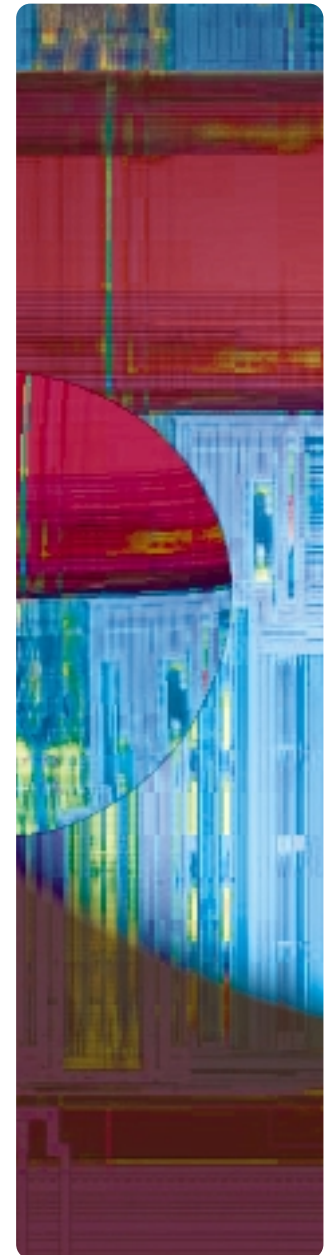
The SD cores are specified in densities ranging from 2 Mb to 32Mb and are capable of operating at frequencies up to 180 MHz. These cores are targeted for applications requiring fast page-mode accesses or large memory blocks.

2 Fast-Access (FA) Cores

The FA cores are intended for smaller memory applications while supporting a clock cycle period of only 12 to 15 ns for random accesses. These cores are ideal for applications requiring very fast random accesses.



Type	SD	FA
Characteristic		
Access Time	48 ns	12-15 ns
Max Clock Frequency	180 MHz	—
Memory Capacity	2 Mb to 32 Mb	2 Mb, 4 Mb, 8 Mb



DRAM Cores for the TC240 Family

TC240D



DRAM cores are also offered for use in ASICs based on the 0.25-micron TC240 family. Both SD and FA cores are available.

Type	SD	FA
Characteristic		
Access Time	69 ns	40 ns
Max Clock Frequency	166 MHz	100 MHz
Memory Capacity	2 Mb to 32 Mb	4 Mb to 16 Mb

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**Toshiba America
Electronic Components, Inc.**

Headquarters-Irvine, CA
9775 Toledo Way, Irvine, CA 92618, U.S.A.
Tel: (949)455-2000 Fax: (949)859-3963

Boulder, CO
3100 Arapahoe Avenue, Ste. 500,
Boulder, CO 80303, U.S.A.
Tel: (303)442-3801 Fax: (303)442-7216

Boynton Beach, FL(Orlando)
11924 W. Forest Hill Blvd., Ste. 22-337,
Boynton Beach, FL 33414, U.S.A.
Tel: (561)374-6193 Fax: (561)374-6194

Deerfield, IL(Chicago)
One Pkwy., North, Suite 500, Deerfield,
IL 60015-2547, U.S.A.
Tel: (847)945-1500 Fax: (847)945-1044

Duluth, GA(Atlanta)
3700 Crestwood Parkway, Ste. 460,
Duluth, GA 30096, U.S.A.
Tel: (770)931-3363 Fax: (770)931-7602

Edison, NJ
2035 Lincoln Hwy. Ste. #3000, Edison
NJ 08817, U.S.A.
Tel: (732)248-8070 Fax: (732)248-8030

Orange County, CA
2 Venture Plaza, #500 Irvine, CA 92618, U.S.A.
Tel: (949)453-0224 Fax: (949)453-0125

Portland, OR
1700 NW 167th Place, #240,
Beaverton, OR 97006, U.S.A.
Tel: (503)629-0818 Fax: (503)629-0827

Raleigh, NC
5511 Capitol Center Dr., #114,
Raleigh, NC 27606, U.S.A.
Tel: (919)859-2800 Fax: (919)859-2898

Richardson, TX(Dallas)
777 East Campbell Rd., Suite 650, Richardson,
TX 75081, U.S.A.
Tel: (972)480-0470 Fax: (972)235-4114

San Jose Engineering Center, CA
1060 Rincon Circle, San Jose, CA 95131, U.S.A.
Tel: (408)526-2400 Fax: (408)526-2410

Wakefield, MA(Boston)
401 Edgewater Place, Suite #360, Wakefield,
MA 01880-6229, U.S.A.
Tel: (781)224-0074 Fax: (781)224-1095

Toshiba Do Brasil S.A.

Electronic Components Div.
Estrada Dos Alvarengas, 5. 500-Bairro Alvarenga
09850-550-Sao Bernardo do campo - SP
Tel: (011)7689-7171 Fax: (011)7689-7189

Toshiba Electronics Europe GmbH
Düsseldorf Head Office
Hansaallee 181, D-40549 Düsseldorf
Germany
Tel: (0211)5296-0 Fax: (0211)5296-400

München Office
Büro München Hofmannstrasse 52,
D-81378, München, Germany
Tel: (089)748595-0 Fax: (089)748595-42

Toshiba Electronics France SARL
Immeuble Robert Schumann 3 Rue de Rome,
F-93561, Rosny-Sous-Bois, Cedex, France
Tel: (1)48-12-48-12 Fax: (1)48-94-51-15

Toshiba Electronics Italiana S.R.L.
Centro Direzionale Colleoni
Palazzo Perseo Ingr. 2-Piano 6,
Via Paracelso n.12,
1-20041 Agrate Brianza Milan, Italy
Tel: (039)68701 Fax: (039)6870205

Toshiba Electronics España, S.A.
Parque Empresarial San Fernando Edificio Europa,
1ª Planta, ES-28831 Madrid, Spain
Tel: (91)660-6700 Fax: (91)660-6799

Toshiba Electronics(UK) Limited
Riverside Way, Camberley Surrey,
GU15 3YA, U.K.
Tel: (01276)69-4600 Fax: (01276)69-4800

Toshiba Electronics Scandinavia AB
Gustavslundsvägen 12, 2nd Floor
S-161 15 Bromma, Sweden
Tel: (08)704-0900 Fax: (08)80-8459

**Toshiba Electronics Asia
(Singapore) Pte. Ltd.**
Singapore Head Office
438B Alexandra Road, #06-08/12 Alexandra
Technopark, Singapore 119968
Tel: (278)5252 Fax: (271)5155

Bangkok Office
135 Moo 5 Bangkok Industrial Park, Tivanon Rd.,
Bangkadi Amphur Muang Pathumthani, Bangkok, 12000,
Thailand
Tel: (02)501-1635 Fax: (02)501-1638

**Toshiba Electronics Trading
(Malaysia) Sdn. Bhd.**
Kuala Lumpur Head Office
Suite W1203, Wisma Consplant, No.2,
Jalan SS 16/4, Subang Jaya, 47500 Petaling Jaya,
Selangor Darul Ehsan, Malaysia
Tel: (3)731-6311 Fax: (3)731-6307

Penang Office
Suite 13-1, 13th Floor, Menard Penang Garden,
42-A, Jalan Sultan Ahmad Shah,
100 50 Penang, Malaysia
Tel: 4-226-8523 Fax: 4-226-8515

Toshiba Electronics Philippines, Inc.
26th Floor, Citibank Tower, Valero Street, Makati,
Manila, Philippines
Tel: (02)750-5510 Fax: (02)750-5511

Toshiba Electronics Asia, Ltd.

Hong Kong Head Office
Level 11, Top Glory Insurance Building, Grand Century
Place, No.193, Prince Edward Road West,
Mong Kok, Kowloon, Hong Kong
Tel: 2375-6111 Fax: 2375-0969

Beijing Office
Rm 714, Beijing Fortune Building,
No.5 Dong San Huan Bei-Lu, Chao Yang District,
Beijing, 100004, China
Tel: (010)6590-8795 Fax: (010)6590-8791

Chengdu Office
Unit F, 18th Floor, New Times Plaza, 42 Wenwu Road,
Xinhua Avenue, Chengdu, 610017, China
Tel: (028)675-1773 Fax: (028)675-1065

Shenzhen Office
Rm 3010-3012, Office Tower Shun Hing Square,
Di Wang Commercial Centre, 333 ShenNan
East Road, Shenzhen, 518008, China
Tel: (0755)246-1582 Fax: (0755)246-1581

Toshiba Electronics Korea Corporation

Seoul Head Office
14/F, KEC B/D, 257-7 Yangjae-Dong,
Seocho-ku, Seoul, Korea
Tel: (02)589-4334 Fax: (02)589-4302

Gumi Office
6/F, Ssangyong Investment Securities B/D,
56 Songjung-Dong, Gumi City
Kyeongbuk, Korea
Tel: (82)54-456-7613 Fax: (82)54-456-7617

**Toshiba Technology Development
(Shanghai) Co., Ltd.**

23F, Shanghai Senmao International Building, 101
Yin Cheng East Road, Pudong New Area, Shanghai,
200120, China
Tel: (021)6841-0666 Fax: (021)6841-5002

**Tsurong Xiamen Xiangyu Trading
Co., Ltd.**

8N, Xiamen SEZ Bonded Goods Market Building,
Xiamen, Fujian, 361006, China
Tel: (0592)562-3798 Fax: (0592)562-3799

**Toshiba Electronics Taiwan
Corporation**

Taipei Head Office
17F, Union Enterprise Plaza Bldg. 109
Min Sheng East Rd., Section 3, 0446 Taipei,
Taiwan
Tel: (02)514-9988 Fax: (02)514-7892

Kaohsiung Office
16F-A, Chung-Cheng Bldg., Chung-Cheng 3Rd.,
80027, Kaohsiung, Taiwan
Tel: (07)222-0826 Fax: (07)223-0046

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In Touch with Tomorrow
TOSHIBA

TOSHIBA CORPORATION

Electronic Devices Sales & Marketing Division
1-1, Shibaura 1-chome, Minato-ku, Tokyo, 105-8001, Japan
Tel: +81-3-3457-3405 Fax: +81-3-5444-9431