TOSHIBA

0.25 µm CMOS ASIC TC240 Families

NEW PRODUCT GUIDE

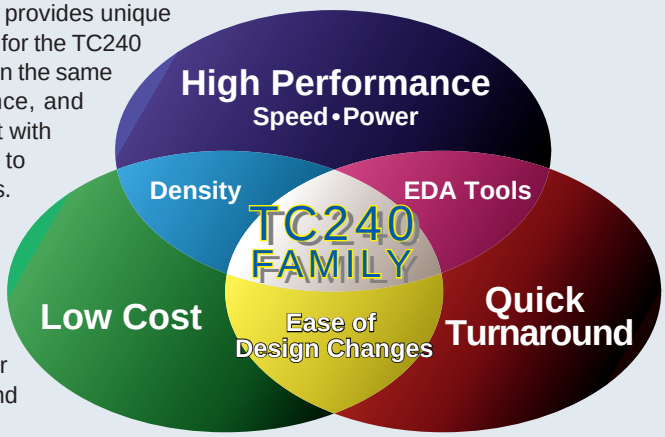
System ASIC Solution TC240 Family

Fabricated on an advanced 0.25-micron process, the TC240 family provides unique capabilities for systems-on-a-chip. The “unified cell architecture” created for the TC240 family allows you to mix gate-array-based logic and cell-based functions in the same design, providing an optimal balance of chip cost, silicon performance, and development time. The TC240 family offers a gallery of cores compliant with Virtual Socket Interface (VSI). In addition, the TC240 family allows you to create a logic design and later port it to a merged DRAM-on-logic process.

Toshiba makes available to you all tools needed for multi-million-gate designs. Encompassing Toshiba's adaptable EDA highlights are static-timing-analysis sign-off and hierarchical designs methodologies. Compliers and debuggers are being totally revamped for microprocessor-based designs.

The TC240 package offerings include a wide range of solutions for every system application, including high-pin-count, high-performance, and high-density packages.

For true system-scale integration, the TC240 family covers a full spectrum of application requirements with a broad range of power, density, and speed solutions, complete with core function and high-performance I/O support.



Key Features

0.25-Micron, 5-Metal Layer Process

The TC240 family is fabricated on a 0.25-micron five-layer stacked-via metal CMOS process, with the world's narrowest line pitch and shallow trench isolation. This new process yields 10 million-plus maximum usable gates — an approximately 3 times gate density improvement compared to the previous generation technology.

Ultra-Fast Speed

The TC240 family features the use of salicide on the gate to reduce parasitic resistance and capacitance. Coupled with an effective channel length of 0.18 micron, this gives rise to a 20 percent speed improvement over the previous generation technology.

Low Power Dissipation

The TC240 family is optimized for low 2.5 V, a de facto industry standard with a quarter-micron technology, reducing power dissipation by 45 percent compared to the existing 3.3-V products. Unique circuit optimization techniques employed during both logic synthesis and physical layout can deliver up to 60 percent reduction in power dissipation (Fig. 1). For best results, four or more drive-strength variations of macrocells are available, allowing the optimal tuning of performance and power. While tailored to run at 2.5 V, the TC240 family gives you a flexibility with your system interface design by offering an optional 3.3-V I/O interfacing.

High I/O Counts

A migration from peripheral leads to an area array format is necessary to achieve reasonable package sizes and silicon/package electrical performance requirements for system chips. With the TC240 family, four of the five metal layers are used for interconnects; the fifth (or the uppermost) is reserved for full-area bonding pad array for flip-chip interconnects. Designs with over 500 I/Os can be captured on a small die (Fig. 2). Flip-chip BGAs are also offered for easy attachment to a circuit board.

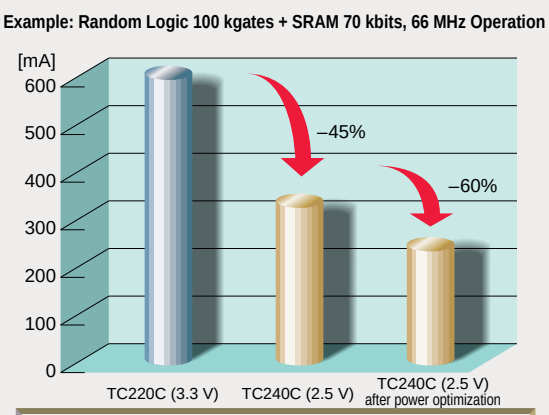


Fig. 1 Power Comparison (TC220C vs. TC240C)

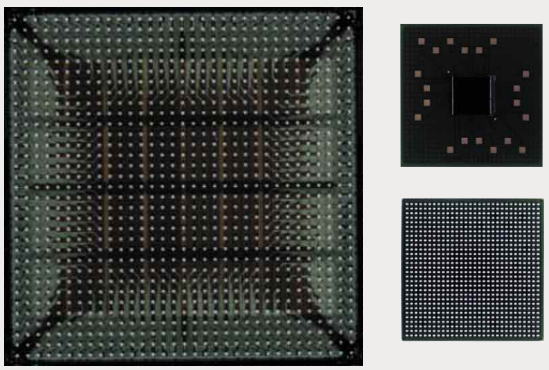


Fig. 2 Area Array Flip-Chip and BGA900

Product Summary

Process Technology		0.25 μm HC²MOS Si-gate five layer metal						
Series		Gate Arrays & Embedded Arrays			Cell-Based ICs			
Maximum Usable Gates*1 (with four metals)		10 Mgates			12 Mgates			
Delay Time (ps)	Cell Name*2	GND2X1	GND2X2	GND2X4	CND2XL	CND2X1	CND2X2	CND2X4
	Fanout=1	77	68	61	87	70	55	54
	Fanout=1+Typical Interconnect	141	101	79	218	118	83	68
Power Dissipation (μW/MHz, Fanout=1)		0.156	0.270	0.487	0.107	0.170	0.296	0.563
Operating Voltage		Core: 2.5 V I/Os: 2.5 V/3.3 V						

*1 Depends on design configurations.
*2 □ND2 X 1: 2-input NAND gate, 1x drive
□ND2 X 2: 2-input NAND gate, 2x drive
□ND2 X 4: 2-input NAND gate, 4x drive
□ND2 X L: 2-input NAND gate, 1/2x drive

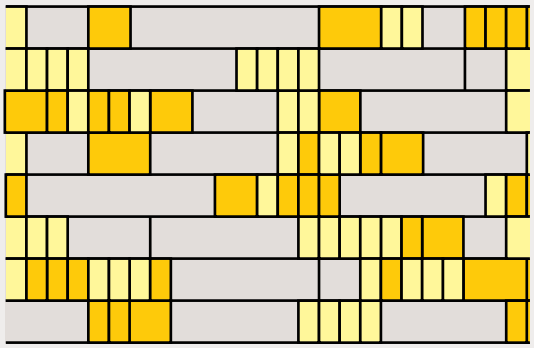
Unified Cell Architecture

Recently, with the markedly increasing levels of integration, specialized large functions such as embedded cores have become indispensable. Thus cell-based ICs have come to command a larger proportion of ASIC business.

However, the move to the quarter-micron generation brings with it not only greater chip densities and higher speed but higher costs and longer turnaround times, mostly due to photomask creation. This equates to greater risks as well. Furthermore, even with the advancement of EDA technologies, designing multi-million-gate designs require several synthesis-layout iterations. Each iteration can be time-consuming and costly. Even when you want to implement only small design changes, a full mask set need be recreated with the cell-based IC technology.

To eliminate this bottleneck, Toshiba created a “unified cell architecture” for embedded arrays. This new architecture uses the same cell height and routing grid structure for gate arrays as it does for cell-based ICs. This enables the designer to mix gate-array-based logic with cell-based functions in the same chip. Implemented in the unified cell architecture, small cells like 2-input NAND gates do not exhibit noticeable differences between gate arrays and cell-based ICs in terms of size and electrical characteristics. In addition, gate array cells can fill all open sites after cores are placed. This creates a block of uncommitted cells fabricated in gate array technology within cell-based ICs. Consequently, the designer can create a bug fix with gate array lead times and costs, because only the metal interconnect masks need be redefined.

Toshiba has teamed with In-Chip Systems, Inc. (Los Altos, Calif.) to offer the new NXT gate array cell architecture. The NXT architecture features low power dissipation and a dramatically increased percentage of routable cells per mm2.



Gate array macrocells
Replace functionally-equivalent cell-based IC cells.

Gate array basic cells
Fill open sites where cells can not be placed due to metal interconnects.

Cell-based IC primitive cells

Normally, with cell-based IC technology, a full mask set need be recreated to make even a few design changes. However, the unified cell architecture of the TC240 family makes it possible to implement gate-array-based engineering change orders (ECOs) in cell-based ICs. ECOs can be done at the final metallization stage in as short a time as embedded arrays can offer.

Quick-Turn ECOs on Cell-Based ICs

Fig. 3 Unified Cell Architecture

Toshiba EDA Environment

To make it easier to take full advantage of Toshiba's world-class silicon capabilities, we have gone to extraordinary lengths to make the Toshiba EDA environment a flexible, adaptable environment. Now the "static sign-off" or the ability to sign off on synchronous designs based on static timing analysis allows you to ensure exhaustive timing coverage while using timing simulation to execute a more focused functional verification. For mega-plus-gate designs, hierarchical design methodologies including RTL floorplanning are essential. Also among Toshiba's adaptable EDA highlights are power optimization at several stages of design, <100-ps skew clock tree synthesis, timing-driven layout, and so on.

For system ASICs with an on-chip microprocessor, compilers, debuggers, and emulators are being improved. In April 1997, Toshiba created the Computer on Silicon (COS) business unit to focus on service and software issues for system ASICs. Toshiba also provides middleware products to ease development of video, audio, communication, and other applications. In addition, Toshiba is working on hardware/software codesign tools.

RTL Floorplanners

Designs are floorplanned at the RTL level before the RTL code is synthesized into gate-level logic. RTL floorplanners can extract design constraints to drive logic synthesis.

Using Floorplanners with Synthesis

If logic simulation reveals any design errors, you must rework your design. You can use a logic synthesis tool to make minor design changes. You can then execute an ECO placement in the floorplanner to make incremental changes to the floorplan/placement.

Pre-Layout Logic Simulation

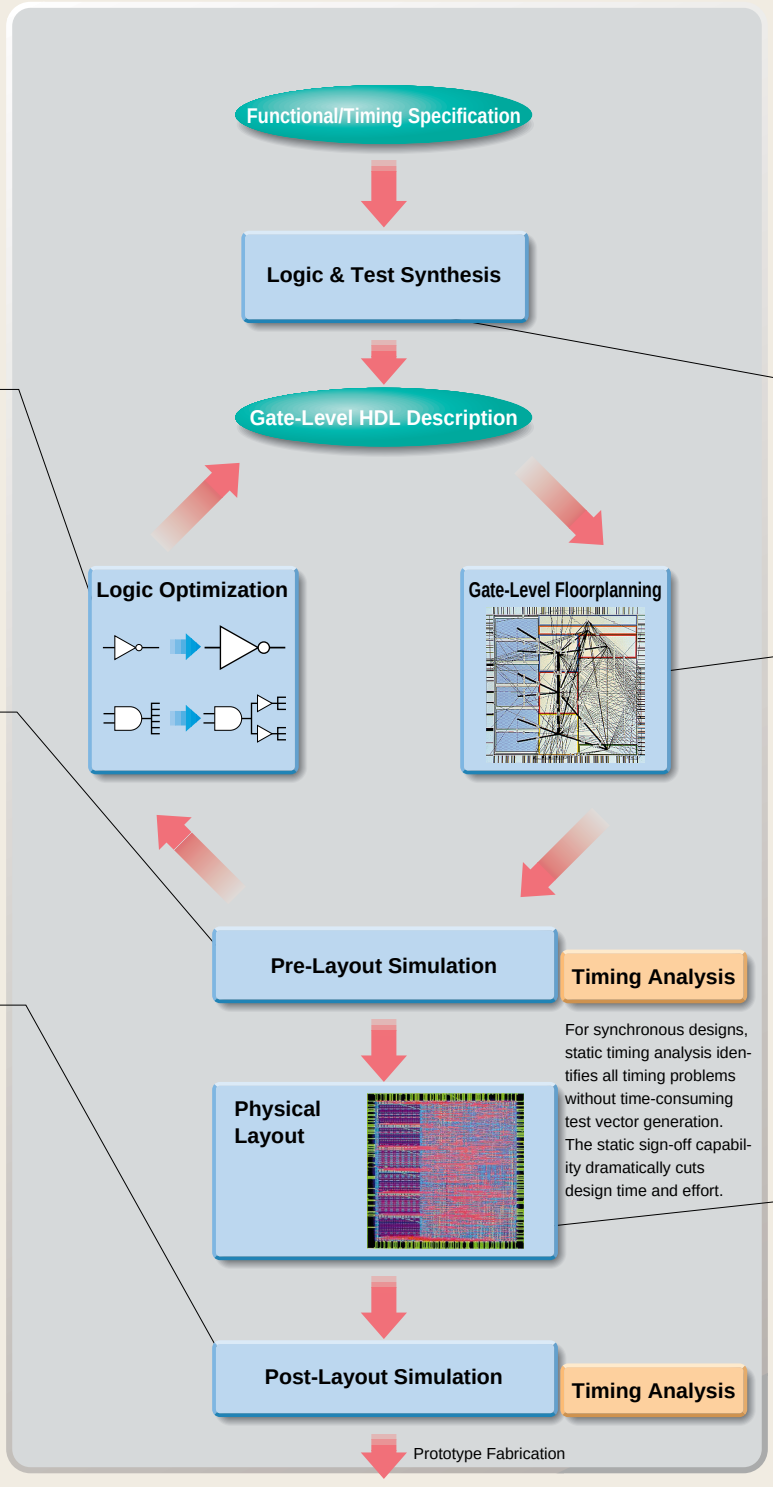
You can forward-annotate more accurate delay information derived from a floorplanner to pre-route simulation. The timing accuracy obtained on a basis of a floorplan/placement minimizes design iterations. If the result of pre-layout simulation is satisfactory, you sign off the circuit, releasing it physical layout.

Post-Layout Logic Simulation

The final delay values are recalculated based on the actual physical layout, and the design is re-simulated. If the post-layout simulation shows that your design performs correctly, you sign off the circuit, authorizing commencement of mask tooling.

Hierarchical Design

For large, complex circuits, hierarchical design methodologies are used. Designs are created, floorplanned, and simulated on a block-by-block basis from the initial stage of development. Finally, each one of the blocks is placed and routed separately and then the blocks are interconnected, taking chip-level timing constraints into account.



Hardware/Software Codesign

The hardware/software codesign environment allows testing of hardware and software together before prototypes are built, providing significant reductions in time-to-market and cost for processor-based systems.

Logic & Test Synthesis

You can take advantage of a top-down approach that starts at a high level of abstraction and moves to lower levels as more design details are made available. Test structures can be synthesized into a circuit concurrently.

Floorplanning

Front-end floorplanners enable you to obtain accurate timing estimates and chip routability measures up front, without getting involved in a "full" placement-and-routing.

Timing Analysis

For synchronous designs, static timing analysis identifies all timing problems without time-consuming test vector generation. The static sign-off capability dramatically cuts design time and effort.

Physical Layout

Physical layout consists of placing macros on a plot of the selected array and then routing interconnect between logic elements and to the I/O pads. Physical layout provides actual net loads, resistance, and pin-to-pin connect delays.

Power Optimization

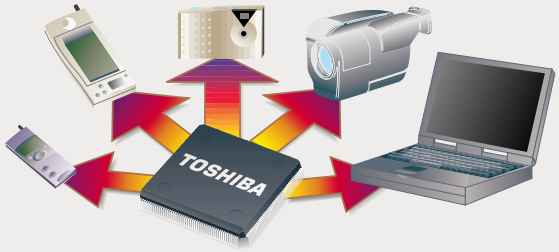
Power optimization techniques are employed at several design steps. Logic synthesis features simultaneous optimization for timing, area, and power. Power-driven layout fine-tunes both timing and power so that the result is the lowest power implementation permitted by the timing constraints on the design.

TC240 Boosts Systems-on-a-Chip Integration

Increasing Need for System Chips

The race is on among electronics manufacturers to roll out multimedia products that capture and present information in a combination of text, graphics, video, animation, and sound. Multimedia chips demand ever increasing levels of performance, versatility, and functionality. At the same time, markets are expanding for such portable products as palmtop PCs, personal digital assistants (PDAs), digital still cameras, digital camcorders, automobile navigation systems, and cellular phones. This trend is creating a demand for longer battery life and increased mobility.

The high-density and lower-power features of the TC240 family are essential elements for the success of advanced designs for system ASICs.

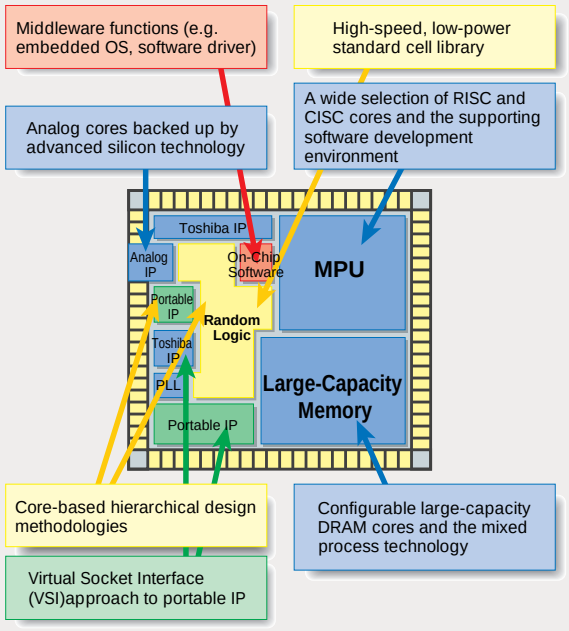


A Gallery of Cores

Typical system chips integrate a wide variety of functions. To meet the challenges of system chips, ASIC core libraries must include a whole suite of core functions such as microprocessor cores, large-capacity memory cores, and many hardware intellectual-property (IP) functions. In addition, system chips may also require soft (or synthe-sizable) IP cores that implement embedded OSes, middleware functions, and software drivers.

Access to a wide range of advanced system building blocks and the supporting infrastructure are the key to the success of system ASICs. An abbreviated list of cores in development for implementation in the TC240 family include:

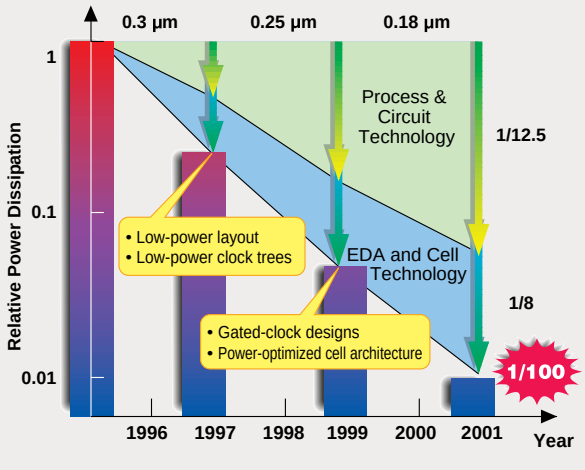
- TX System RISC processor cores (MIPS RISC cores)
- Toshiba-original CISC controller cores
- Media compression/decompression cores
- Network/communication cores
- Protocol controller cores
- Analog cores
- DRAM cores
- I/O interface cores



Low Power Technology

The benefits of high integration can only be appreciated if power dissipation is reduced. The need for power reduction is increasingly acute as portable products become more commonplace. Power minimization is of utmost importance since customers of these products rank long battery life at the top of their feature preferences. Power dissipation problems also arise due to the ever increasing complexity of ASIC designs. Power-hungry chips may weight down ASIC and system designs because of overheating issues.

In October 1995, Toshiba launched the 100x Power Savings Project. The roadmap seeks to reduce power dissipation to one-hundredth within this century. The project consists of two working parties, one putting an emphasis on finer- and lower-power processes and advanced circuit architectures, and the other on more efficient EDA tools and new design optimization techniques.



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