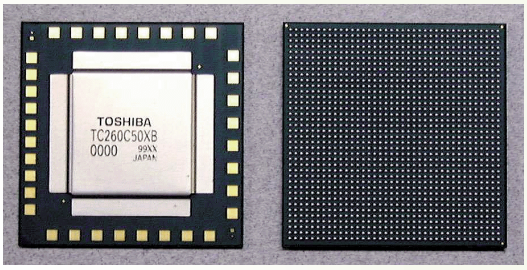
TOSHIBA

0.14μm CMOS ASIC TC260 Family

PRODUCT GUIDE

SLI ASIC for High-Function, Low-Power Applications

TC260 Family



The TC260 family of System-Level Integration (SLI) ASICs are designed for applications needing the highest performance with the smallest die size and lowest power. The family includes TC260C cell-based ICs for best density and TC260E embedded arrays for fast turnaround time. Using a highly sophisticated transistor design, the TC260 achieves an effective channel length of 0.12 µm (0.14 µm-drawn), with 125 kgates per mm^2. Toshiba's TC260 technology is 30% faster than the previous generation technology, and it also cuts power dissipation by 80% while increasing the logic density by 3.4 times.

Toshiba offers two types of embedded DRAM, one targeted for high bandwidth, the other for low latency with SRAM-like ease of use. The embedded DRAM cores are based on Toshiba's leading trench capacitor technology, which permits mixing of logic and DRAM without compromising logic performance. Toshiba's IP library includes a full line of MIPS-based RISC, and cores that serve the multimedia, networking, communications, data processing, computing, digital consumer electronics and mobile applications.

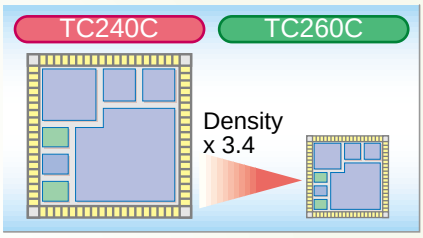
Toshiba delivers proven cell libraries, design methodologies and tools to help reduce design time and iterations. Encompassing Toshiba's tool suite are hardware/software coverification, hierarchical layout, near-zero clock skew management, etc.

Features of the TC260 Family

Ultra-High Density and Ultra-Low Power

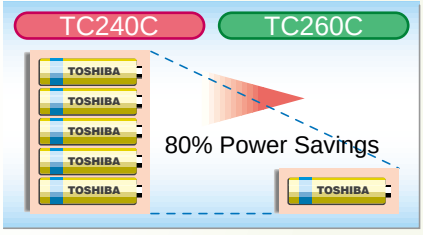
Fabricated using a 0.14 µm-drawn (Leff=0.12 µm) CMOS process and 6 levels of metal, the TC260 provides three major advantages over the previous 0.25-µm TC240 technology:

- x3.4 improvement in logic density
- 80% power savings per gate
- 30% reduction in gate delay



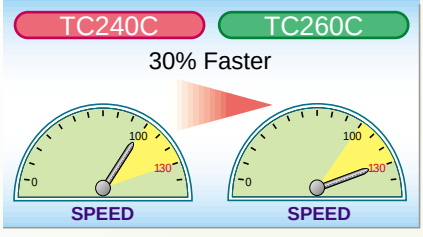
Embedded DRAM

Embedded DRAM offers a significant advantage over off-chip memory solutions that stems from the flexibility of choosing wide memory buses and lower power dissipation due to lower capacitance on-chip connections. Since the embedded DRAM cores are based on Toshiba's leading trench capacitor technology, logic performance is not degraded.



High-Speed and High-Density SRAM Cells

The TC260 family offers two types of SRAM cells. The high-speed type can go as high as 500 MHz; the high-density type requires approximately 1/3 the chip's real estate of conventional SRAMs.

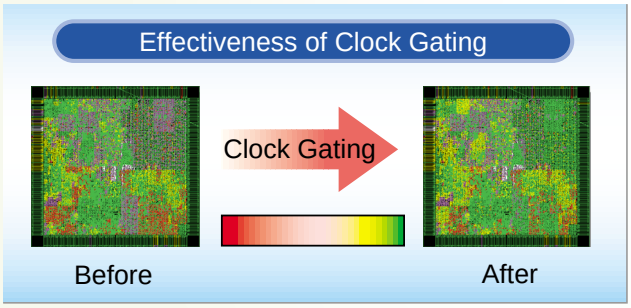


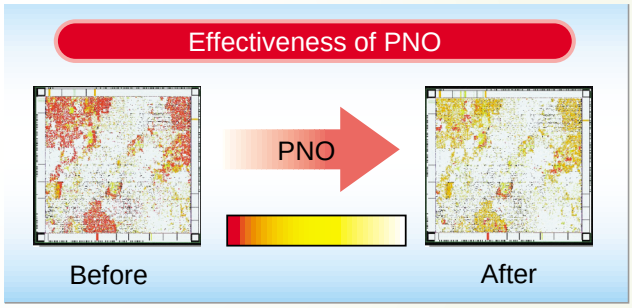
General Product Specifications

Gate Length	CMOS process, 6-layer Al
Power Supply	VDD = 1.5 V (Core); 2.5 V or 3.3V (I/O)
Gate Delay (F/O=1, CIVX2 Cell)	18 ps (standard type), 15 ps (high-speed type) * Two types of transistors are available with different threshold voltages.
Gate Density	125 kgates/mm^2 (TC260C cell-based ICs)
Power Dissipation	15 nW/MHz/gate (CIVXL cell)

Low-Power Technology Front-End and Back-End Optimizations

With the ever growing complexity of deep-submicron designs, the need for low-power design is increasingly acute. Clock gating is a common power reduction technique. Toshiba's new design methodologies automate the process of inserting clock gating logic in a design. You can embrace clock gating up front as early as at RTL. Additionally, during physical layout, Toshiba's circuit optimization tool, PNO, employs unique techniques to create the lowest power implementation permitted by the timing constraints on a design. For best results, cell libraries contain several functionally-equivalent cells differing in drive strength, allowing the optimal tuning of performance and power.





DRAM Cores and Application-Specific IP

Toshiba supports an ever-growing selection of IP cores. These range from general cells such as RISC processors and DRAMs through application-specific IP.

MPU	: TX System RISC
Protocol Control	: IEEE1394, IEEE1284, PCI, USB, IrDA, PCMCIA
High-Performance I/O	: PCI, AGP, USB, LVDS
Multimedia	: JPEG, MPEG, Smart Media™
Networking	: Ethernet Controller
Analog cores	: ADC, DAC, PLL
Memory	: DRAM, SRAM, ROM

SD Type
(High-bandwidth SDRAM)

Maximum clock rate: 200 MHz
Maximum data rate: 6.4 GB/s
Random access cycle: 48 ns
Size: 2 to 32 Mb

FA Type
(Fast-access SDRAM with SRAM-like easy of use)

Latency: < 2 cycles
Random access cycle: 30 ns
Size: 1 to 4 Mb

Benefits of Embedded DRAM Cores

1) Flexibility in configuring the DRAM cells based on application requirements; 2) high bandwidth due to wide and fast memory buses; 3) faster access time than discrete DRAM components; 4) lower power dissipation due to lower-capacitance on-chip connections; and lower switching noise on data bus between memory and logic.
The TC260 offers two types of DRAM cores, SD type for high bandwidth and FA type for low latency.

Packaging

Toshiba's comprehensive packaging options include electrically enhanced, 4-layer EPBGAs (352 to 576 pins), high-performance, high-pin-count PBGA[FC]s (>800 pins), chip-scale PFBGAs with <15mm×15mm body size (109 to 265 pins) and fine-pitch TBGAs (256 to 768 pins). Toshiba also supports a wide range of cost/performance requirements with QFPs having 44 to 304 pins.

EDA Tools

To ease the burden of designing multi-million-gate SLI ASICs, Toshiba supports many industry-standard EDA tools for logic synthesis, sign-off simulation, static timing analysis, design-for-test, formal verification, floorplanning and emulation. Such back-end features as near-zero clock skew management, multi-layer routing and timing/power optimization are designed to minimize layout-related design iterations in order to help reduce development time and improve market responsiveness.

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